AVL6261C

DVB-S2X/S2/S Demodulator

OVERVIEW

- Conforms to the following standards:
  ETSI EN 302-307-1 V1.4.1
  Part I (DVB-S2)
  Part II (DVB-S2X)
  ETSI EN 300-421 V1.1.2 (DVB-S)
- Ultra-compact 48 pin QFN 6x6 mm package and pin-to-pin compatible with Availink DTMB and multi-standards demodulator family

FEATURES

DVB-S2X/S2

- MODCOD
  All normative MODCODs of interactive service profile
- Both normal (64800 bits) and short (16200 bits) FECFRAME supported
- Normal FECFRAME Symbol rate

QPSK	1-60MSps
8PSK/APSK	1-60MSps
16APSK	1-58MSps
32APSK	1-55MSps
64APSK	1-34MSps

- CCM, VCM and ACM supported
- Roll-off factors for pulse shaping: 0.05 to 0.35

DVB-S

- Symbol Rates: 1-60 MSps
- Code Rates: 1/2, 2/3, 3/4, 5/6, 7/8

General

- Fast automatic blind scan
- Multi-stream support
- T2MI parsing
- Carrier frequency acquisition range:
  ±5MHz when Symbol rate >3 MSps
  ±3MHz when remaining Symbol rate
- Multi-purpose modulator for DiSEqC™ 2.0 application
- Single crystal 16~30MHz frequency with overall tolerance ±70ppm or by connection to 16-30MHz tuner reference clock
- Satellite zero IF input is supported
- I2C repeaters to reduce tuner noise
- I2C supports 400kHz operation
- Flexible AGC and GPIO outputs for tuner and LNB controls
- TS Interface
- Parallel and 1-bit Serial MPEG transport stream output capability
- Supports a tri-state MPEG output interface
- SQI, SSI and BER/PER monitors
- 1.2V core voltage and 3.3V I/O supply
- Temperature range –10C to +85C

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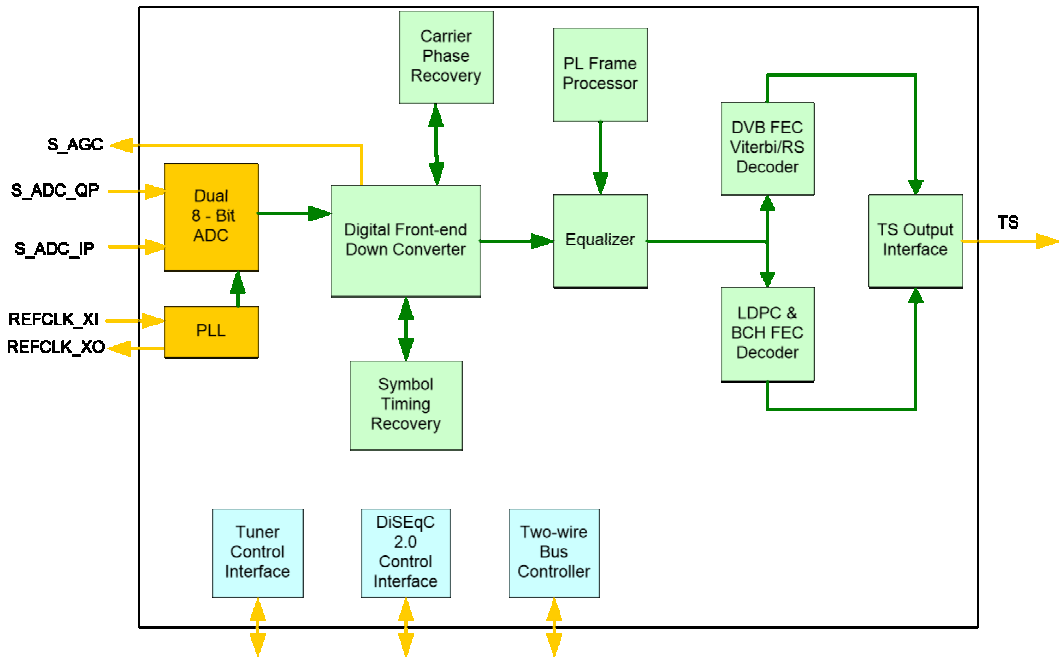
Block Diagram



Description

The AVL6261C is a highly integrated DVB-S2X/S2/S channel receiver IC. It converts a baseband IQ signal from a satellite tuner and performs a set of sophisticated demodulating and decoding operations to output a transport stream. The AVL62621C provides simple and flexible control via a standard two-wire bus.

The AVL6261C includes dual, differential, high performance, analog to digital converters (ADC) with an input correction circuit comprised of dual DC removers and an IQ imbalance compensator. An RF AGC output is provided for simple gain control of the satellite tuner via an RC network.

The corrected signal is processed through decimation filter with digital AGC, a matched filter, a symbol timing recovery loop, a carrier frequency and phase tracking loop, and equalizer and FEC decoders and finally the data is packetized in TS output interface block.

The configuration of the AVL6261C is easily performed through a set of register via a standard two-wire bus. To simplify the interface to the host system, this same two-wire bus is used to communicate with the separate tuner two-wire bus and the DiSEqC™ interface to LNB.

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