JIANG LONGXING, MSc

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Personal Information

- **Gender:** Male
- **Date of Birth:** 19/08/1998
- **Location:** Chengdu, China

Education Background

Central South University **09/2016-06/2020**

- **Major:** Microelectronics Science and Engineering
- **Degree:** Bachelor Degree of Engineering
- **Arithmetic Average Score:** 81.47/100，**Weighted Average Score:**81.03/100

Delft University of Technology **09/2020-11/2022**

- **Major:** Electrical Engineering
- **Degree:** Master of science
- **Thesis project Score:** 8.5/10

Working Experience

Digital Circuit Engineer | Huawei company, Hisilicon department **12/2022 - Now**

- Be responsible for the implementation of a submodule in chip SD8062V100 according to the well-written architectural scheme.
- Serve as the Back End Support (BES) and the high-level block (HLB) owner for chip Diracv300. Be responsible for guaranteeing the correctness of clock and reset generation, module internal connection, design constraint setting, HLB synthesis, the results of Synopsys Formality.
- Independently design a submodule in chip SD8026. Be responsible for chip document writing (functional, architectural, and detailed design schemes) , digital circuit conversion, PPA (power, performance, and area) refinement, and module verification.

Project Experience

Bachelor Graduation Design：Research of Speech Noise Reduction Based on Multi-source Vibration Signal Fusion

- Use Matlab to simulate a simple multi-source de-noising system based on LMS (Least Mean Square) algorithm.
- Convert LMS-based denoising system into digital circuit and then implement it in FPGA.

EE4690 Hardware Architecture for Artificial Intelligence Course Project

- Use C++ to simulate edge detector using Sober operator.
- Convert Sober-based edge detector into digital circuit using HLS.

ET4370 Reconfigurable Computing Design Course project

- Use Pytorch to build a simple image classifier with MNIST benchmark based on Binary network (BNN).
- Convert BNN-based image classifier into digital circuit using Verilog.

European New control project

- Use C++ to simulate the control process of a CNN accelerator.
- Design a systolic-array architecture prototype for functional verification.
- Convert the control process of systolic-array-based CNN accelerator into digital circuit using Verilog, and then guarantee the correctness of the internal connection between control module and computation module (done by a postdoc colleague).

Master Thesis Project：A New Logarithmic Quantization Technique and Corresponding Processing Element Design for CNN Accelerators

- Software part: Propose a new quantization method name JLQ that performs well when the bit width of the operands becomes very small.
- Hardware part: Develop a new Processing Element that can effectively implement Multiply-And-Accumulate (MAC) operations in convolution computation when the weights are JLQ-ed.
- Resource utilization, area, and power consumption of the new PE both standing alone and with a real CNN accelerator are reported.

Academic Publication

Jumping Shift: A Logarithmic Quantization Method for Low-Power CNN Acceleration; **First author**

- Published in: 2023 Design, Automation & Test in Europe Conference & Exhibition (DATE)
- DOI: 10.23919/DATE56975.2023.10137169

Awards and Honors

- 12/2017 Third-class Scholarship
- 08/2018 Third Prize of Mathematical Contest in Modeling in Central South University
- 04/2019 National Project Approval in College Students Innovation and Entrepreneurship Competition

Skills

- Language Proficiency: overall band score: 6.5 (L: 7, R: 6.5, W: 6, S: 6); tested on 22/06/2019
- GRE：320 (V:150+Q:170) AW:3; tested on 20/09/2019
- Programming: Python (Pytorch mainly), C++, Matlab, Verilog.