Experiment #3– Function Generator

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1.Digital to Analog conversion using PWM

1.1

```
module DAC(output reg out,input[7:0]in,input clk,rst);
    reg[7:0] counter;
    always @(posedge clk, negedge rst) begin
            if(~rst)
              counter <= 8'd0;
            else
              counter <= counter + 1'b1;
    end
    always@(counter,in)begin
             if(counter > in)
         out = 1'b0;
        else
                  out = 1'b1;
    end
endmodule
```

Fig. 1 Dac verilog

1.2

Fig. 2 Dac waveform

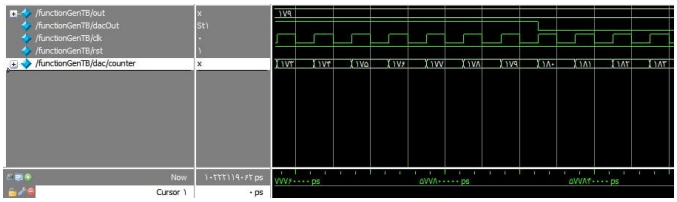

Fig. 3 Dac waveform

2.Waveform Generator

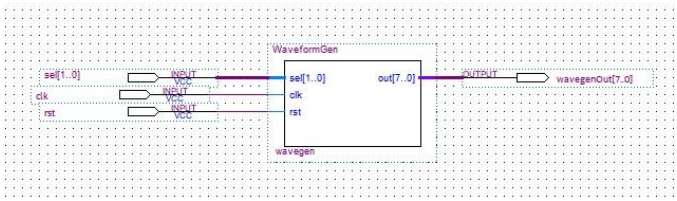

Fig. 4 Waveform generator

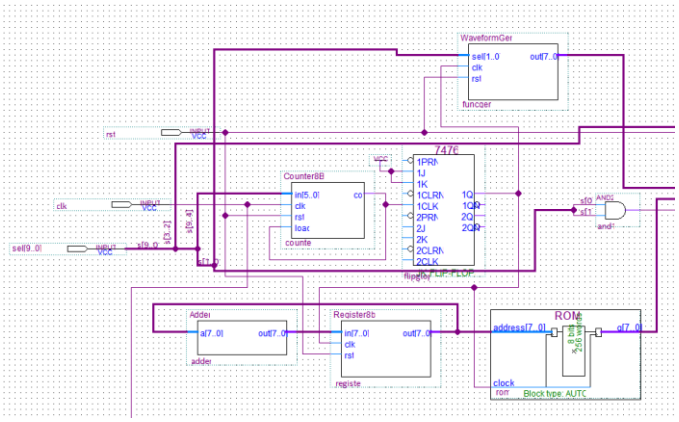

Fig. 5 Waveform generator

1.

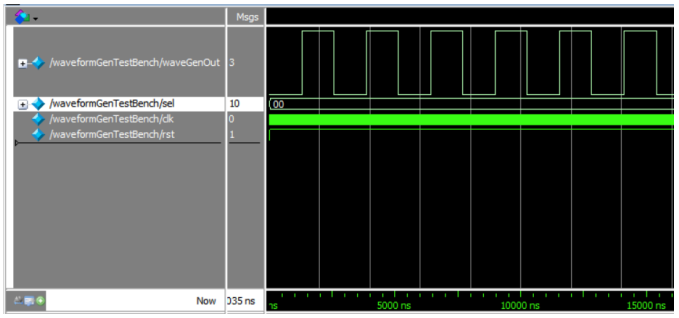

Fig. 6 Square output

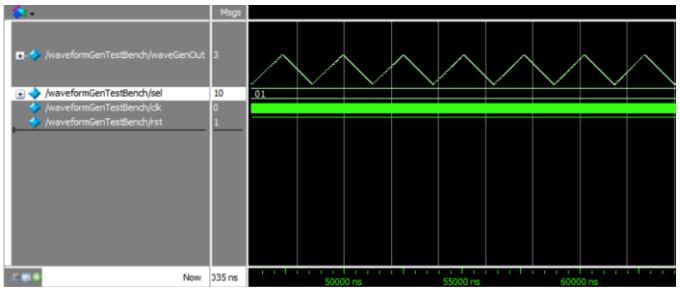

Fig. 7 Triangle output

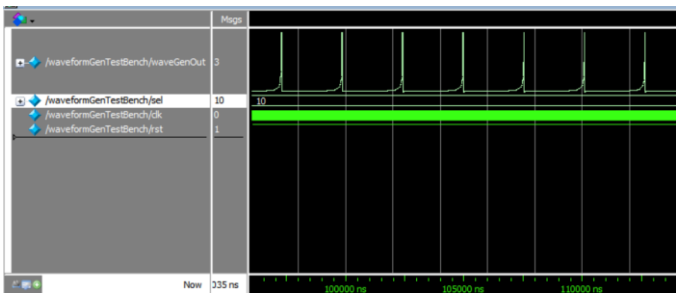

Fig. 8 Reciprocal output

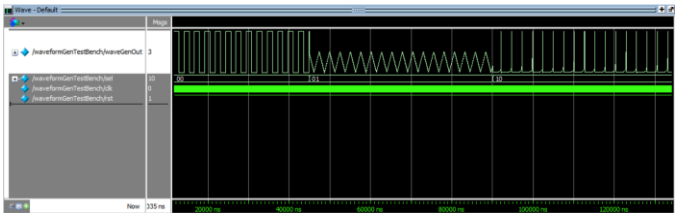

Fig. 9 Waveform generator output

2

Flow Summary	
<<Filter>>	
Flow Status	Successful - Sat May 28 14:33:51 2022
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	WaveformGen
Top-level Entity Name	WaveformGen
Family	Cyclone IV E
Device	EP4CE6E22A7
Timing Models	Final
Total logic elements	107 / 6,272 (2 %)
Total registers	8
Total pins	12 / 92 (13 %)
Total virtual pins	0
Total memory bits	0 / 276,480 (0 %)
Embedded Multiplier 9-bit elements	0 / 30 (0 %)
Total PLLs	0 / 2 (0 %)

Fig. 10 Synthesis summary

3.

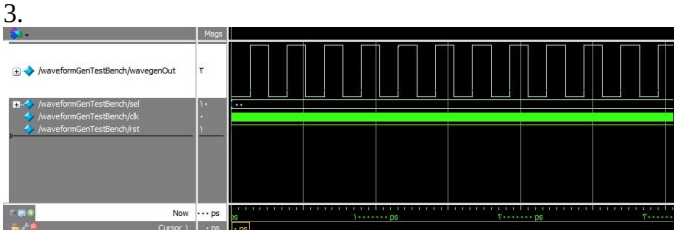

Fig. 11 Square waveform

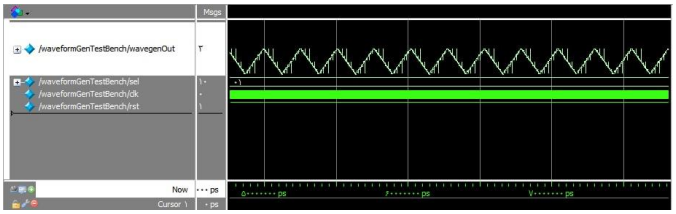

Fig. 12 Triangle waveform

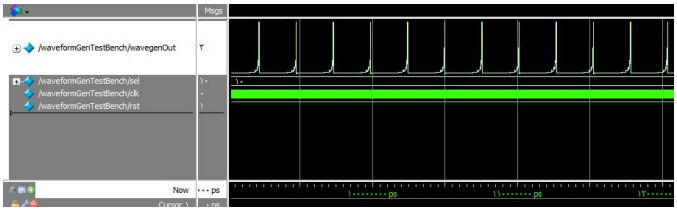

Fig. 13 Reciprocal waveform

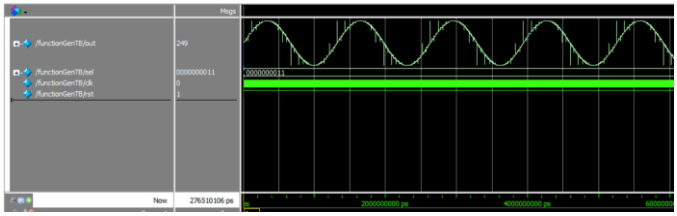

Fig. 14 Sin waveform

3.Frequency Selector

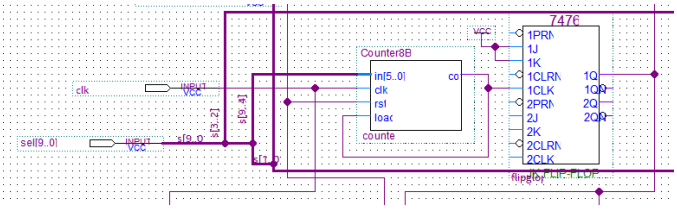

Fig. 15 Frequency Selector

4.

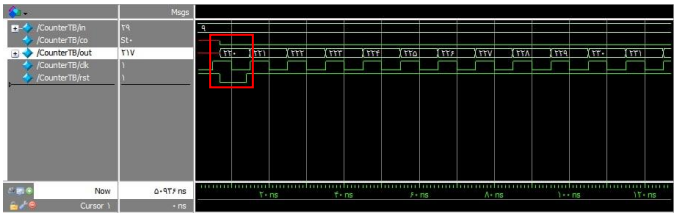

Fig. 16 input = 9

The 8bit Counter loads 256 – input when Co(wired to load) becomes 1. 2 least significant bits of input are 2'b00 so input = {in, 2'b00}.
Output = 256 – {9, 2'b00} = 256 – 9 * 4 = 220.

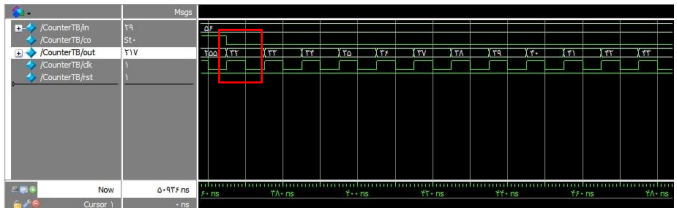

Fig. 17 input = 56

Output = 256 – {56, 2'b00} = 256 – 56 * 4 = 32.

5.

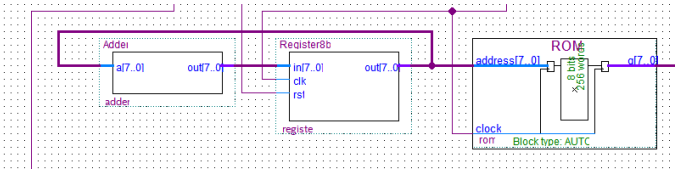

Fig. 18 DDS

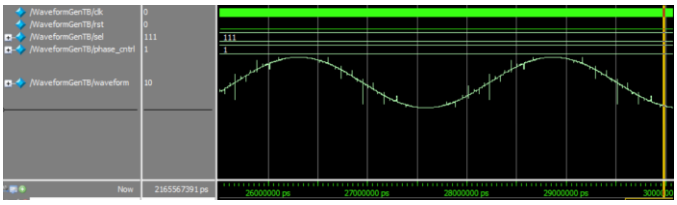

Fig. 19 Phase_cntrl = 1

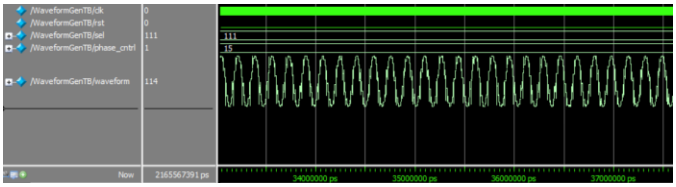

Fig. 19 Phase_cntrl = 15

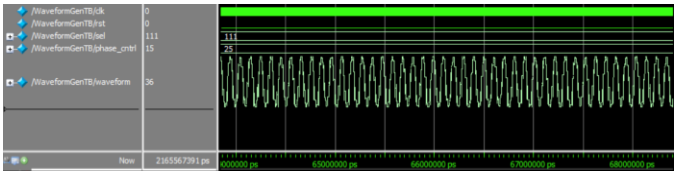

Fig. 20 Phase_cntrl = 25

When the value of Phase_cntrl is 1, every block of the rom will be shown but when the value of Phase_cntrl increases, some of the rom blocks will be skipped.

4.Amplitude Selector

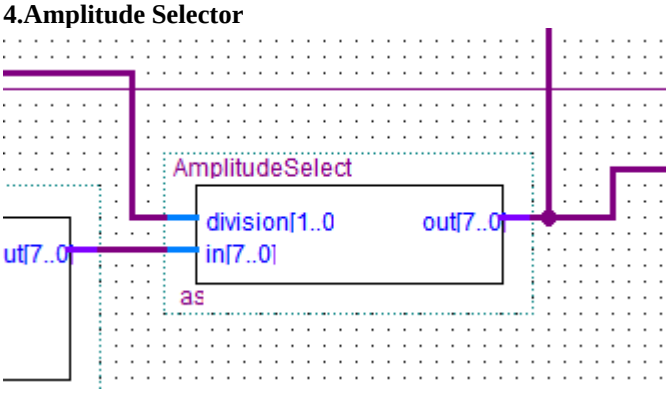

Fig. 21 amplitude selector

2.

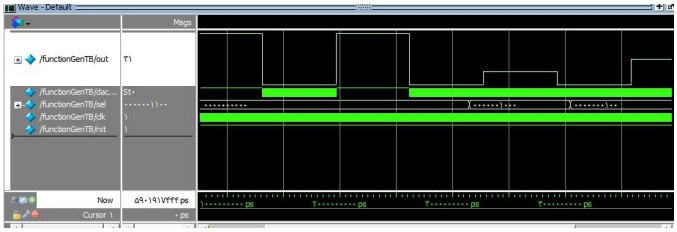

Fig. 22 Shifted Square

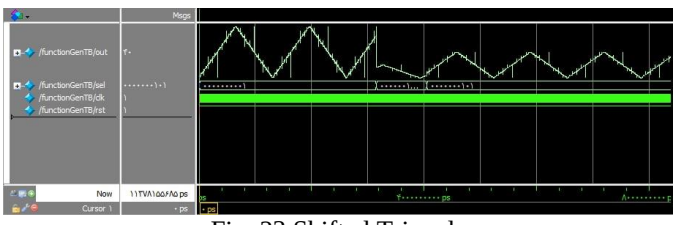

Fig. 23 Shifted Triangle

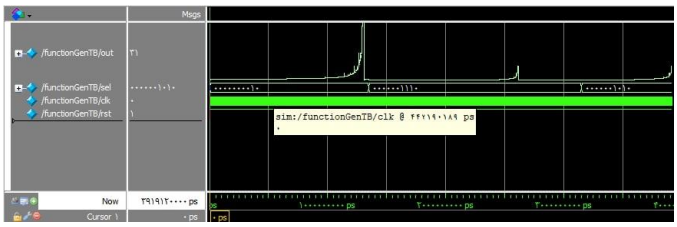

Fig. 24 Shifted Reciprocal

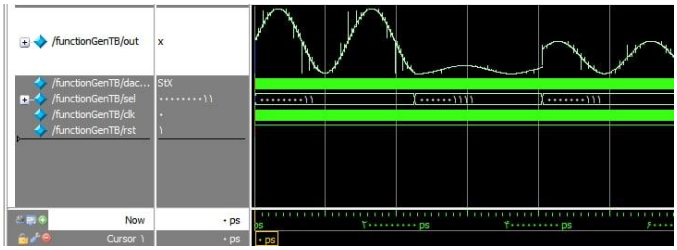

Fig. 25 Shifted Sin

5.The total design

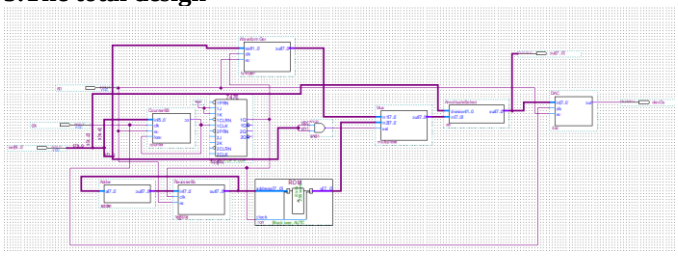

Fig. 26 Total design

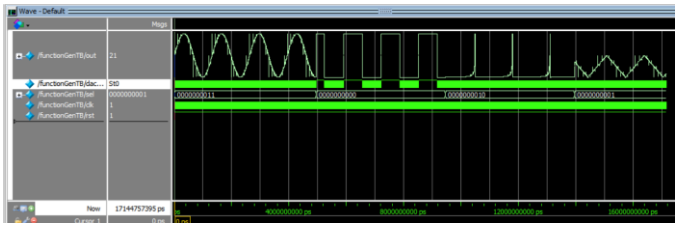

Fig. 27 Waveforms

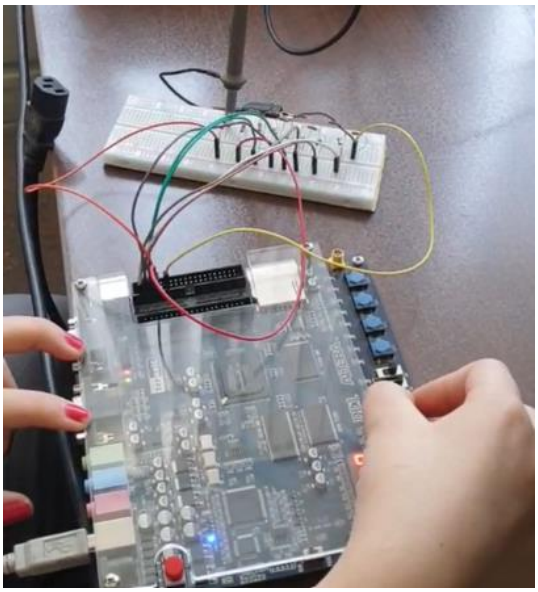

Fig. 28 Circuit

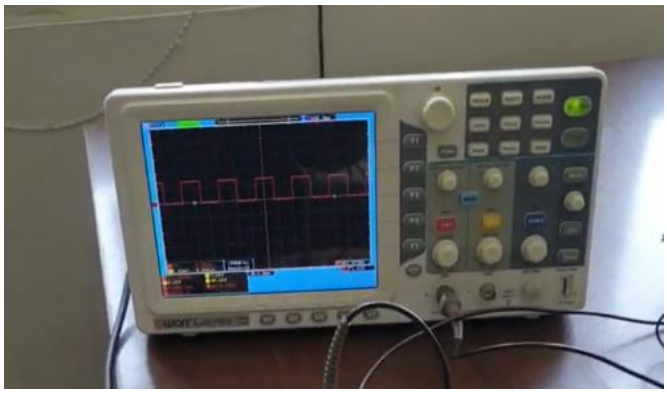

Fig. 29 Square Waveform without shift

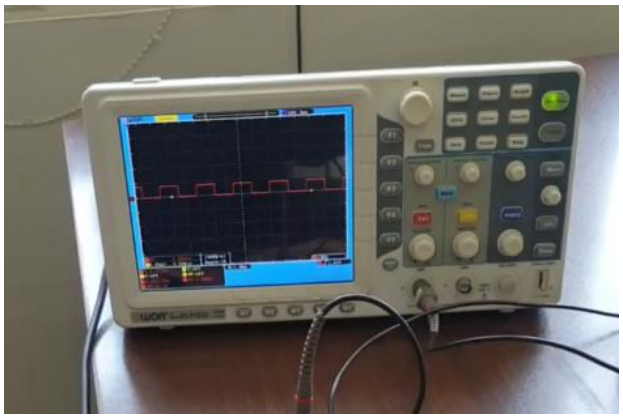

Fig. 30 Square Waveform with one shift

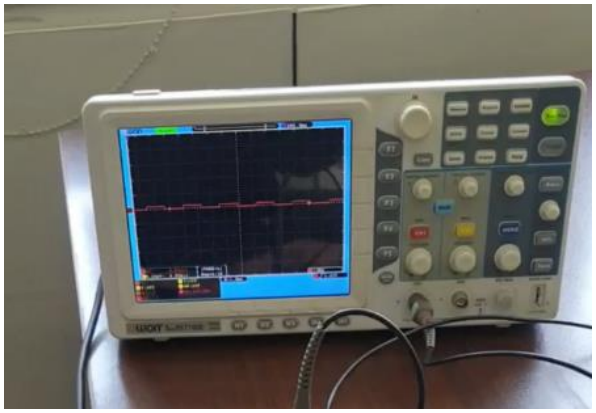

Fig. 31 Square Waveform with two shifts

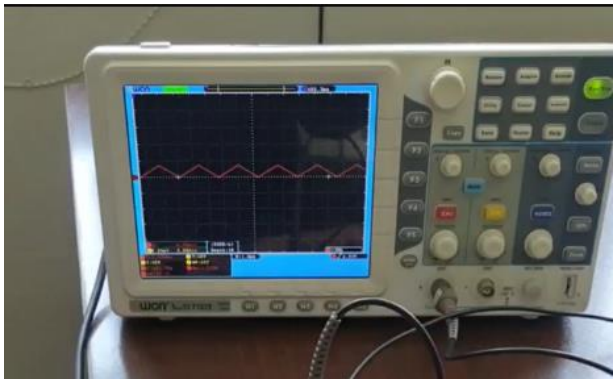

Fig. 32 Triangle Waveform without shift

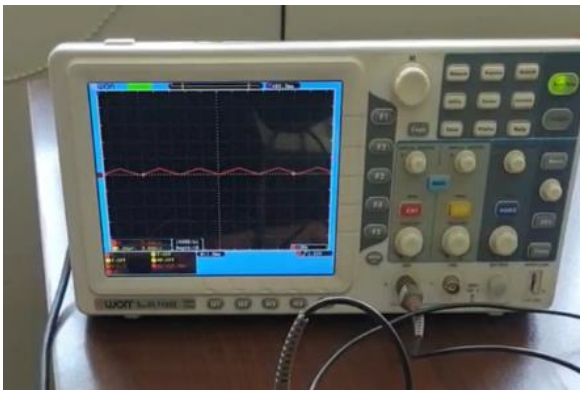

Fig. 33 Triangle Waveform with one shift

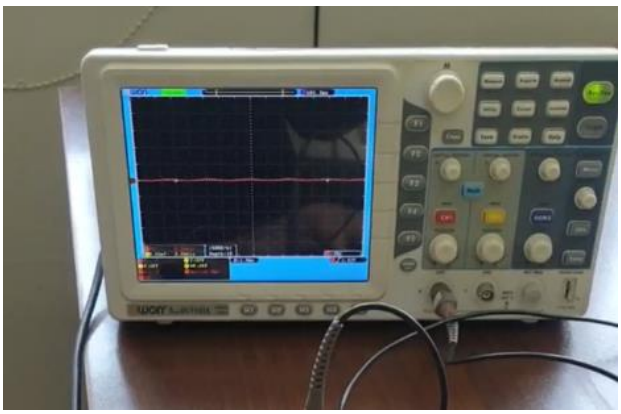

Fig. 34 Triangle Waveform with two shifts

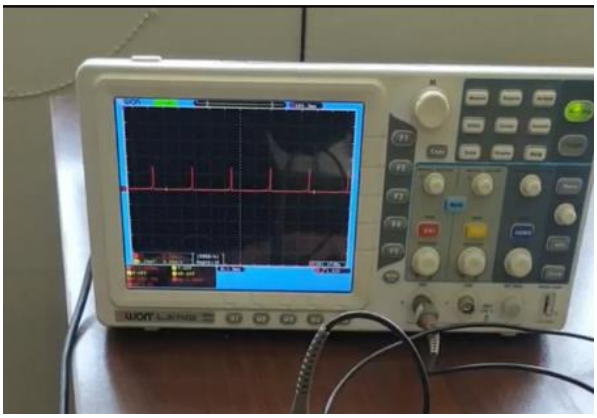

Fig. 35 Reciprocal Waveform without shift

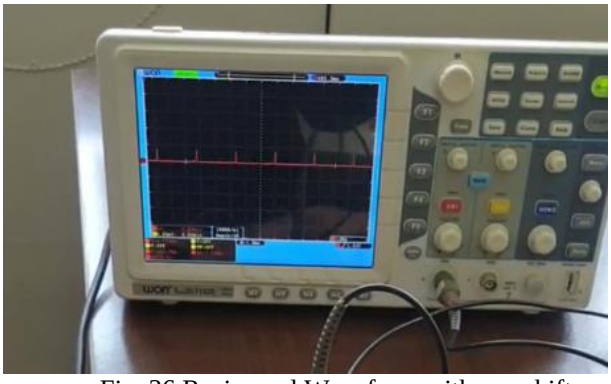

Fig. 36 Reciprocal Waveform with one shift

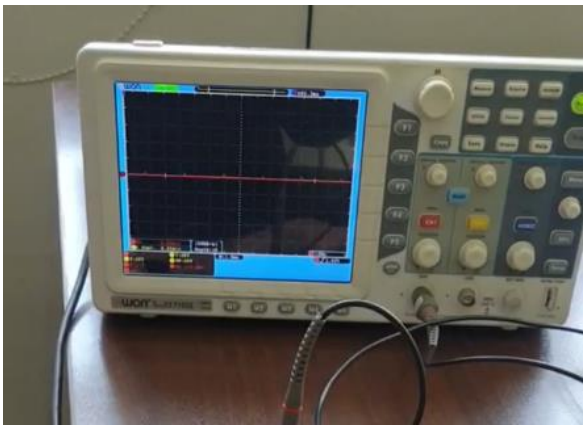

Fig. 37 Reciprocal Waveform with two shifts

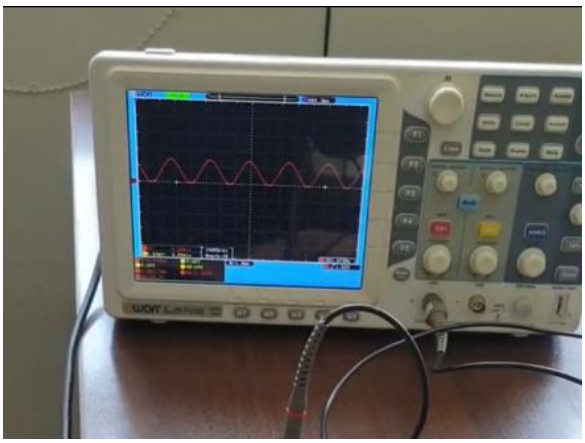

Fig. 38 Sin Waveform without shift

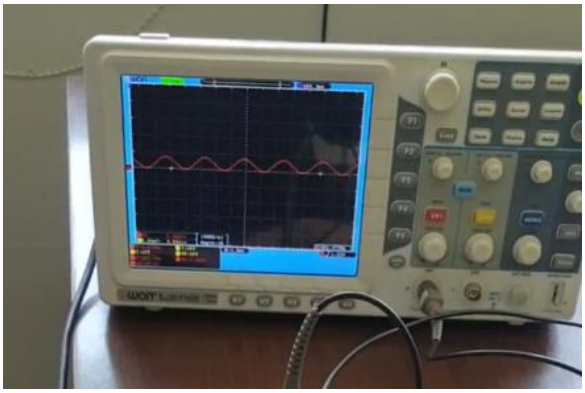

Fig. 39 Sin Waveform with one shift

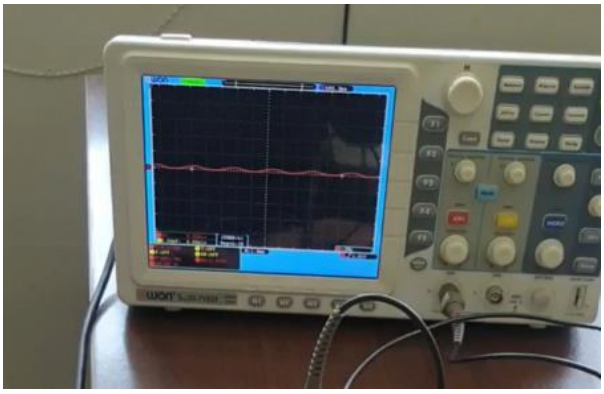

Fig. 40 Sin Waveform with two shifts