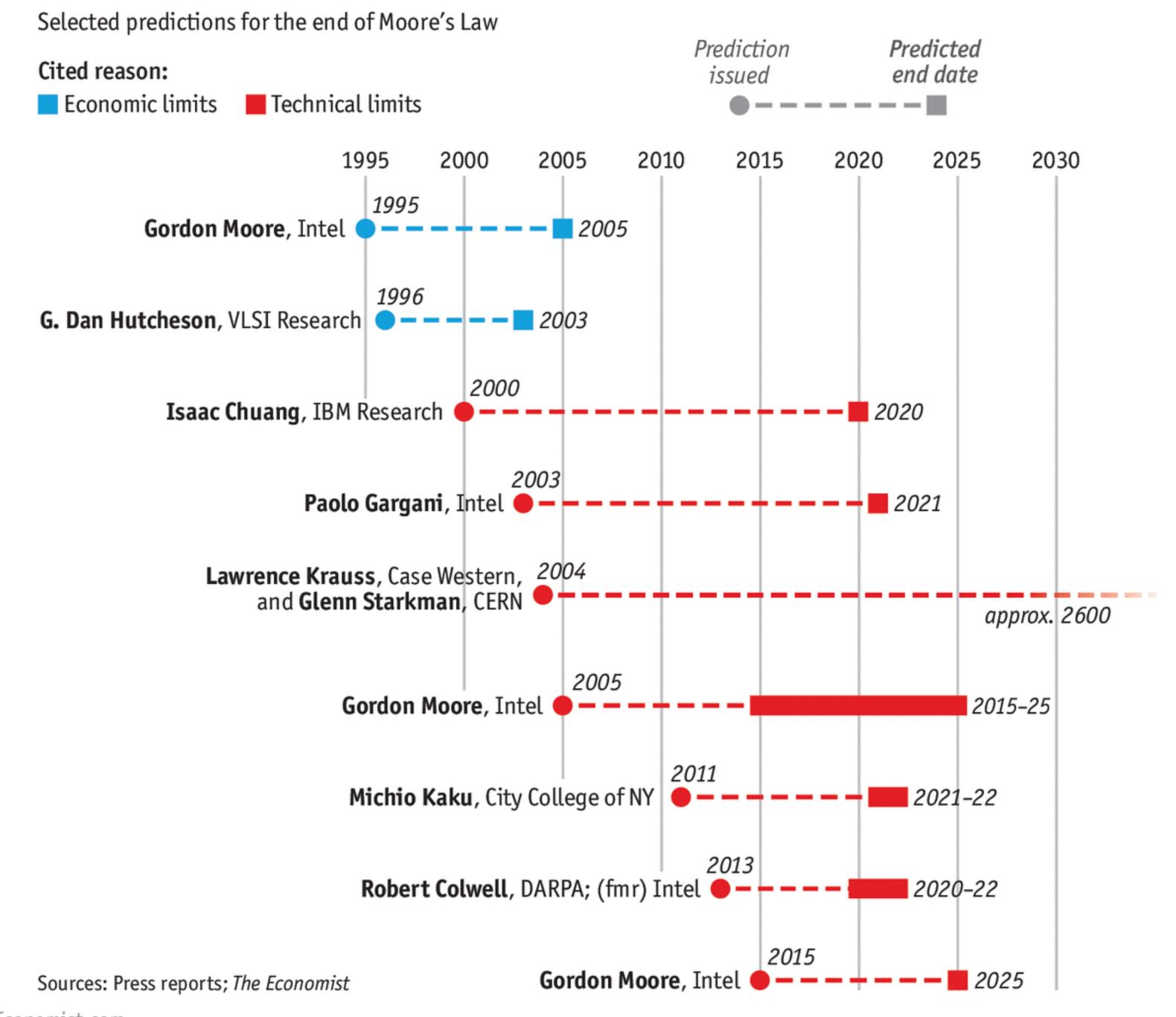
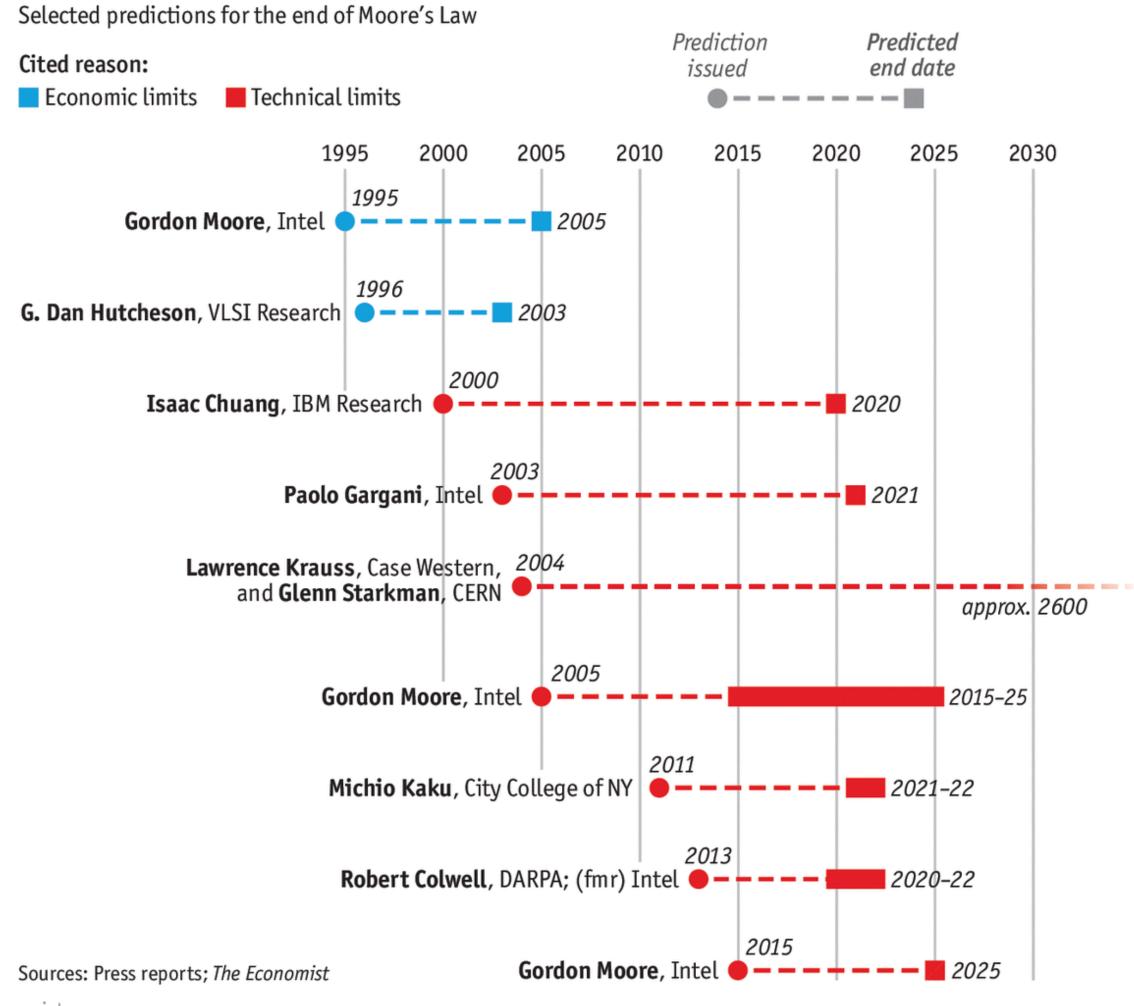
A Synthesis-Aided Compiler for Manycore Computation

emergent trend in computer architecture:

emergent trend in computer architecture:

end of Moore's law?!?



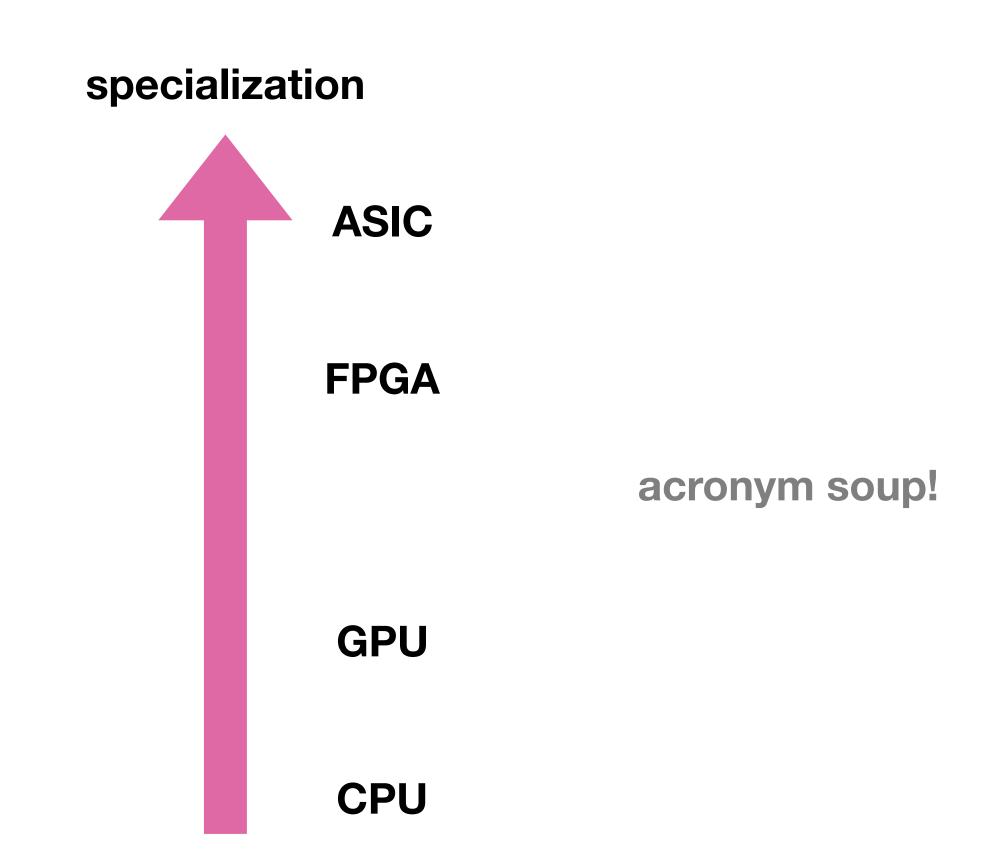


Economist.com

motivation for new, specialized architectures/accelerators

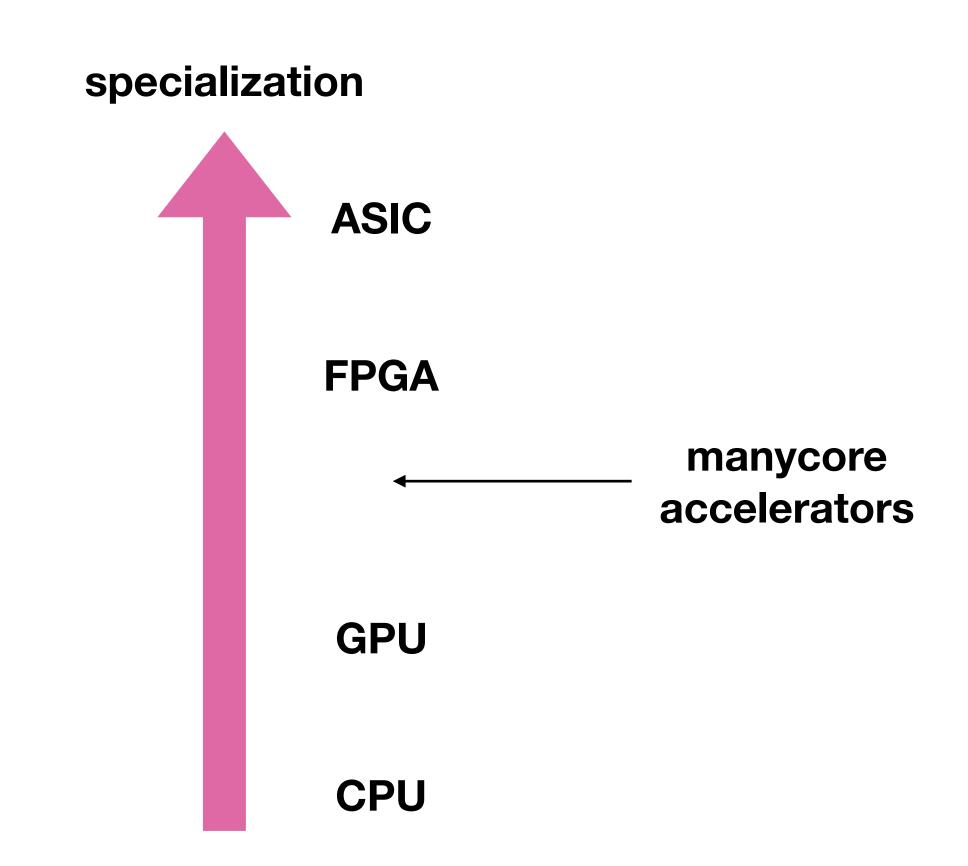
Selected predictions for the end of Moore's Law Prediction Predicted Cited reason: end date issued ■ Economic limits ■ Technical limits 2025 2030 2015 2020 1995 2000 2005 2010 1995 Gordon Moore, Intel 2005 1996 **G. Dan Hutcheson**, VLSI Research **---** 2003 2000 Isaac Chuang, IBM Research 2020 2003 Paolo Gargani, Intel 2021 Lawrence Krauss, Case Western, 2004 and Glenn Starkman, CERN approx. 2600 Gordon Moore, Intel 2015-25 2011 Michio Kaku, City College of NY 2021-22 2013 Robert Colwell, DARPA; (fmr) Intel 2020-22 2015 **Gordon Moore**, Intel • - - - - = 2025 Sources: Press reports; The Economist Economist.com

motivation for new, specialized architectures/accelerators

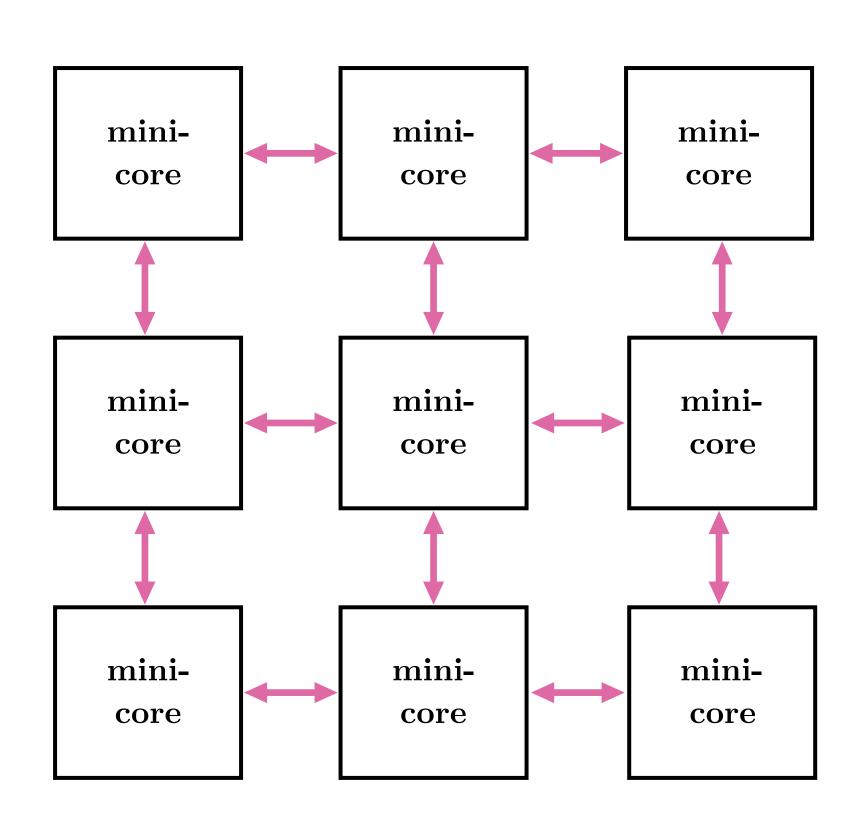


Selected predictions for the end of Moore's Law Prediction Predicted Cited reason: end date issued ■ Economic limits ■ Technical limits 2025 2030 2015 2020 1995 2000 2005 2010 1995 Gordon Moore, Intel 2005 1996 **G. Dan Hutcheson**, VLSI Research **---** 2003 2000 Isaac Chuang, IBM Research 2020 2003 Paolo Gargani, Intel 2021 Lawrence Krauss, Case Western, 2004 and Glenn Starkman, CERN approx. 2600 Gordon Moore, Intel 2015-25 2011 Michio Kaku, City College of NY 2021-22 2013 Robert Colwell, DARPA; (fmr) Intel 2020-22 2015 Gordon Moore, Intel • - - - - - -Sources: Press reports; The Economist Economist.com

motivation for new, specialized architectures/accelerators



manycore accelerators

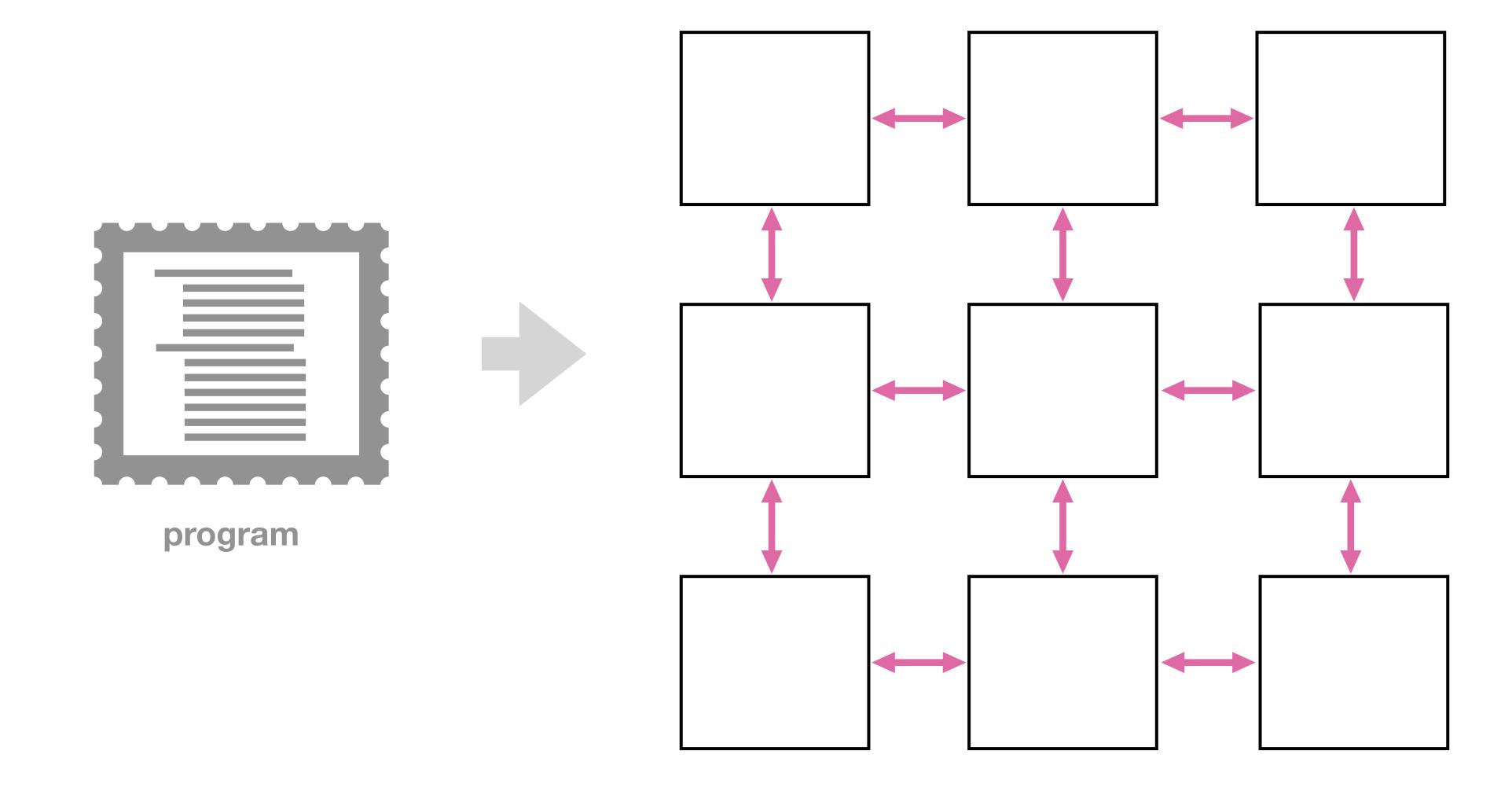


- differ from "multicore" processors
- combine many small, simple processor cores in a spatial layout
- communication via nearest neighbors
- programmer or compiler must specify partitioning

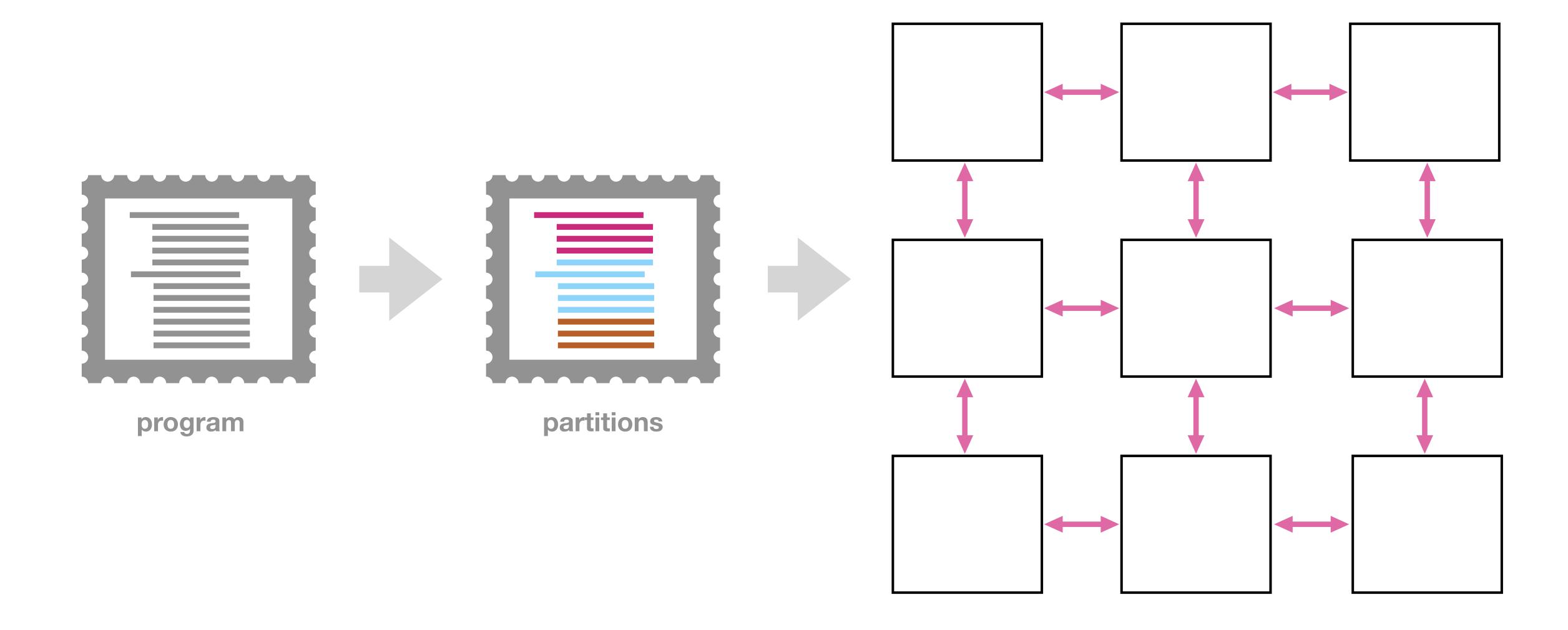
the challenge:

write programs at a higher level that leverage the spatial layout

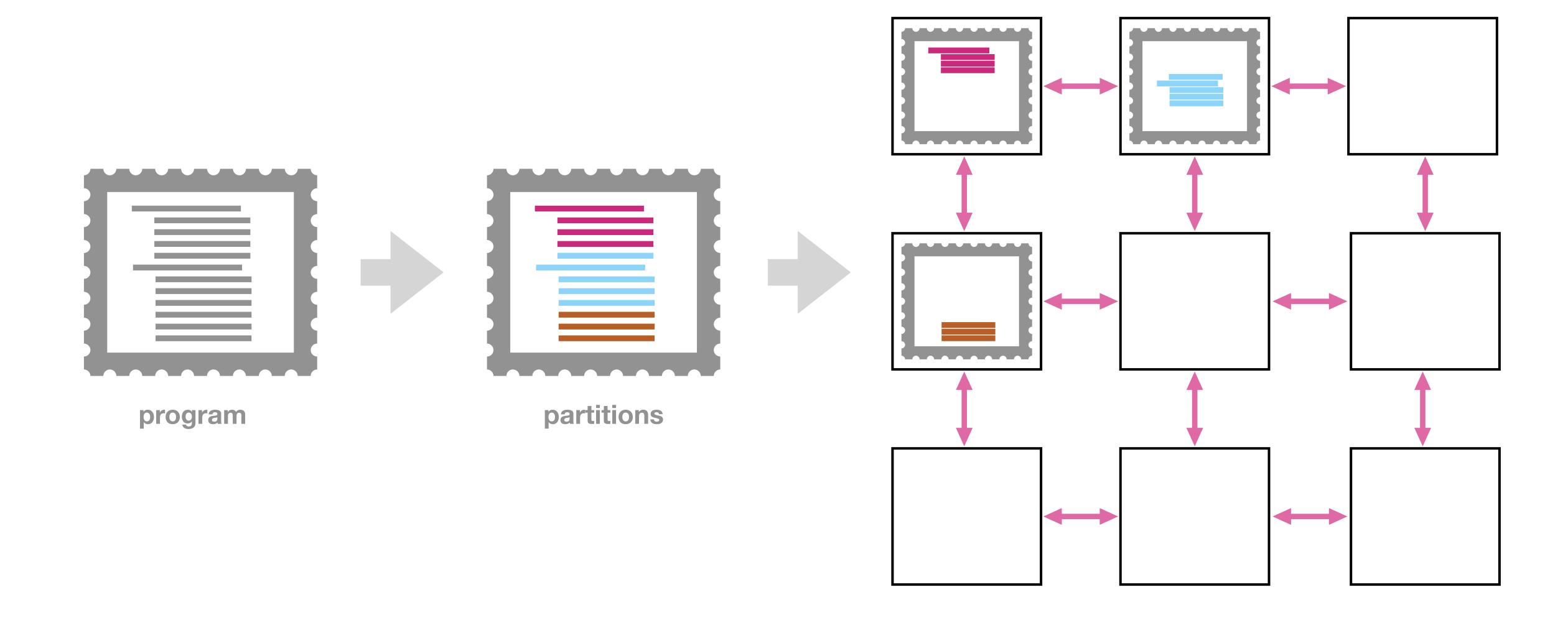
partitioning



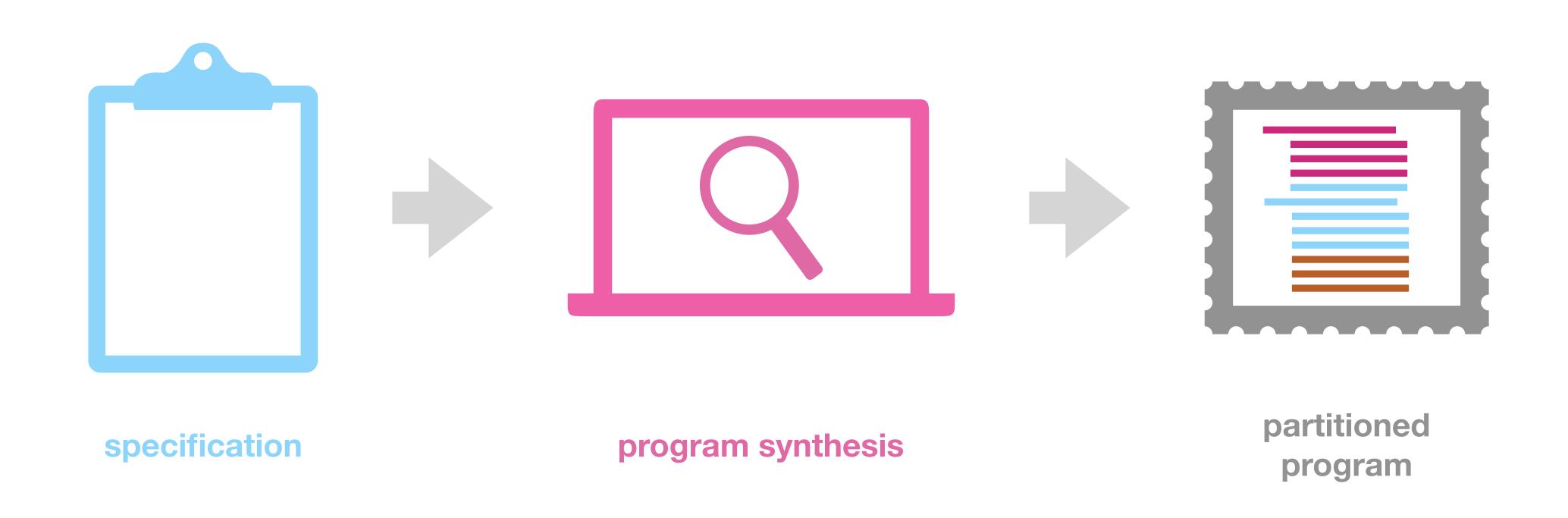
partitioning



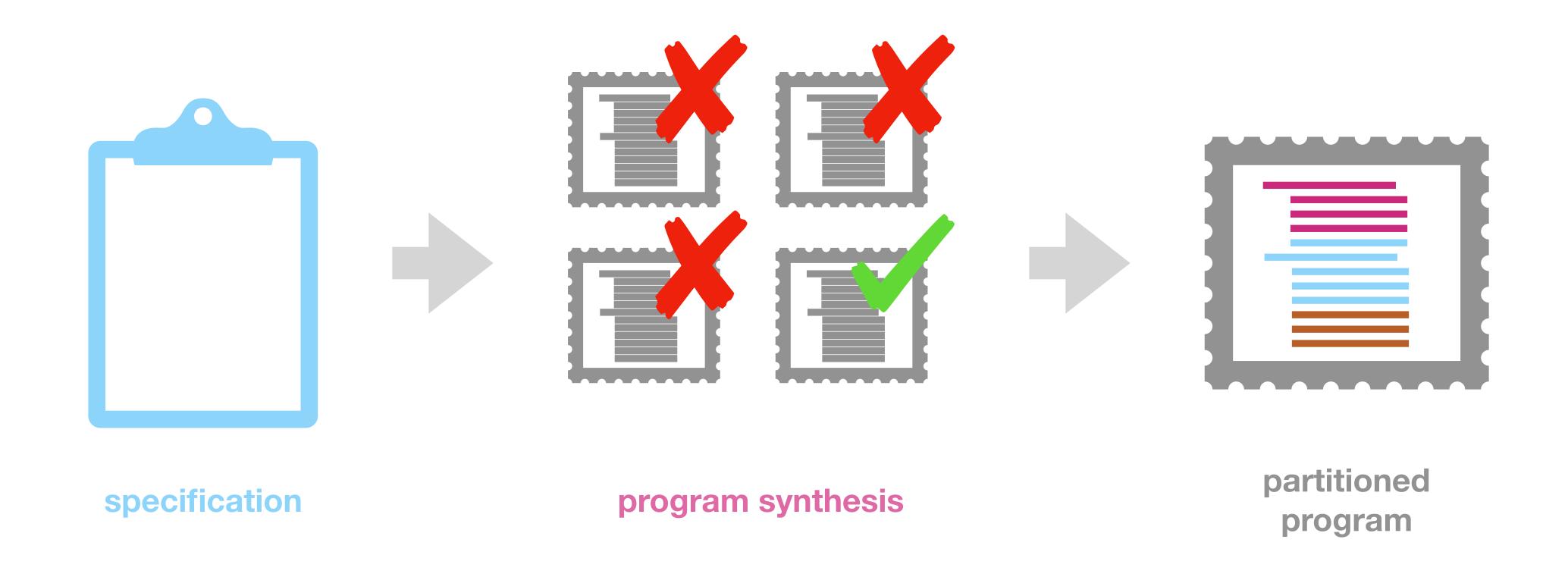
partitioning



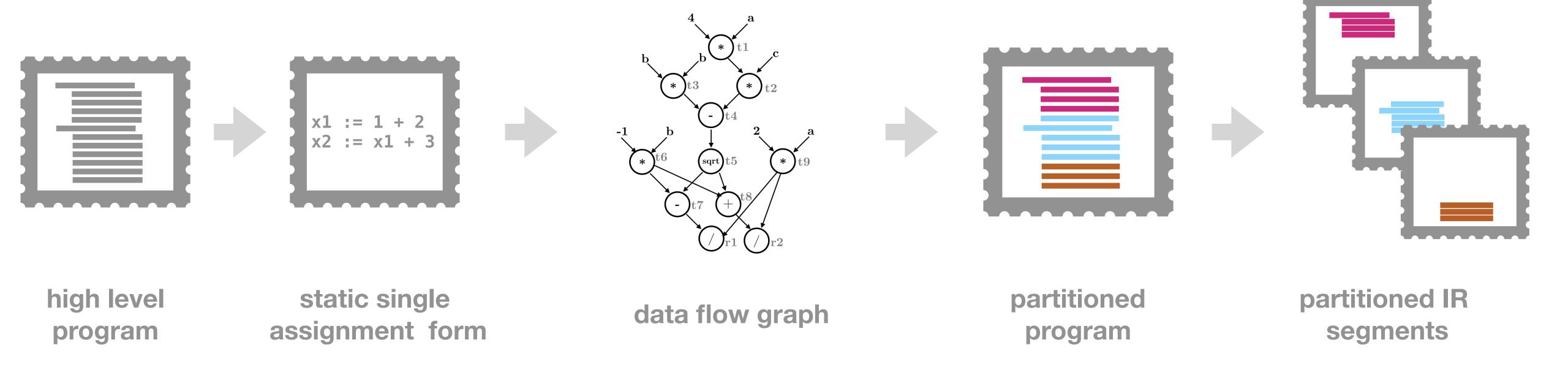
program synthesis



program synthesis

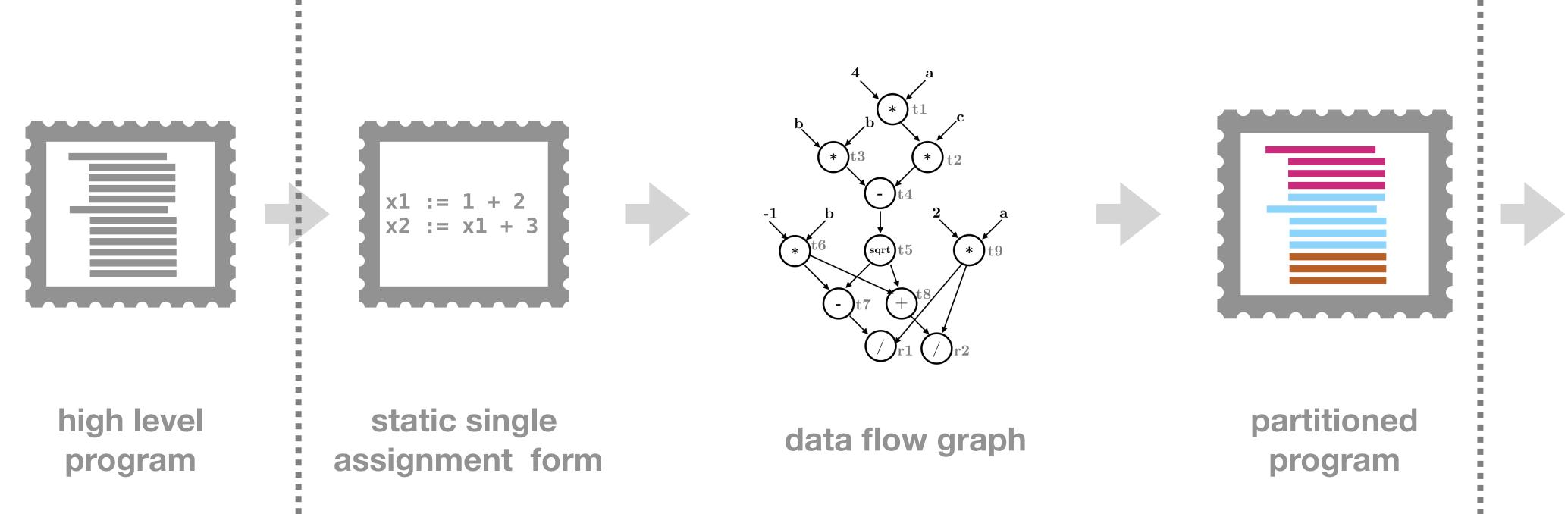


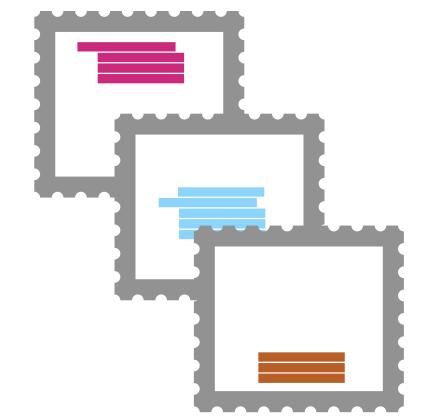
compiler overview



compiler overview

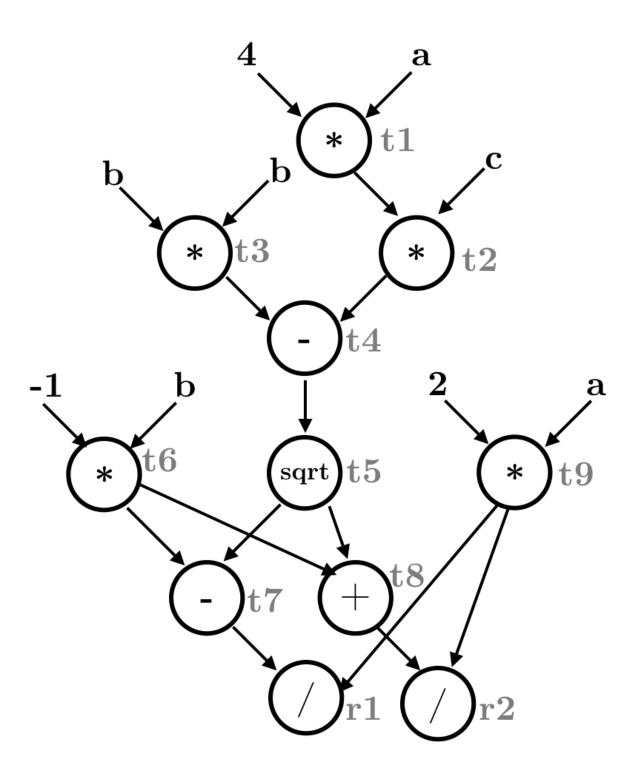
focus for this semester





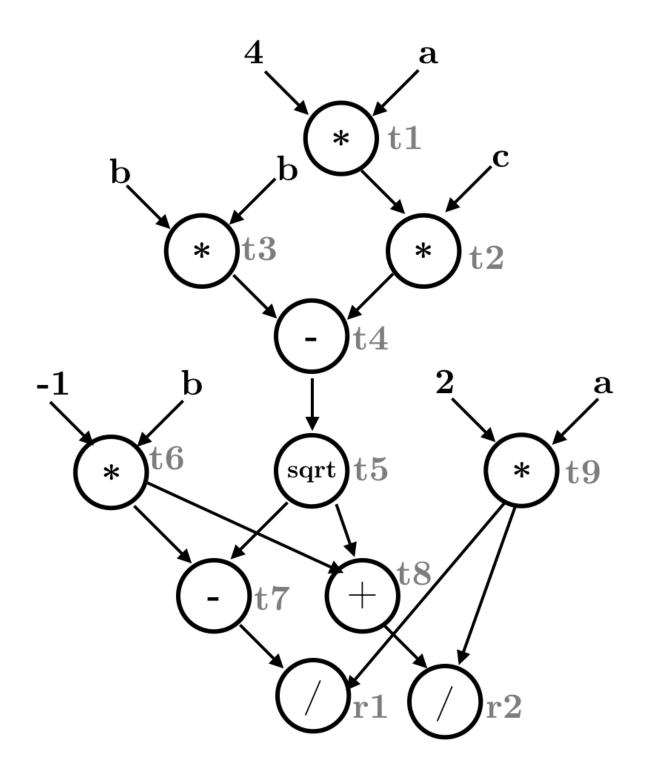
partitioned IR segments

$$\frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$



track partition and start/end times (p, (t1, t2))
 per operation

$$\frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

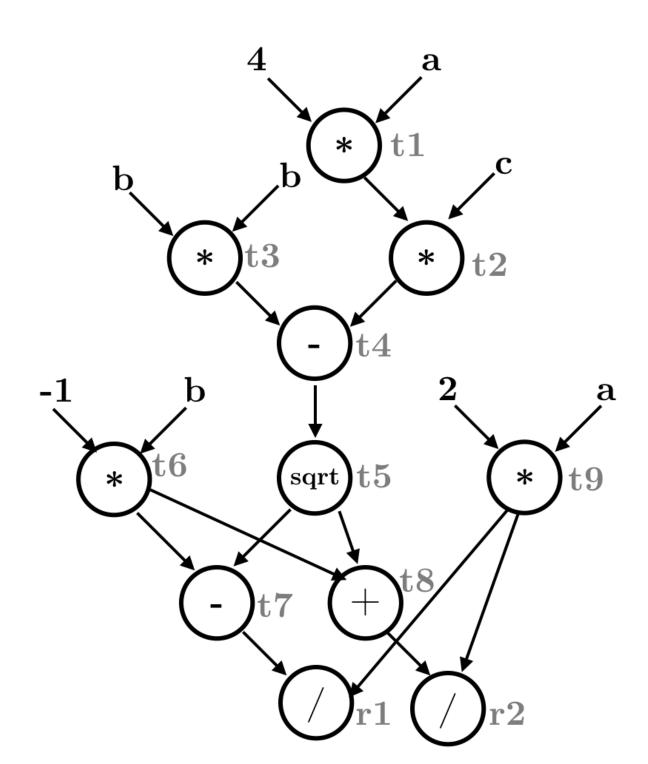


track partition and start/end times (p, (t1, t2))
 per operation

time example: no 2 operations on the same core at the same time

$$-b \pm \sqrt{b^2 - 4ac}$$

$$2a$$



track partition and start/end times (p, (t1, t2))
 per operation

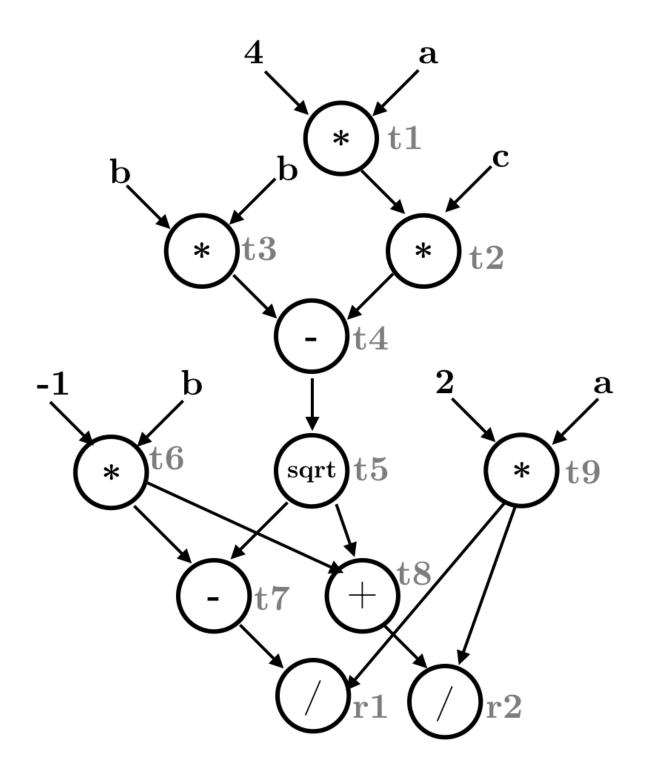
time example: no 2 operations on the same core at the same time



∀ disj. n, n'.

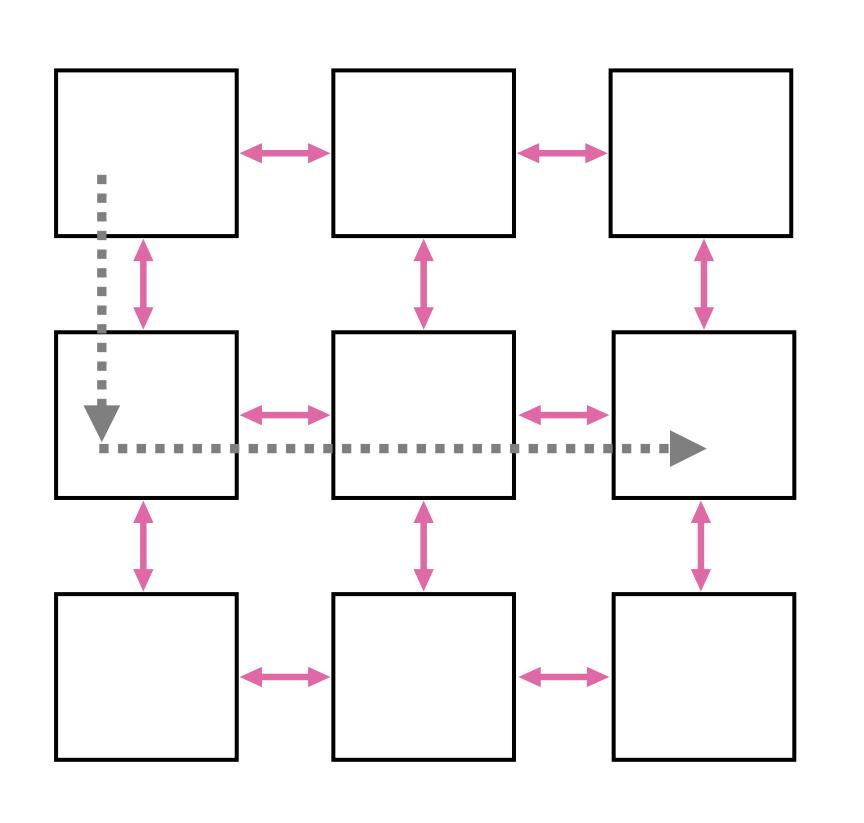
$$(p != p') => (t2 < t1') v (t1 > t2')$$

$$\frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$



track partition and start/end times (p, (t1, t2))
 per operation

communication example: delay between partitions is the Manhattan distance (number of hops)



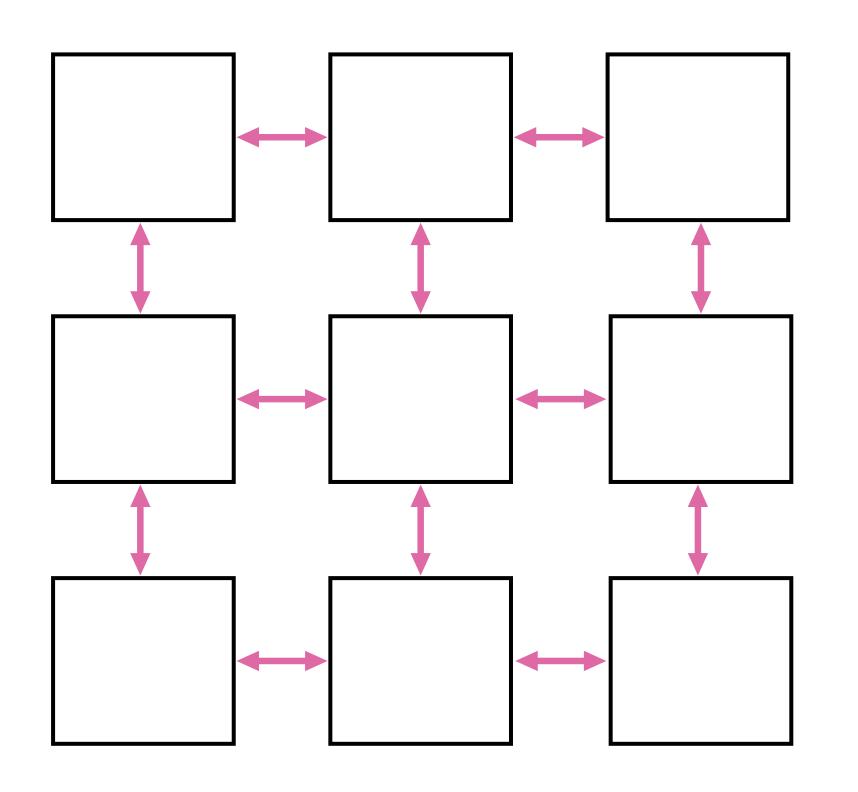
track partition and start/end times (p, (t1, t2))
 per operation

communication example: delay between partitions is the Manhattan distance (number of hops)



 \forall edges n, n'. t1' >= t2 + dist(p, p')

dist = abs(x - x') + abs(y - y')



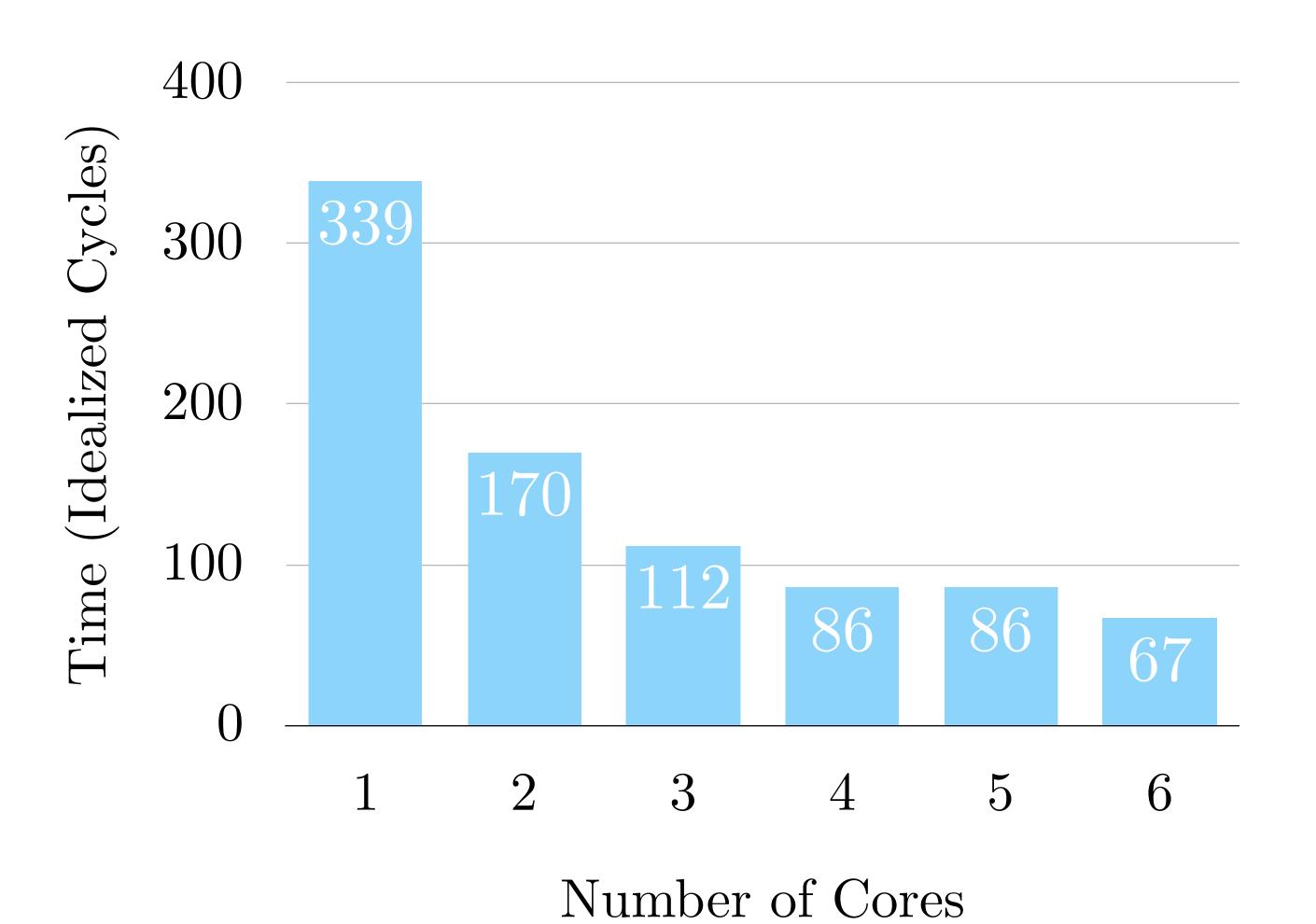
track partition and start/end times (p, (t1, t2))
 per operation

final goal: find an assignment where the latest time is <= the goal



iterative solution starting at the sequential upper-bound

evaluation



- goal: run IR fragments on a cyclelevel simulator
- current: compare the model's time (idealized cycles) across core configurations
- shown: 50 LOC program, idealized upper bound 339 cycles