Ava Zahedi
ME 333

Problems 3-16 of Chapter 2

3. Pin 12
- AN4: analog-to-digital (ADC) input
- C1IN-: comparator negative input
- CN6: change notification; voltage changes on these pins can generate interrupts
- RB4: digital I/O pin

4. TRISC

5. Reset value is 0x00C3

6.
- SYSCLK: The system clock keeps track of system time and clocks the CPU at frequencies between 0 Hz and 80 MHz.

- PBCLK: The peripheral bus clock is used by many peripherals and has a frequency set to SYSCLK's frequency divided by a factor of 1, 2, 4, or 8.

- PORTA to PORTG: Digital I/O ports that allow you to read or output a digital voltage. PORTB can be used for analog input.

- Timer1 to Timer5: 16-bit counters/timers that count the number of pulses of a signal.

- 10-bit ADC: An analog-to-digital converter which can distinguish 1024 different voltage levels.

- PWM OC1-5: Output compare (OC) pins that are used to generate pulse-width modulated (PWM) that can control motors or be low-pass filtered to create a specified analog voltage output.

- Data RAM: Random-access memory (RAM) is volatile memory that stores temporary data; however this data is not preserved when the device is powered off.

- Program Flash Memory: Nonvolatile memory that stores your program; this program is preserved even when the device is powered off.

- Prefetch Cache Module: Stores recently executed program instructions, which are likely to be executed again soon, with the goal to have the next instruction requested by the CPU already in the cache.

7. Peripherals not clocked by PBCLK:
- Priority interrupt controller
- USB
- CAN1, CAN2
- Ethernet
- DMAC
- ICD
- PORTA to PORTG
- Prefetch module
- Peripheral bridge

8. (3.3-0)/1024 = 0.00322 V is the largest voltage difference that it may not be able to detect

9. 256 bytes is the maximum size of a program loop that can be completely stored in the cache.

10. Because flash is slow and has a max speed of 30 MHz, reading a program instruction from flash can take 3 CPU cycles when operating at the max speed of the SYSCLK at 80 MHz. Having the prefetch cache module be 128 bits wide can account for this so that the CPU doesn't have to wait for the instructions to load from flash. 32 and 64 bits would still require the CPU to wait and 256 bits would be giving more memory than necessary to achieve the same result as having 128 bits.

11. An output pin can also be configured as an open drain, which would have the pin connected by an external pull-up resistor to a voltage up to 5.5 V. Because it is externally connected, it can go beyond 3.3 V.

12. Flash memory could store a maximum of 41943040 bytes = 0x02800000. RAM could store a maximum of 486539264 bytes (~486 MB) = 0x1D000000.

13.
a. To make the PBCLK frequency to be half the frequency of SYSCLK, modify bits 13-12 of Device Configuration Register 28-2 DEVCFG1. Give the values 01 to those bits.
b. Bit 23 on Register 28-2 DEVCFG1 enables the watchdog timer. Bits 20-16 set the postscale that determines the time interval during which the watchdog must be reset to prevent it from restarting the PIC32. To enable, set bit 23 to 1 and to maximize the time interval, give bits 20-16 values of 10100.
c. Bits 2-0 on Register 28-2 DEVCFG1, set to 011, enable the primary oscillator and turn on the PLL module.

14. 16.67 ohms is the smallest resistance that would be safe. This is because a current of higher than 300mA is unsafe for humans. 5/0.3 = 16.67 ohms.

15. Minimum of 6V and maximum of 9V because the textbook states the plug should provide DC 6V or more. The textbook also recommends not going higher than 9V because the regulators will heat up if you do.

16.

- Buttons:
    - 7, with function MCLR
    - 55, with functions ETXCLK/AERXERR/CN16/RD7
- LEDs:
    - 58, with functions C1RX/AETXD1/ERXD3/RF0
    - 59, with functions C1TX/AETXD0/ERXD2/RF1