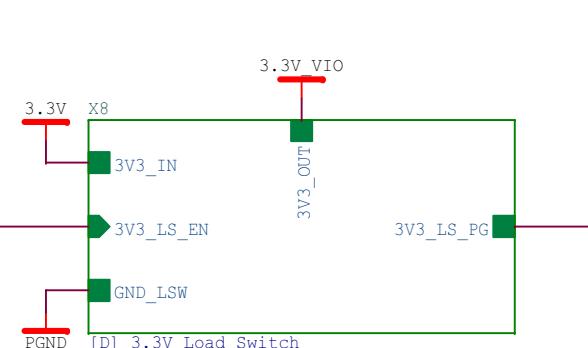
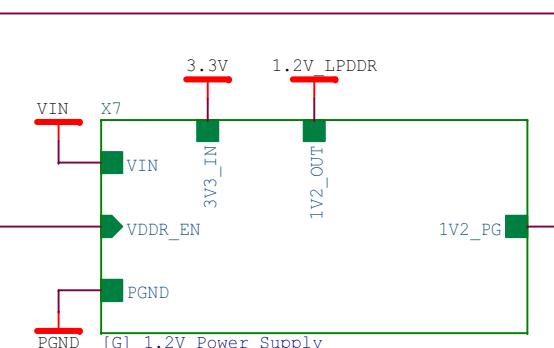
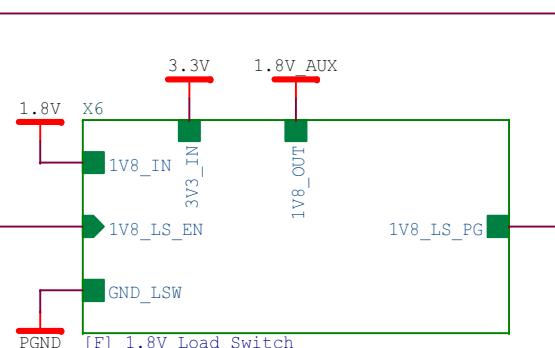
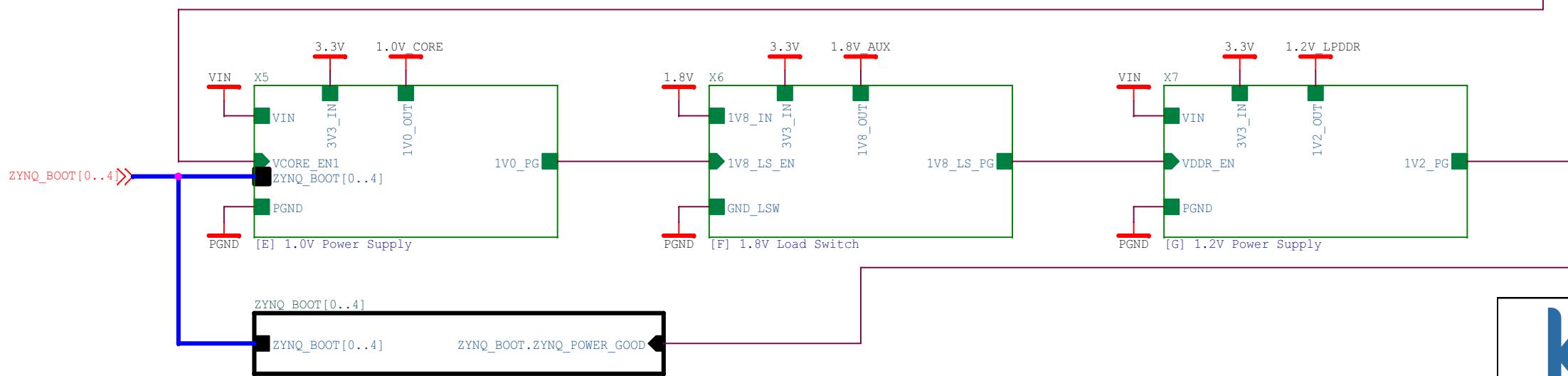
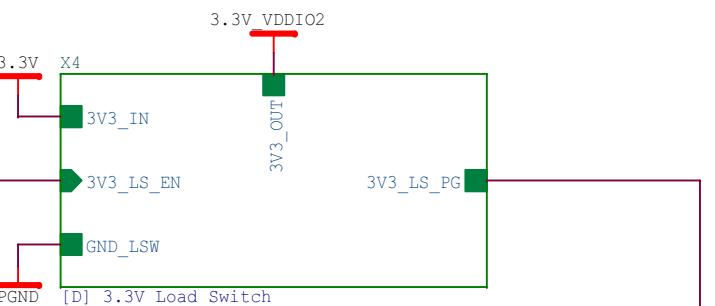
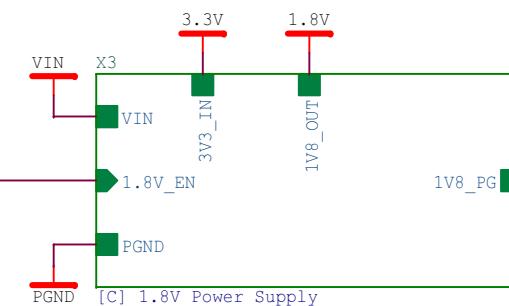
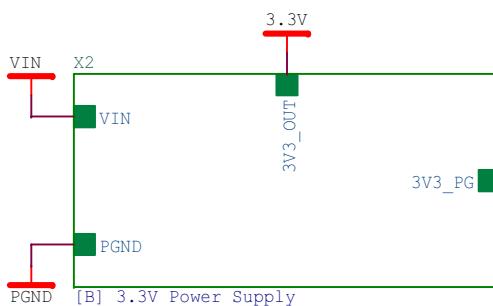
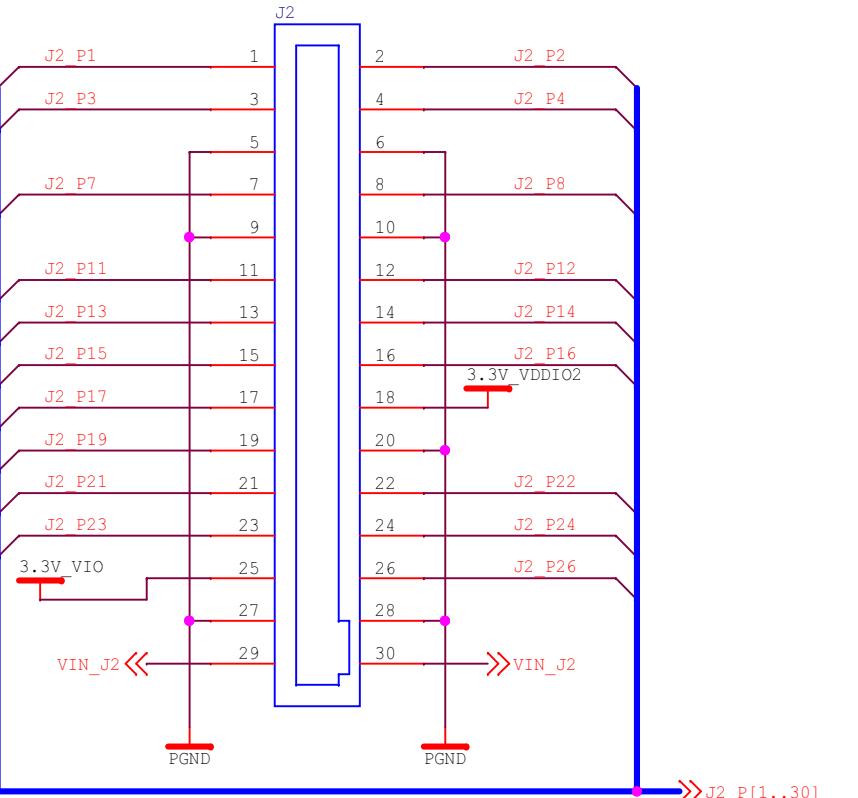
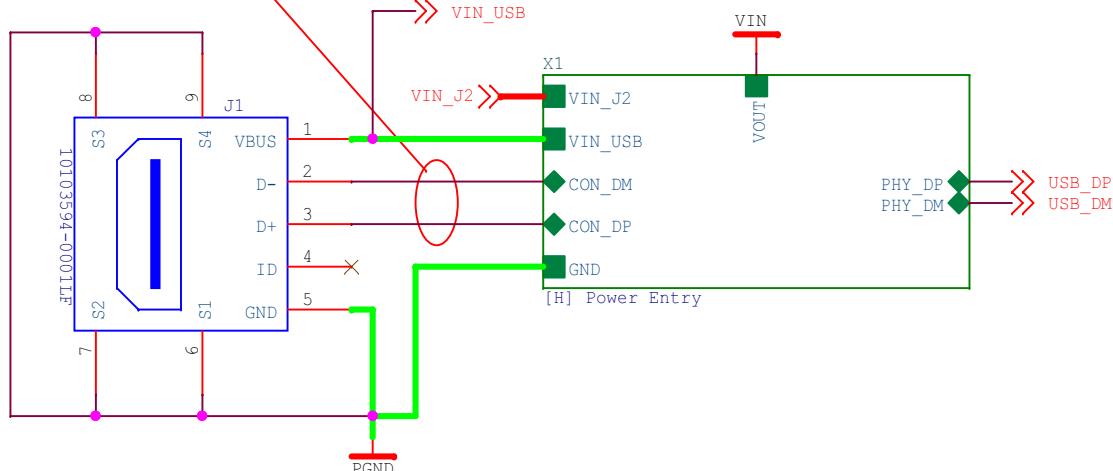


Rev.	Description	CO Number	Date	Approved By	Checked By
2	Alpha 2 Prototype	00001	09/01/2015	JJW	BEH
3	Beta 3 Prototype	00007	04/26/2016	JJW	BEH
4	Gamma 4 Prototype	00010	07/11/2016	JJW	BEH
4.1	snickerdoodle blue	00014	10/25/2016	JJW	BEH

Power/JTAG/SWD/BT Audio/I2C/DAC/ADC

ASSY 15081800/01-22: SAMTEC TFM-115-01-F-D-A  
 ASSY 15081800/02-22: SAMTEC SFM-115-L3-F-D-A  
 ASSY 15081800/03-22: SAMTEC TFM-115-01-F-D-A  
 ASSY 15081800/04-22: SAMTEC SFM-115-L3-F-D-A  
 ASSY 15081800/05-22: SAMTEC TFM-115-01-F-D-A  
 ASSY 15081800/06-22: SAMTEC SFM-115-L3-F-D-A

Layout Note: CON\_DM and CON\_DP form a 90 ohm differential pair.



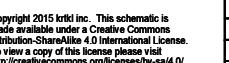
Minimum Trace Ratings	
6000mA	
4000mA	
2000mA	
1000mA	
200mA	

Minimum Plane Ratings	
+VIN	4000mA
+3.3V	4000mA
+1.8V	2000mA
+3.3V_VDDIO2	4000mA
+1.0V_CORE	6000mA
+1.8V_AUX	2000mA
+1.2V_LPDDR	2000mA
+3.3V_VIO	4000mA



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TITLE		snickerdoodle FPGA Module	
PATH		/	
DESCRIPTION		Top Level Block Diagram	
SIZE	DRAWING NO.	REV	
B	15081800-01	4.1	
SHEET 1	of 30		

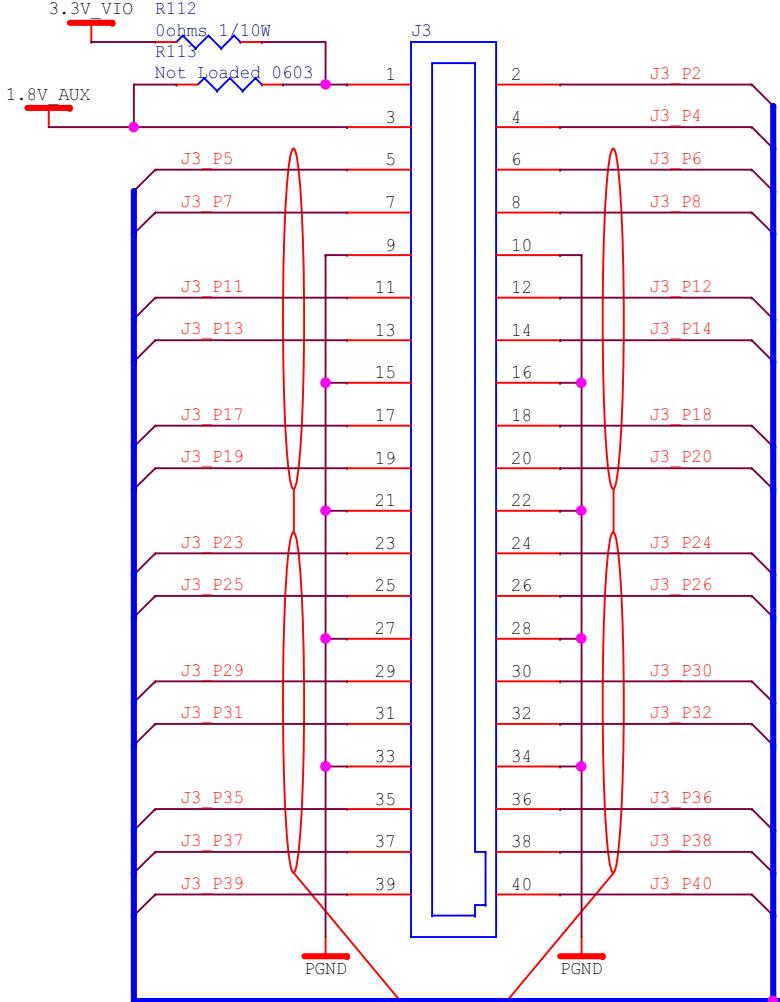


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**Warning: snickerdoodle rev 3 and earlier have 1.8V on pin 1 and an unconnected pin 3. Please confirm compatibility of 3.3V default on pin 1 and 1.8V on pin 3 prior to connection of external hardware.**

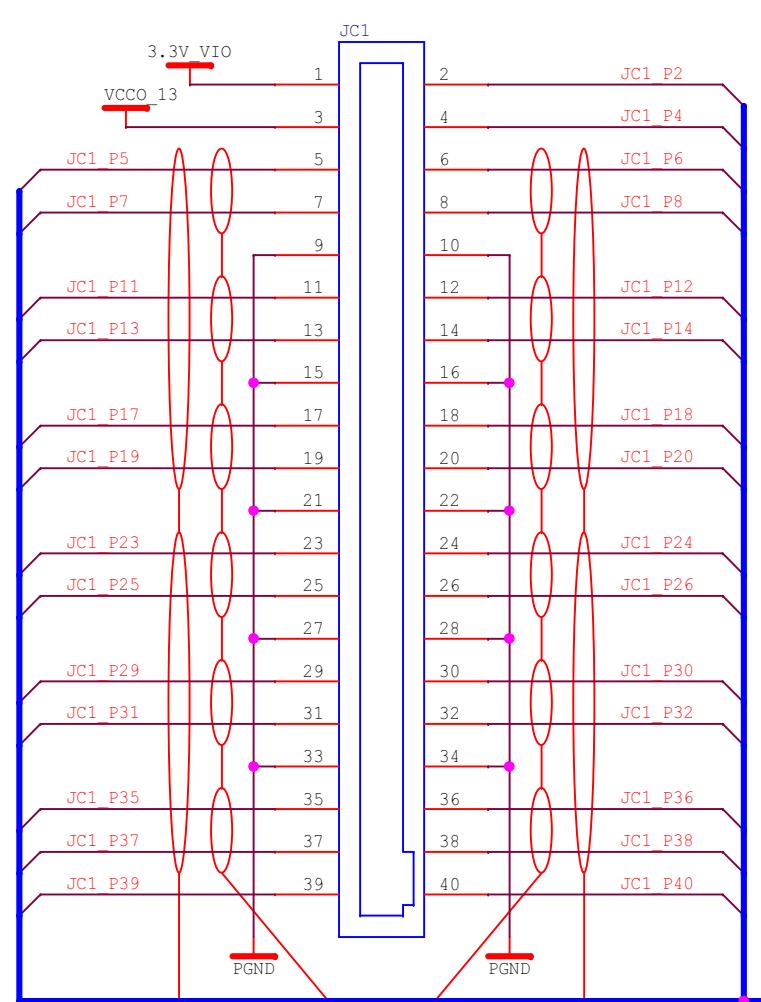
CPU GPIO/USB ULPI/GigE RGMII/SPI/I2C/UART/CAN

ASSY 15081800/01-22: SAMTEC TFM-120-01-F-D-A  
 ASSY 15081800/02-22: SAMTEC SFM-120-L3-F-D-A  
 ASSY 15081800/03-22: SAMTEC TFM-120-01-F-D-A  
 ASSY 15081800/04-22: SAMTEC SFM-120-L3-F-D-A  
 ASSY 15081800/05-22: SAMTEC TFM-120-01-F-D-A  
 ASSY 15081800/06-22: SAMTEC SFM-120-L3-F-D-A



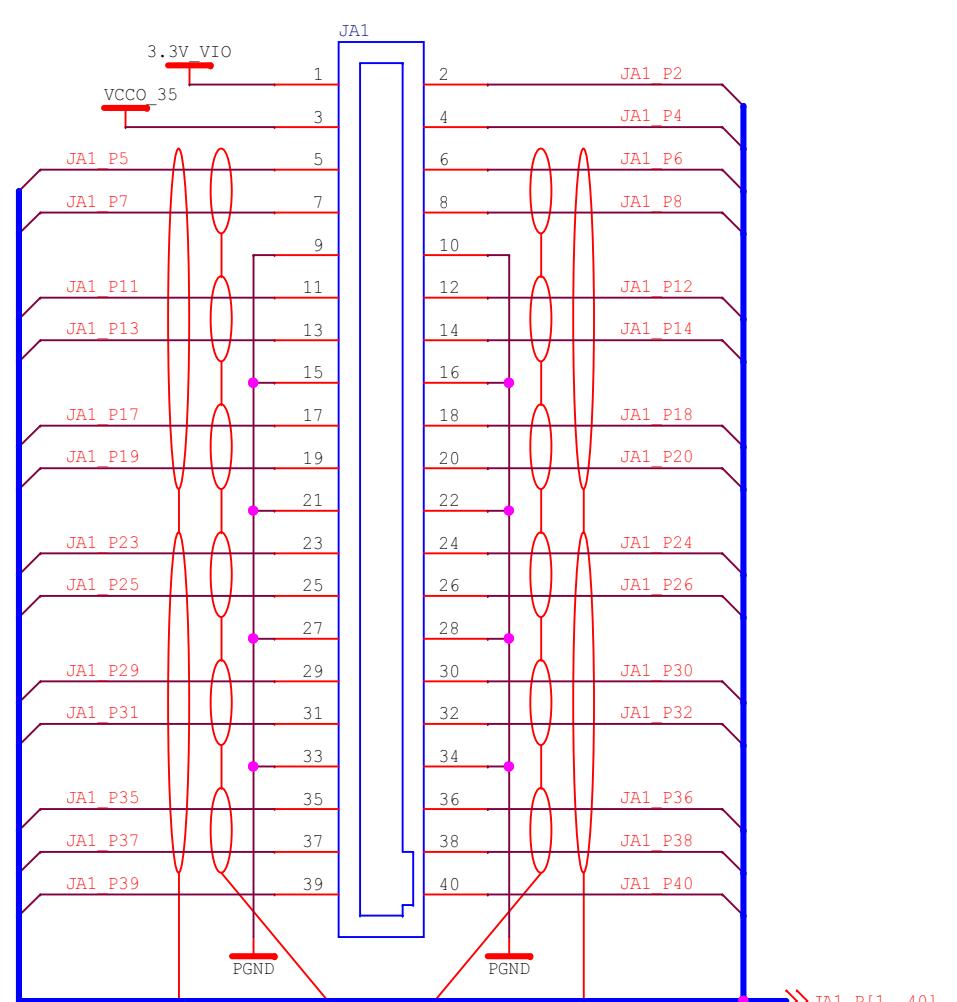
FPGA I/O

ASSY 15081800/01-22: NOT STUFFED  
 ASSY 15081800/02-22: NOT STUFFED  
 ASSY 15081800/03-22: SAMTEC TFM-120-01-F-D-A  
 ASSY 15081800/04-22: SAMTEC SFM-120-L3-F-D-A  
 ASSY 15081800/05-22: SAMTEC TFM-120-01-F-D-A  
 ASSY 15081800/06-22: SAMTEC SFM-120-L3-F-D-A



FPGA I/O

ASSY 15081800/01-22: SAMTEC TFM-120-01-F-D-A  
 ASSY 15081800/02-22: SAMTEC SFM-120-L3-F-D-A  
 ASSY 15081800/03-22: SAMTEC TFM-120-01-F-D-A  
 ASSY 15081800/04-22: SAMTEC SFM-120-L3-F-D-A  
 ASSY 15081800/05-22: SAMTEC TFM-120-01-F-D-A  
 ASSY 15081800/06-22: SAMTEC SFM-120-L3-F-D-A



Layout Note: Grouped signal traces to be length matched to within 5mils with 50ohm single-ended characteristic impedance.

Layout Note: Each grouped pair of signals to have 100ohm differential characteristic impedance.

Layout Note: Grouped signal traces to be length matched to within 10mils.

Layout Note: Each grouped pair of signals to have 100ohm differential characteristic impedance.

Layout Note: Grouped signal traces to be length matched to within 10mils.

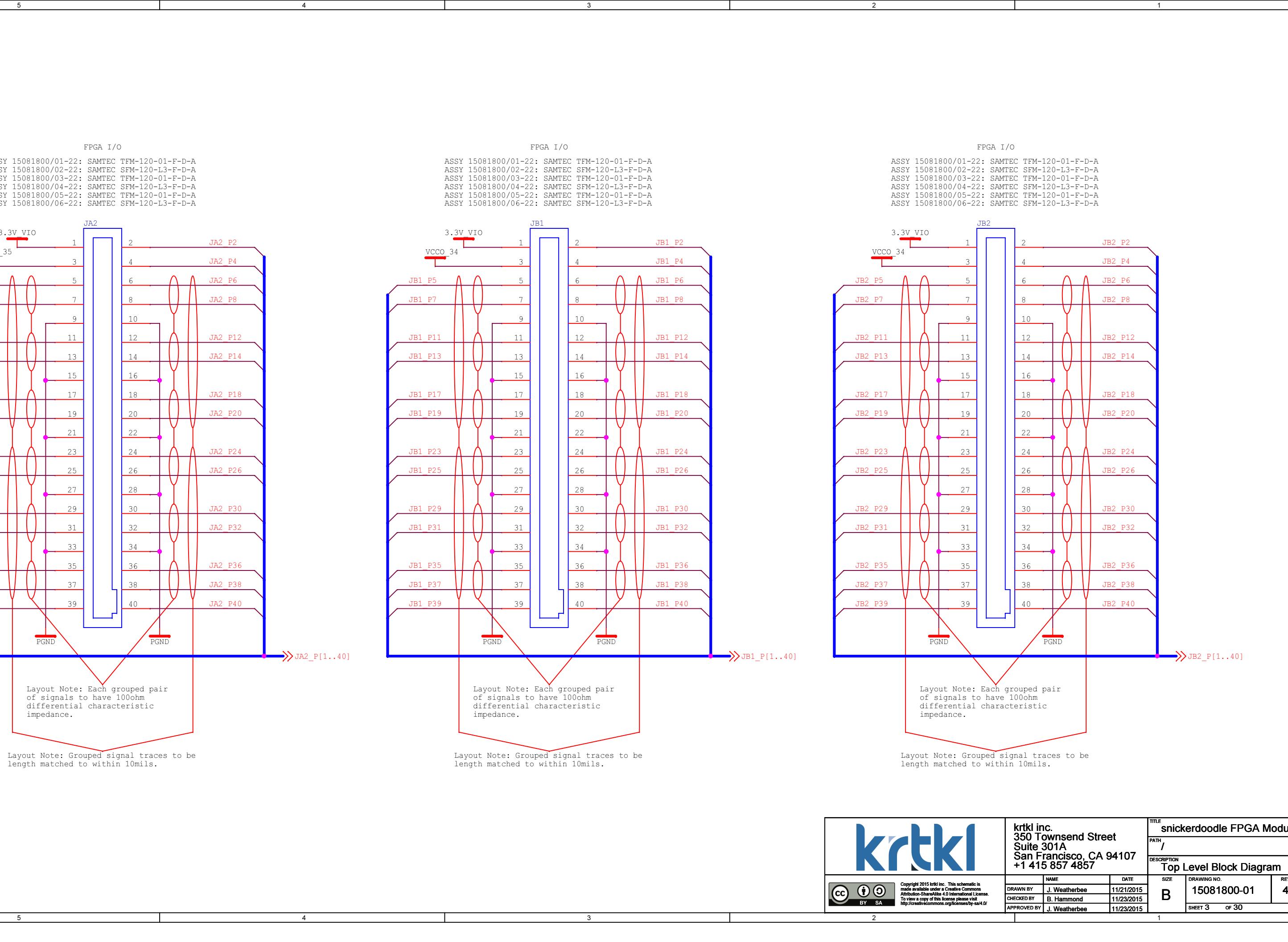


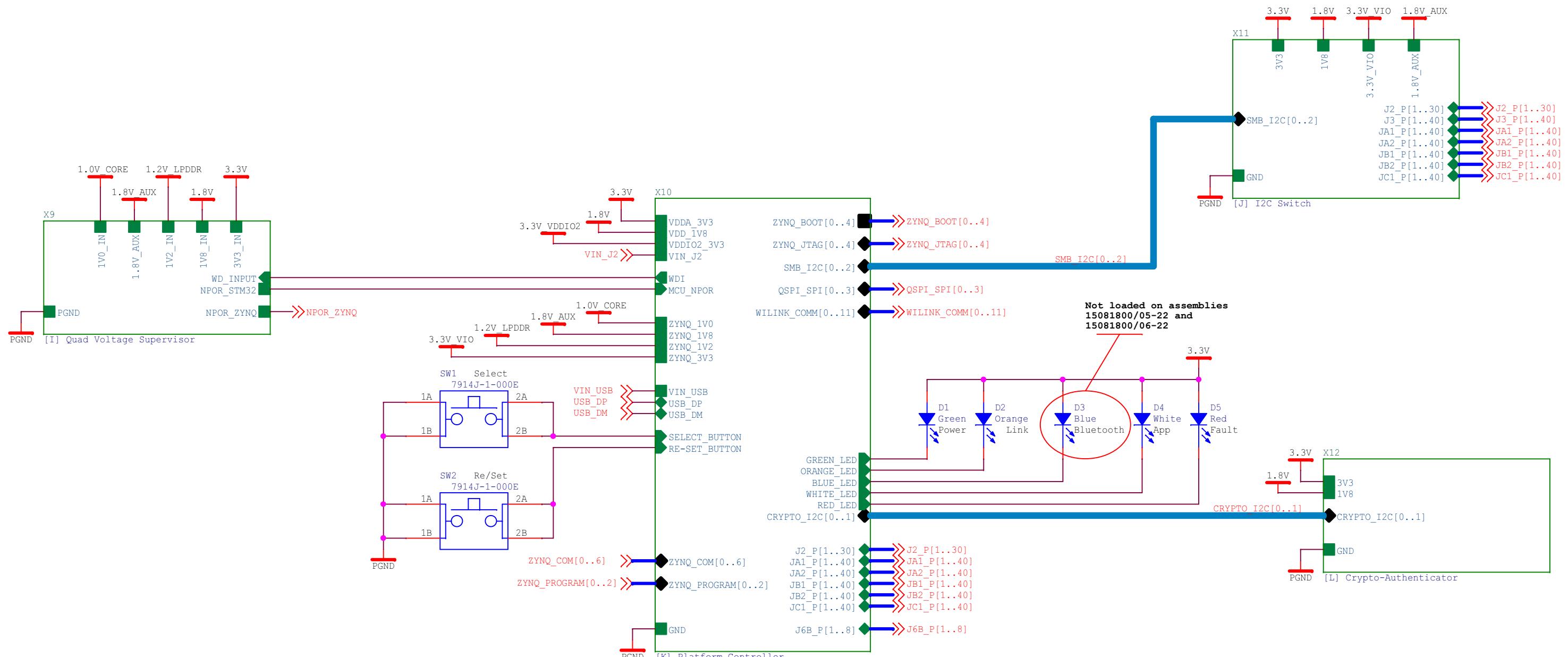
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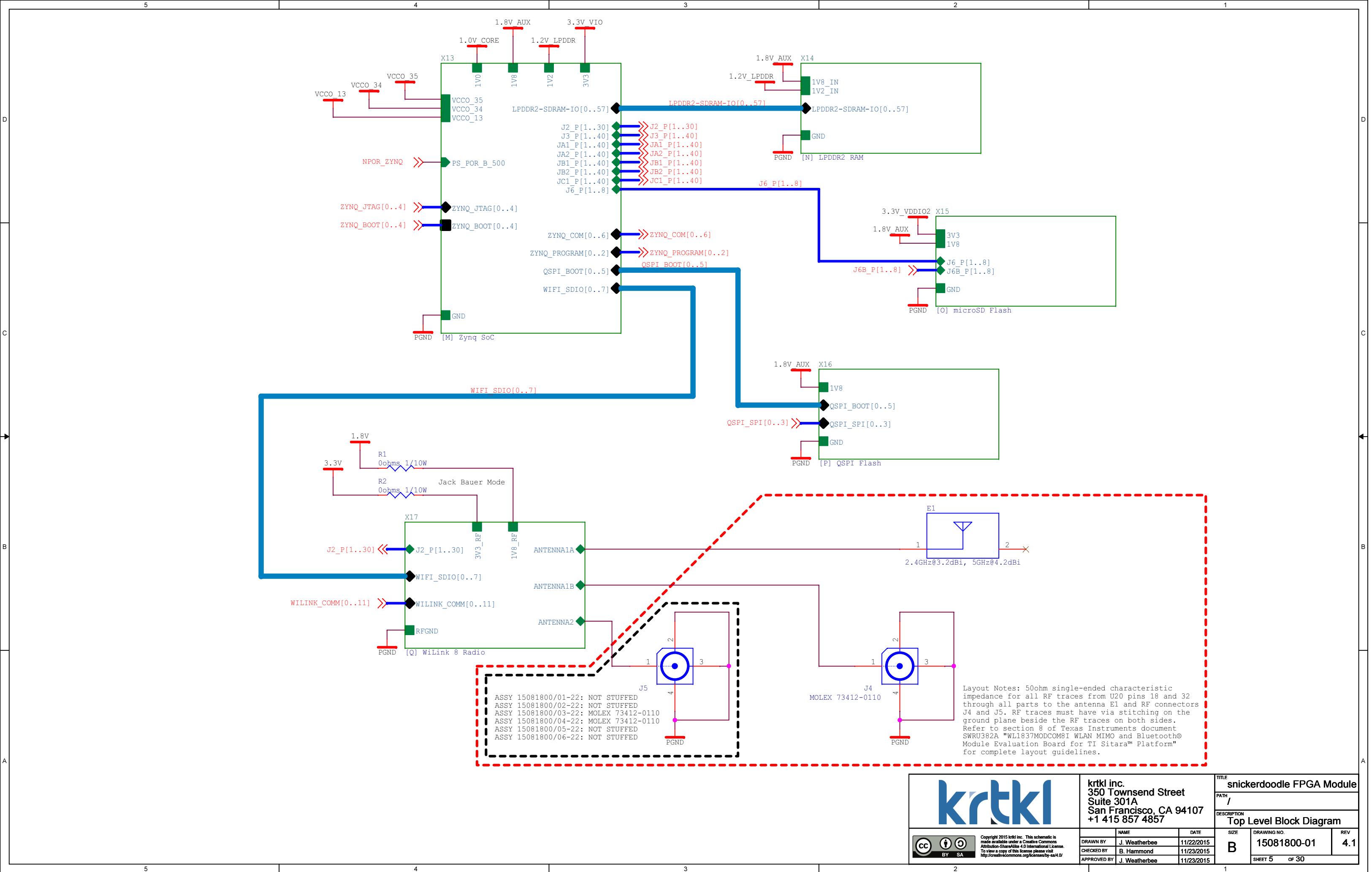
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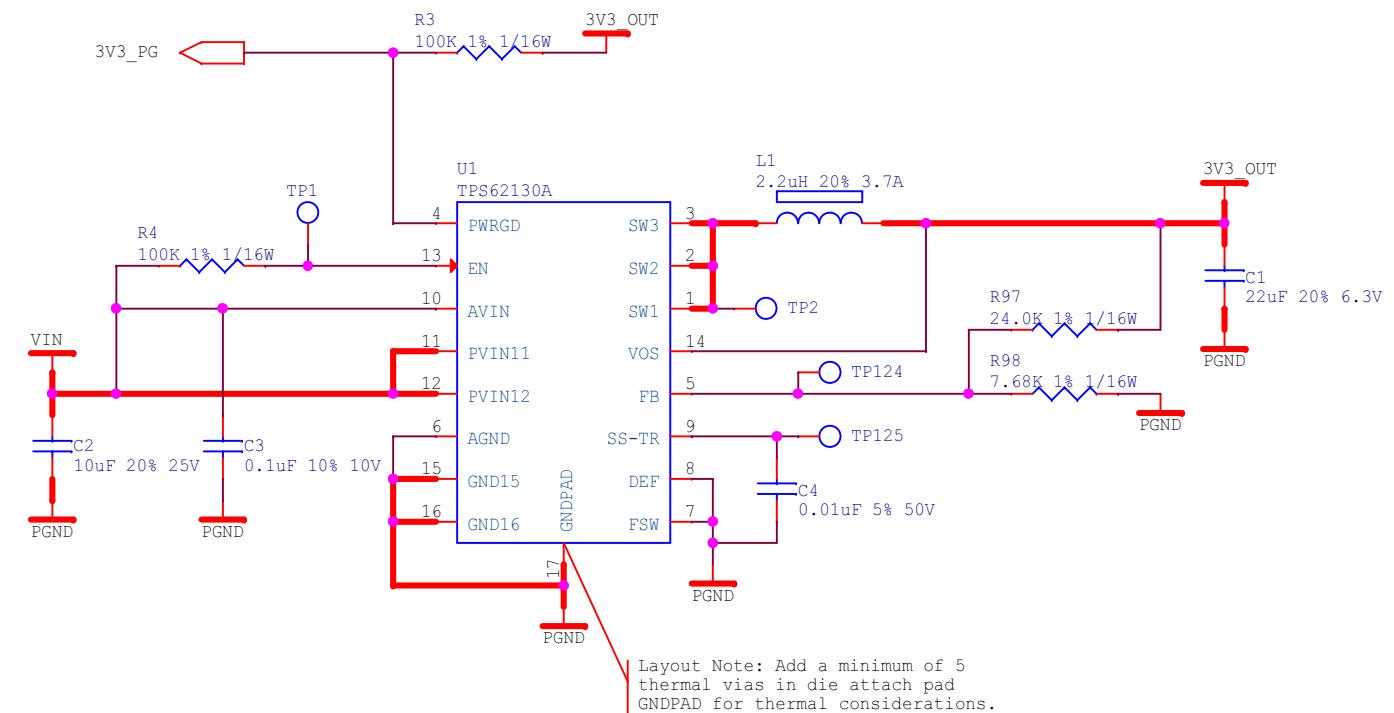
TITLE		
snickerdoodle FPGA Module		
PATH /		
DESCRIPTION		
SIZE	DRAWING NO.	REV
B	15081800-01	4.1
SHEET 2 of 30		



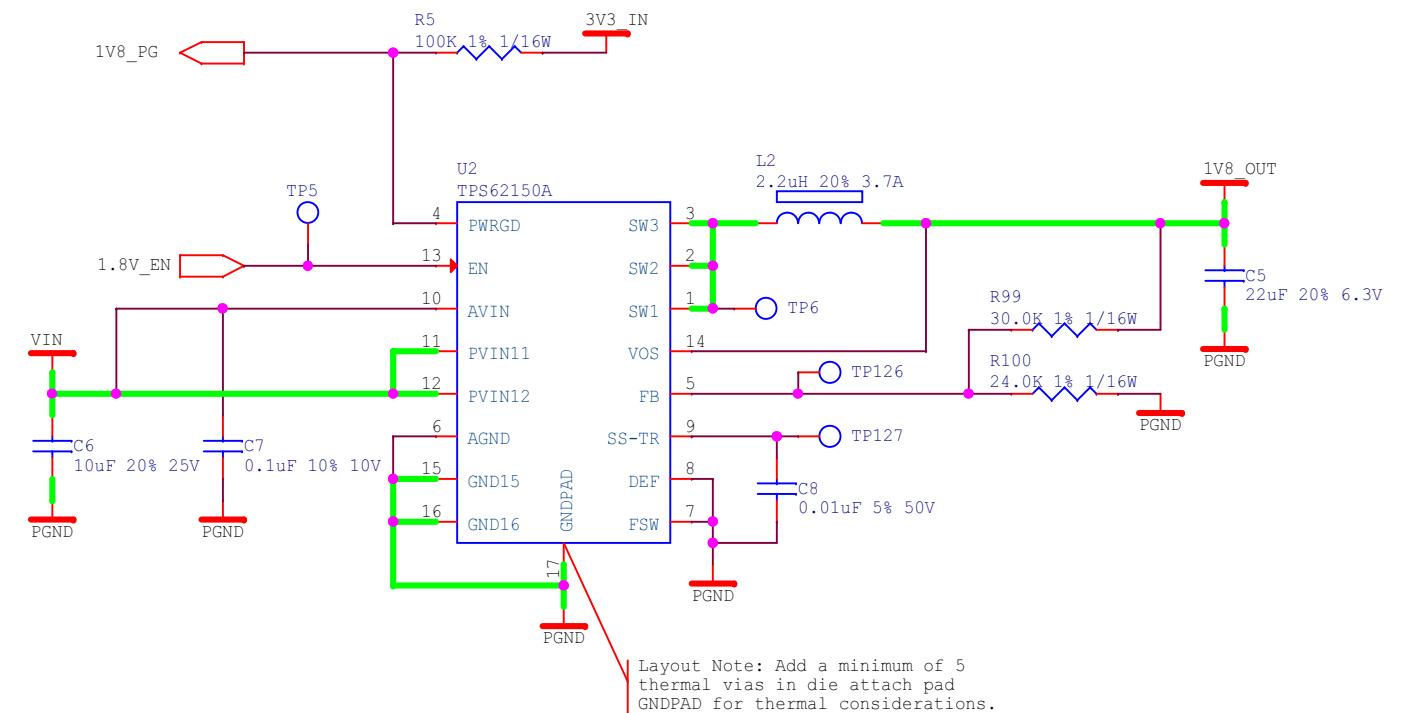


krtkl inc. 350 Townsend Street Suite 301A San Francisco, CA 94107 +1 415 857 4857			TITLE	snickerdoodle FPGA Module	
			PATH	/	
			DESCRIPTION	Top Level Block Diagram	
	NAME	DATE	SIZE <b>B</b>	DRAWING NO.	REV <b>4.1</b>
DRAWN BY	J. Weatherbee	11/22/2015		15081800-01	
CHECKED BY	B. Hammond	11/23/2015			
APPROVED BY	J. Weatherbee	11/23/2015		SHEET 4 OF 30	

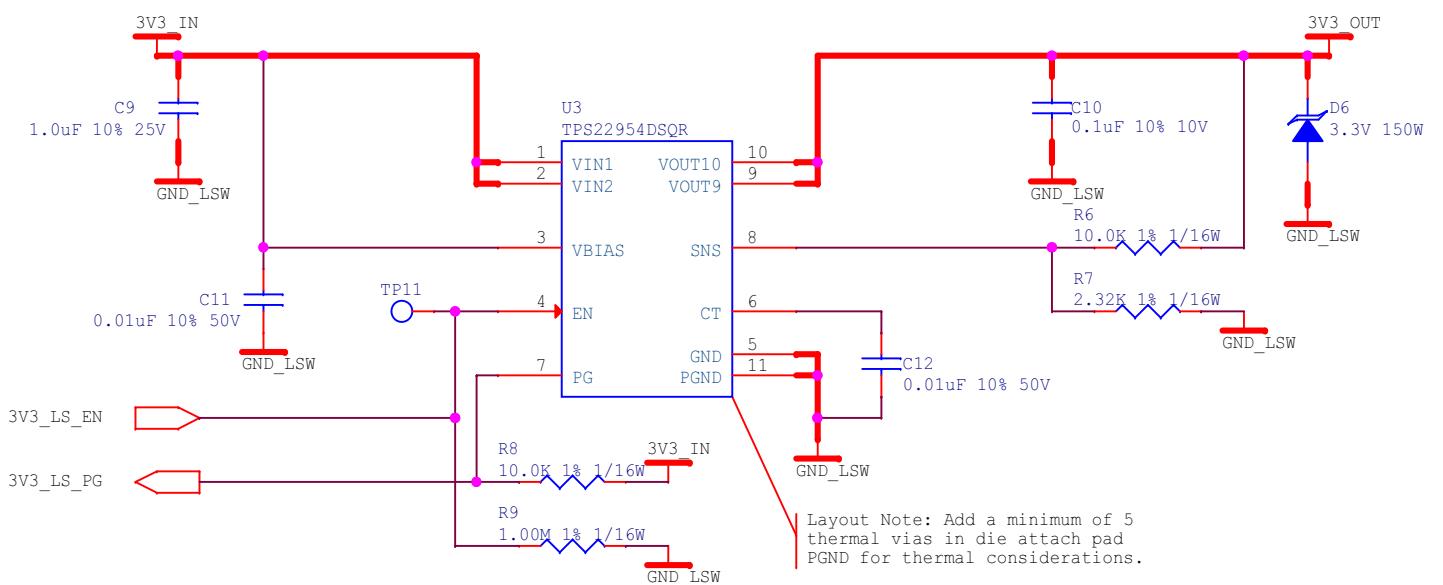




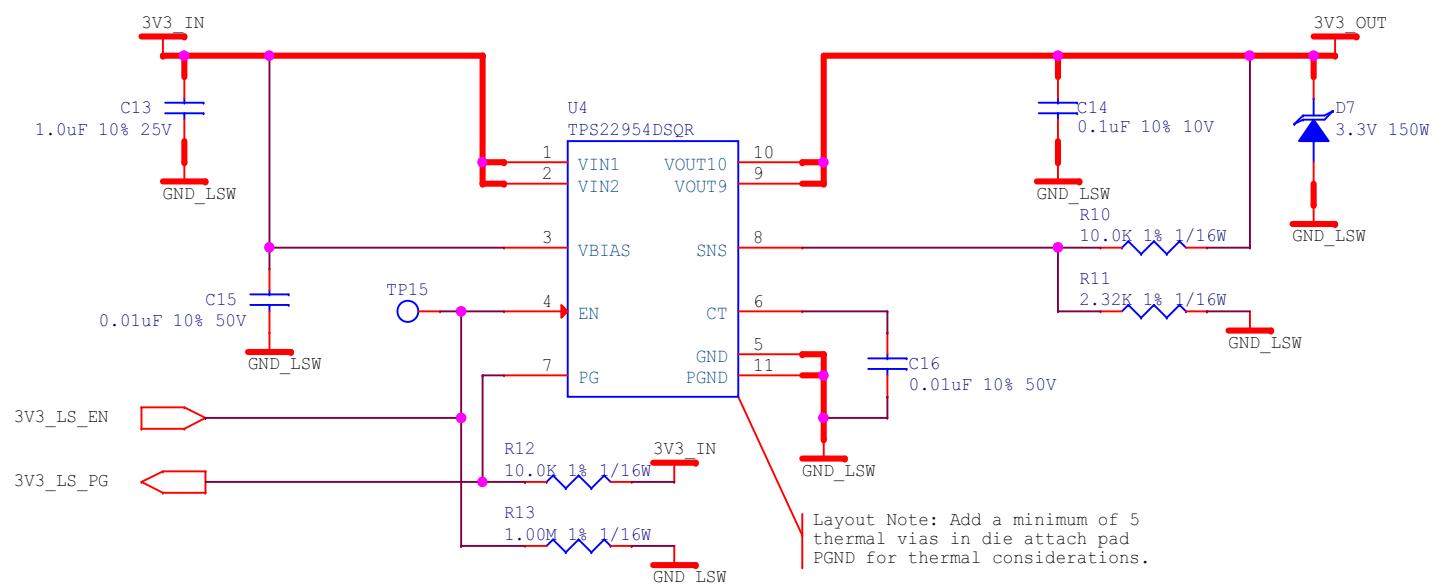
krtkl inc.			TITLE snickerdoodle FPGA Module		
			PATH /X2		
			DESCRIPTION 3.3V Power Supply		
	NAME	DATE		SIZE	DRAWING NO.
	B. Hammond	11/21/2015		B	15081800-01
	J. Weatherbee	11/23/2015			REV 4.1
	J. Weatherbee	11/23/2015			SHEET 6 of 30



krtkl inc.			TITLE snickerdoodle FPGA Module		
			PATH /X3		
			DESCRIPTION 1.8V Power Supply		
	NAME	DATE	SIZE	DRAWING NO.	REV
BY SA	B. Hammond	11/21/2015	B	15081800-01	4.1
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DRAWN BY	J. Weatherbee	11/23/2015	SHEET	7	of 30
CHECKED BY	J. Weatherbee	11/23/2015			
APPROVED BY	J. Weatherbee	11/23/2015			



krtkl inc.			TITLE snickerdoodle FPGA Module		
			PATH /X4		
			DESCRIPTION 3.3V Load Switch		
	Copyright 2015 krtkl inc. This schematic is made available under a Creative Commons Attribution-ShareAlike 4.0 International License. To view a copy of this license please visit <a href="http://creativecommons.org/licenses/by-sa/4.0/">http://creativecommons.org/licenses/by-sa/4.0/</a>		DRAWN BY	B. Hammond	DATE 11/21/2015
			CHECKED BY	J. Weatherbee	11/21/2015
			APPROVED BY	J. Weatherbee	11/21/2015
B	15081800-01	4.1	SHEET 8	of 30	

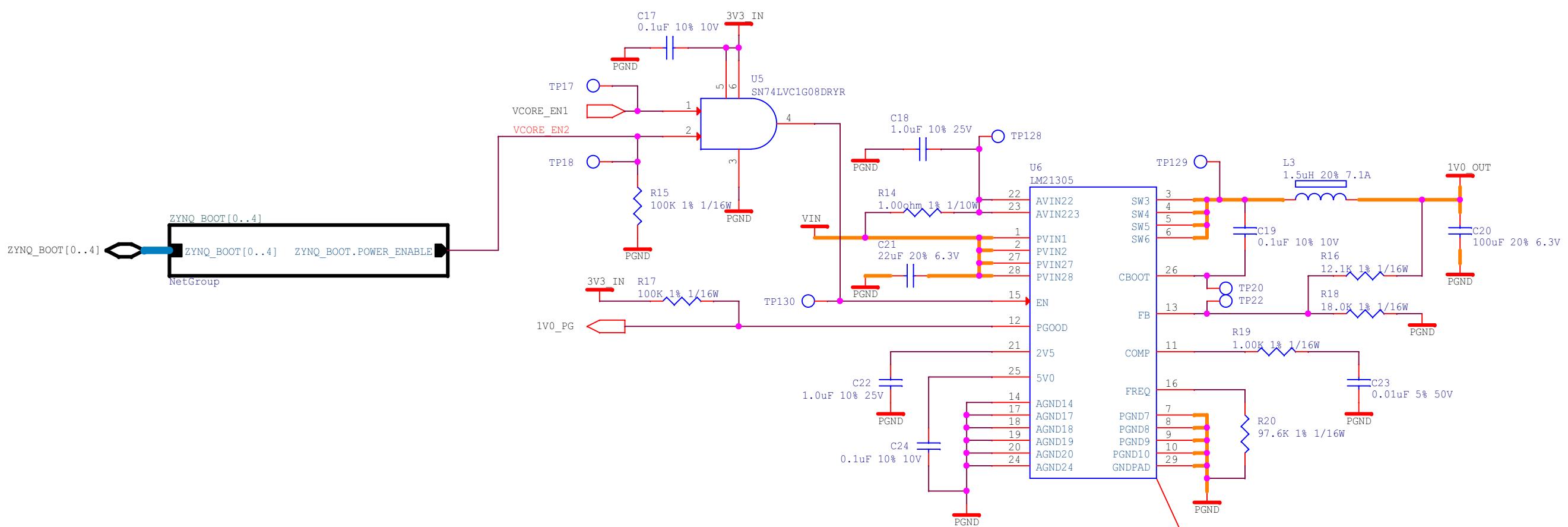


Layout Note: Add a minimum of 5 thermal vias in die attach pad PGND for thermal considerations.



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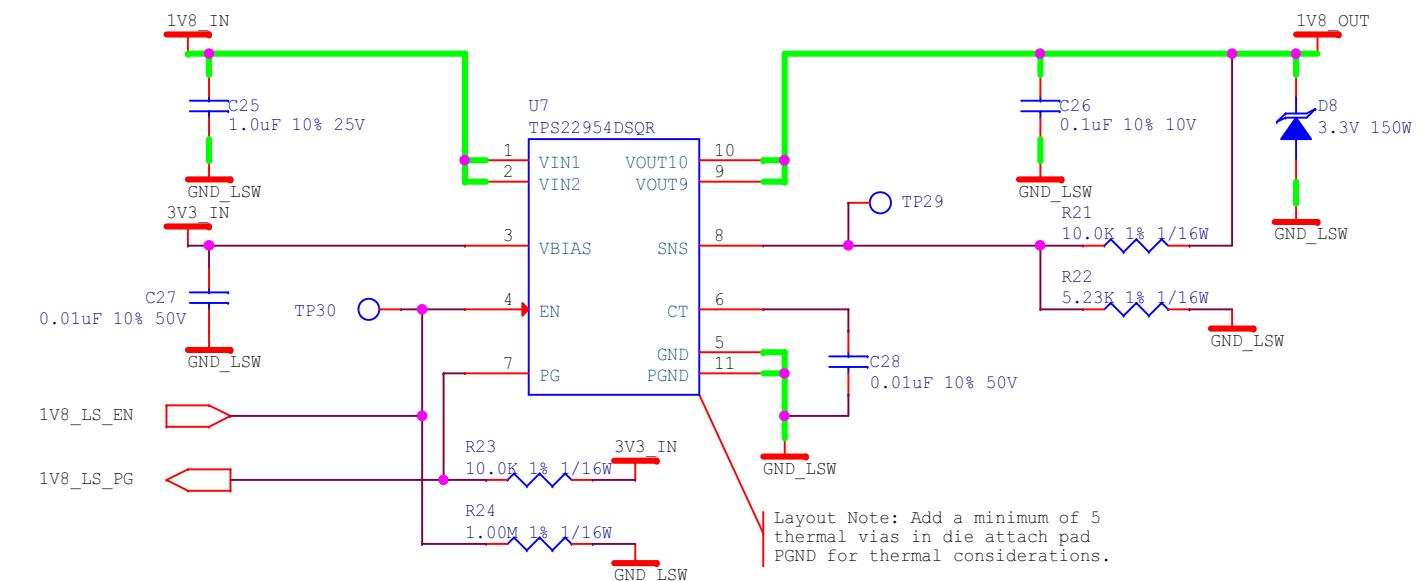
TITLE		
snickerdoodle FPGA Module		
PATH		
/X8		
DESCRIPTION		
3.3V Load Switch		
DRAWN BY	NAME	DATE
B. Hammond		11/21/2015
CHECKED BY	J. Weatherbee	11/21/2015
APPROVED BY	J. Weatherbee	11/21/2015
SHEET	DRAWING NO.	REV
9	15081800-01	4.1
SHEET 9 of 30		



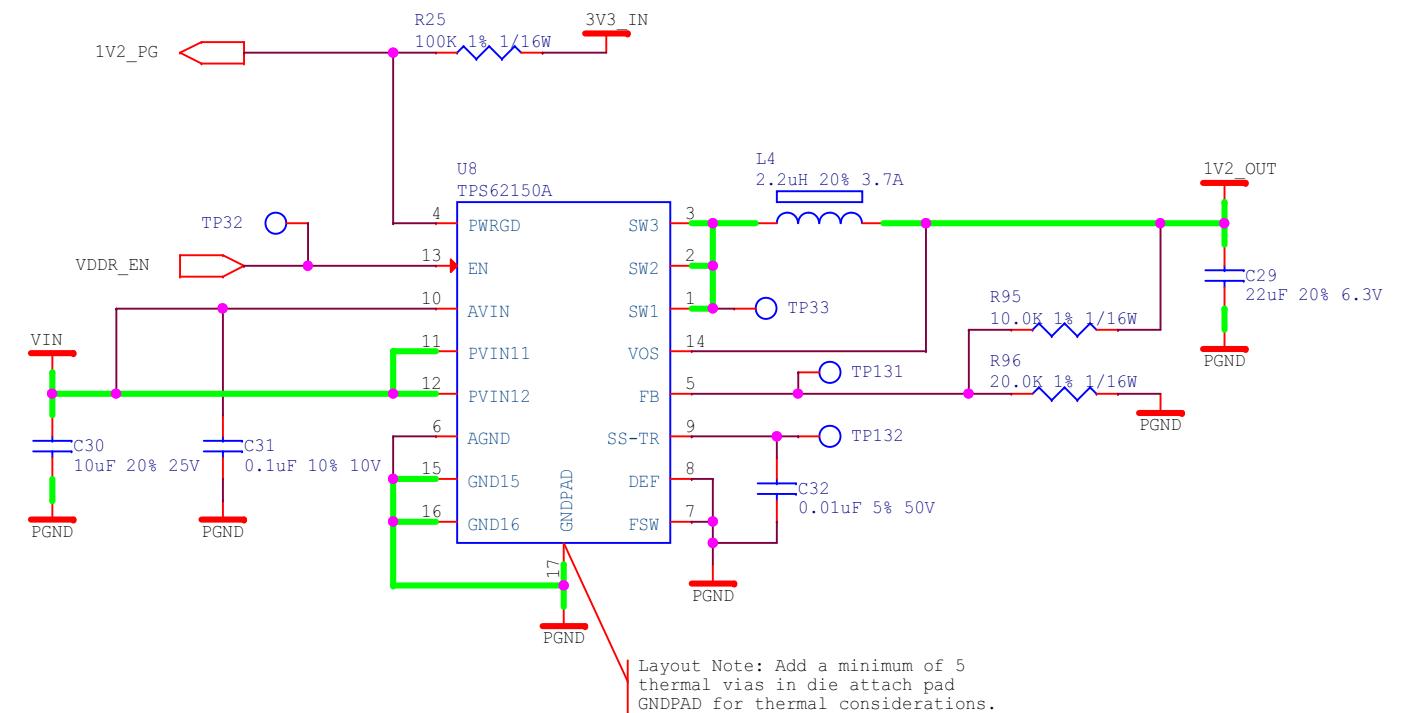
Layout Note: Add a minimum of 9 thermal vias in die attach pad GNDPAD for thermal considerations.



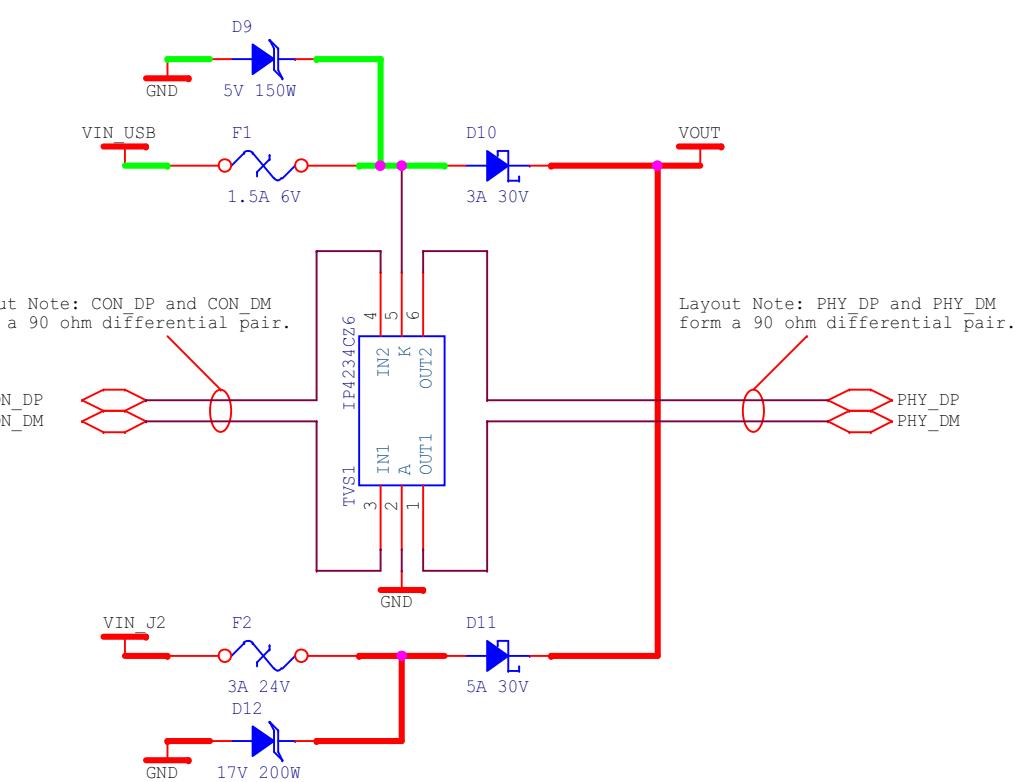
krtkl inc. 350 Townsend Street Suite 301A San Francisco, CA 94107 +1 415 857 4857		TITLE			
		snickerdoodle FPGA Module			
		PATH			
		/X5			
		DESCRIPTION			
		1.0V Power Supply			
DRAWN BY	B. Hammond	DATE	SIZE	DRAWING NO.	
CHECKED BY	J. Weatherbee	11/23/2015	B	15081800-01	REV
APPROVED BY	J. Weatherbee	11/23/2015		SHEET 10 OF 30	4.1



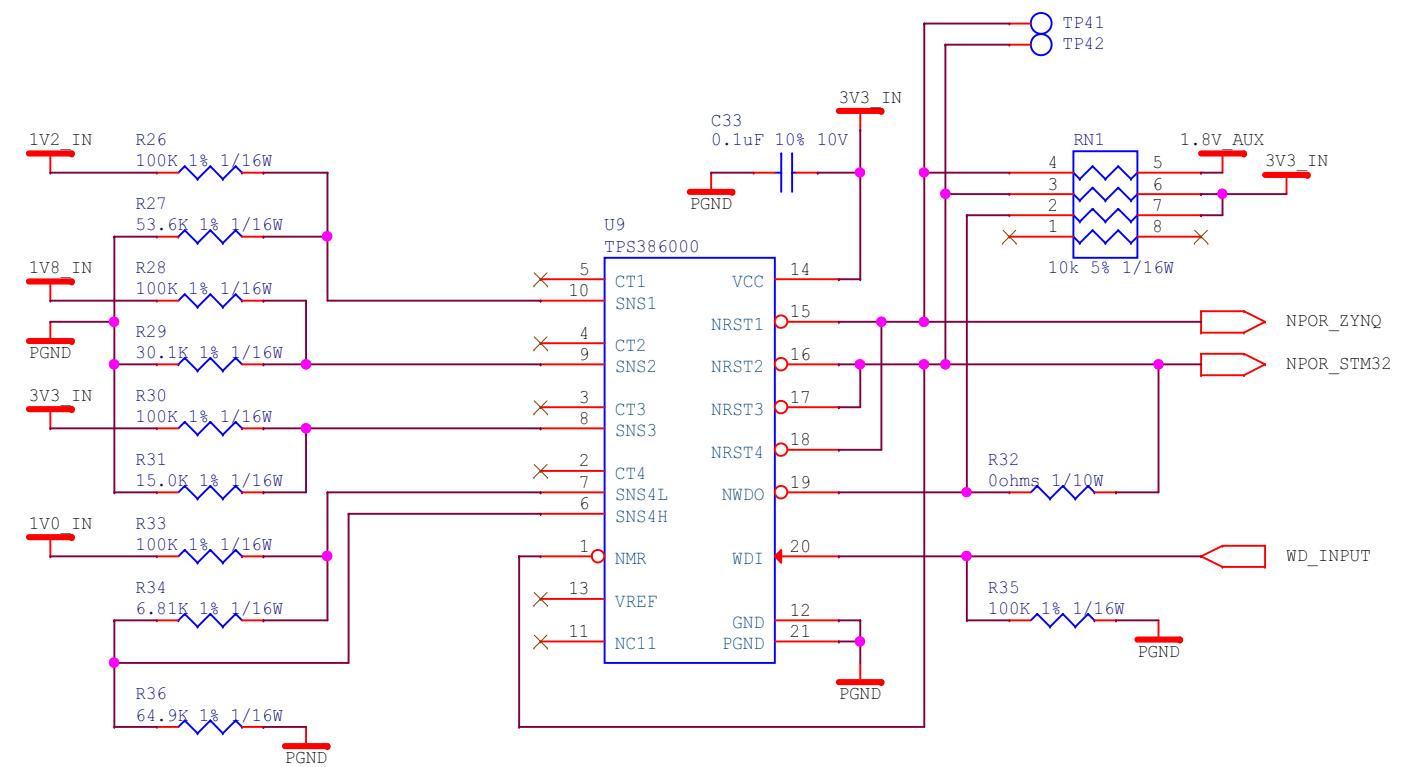
krtkl inc.			TITLE snickerdoodle FPGA Module		
			PATH /X6		
			DESCRIPTION 1.8V Load Switch		
	NAME	DATE	SIZE	DRAWING NO.	REV
BY SA	B. Hammond	11/21/2015	B	15081800-01	4.1
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CHECKED BY	J. Weatherbee	11/23/2015			
APPROVED BY	J. Weatherbee	11/23/2015			



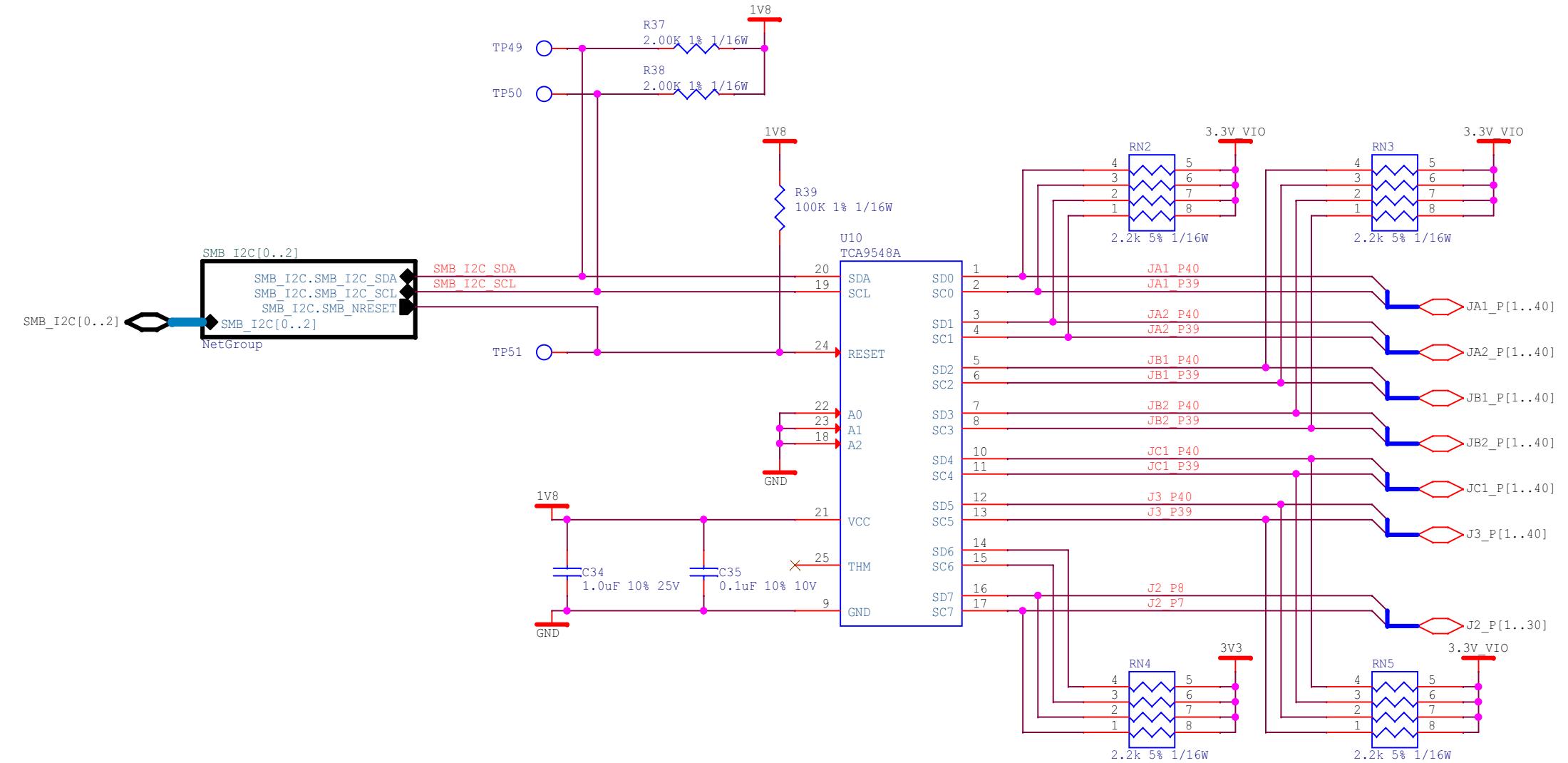
 <small>Copyright 2015 krtk inc. This schematic is made available under a Creative Commons Attribution-ShareAlike 4.0 International License. To view a copy of this license please visit <a href="http://creativecommons.org/licenses/by-sa/4.0/">http://creativecommons.org/licenses/by-sa/4.0/</a></small>	krtk inc. 350 Townsend Street Suite 301A San Francisco, CA 94107 +1 415 857 4857			TITLE snickerdoodle FPGA Module
	PATH /X7			
DESCRIPTION 1.2V Power Supply				
DRAWN BY	NAME	DATE	SIZE	DRAWING NO.
B. Hammond		11/21/2015	B	15081800-01
CHECKED BY	J. Weatherbee	11/23/2015		
APPROVED BY	J. Weatherbee	11/23/2015		
REV 4.1				
SHEET 12 OF 30				

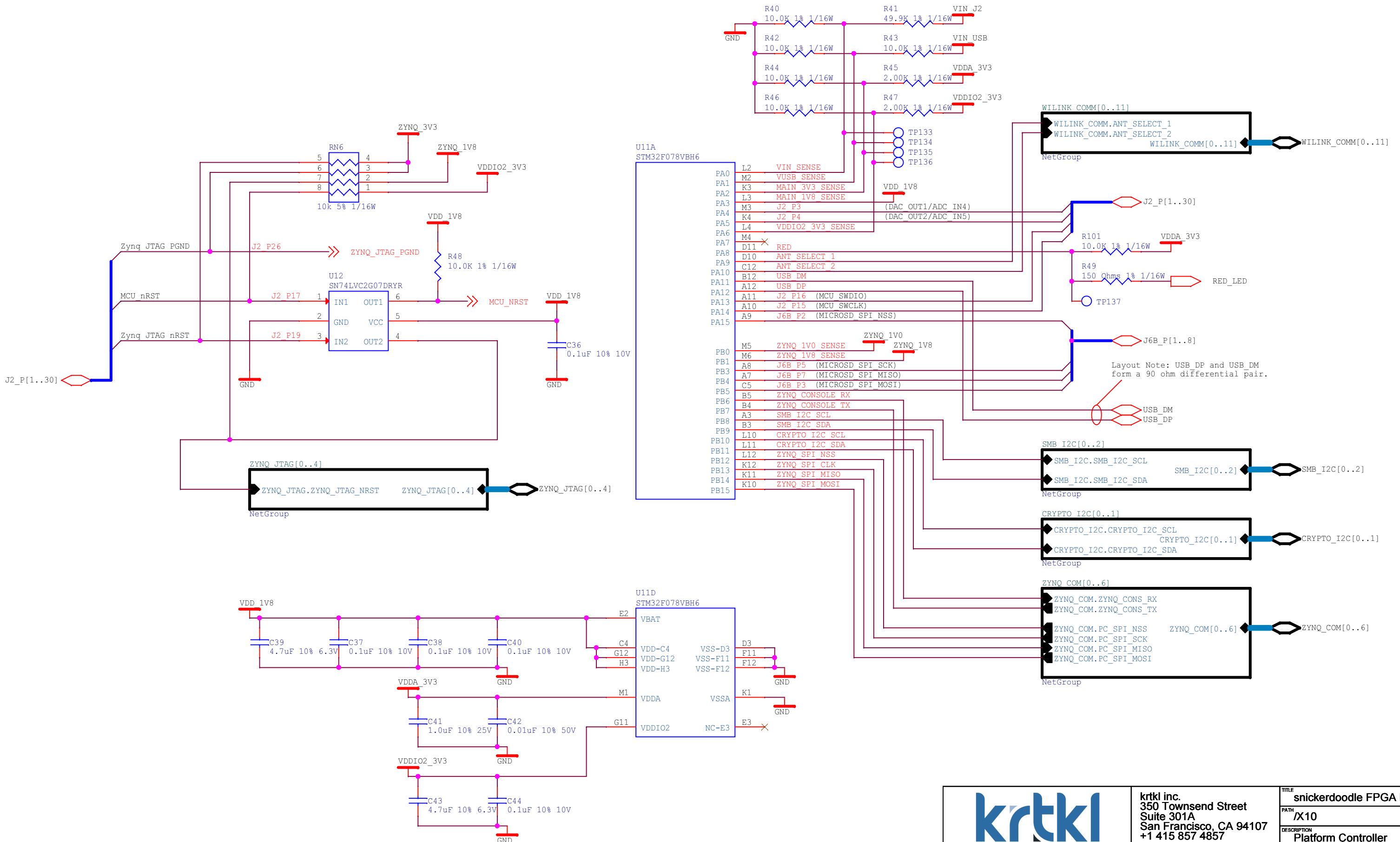


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	PATH <b>/X1</b>			SIZE <b>B</b>	
DESCRIPTION <b>Power Entry</b>			DRAWING NO. <b>15081800-01</b>	REV <b>4.1</b>	
DRAWN BY <b>J. Weatherbee</b>	NAME <b>J. Weatherbee</b>	DATE <b>11/23/2015</b>			
CHECKED BY <b>J. Weatherbee</b>	NAME <b>J. Weatherbee</b>	DATE <b>11/23/2015</b>			
APPROVED BY <b>J. Weatherbee</b>	NAME <b>J. Weatherbee</b>	DATE <b>11/23/2015</b>			
SHEET <b>13</b> OF <b>30</b>					1



krtkl inc.			TITLE snickerdoodle FPGA Module		
			PATH /X9		
			DESCRIPTION Quad Voltage Supervisor		
	NAME	DATE		SIZE	DRAWING NO.
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CHECKED BY	J. Weatherbee	11/23/2015			
APPROVED BY	J. Weatherbee	11/23/2015			
SHEET 14 OF 30					

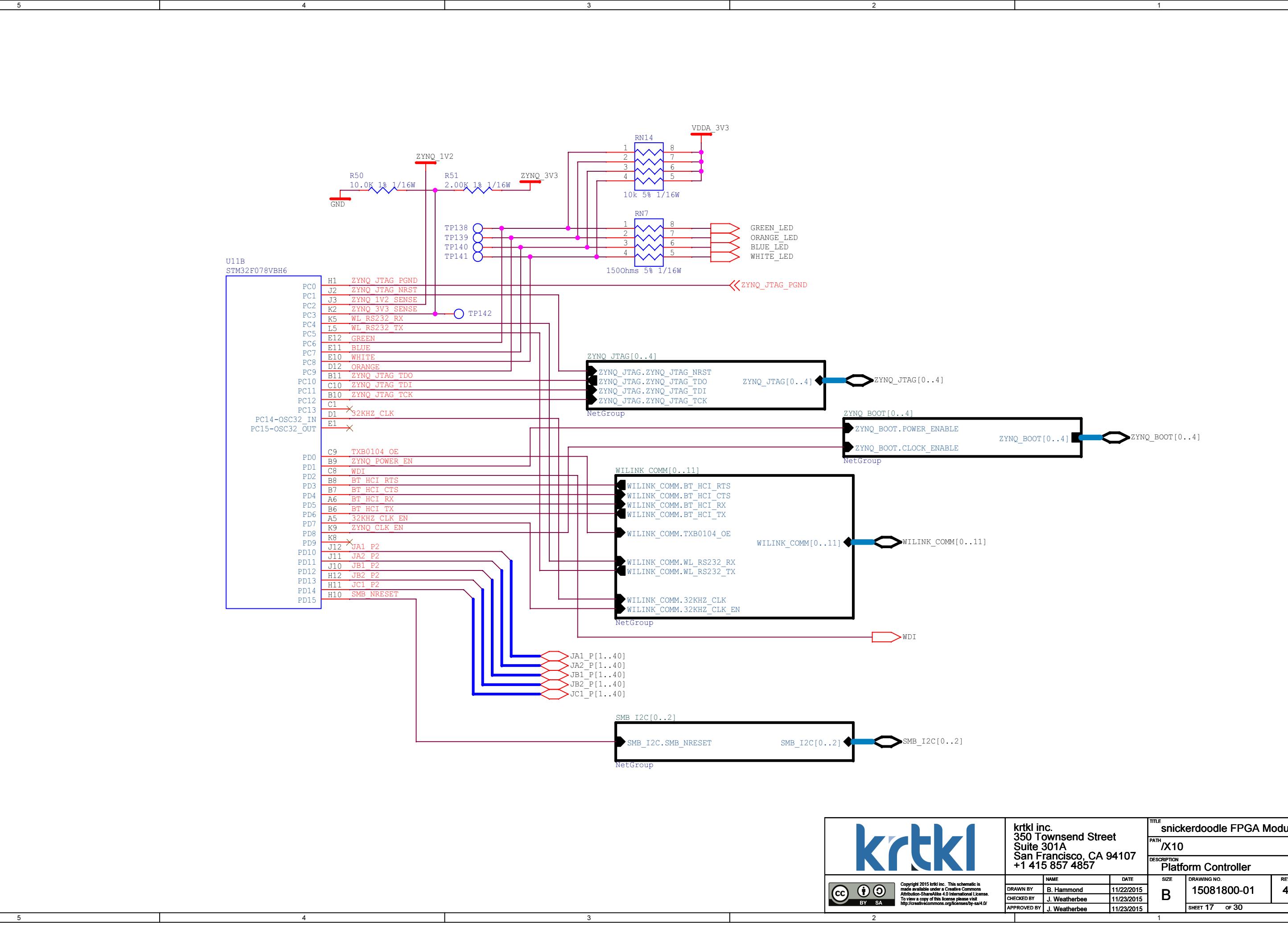


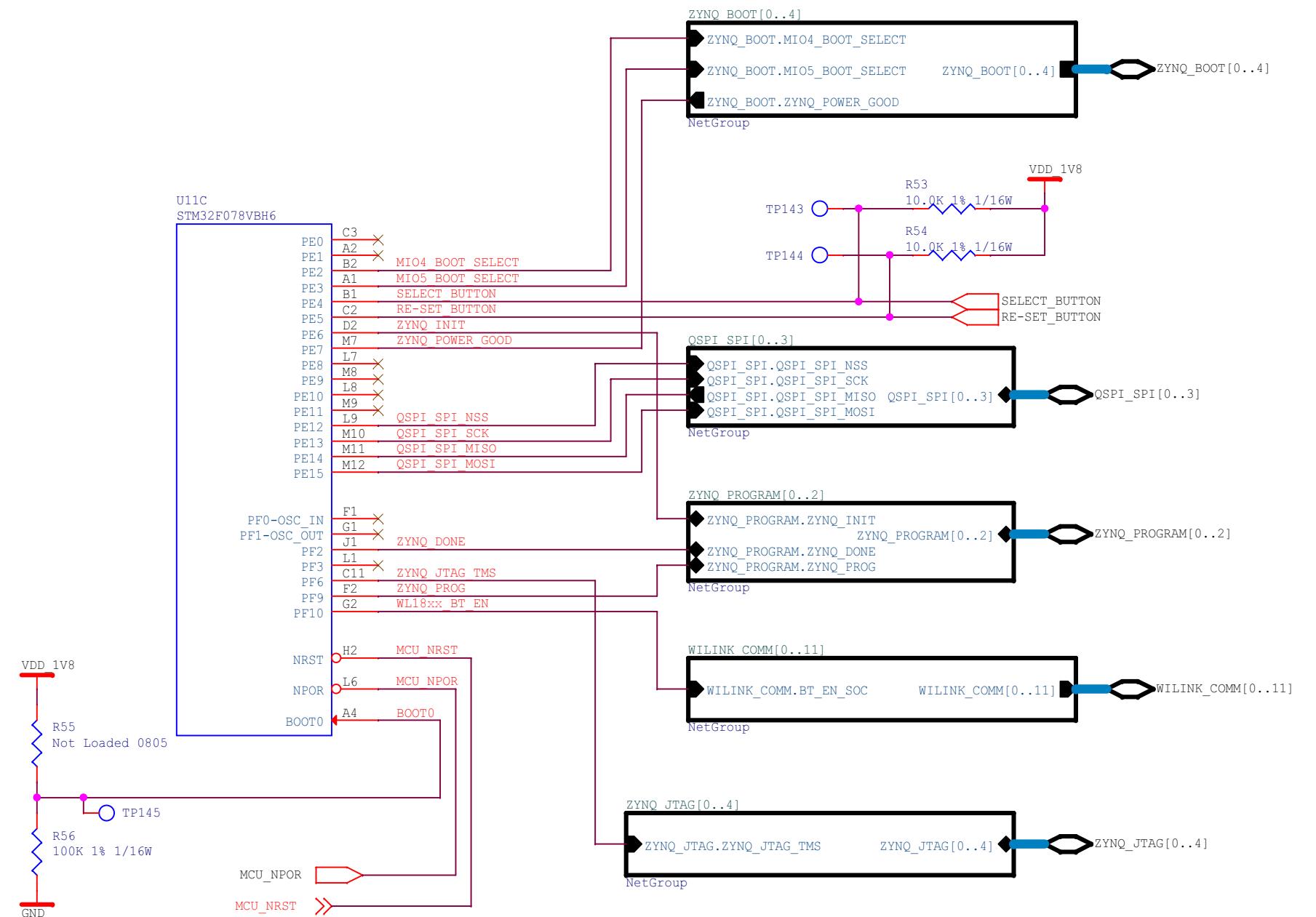


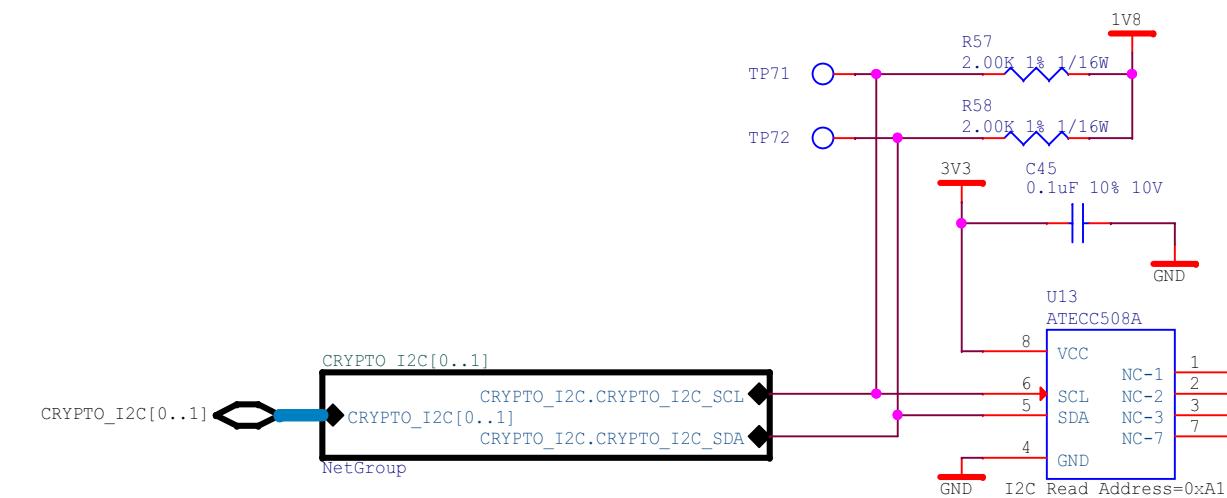
TITLE		
snickerdoodle FPGA Module		
PATH		
/X10		
DESCRIPTION		
Platform Controller		
SIZE	DRAWING NO.	REV
B	15081800-01	4.1
SHEET 16 OF 30		



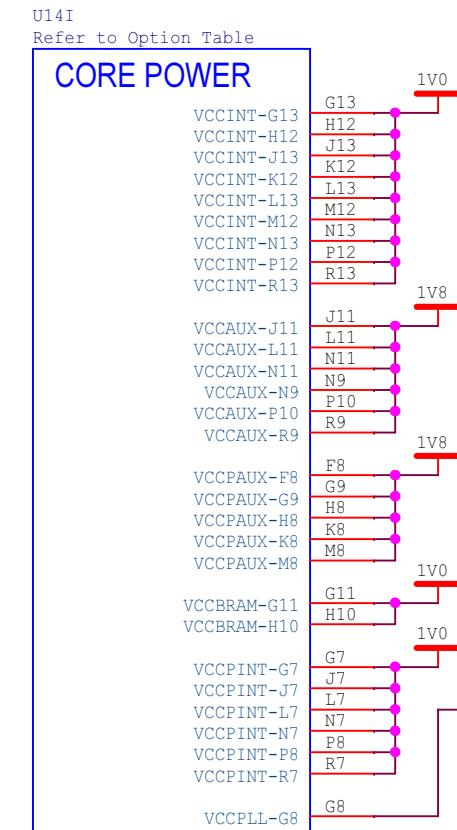
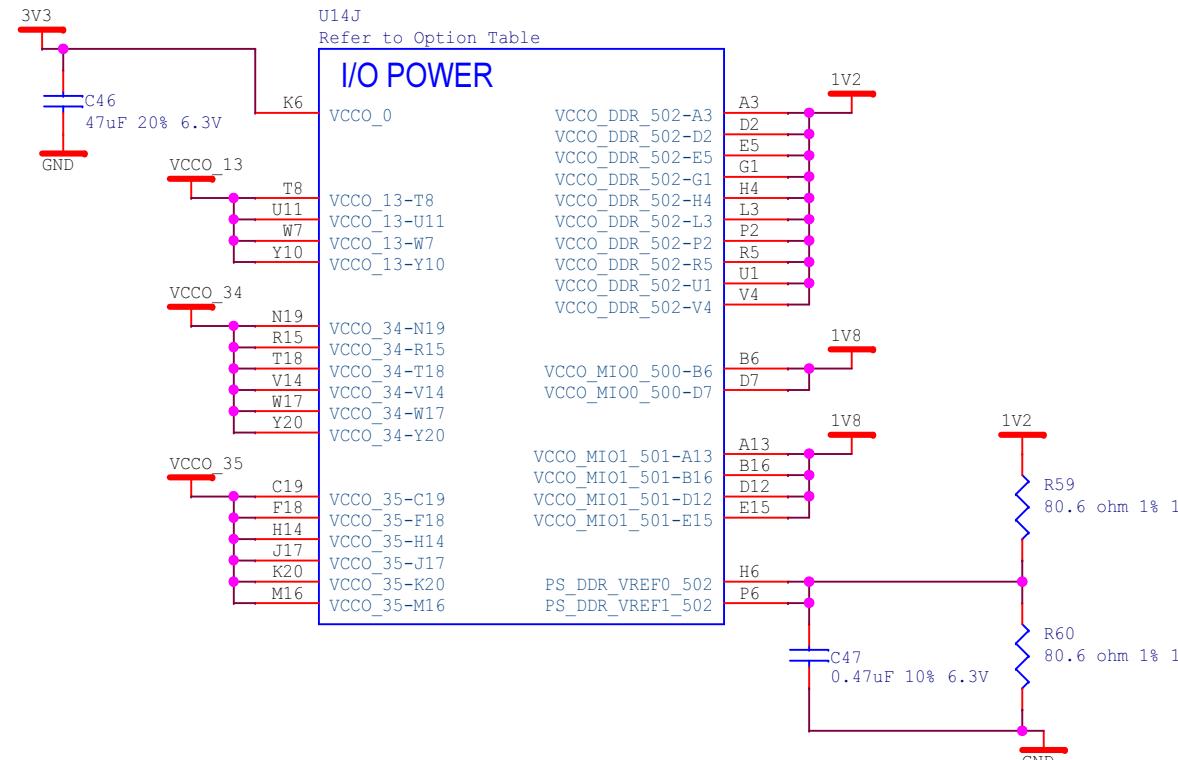
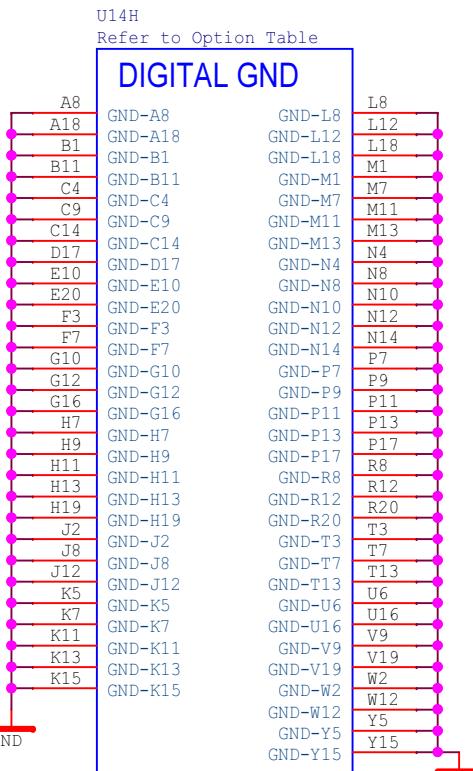
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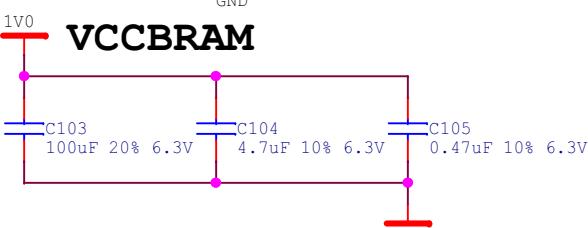
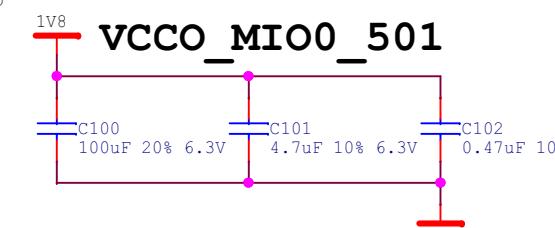
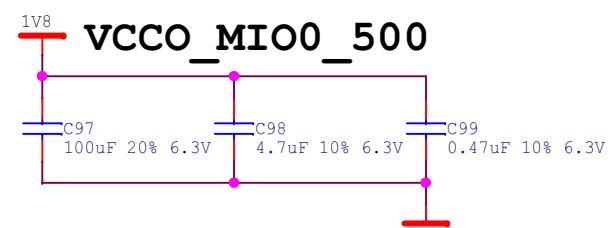
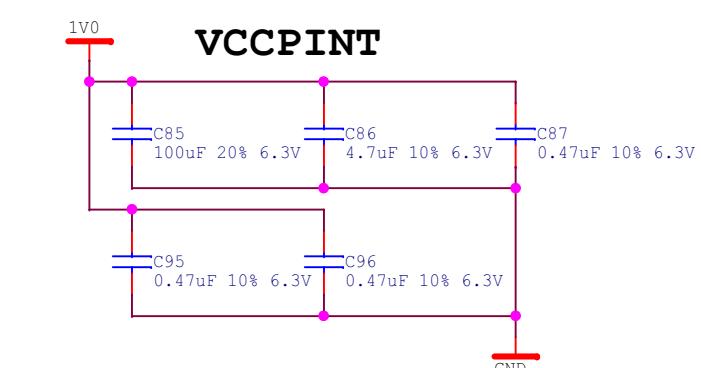
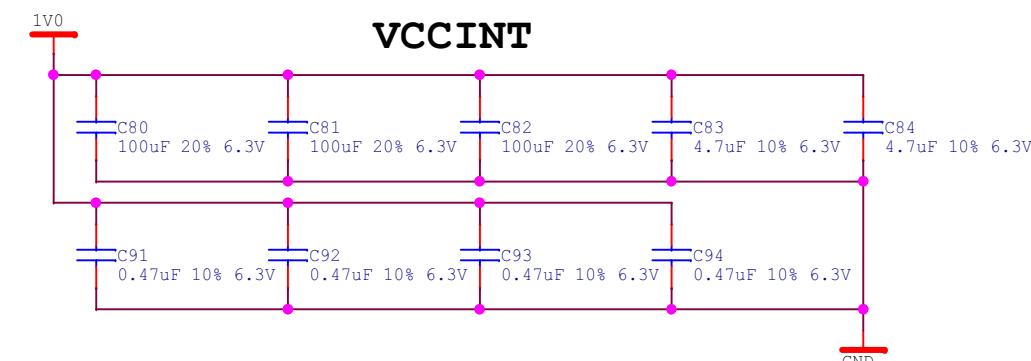
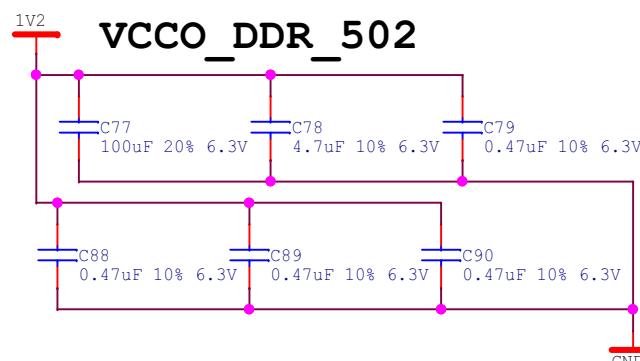
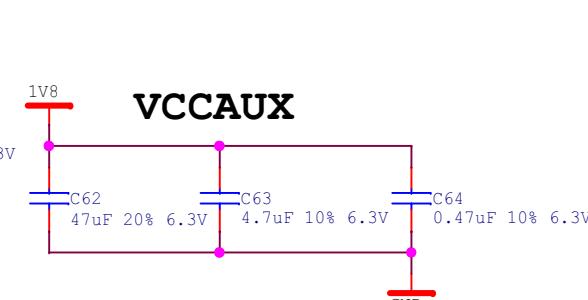
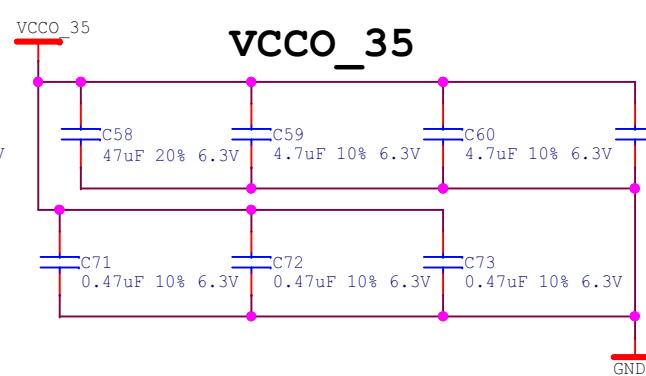
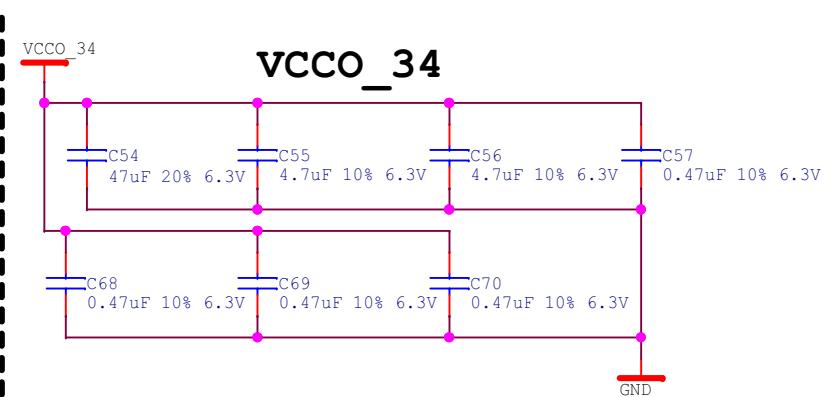
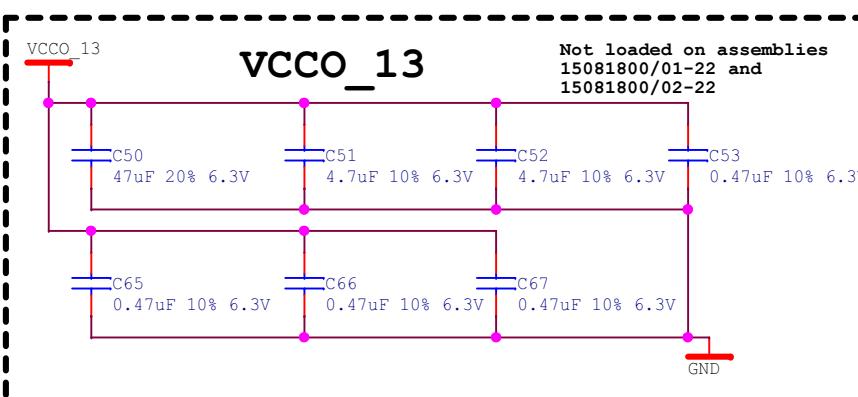




	krkt inc. 350 Townsend Street Suite 301A San Francisco, CA 94107 +1 415 857 4857	TITLE snickerdoodle FPGA Module
	PATH /X12	PATH
	DESCRIPTION Crypto-Authenticator	DESCRIPTION
	Copyright 2015 krkt inc. This schematic is made available under a Creative Commons Attribution-ShareAlike 4.0 International License. To view a copy of this license please visit <a href="http://creativecommons.org/licenses/by-sa/4.0/">http://creativecommons.org/licenses/by-sa/4.0/</a>	SIZE B
	DRAWN BY B. Hammond CHECKED BY J. Weatherbee APPROVED BY J. Weatherbee	DRAWING NO. 15081800-01
	DATE 11/22/2015 11/23/2015 11/23/2015	REV 4.1
		SHEET 19 OF 30

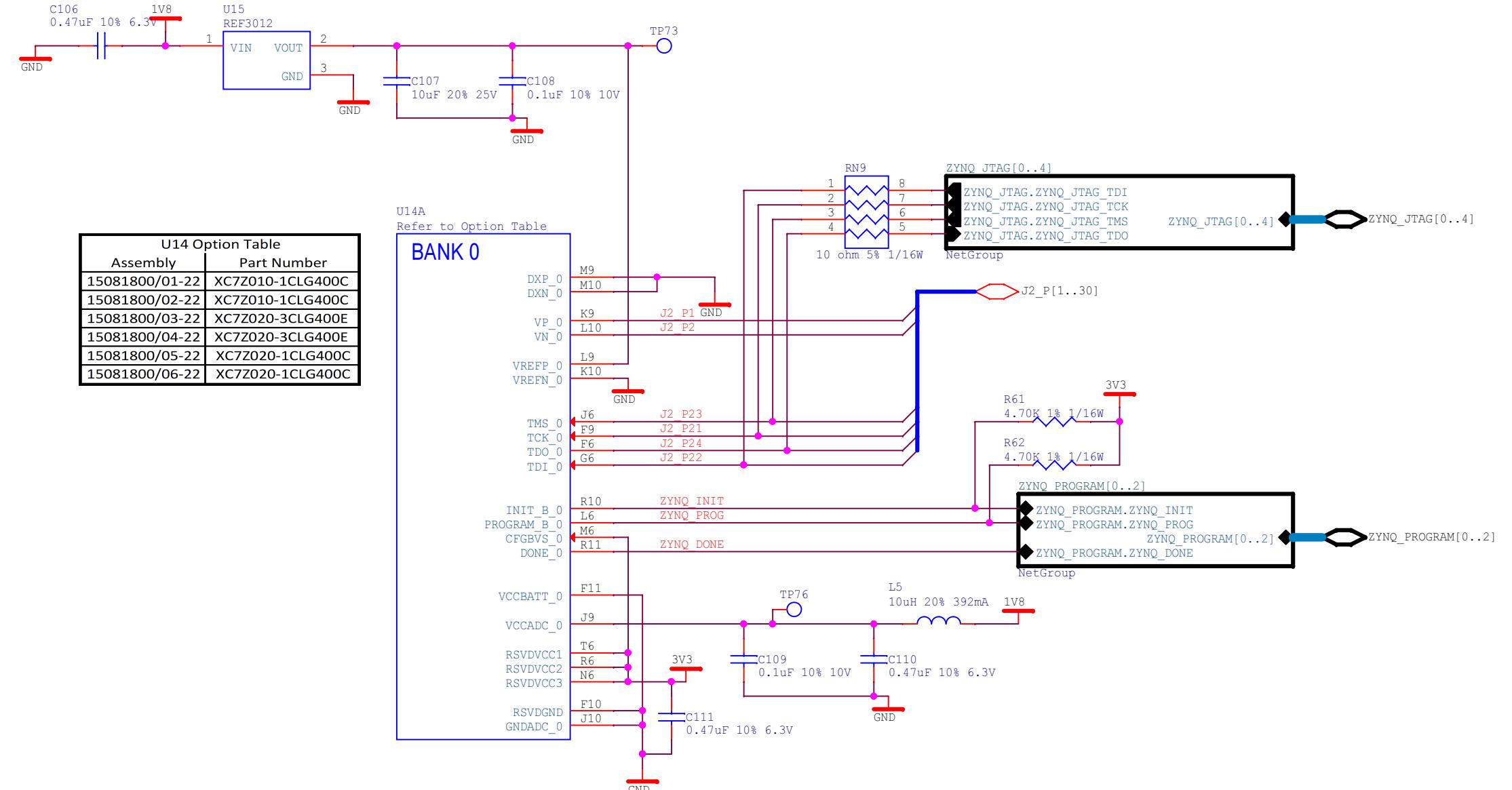


U14 Option Table	
Assembly	Part Number
15081800/01-22	XC7Z010-1CLG400C
15081800/02-22	XC7Z010-1CLG400C
15081800/03-22	XC7Z020-3CLG400E
15081800/04-22	XC7Z020-3CLG400E
15081800/05-22	XC7Z020-1CLG400C
15081800/06-22	XC7Z020-1CLG400C

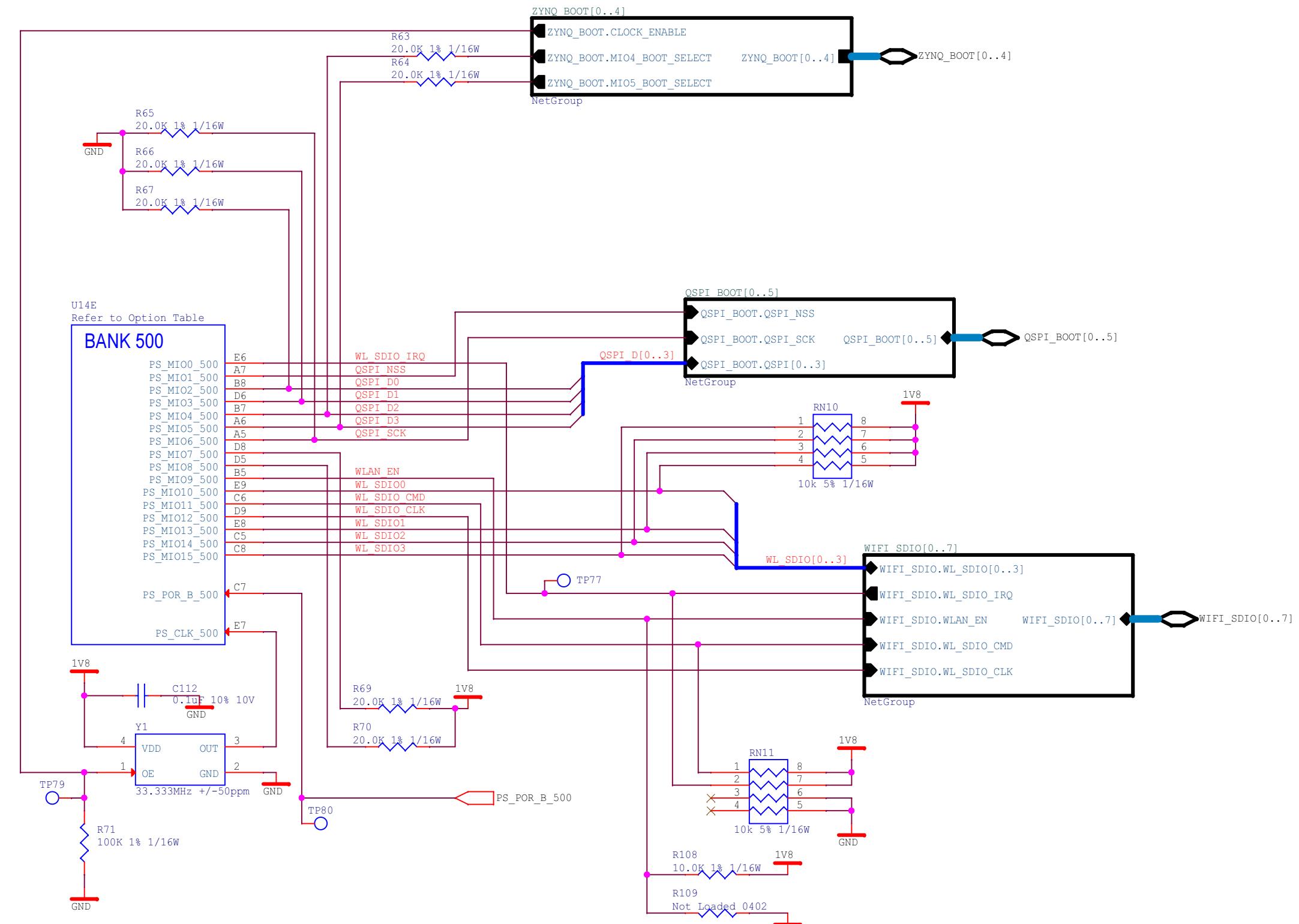


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nickerdoodle FPGA Module		
K13		
TION		
ynq SoC		
ZE	DRAWING NO.	REV
3	15081800-01	4.1
SHEET 20 OF 30		



U14 Option Table	
Assembly	Part Number
15081800/01-22	XC7Z010-1CLG400C
15081800/02-22	XC7Z010-1CLG400C
15081800/03-22	XC7Z020-3CLG400E
15081800/04-22	XC7Z020-3CLG400E
15081800/05-22	XC7Z020-1CLG400C
15081800/06-22	XC7Z020-1CLG400C



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TITLE		
snickerdoodle FPGA Module		
PATH		
/X13		
DESCRIPTION	SIZE	DRAWING NO.
Zynq SoC	B	15081800-01
		REV 4.1
		SHEET 22 of 30



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NAME

DATE

11/22/2015

DRAWN BY

B. Hammond

11/22/2015

CHECKED BY

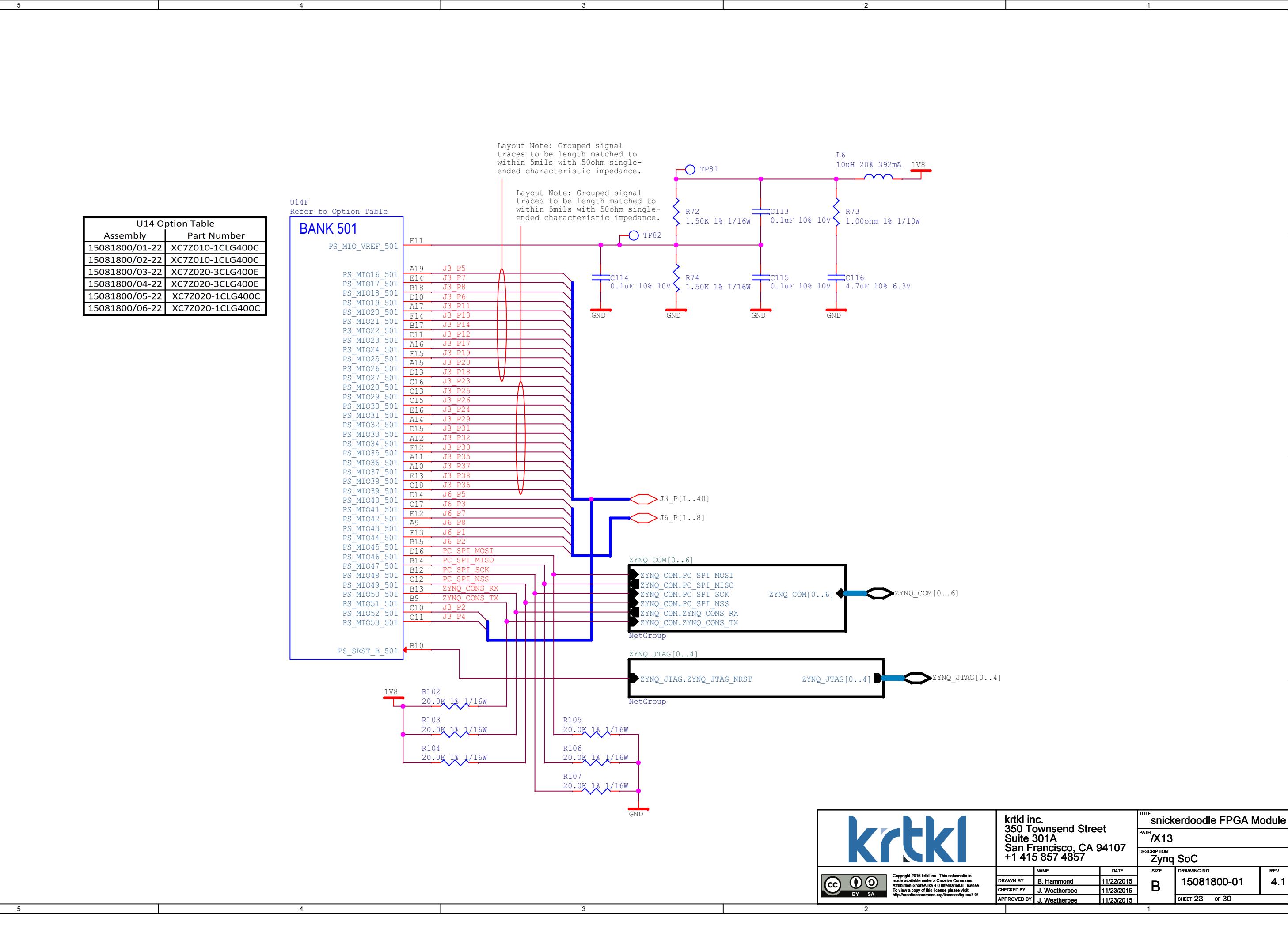
J. Weatherbee

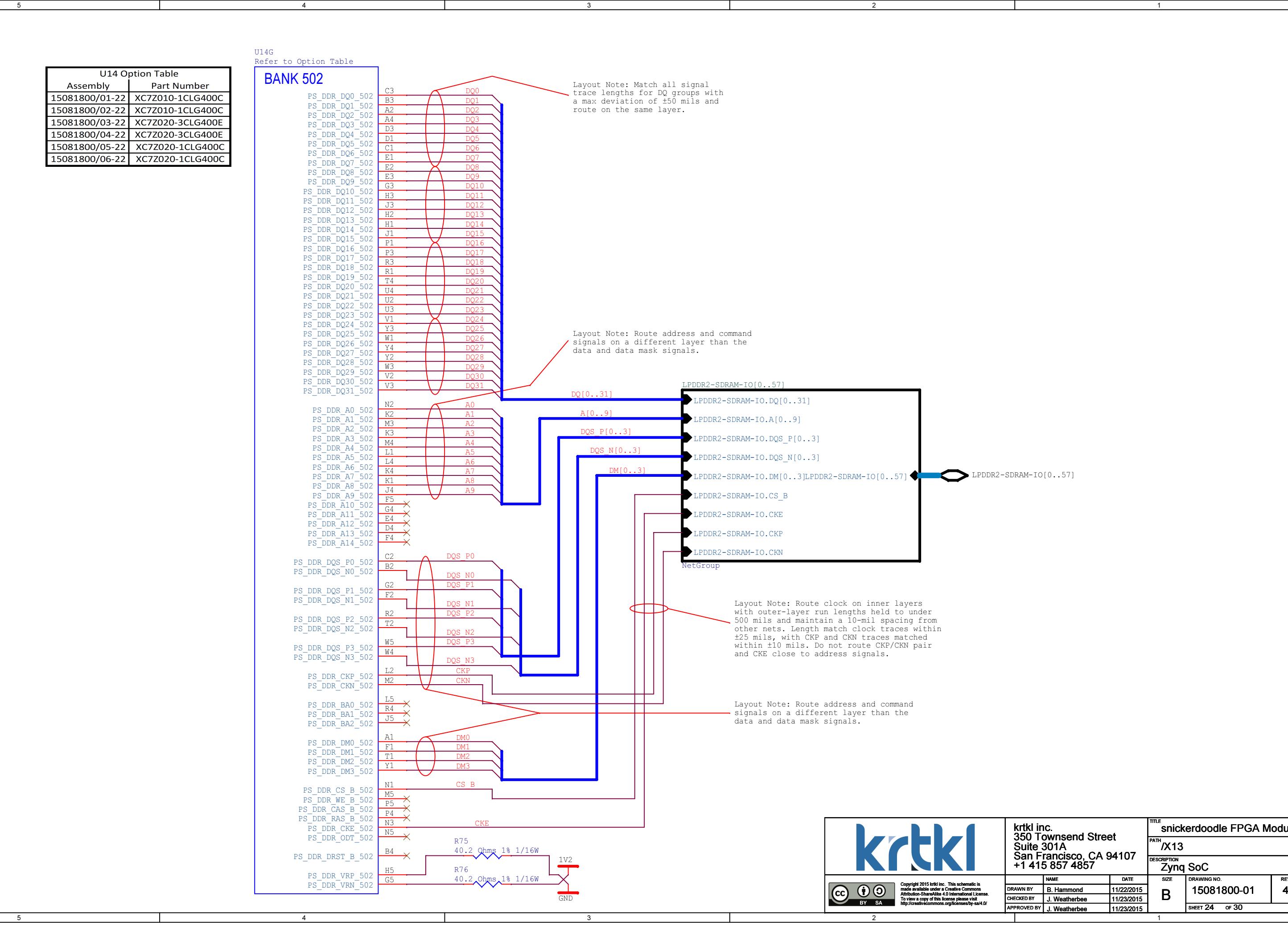
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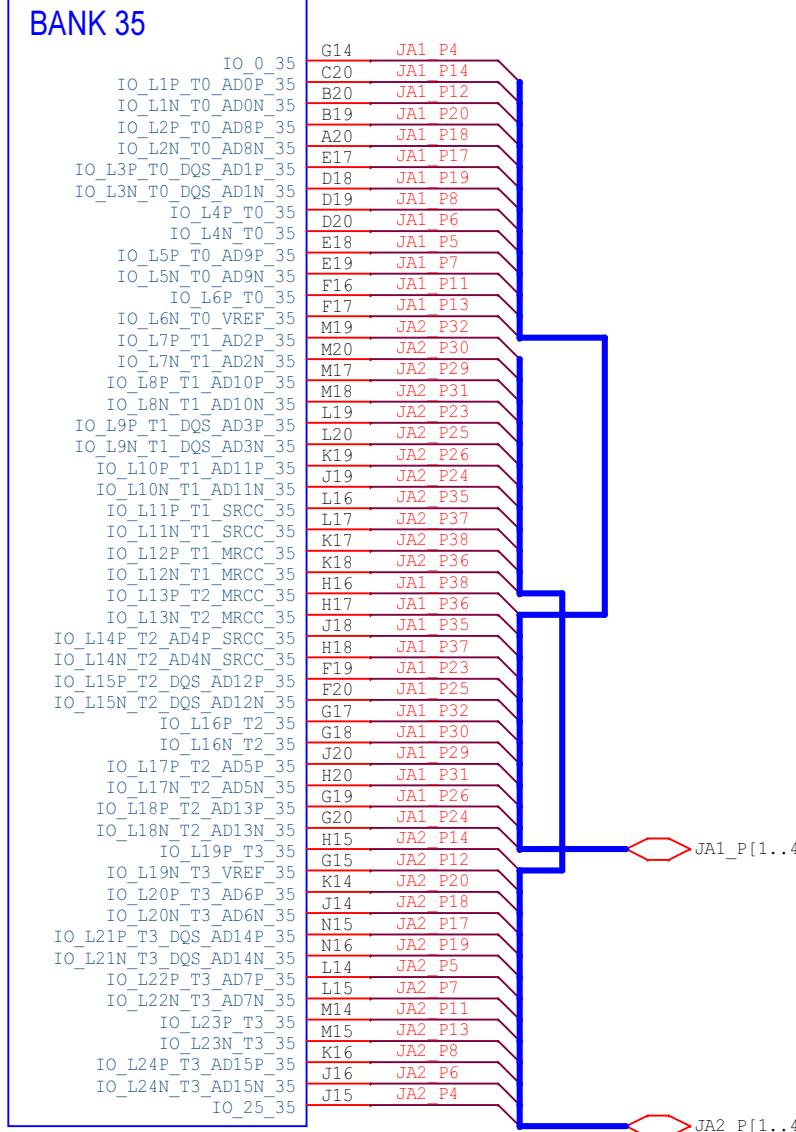
J. Weatherbee

11/23/2015

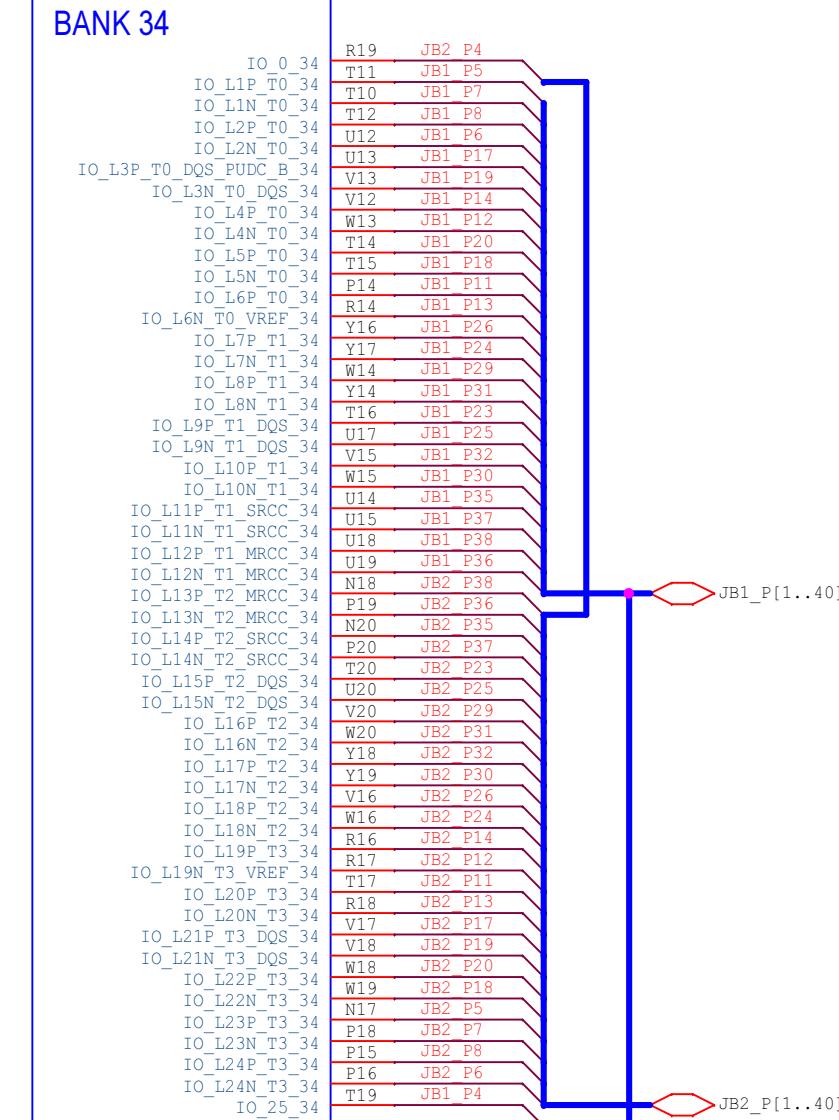




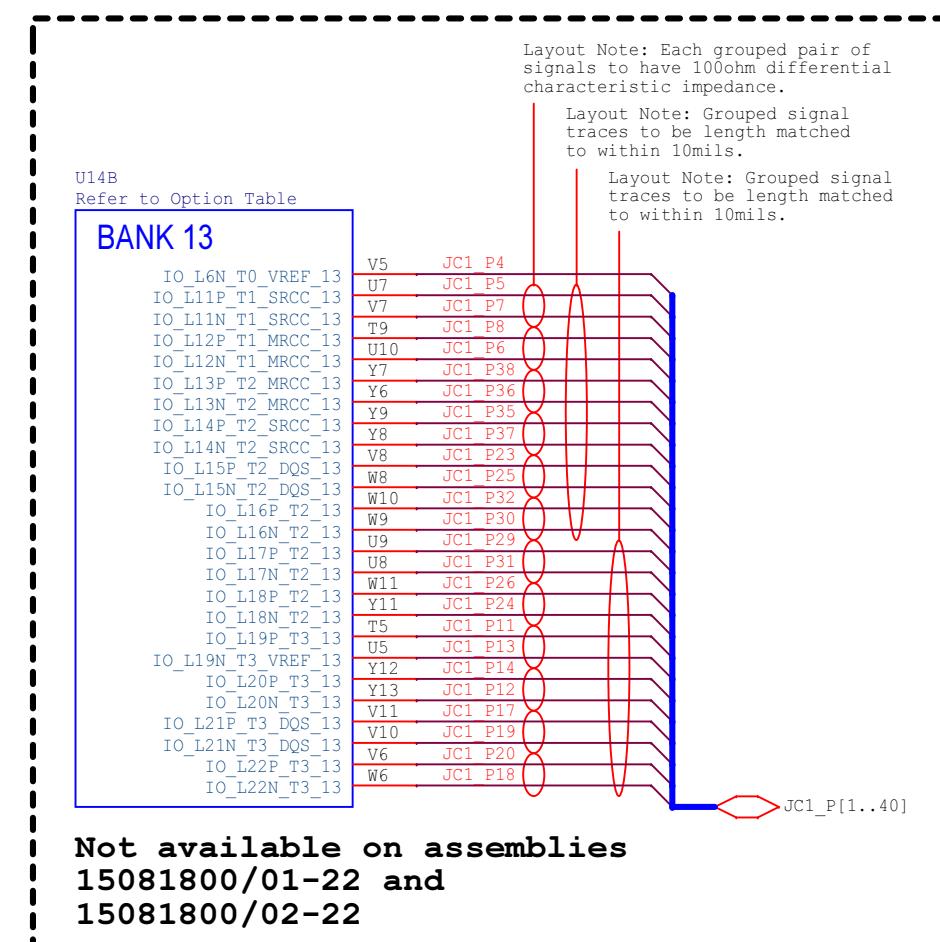
D  
U14D  
Refer to Option Table



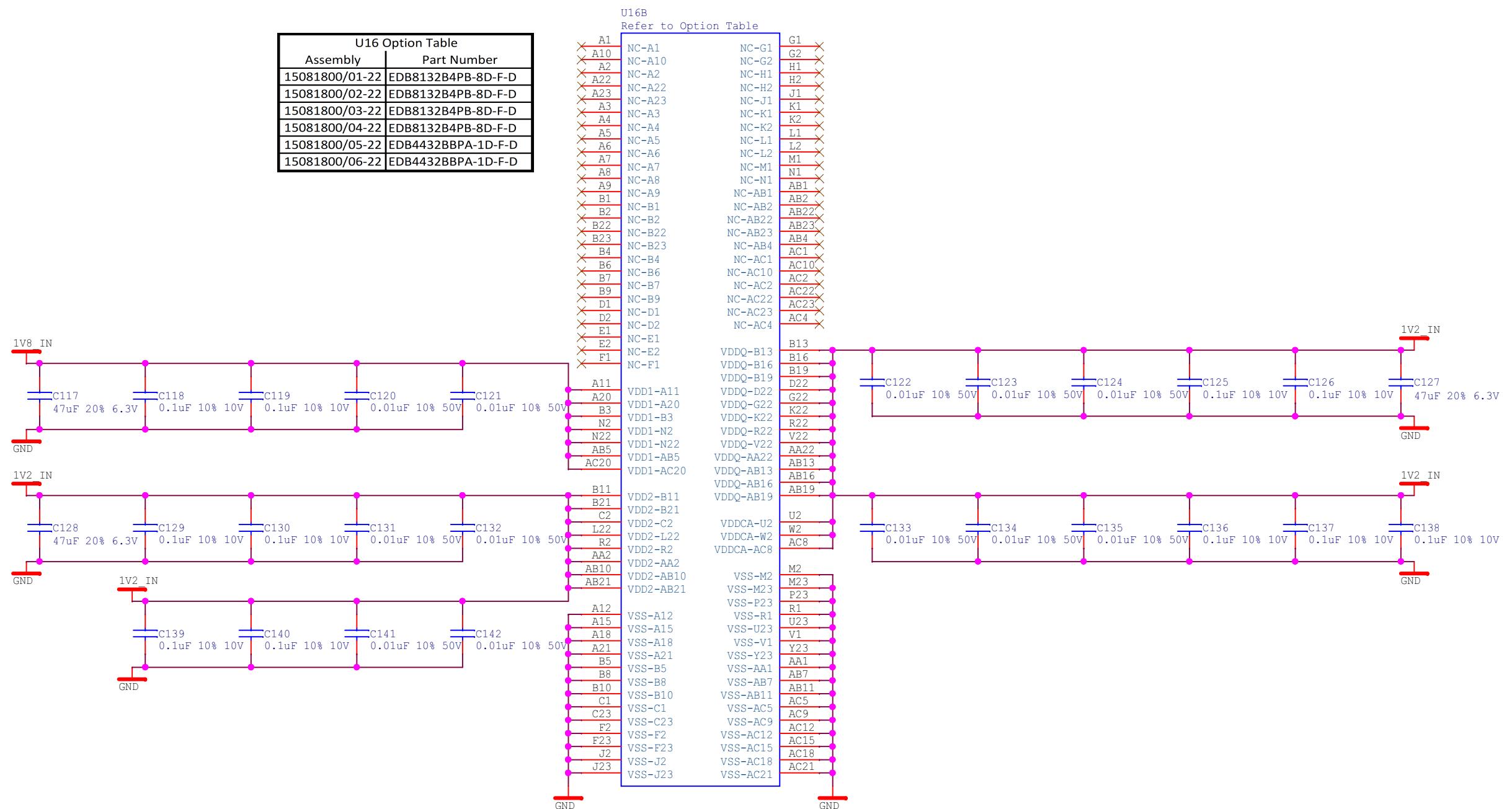
U14C  
Refer to Option Table



U14 Option Table	
Assembly	Part Number
15081800/01-22	XC7Z010-1CLG400C
15081800/02-22	XC7Z010-1CLG400C
15081800/03-22	XC7Z020-3CLG400E
15081800/04-22	XC7Z020-3CLG400E
15081800/05-22	XC7Z020-1CLG400C
15081800/06-22	XC7Z020-1CLG400C

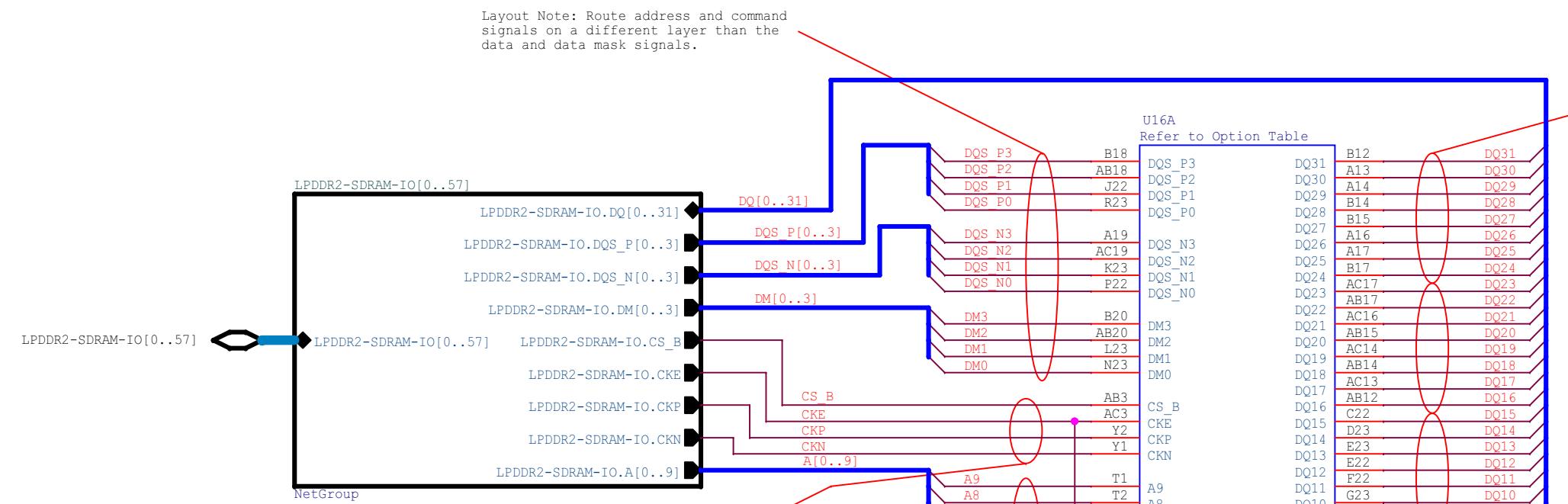


U16 Option Table	
Assembly	Part Number
15081800/01-22	EDB8132B4PB-8D-F-D
15081800/02-22	EDB8132B4PB-8D-F-D
15081800/03-22	EDB8132B4PB-8D-F-D
15081800/04-22	EDB8132B4PB-8D-F-D
15081800/05-22	EDB4432BBPA-1D-F-D
15081800/06-22	EDB4432BBPA-1D-F-D

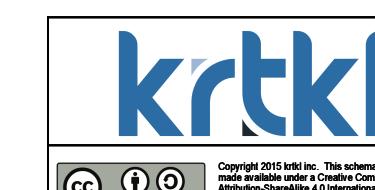
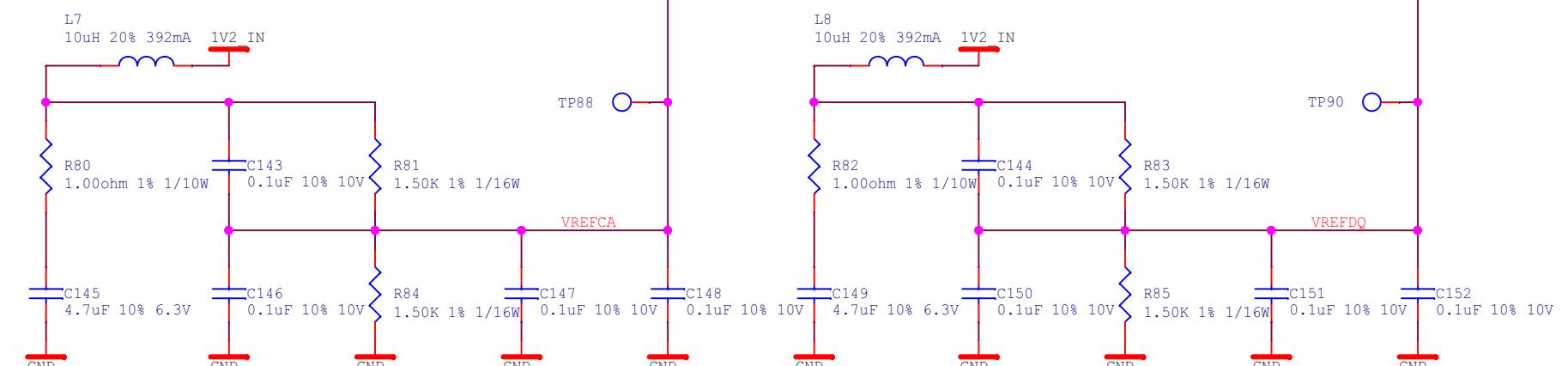
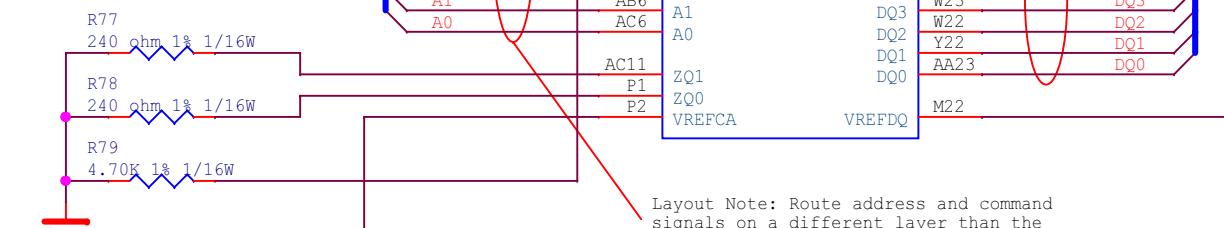


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350 Townsend Street  
Suite 301A  
San Francisco, CA 94107  
+1 415 857 4857

<b>TITLE</b>		
snickerdoodle FPGA Module		
<b>ATH</b>		
/X14		
<b>DESCRIPTION</b>		
LPDDR2 RAM		
<b>SIZE</b>	DRAWING NO.	REV
B	15081800-01	4.1
SHEET 26 OF 30		



Layout Note: Route clocks on inner layers with outer-layer run lengths held to under 500 mils and maintain a 10 mil spacing from other nets. Length match all clock traces within ±25 mils, with CKP and CKN traces matched within ±10 mils. Do not route CKP/CKN pair and CKE close to address signals.



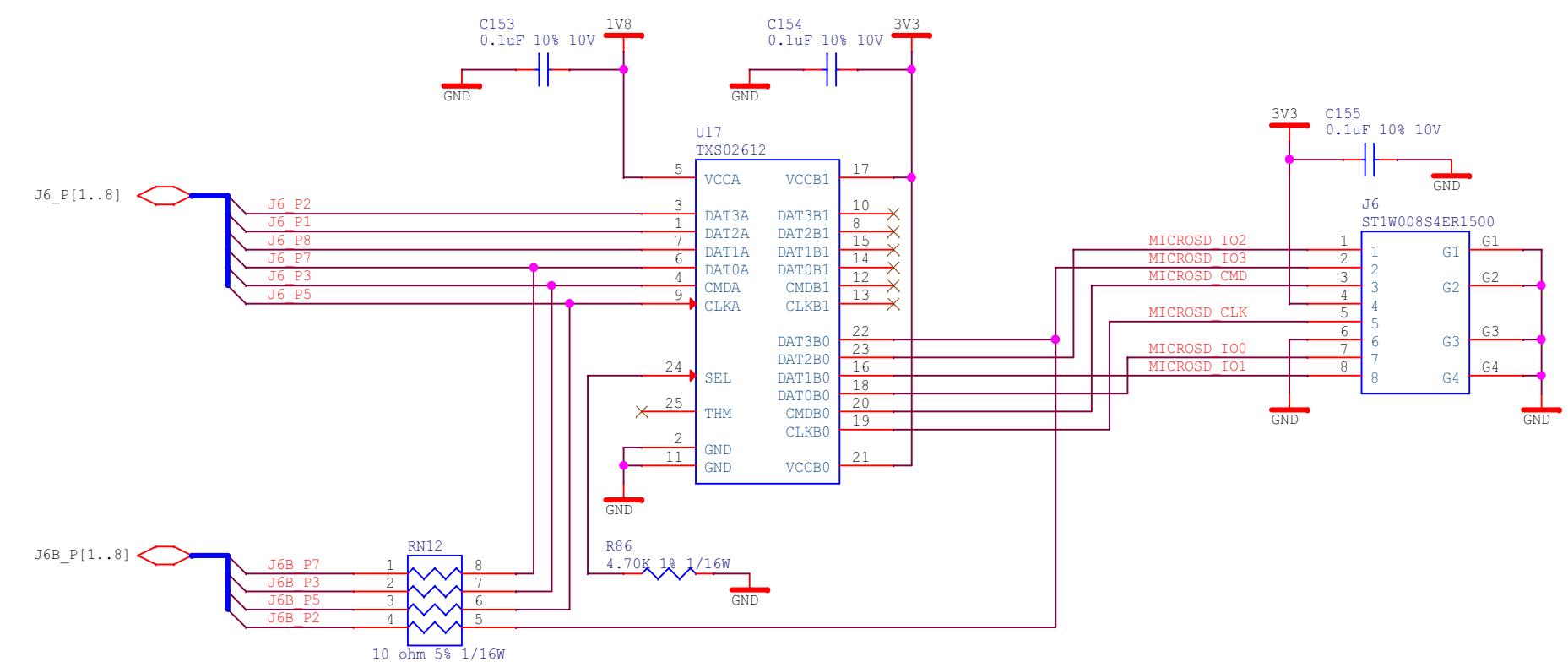
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+1 415 857 4857



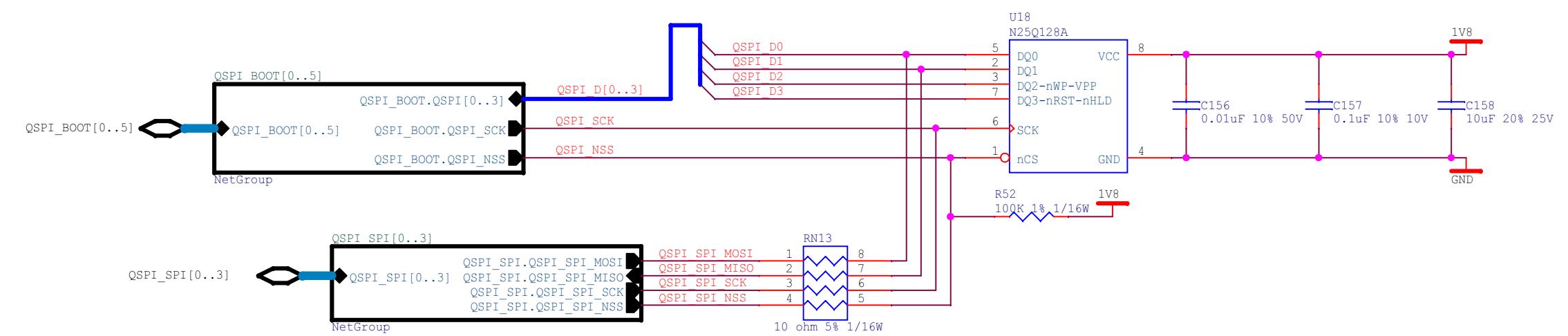
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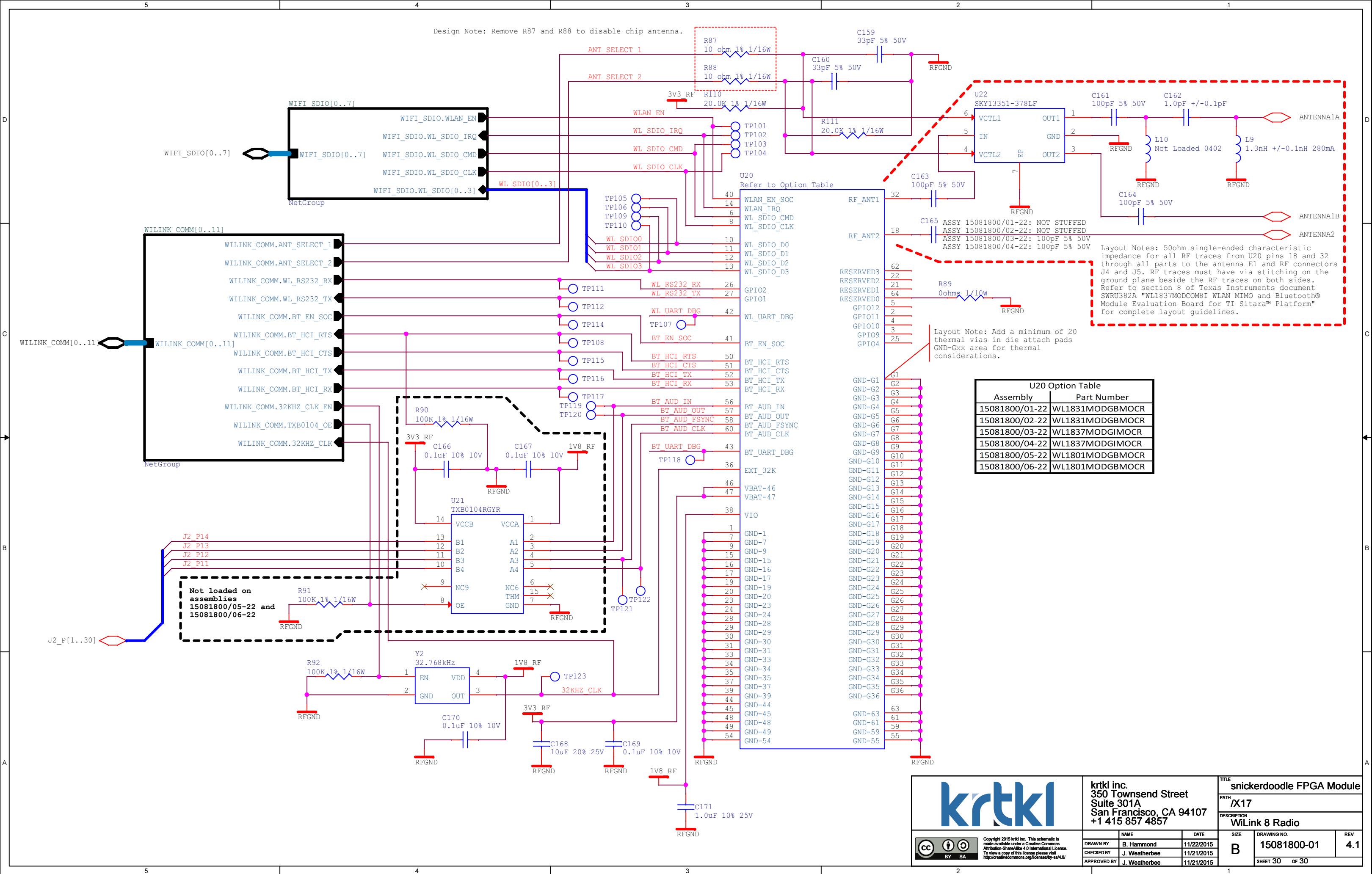
NAME	DATE	PATH	TITLE
B. Hammond	11/22/2015	/X14	snickerdoodle FPGA Module
J. Weatherbee	11/23/2015		
J. Weatherbee	11/23/2015		DESCRIPTION LPDDR2 RAM
<b>B</b>	<b>15081800-01</b>	<b>4.1</b>	
			SHEET 27 OF 30



krtkl inc.			TITLE snickerdoodle FPGA Module		
			PATH /X15		
			DESCRIPTION microSD Flash		
	NAME	DATE			
DRAWN BY B. Hammond	11/22/2015				
CHECKED BY J. Weatherbee	11/21/2015				
APPROVED BY J. Weatherbee	11/21/2015				
SHEET 28 OF 30					



	<b>krtk inc.</b> 350 Townsend Street Suite 301A San Francisco, CA 94107 +1 415 857 4857	<b>snickerdoodle FPGA Module</b>
	<small>Copyright 2015 krtk inc. This schematic is made available under a Creative Commons Attribution-ShareAlike 4.0 International License. To view a copy of this license please visit <a href="http://creativecommons.org/licenses/by-sa/4.0/">http://creativecommons.org/licenses/by-sa/4.0/</a></small>	<b>PATH</b> <b>/X16</b>
	<b>DESCRIPTION</b> <b>QSPI Flash</b>	<b>SIZE</b> <b>B</b>
	<b>DRAWN BY</b> B. Hammond <b>CHECKED BY</b> J. Weatherbee <b>APPROVED BY</b> J. Weatherbee	<b>DRAWING NO.</b> <b>15081800-01</b>
		<b>REV</b> <b>4.1</b>
		<b>SHEET</b> 29 <b>of</b> 30



Net Length (mm)	FPGA Pin	FPGA Signal	JA1	FPGA Signal	FPGA Pin	Net Length (mm)
		VIO_OUT (+3.3V)	1 C19	2 VCCO_35	JA1_SMB_nINT	
67.528	E18	IO_L5P_T0_AD9P_35	5	6 IO_0_35	G14	36.462
67.517	E19	IO_L5N_T0_AD9N_35	7	8 IO_L4N_T0_35	D20	67.516
		GND	9 10	GND	D19	67.527
67.521	F16	IO_L6P_T0_35	11	12 IO_L1N_T0_AD0N_35	B20	67.682
67.524	F17	IO_L6N_T0_VREF_35	13	14 IO_L1P_T0_AD0P_35	C20	67.533
		GND	15 16	GND		
67.516	E17	IO_L3P_T0_DQS_AD1P_35	17	18 IO_L2N_T0_AD8N_35	A20	67.530
67.531	D18	IO_L3N_T0_DQS_AD1N_35	19	20 IO_L2P_T0_AD8P_35	B19	67.521
		GND	21 22	GND		
67.137	F19	IO_L15P_T2_DQS_AD12P_35	23	24 IO_L18N_T2_AD13N_35	G20	67.143
67.155	F20	IO_L15N_T2_DQS_AD12N_35	25	26 IO_L18P_T2_AD13P_35	G19	67.150
		GND	27 28	GND		
67.155	J20	IO_L17P_T2_AD5P_35	29	30 IO_L16N_T2_35	G18	67.152
67.139	H20	IO_L17N_T2_AD5N_35	31	32 IO_L16P_T2_35	G17	67.148
		GND	33 34	GND		
67.156	J18	IO_L14P_T2_AD4P_SRCC_35	35	36 IO_L13N_T2_MRCC_35	H17	67.149
67.133	H18	IO_L14N_T2_AD4N_SRCC_35	37	38 SMB_I2C_SCL0	H16	67.134
		SMB_I2C_SCL0	39 40	SMB_I2C_SDA0		

Net Length (mm)	FPGA Pin	FPGA Signal	JA2	FPGA Signal	FPGA Pin	Net Length (mm)
		VIO_OUT (+3.3V)	1 C19	2 VCCO_35	JA2_SMB_nINT	
37.541	L14	IO_L22P_T3_AD7P_35	5	6 IO_25_35	J15	21.780
37.550	L15	IO_L22N_T3_AD7N_35	7 8	IO_L24N_T3_AD15N_35	J16	37.545
		GND	9 10	GND	K16	37.542
37.547	M14	IO_L23P_T3_35	11	12 IO_L19N_T3_VREF_35	G15	37.543
37.543	M15	IO_L23N_T3_35	13	14 IO_L19P_T3_35	H15	37.550
		GND	15 16	GND		
37.563	N15	IO_L21P_T3_DQS_AD14P_35	17	18 IO_L20N_T3_AD6N_35	J14	37.557
37.549	N16	IO_L21N_T3_DQS_AD14N_35	19	20 IO_L20P_T3_AD6P_35	K14	37.546
		GND	21 22	GND		
65.700	L19	IO_L9P_T1_DQS_AD3P_35	23	24 IO_L10N_T1_AD11N_35	J19	65.691
65.693	L20	IO_L9N_T1_DQS_AD3N_35	25	26 IO_L10P_T1_AD11P_35	K19	65.689
		GND	27 28	GND		
65.710	M17	IO_L8P_T1_AD10P_35	29	30 IO_L7N_T1_AD2N_35	M20	65.704
65.703	M18	IO_L8N_T1_AD10N_35	31	32 IO_L7P_T1_AD2P_35	M19	65.714
		GND	33 34	GND		
65.703	L16	IO_L11P_T1_SRCC_35	35	36 IO_L12N_T1_MRCC_35	K18	65.666
65.688	L17	IO_L11N_T1_SRCC_35	37	38 SMB_I2C_SCL1	K17	65.704
		SMB_I2C_SCL1	39 40	SMB_I2C_SDA1		

Net Length (mm)	FPGA Pin	FPGA Signal	JB1	FPGA Signal	FPGA Pin	Net Length (mm)
		VIO_OUT (+3.3V)	1	2	JB1_SMB_nINT	
	N19	VCCO_34	3	4	IO_25_34	
65.260	T11	IO_L1P_T0_34	5	6	IO_L2N_T0_34	T19 56.313
65.256	T10	IO_L1N_T0_34	7	8	IO_L2P_T0_34	U12 65.247
		GND	9	10	GND	T12 65.252
65.261	P14	IO_L6P_T0_34	11	12	IO_L4N_T0_34	W13 65.232
65.264	R14	IO_L6N_T0_VREF_34	13	14	IO_L4P_T0_34	V12 65.257
		GND	15	16	GND	
65.256	U13	IO_L3P_T0_DQS_PUDC_B_34	17	18	IO_L5N_T0_34	T15 65.271
65.264	V13	IO_L3N_T0_DQS_34	19	20	IO_L5P_T0_34	T14 65.267
		GND	21	22	GND	
37.095	T16	IO_L9P_T1_DQS_34	23	24	IO_L7N_T1_34	Y17 37.097
37.107	U17	IO_L9N_T1_DQS_34	25	26	IO_L7P_T1_34	Y16 37.103
		GND	27	28	GND	
37.095	W14	IO_L8P_T1_34	29	30	IO_L10N_T1_34	W15 37.096
37.109	Y14	IO_L8N_T1_34	31	32	IO_L10P_T1_34	V15 37.100
		GND	33	34	GND	
37.090	U14	IO_L11P_T1_SRCC_34	35	36	IO_L12N_T1_MRCC_34	U19 37.104
37.107	U15	IO_L11N_T1_SRCC_34	37	38	IO_L12P_T1_MRCC_34	U18 37.088
		SMB_I2C_SCL2	39	40	SMB_I2C_SDA2	

Net Length	FPGA Pin	FPGA Signal	JB2	FPGA Signal	FPGA Pin	Net Length (mm)
		VIO_OUT (+3.3V)	1	2	JB2_SMB_nINT	
	N19	VCCO_34	3	4	IO_0_34	R19 65.687
43.088	N17	IO_L23P_T3_34	5	6	IO_L24N_T3_34	P16 43.091
43.092	P18	IO_L23N_T3_34	7	8	IO_L24P_T3_34	P15 43.091
		GND	9	10	GND	
43.087	T17	IO_L20P_T3_34	11	12	IO_L19N_T3_VREF_34	R17 43.092
43.090	R18	IO_L20N_T3_34	13	14	IO_L19P_T3_34	R16 43.090
		GND	15	16	GND	
43.083	V17	IO_L21P_T3_DQS_34	17	18	IO_L22N_T3_34	W19 43.097
43.086	V18	IO_L21N_T3_DQS_34	19	20	IO_L22P_T3_34	W18 43.083
		GND	21	22	GND	
25.380	T20	IO_L15P_T2_DQS_34	23	24	IO_L18N_T2_34	W16 25.376
25.392	U20	IO_L15N_T2_DQS_34	25	26	IO_L18P_T2_34	V16 25.388
		GND	27	28	GND	
25.392	V20	IO_L16P_T2_34	29	30	IO_L17N_T2_34	Y19 25.381
25.378	W20	IO_L16N_T2_34	31	32	IO_L17P_T2_34	Y18 25.379
		GND	33	34	GND	
25.383	N20	IO_L14P_T2_SRCC_34	35	36	IO_L13N_T2_MRCC_34	P19 25.387
25.381	P20	IO_L14N_T2_SRCC_34	37	38	IO_L13P_T2_MRCC_34	N18 25.381
		SMB_I2C_SCL3	39	40	SMB_I2C_SDA3	

Net Length (mm)	FPGA Pin	FPGA Signal	JC1	FPGA Signal	FPGA Pin	Net Length (mm)	
	T8	VIO_OUT (+3.3V)	1	2	JC1_SMB_nINT		
62.825	U7	VCCO_13	3	4	IO_L6N_T0_VREF_13	V5	100.858
62.828	V7	IO_L11P_T1_SRCC_13	5	6	IO_L12N_T1_MRCC_13	U10	62.935
		IO_L11N_T1_SRCC_13	7	8	IO_L12P_T1_MRCC_13	T9	62.897
		GND	9	10	GND		
62.837	T5	IO_L19P_T3_13	11	12	IO_L20N_T3_13	Y13	62.750
62.835	U5	IO_L19N_T3_VREF_13	13	14	IO_L20P_T3_13	Y12	62.723
		GND	15	16	GND		
62.823	V11	IO_L21P_T3_DQS_13	17	18	IO_L22N_T3_13	W6	63.185
62.834	V10	IO_L21N_T3_DQS_13	19	20	IO_L22P_T3_13	V6	63.089
		GND	21	22	GND		
60.578	V8	IO_L15P_T2_DQS_13	23	24	IO_L18N_T2_13	Y11	60.516
60.556	W8	IO_L15N_T2_DQS_13	25	26	IO_L18P_T2_13	W11	60.505
		GND	27	28	GND		
60.561	U9	IO_L17P_T2_13	29	30	IO_L16N_T2_13	W9	60.558
60.570	U8	IO_L17N_T2_13	31	32	IO_L16P_T2_13	W10	60.565
		GND	33	34	GND		
60.570	Y9	IO_L14P_T2_SRCC_13	35	36	IO_L13N_T2_MRCC_13	Y6	60.566
60.563	Y8	IO_L14N_T2_SRCC_13	37	38	IO_L13P_T2_MRCC_13	Y7	60.562
		SMB_I2C_SCL4	39	40	SMB_I2C_SDA4		

Net Length (mm)	FPGA Pin	FPGA Signal	J3	FPGA Signal	FPGA Pin	Net Length (mm)	
	A13	VIO_OUT (+3.3V)	1	2	PS_MIO52_501	C10	
79.274	A19	VCCO_MIO1_501 (+1.8V)	3	4	PS_MIO53_501	C11	
79.314	E14	PS_MIO16_501	5	6	PS_MIO19_501	D10	79.294
		PS_MIO17_501	7	8	PS_MIO18_501	B18	79.283
		GND	9	10	GND		
79.277	A17	PS_MIO20_501	11	12	PS_MIO23_501	D11	79.276
79.287	F14	PS_MIO21_501	13	14	PS_MIO22_501	B17	79.455
		GND	15	16	GND		
79.284	A16	PS_MIO24_501	17	18	PS_MIO27_501	D13	79.265
79.292	F15	PS_MIO25_501	19	20	PS_MIO26_501	A15	79.289
		GND	21	22	GND		
63.747	C16	PS_MIO28_501	23	24	PS_MIO31_501	E16	63.679
63.800	C13	PS_MIO29_501	25	26	PS_MIO30_501	C15	63.781
		GND	27	28	GND		
63.687	A14	PS_MIO32_501	29	30	PS_MIO35_501	F12	63.747
63.700	D15	PS_MIO33_501	31	32	PS_MIO34_501	A12	63.680
		GND	33	34	GND		
63.691	A11	PS_MIO36_501	35	36	PS_MIO39_501	C18	63.685
63.687	A10	PS_MIO37_501	37	38	PS_MIO38_501	E13	63.691
		SMB_I2C_SCL5	39	40	SMB_I2C_SDA5		

**Net Length (mm)    FPGA Pin**

K9

	<b>FPGA Signal</b>	<b>J2</b>	<b>FPGA Signal</b>	
	VP_0	1	2	VN_0
	DAC_OUT1/ADC_IN4	3	4	DAC_OUT2/ADC_IN5
	GND	5	6	GND
	SMB_I2C_SCL7	7	8	SMB_I2C_SDA7
	GND	9	10	GND
	BT_AUD_CLK	11	12	BT_AUD_FSYNC
	BT_AUD_OUT	13	14	BT_AUD_IN
Zynq	MCU_SWCLK/PA13	15	16	MCU_SWDIO/PA14
	MCU_nRST	17	18	MCU_VDDIO2 (+3.3V)
	nRST(PS_SRST_B_501)	19	20	GND
	TCK_0	21	22	TDI_0
	TMS_0	23	24	TDO_0
	VCCO_0 (+3.3V)	25	26	PGND
	GND	27	28	GND
	VIN (+3.7-17V)	29	30	VIN (+3.7-17V)

**FPGA Pin    Net Length (mm)**

L10

G6

F6

REV	DESCRIPTION	APPD BY	DATE
V1.0			08/01/15
V2.0			01/20/16
V3.0			05/02/16
V4.0			08/08/16
V4.1			11/02/16

NOTES: UNLESS OTHERWISE SPECIFIED.

ALL SPECIFICATIONS REFERENCED SHALL BE OF THE LATEST REVISION.

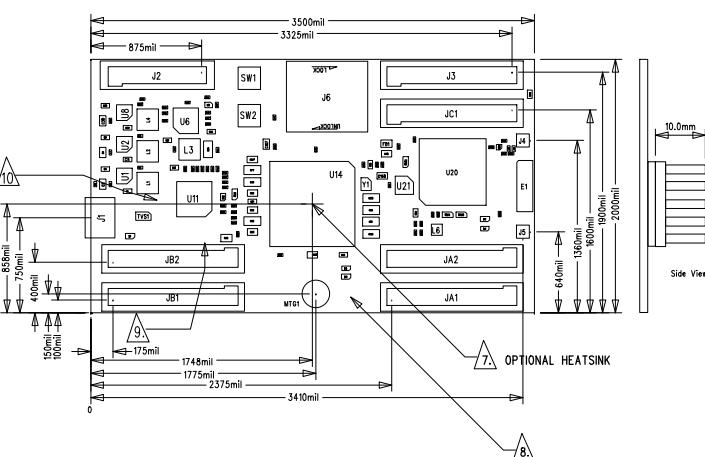
- CONTROLLING DIMENSIONS AND SUPPLIED DATA ARE IN INCHES.  
DIMENSIONS AND TOLERANCES PER ASME Y14.5M.
- ASSEMBLE IN ACCORDANCE WITH IPC-A-610 CLASS 2.
- ESD PRECAUTIONS DURING HANDLING AND ASSEMBLY TO BE IN ACCORDANCE WITH EIA JESD 625.
- MAXIMUM LEAD PROTRUSION ON SECONDARY SIDE TO BE 1.5 MAX.
- Use water soluble flux for SMT, and no clean flux for secondary solder steps if required.
- Board Cleaning: removal of flux residue is required after first pass SMT, hand solder and rework.

7 OPTIONAL HEATSINK (HS1)

8 2D SERIAL NUMBER BARCODE TO BE APPLIED AT LOCATION INDICATED

9 WRITE IN THE ASSEMBLY VARIANT IN THIS BOX ON PRIMARY SIDE SILKSCREEN LAYER

10 WRITE IN THE REVISION IN THIS BOX ON PRIMARY SIDE SILKSCREEN LAYER



DRAWING DESCRIPTION			DOCUMENT NUMBER		REV.
PCB Assembly Primary Side (TopLayer)			15081800-06		4.1
TITLE			PCB, Snickerdoodle		
DESIGNER	D. BEANE / J. COX	01AUG2015			
ENGINEER	J. WEATHERBEE	20JAN2016			
CHECK BY	B. HAMMOND	20JAN2016			
O. A. BY	J. WEATHERBEE	20JAN2016			
SHEET	1 of 1	SIZE C	SCALE	1:1	
SECURITY LEVEL	CONFIDENTIAL - STEALTH MODE				
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8

7

6

5

4

3

2

1

REV

SHT

REV

CORP. NO.

DRAWING DESCRIPTION

REV	DESCRIPTION	APPD BY	DATE
V1.0			08/01/15
V2.0			01/20/16
V3.0			05/02/16
V4.0			08/08/16
V4.1			11/02/16

D

D

C

C

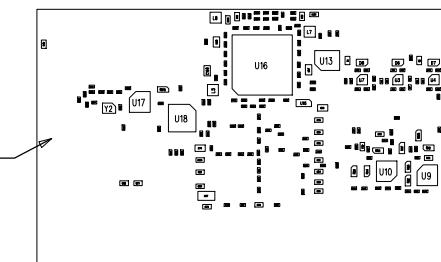
B

B

A

A

SERIAL NUMBER LABEL TO BE APPLIED AT LOCATION INDICATED



DRAWING DESCRIPTION			DOCUMENT NUMBER		REV.
PCB Assembly			15081800-06		4.0
Secondary Side (BottomLayer)			TITLE		
DESIGNER	D. BEANE / J. COX	01AUG2015			
ENGINEER	J. WEATHERBEE	20JAN2016			
CHECK BY	B. HAMMOND	20JAN2016	SHEET		
O. A. BY	J. WEATHERBEE	20JAN2016	2 of 2	SIZE	SCALE
SECURITY LEVEL			C	1:1	
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