Lab 5 grading sheet Circle professor

1) Name Last_____ First_____ EID_____VJR, MT, JV, RY

2) Name Last_____ First_____ EID_____VJR, MT, JV, RY

Use same spelling as listed on Blackboard

1. All source files that you have changed or added (like main.c) should be committed to SVN. Please do not commit other file types.
2. Deliverables 20%:
   0) This sheet

Combine the following components in this order into one pdf file and commit it to Lab5 folder in SVN before your checkout time. Have this file open on the computer during demonstration.

1) Logic analyzer screen shot showing the system running in simulation mode when cars are present on both roads (like Figure 5.4).
2) Circuit diagram (with your name and date) using PCB Artist
3) Drawing of the finite state machine

3. Performance 35%:
   Does it handle correctly all situations as specified?

4. Adhere to coding standard 5%
   Good Names have meaning
   Variables have units in comments
   Consistent indentation
   Consistent use of braces
   C99 style

1)	2)

5. Demonstration 40%:

During checkout, you will be asked to show both the simulated and actual TM4C123 systems to the TA. The TAs will expect you to know how the **`SysTick_Wait`** function works, and know how to add more input signals and/or output signals. An interesting question that may be asked during checkout is how you could experimentally prove your system works. In other words, what data should be collected and how would you collect it? If there were an accident, could you theoretically prove to the judge and jury that your software implements the FSM? What type of FSM do you have? What other types are there? How many states does it have? In general, how many next-state arrows are there? Explain how the linked data structure is used to implement the FSM. Explain the mathematical equation used to calculate the address of the next state, depending on the current state and the input. Be prepared to write software that delays 1 second without using the timer (you can use a calculator and manual). How do you prove the delay will be 1 second? Explain the assembly code created by the compiler for the main loop implementing the FSM, how are the data in the struct accessed? List some general qualities that would characterize a good FSM.

	1)	2)
Total:		