

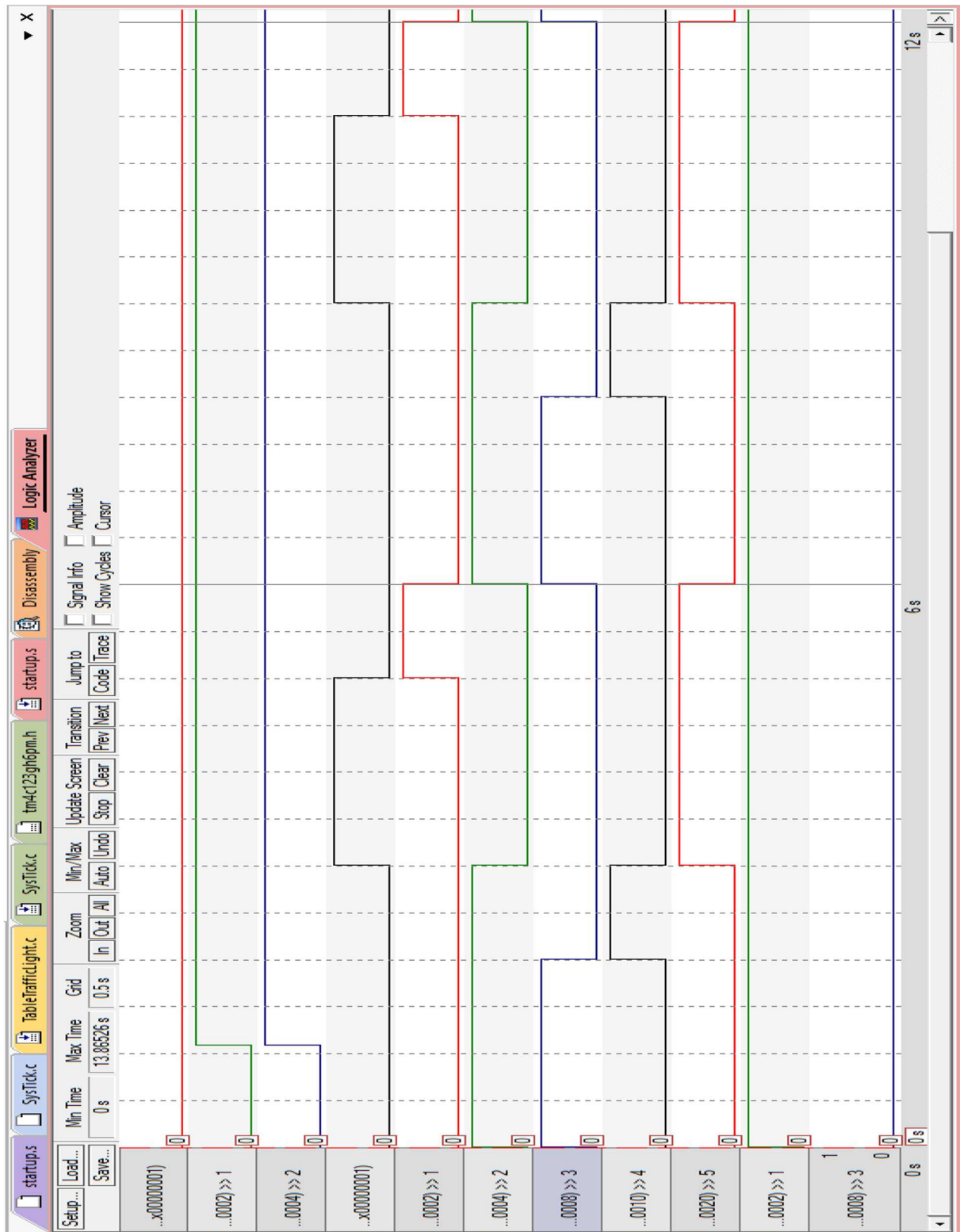
Lab 5 Deliverables

Akaash Chikarmane and Milan Feliciello

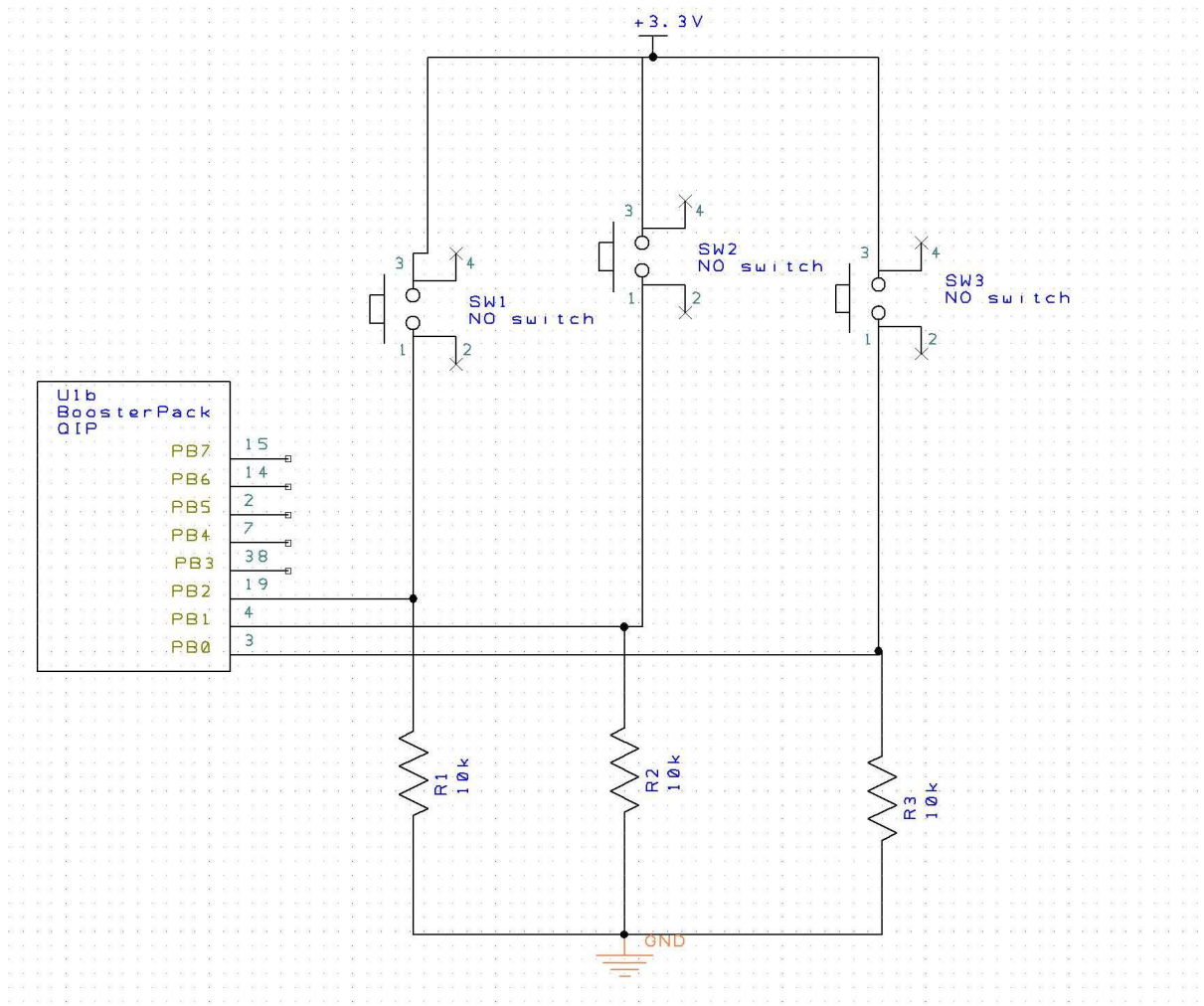
Section: 16085

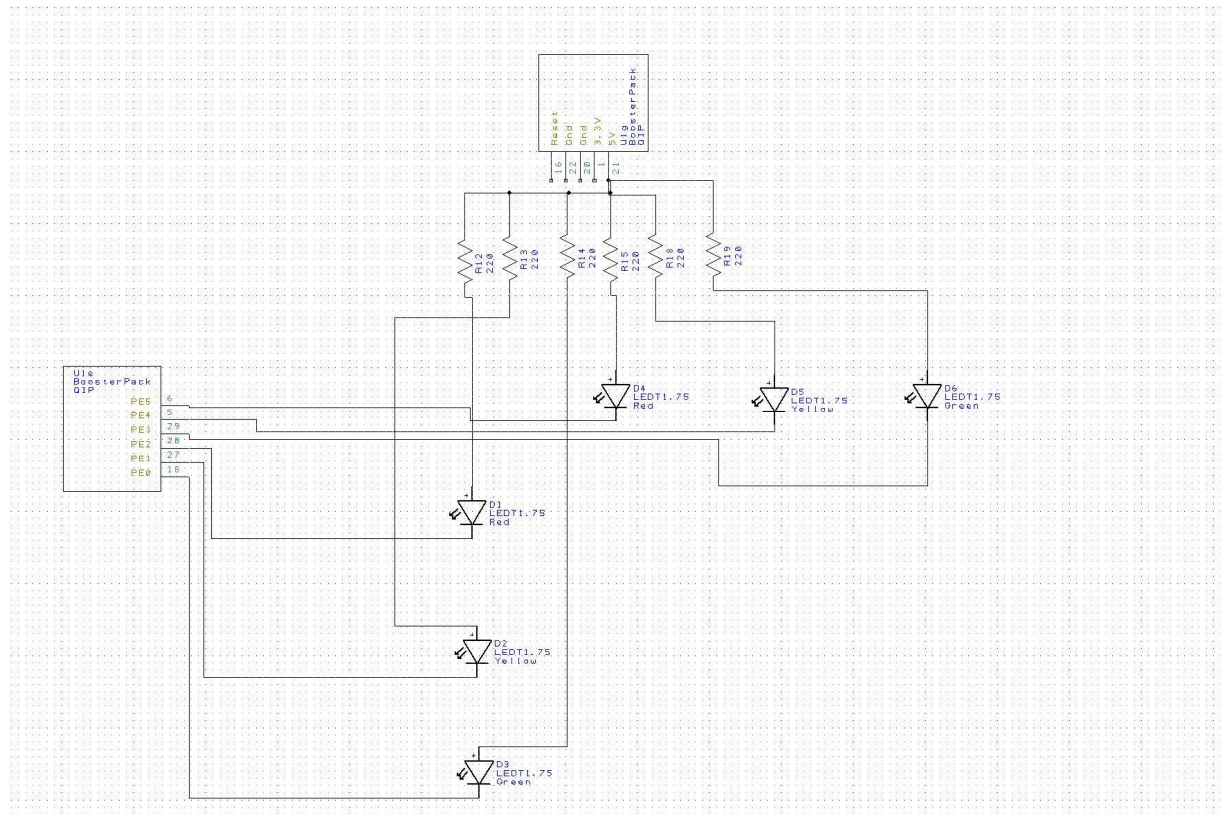
Spring 2016

Logic Analyzer – cars on both roads



Circuit Diagram





Finite State Machine

