Practical
Part C: CMOS Implementation

To prepare CMOS layout in selected technology, simulate with and without capacitive load, comment on rise, and fall times.

Practical : *Design and implementation of Layout using CMOS 0.25 micron Technology in Microwind.*

A. Inverter

B. NAND

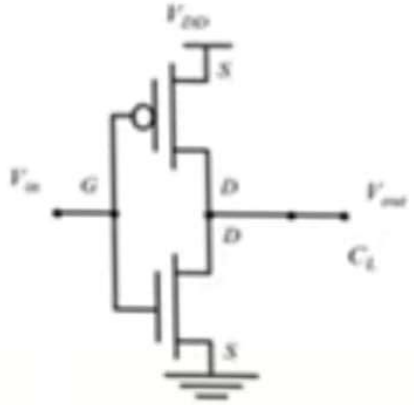
C. NOR

PMOS completed

now interconnection of PMOS and NMOS to complete inverter

connect source of PMOS to VDD and source of NMOS to VSS

short the drain of both PMOS and NMOS



Practical
Part C: CMOS Implementation

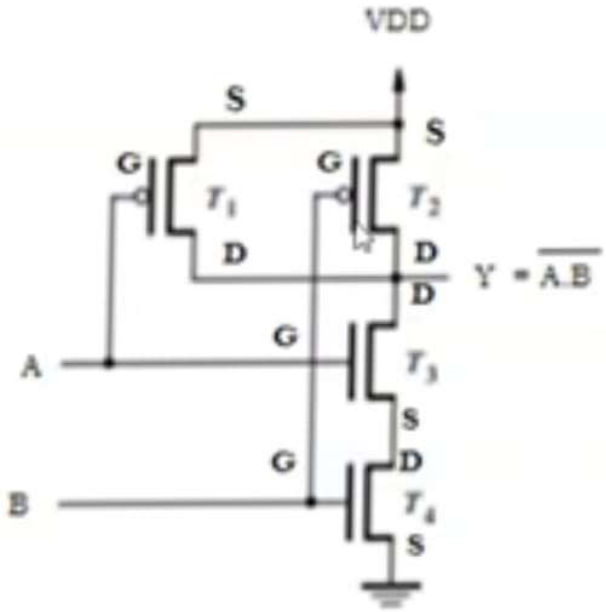
To prepare CMOS layout in selected technology, simulate with and without capacitive load, comment on rise, and fall times.

Practical : *Design and implementation of Layout using CMOS 0.25 micron Technology in Microwind.*

A. Inverter

B. NAND

C. NOR



Practical
Part C: CMOS Implementation

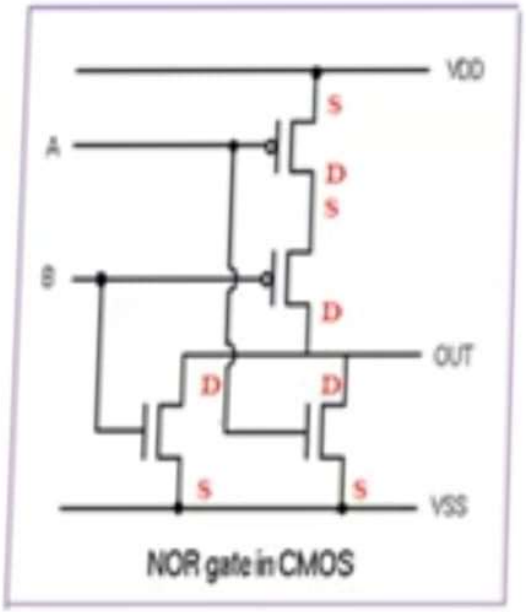
To prepare CMOS layout in selected technology, simulate with and without capacitive load, comment on rise, and fall times.

Practical : *Design and implementation of NOR Gate Layout using CMOS 0.25 micron Technology in Microwind.*

A. Inverter

B. NAND

C. NOR



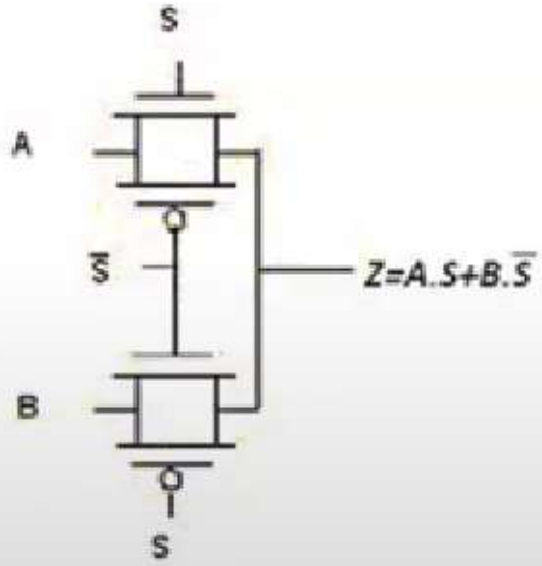
NOR gate in CMOS

Practical
Part C: CMOS Implementation of 2:1 Mux using TG

To prepare CMOS layout in selected technology, simulate with and without capacitive load, comment on rise, and fall times.

Practical : *Design and implementation of 2:1 Mux Layout using CMOS 0.25 micron Technology in Microwind.*

Sel	Y
0	B
1	A



Inputs			
A	I_1	I_0	Q
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

One Bit SRAM Cell