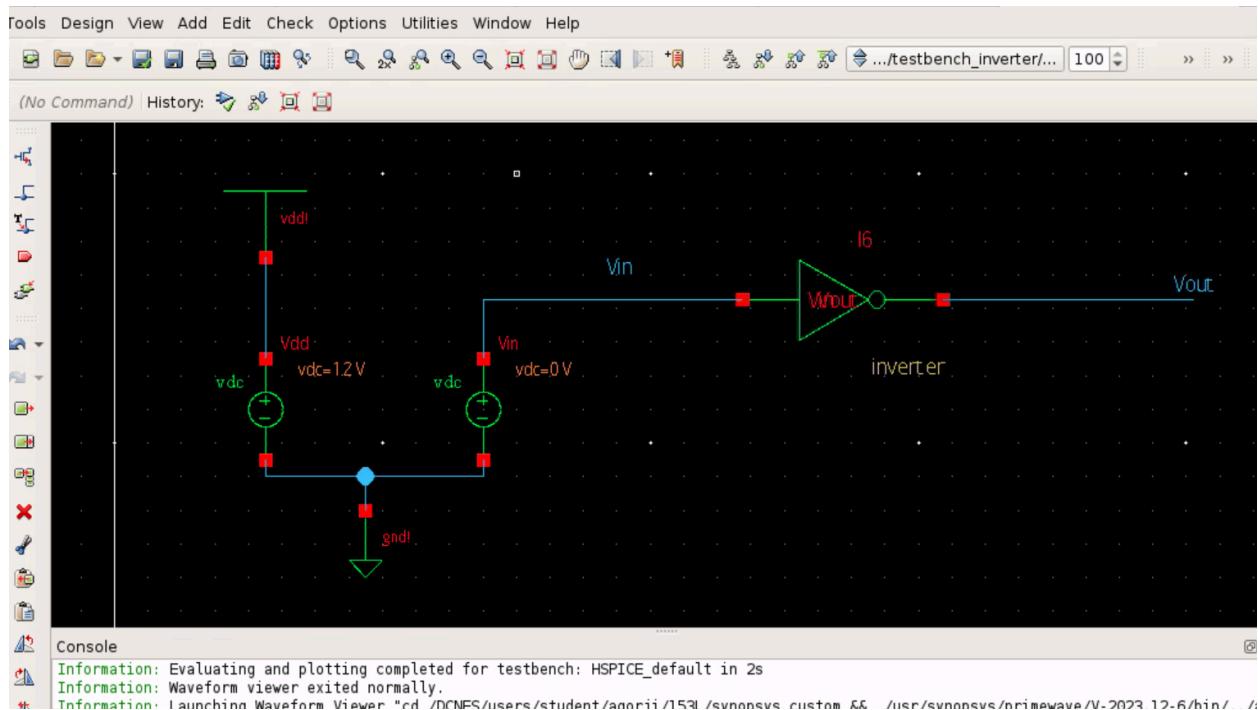
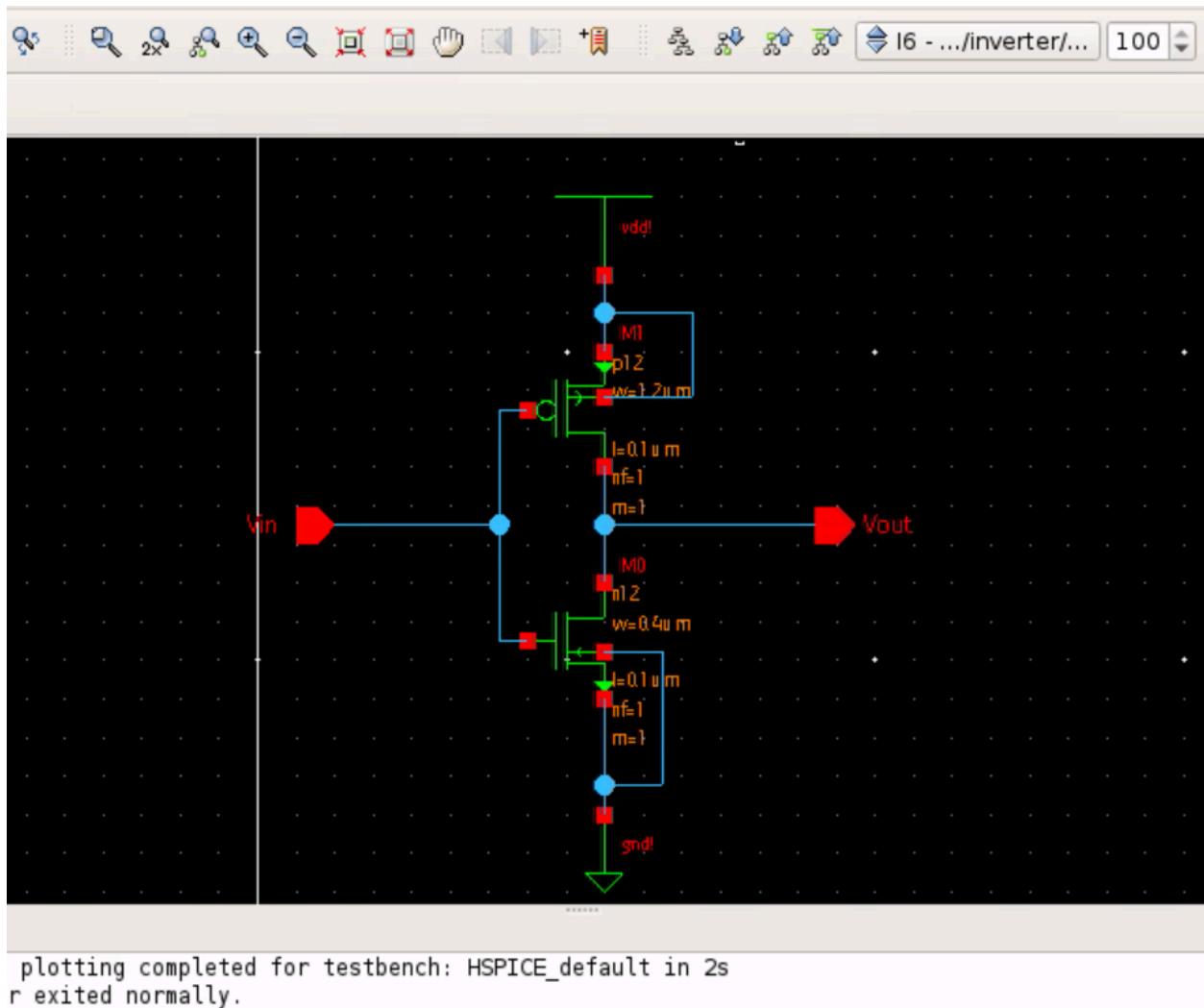
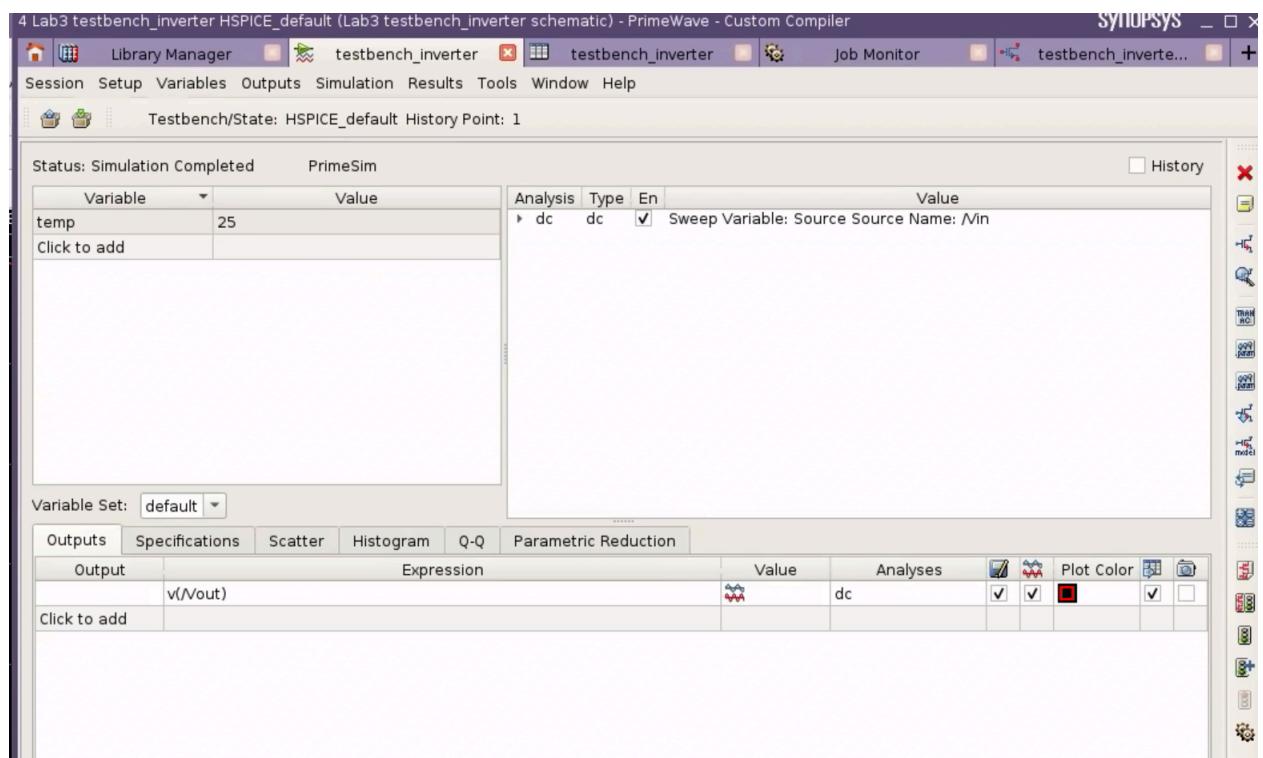


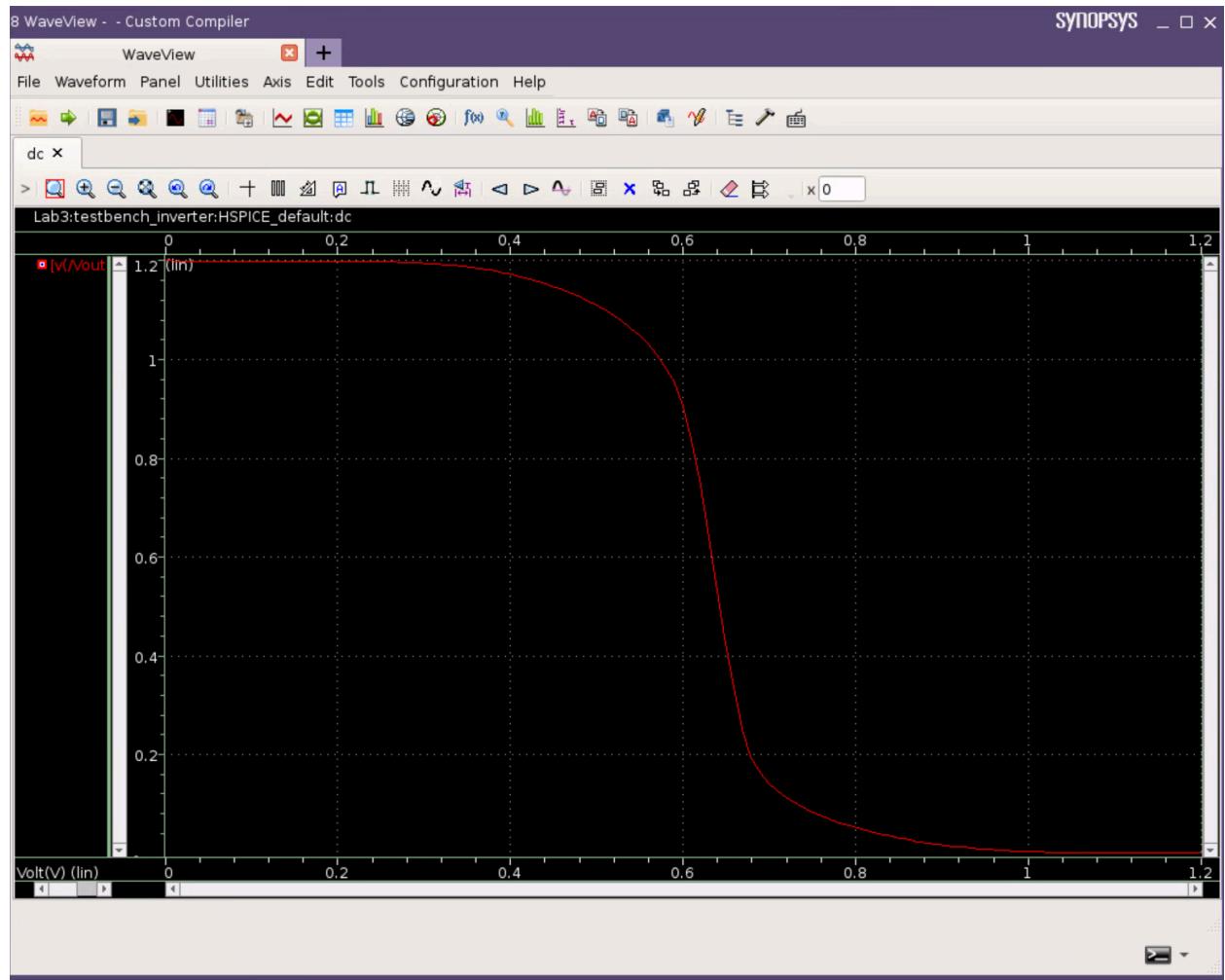
# ECEN 153L Lab 3 Report: CMOS Inverter

Aveed Gorji 1/26/26

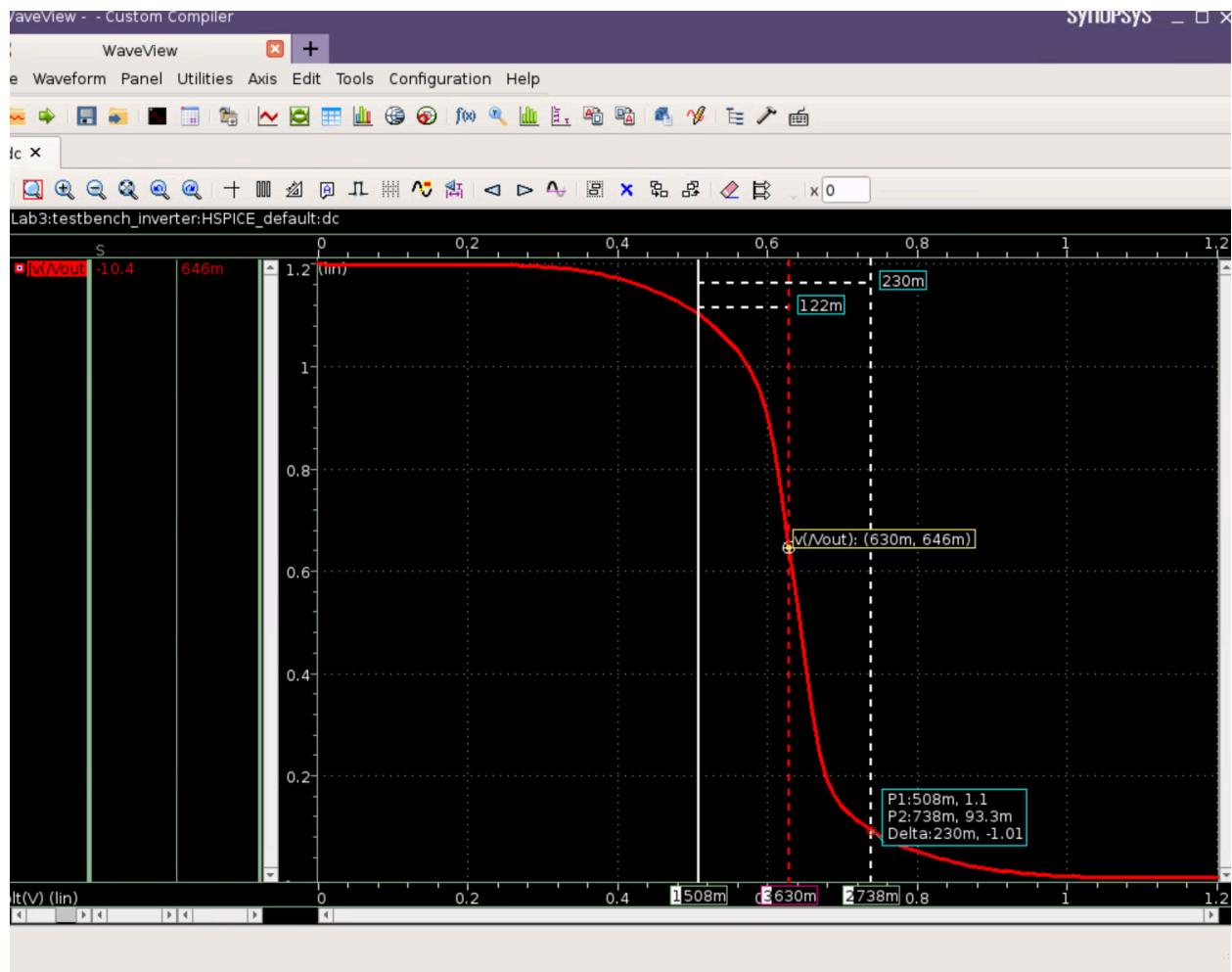








## Part 1: Inverter VTC



$V_{IH} = 0.736 \text{ V}$

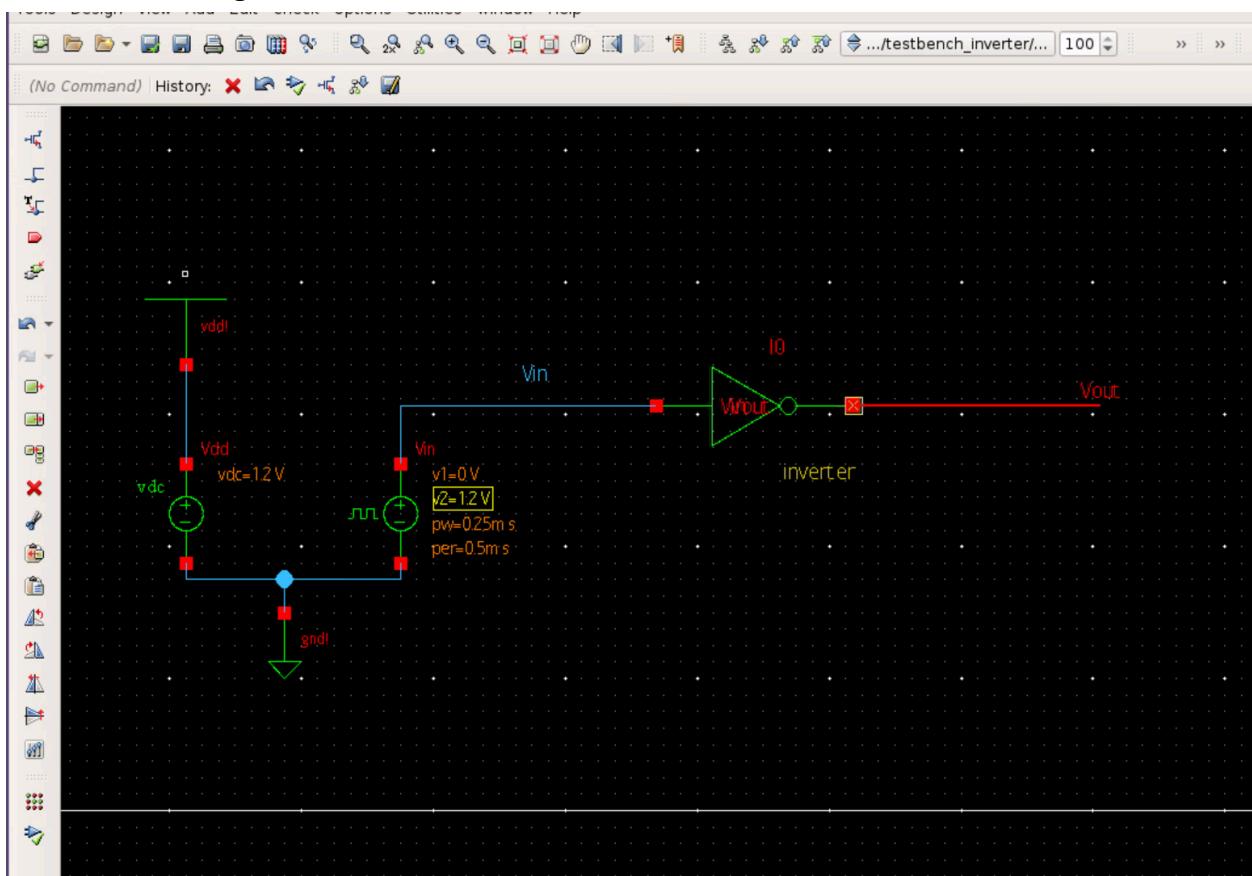
$V_{IL} = 0.508 \text{ V}$

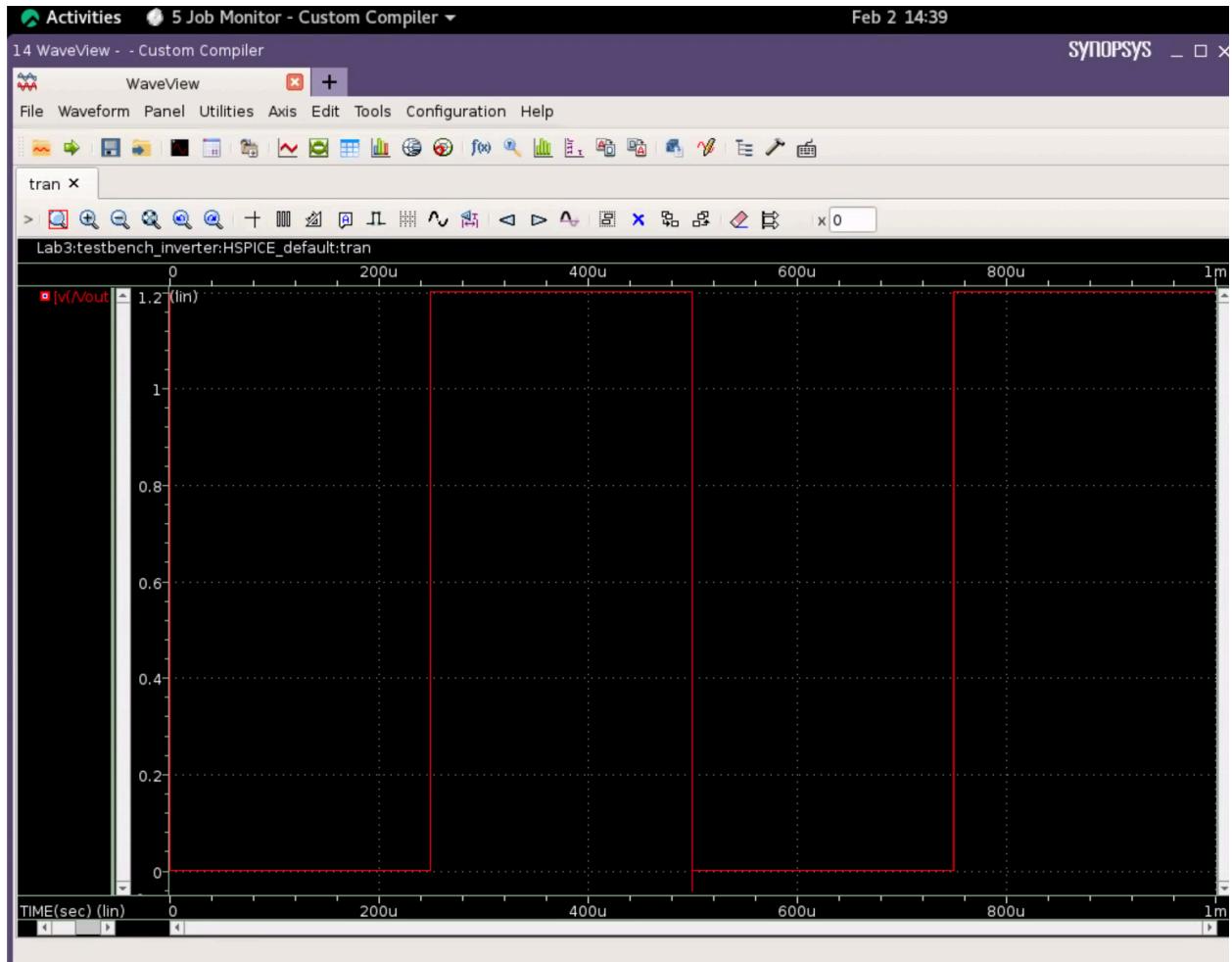
$V_{OL} = 0.0948 \text{ V}$

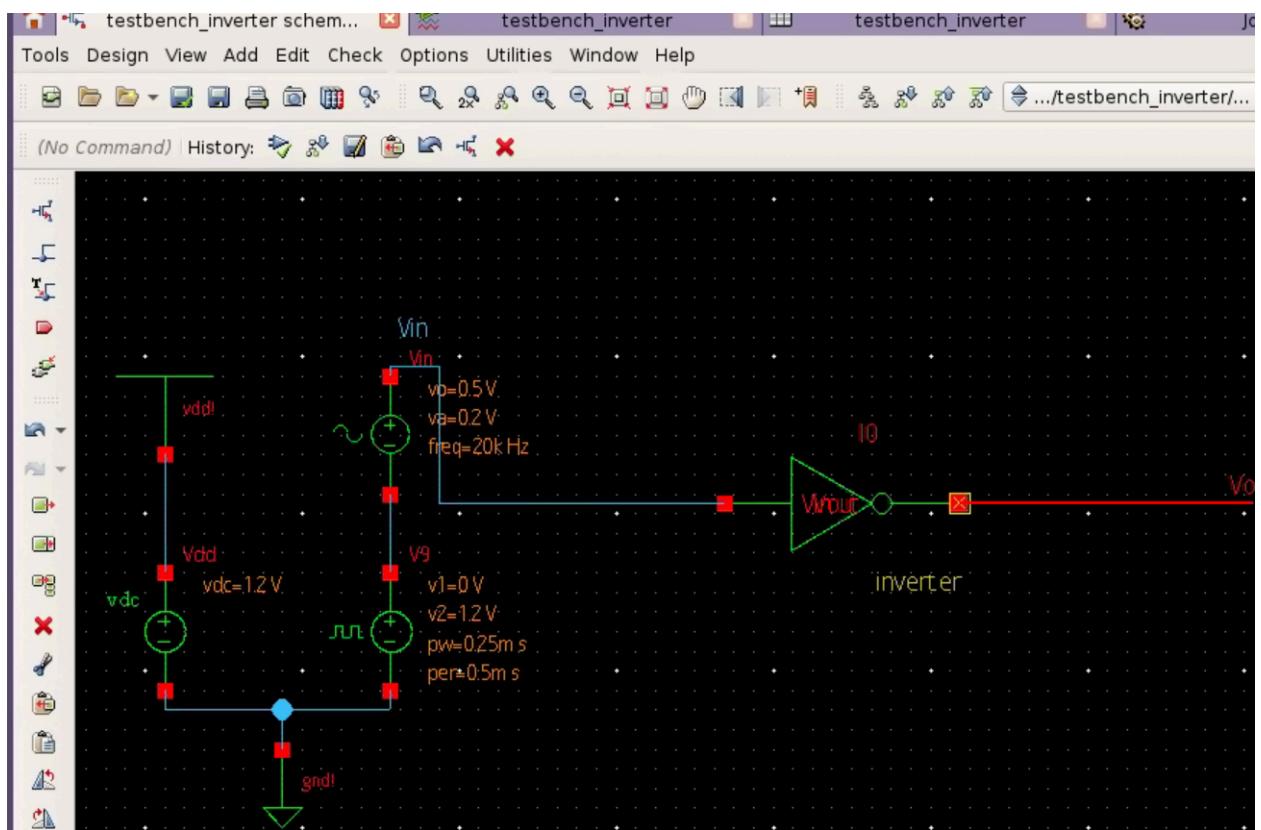
$V_{OH} = 1.1 \text{ V}$

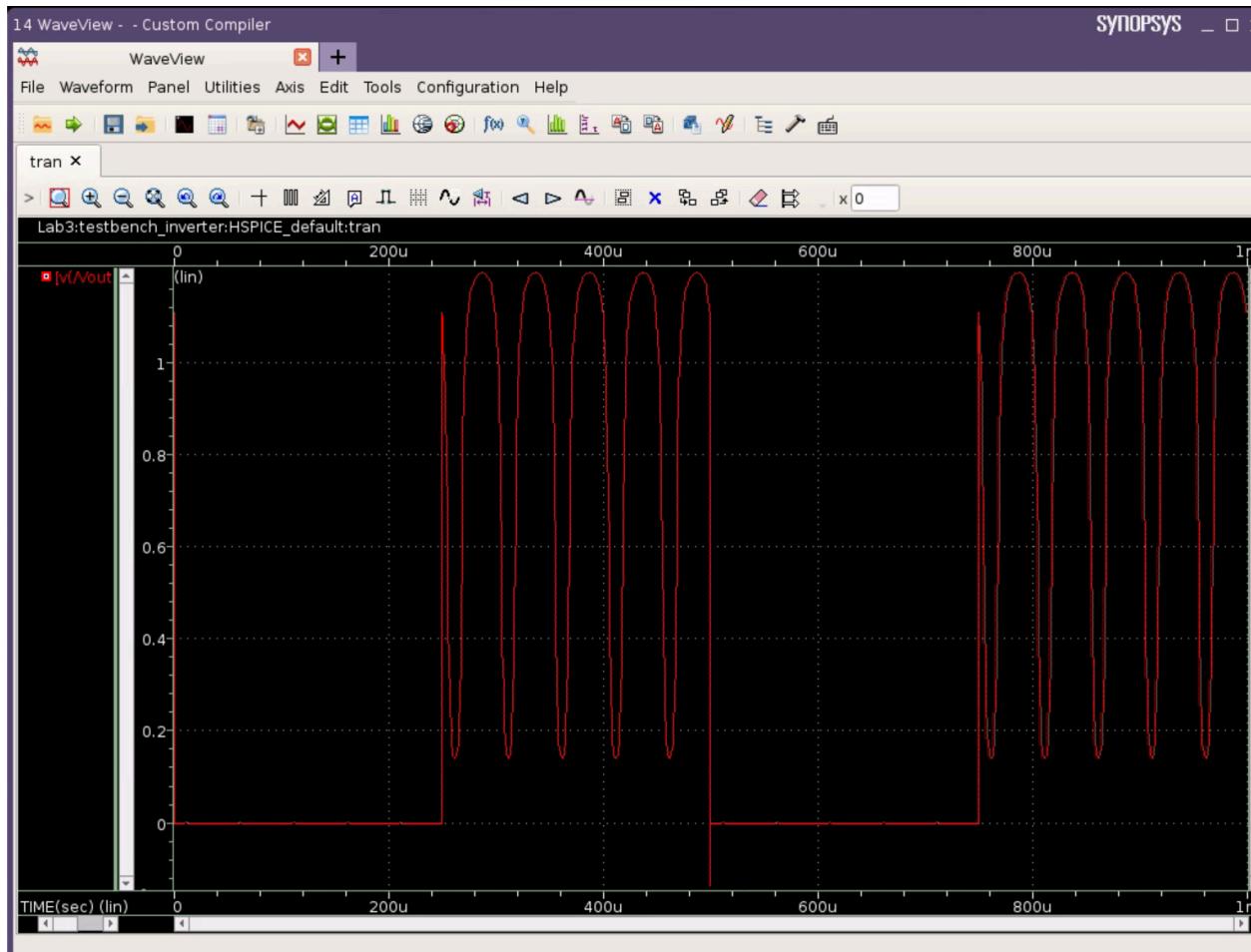
$V_M = 0.640 \text{ V}$

## Part 2: Noise Margins









*What do you observe?*

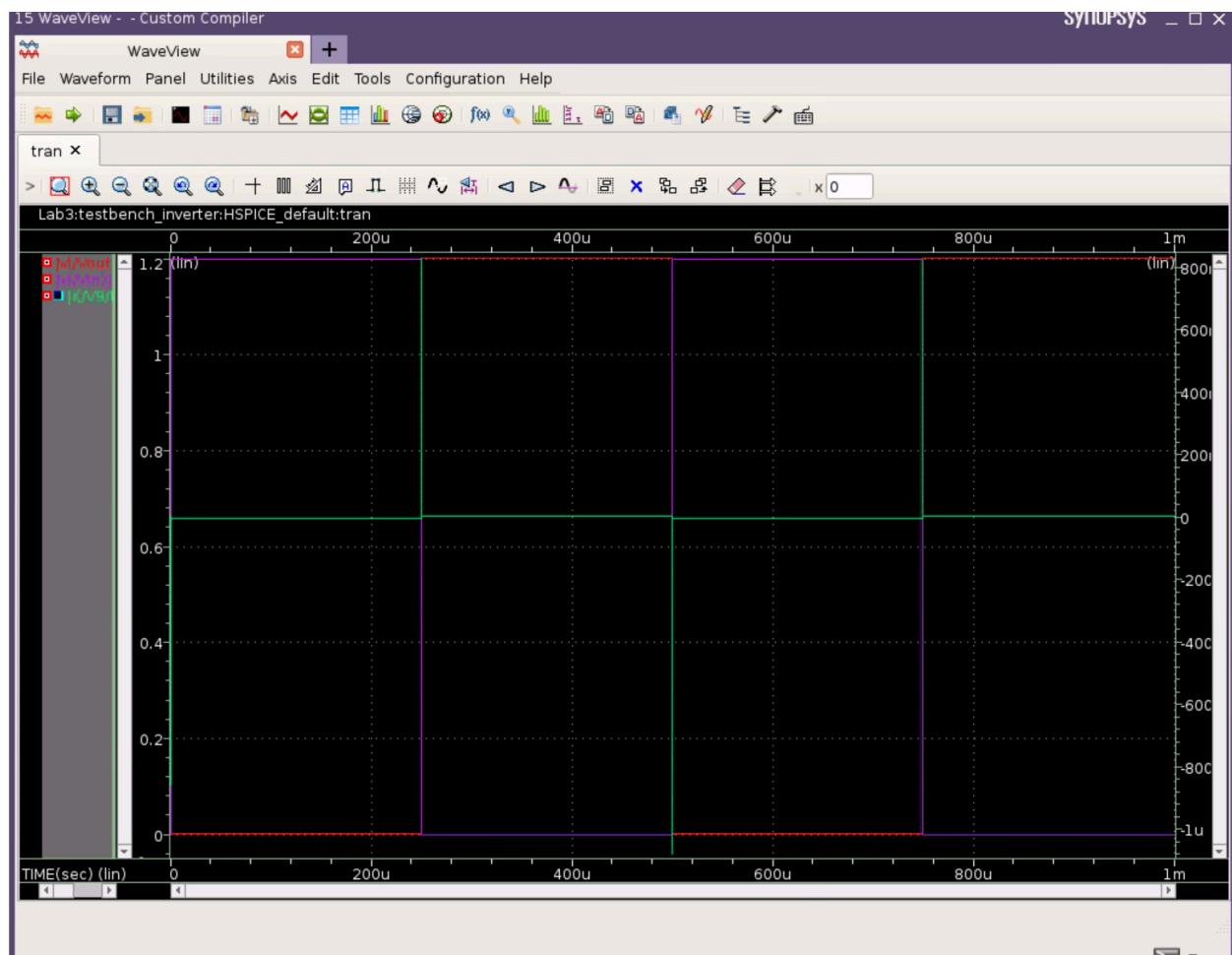
output is only on when the input drops into a specific lower voltage range so the inverter is like a level-sensitive gate for the signal

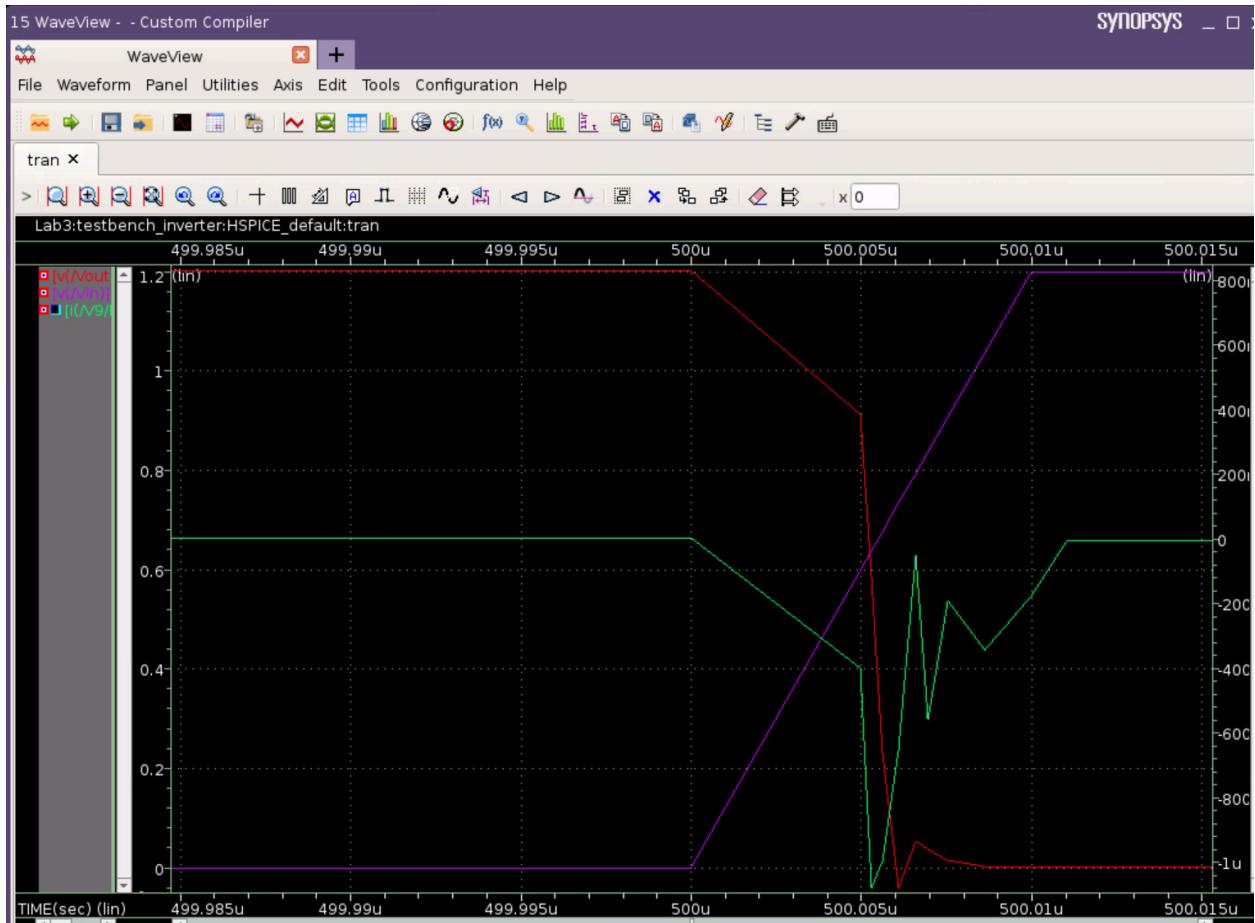
### Part 3: Propagation delay



tp<sub>LH</sub> = 157ps

tp<sub>HL</sub> = 317ps



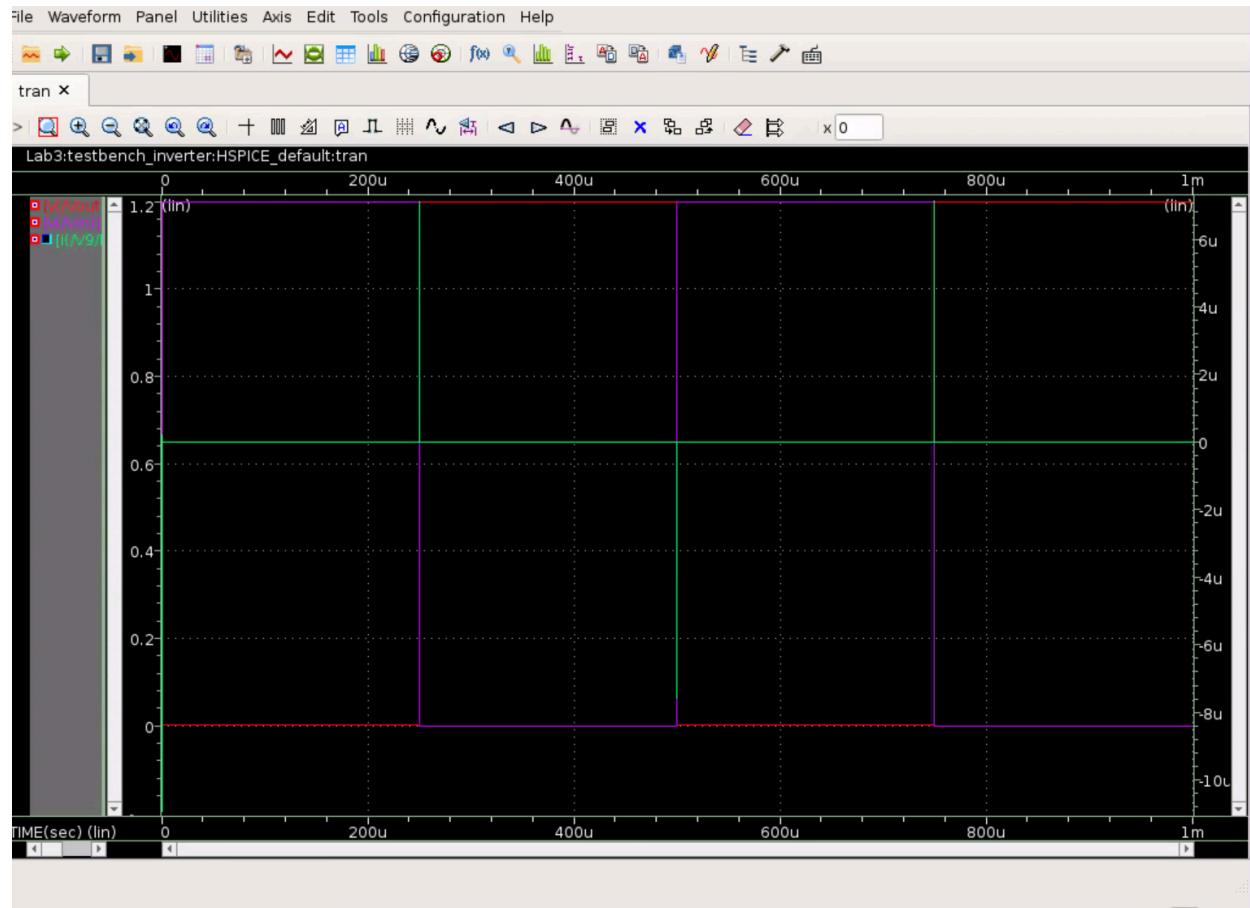


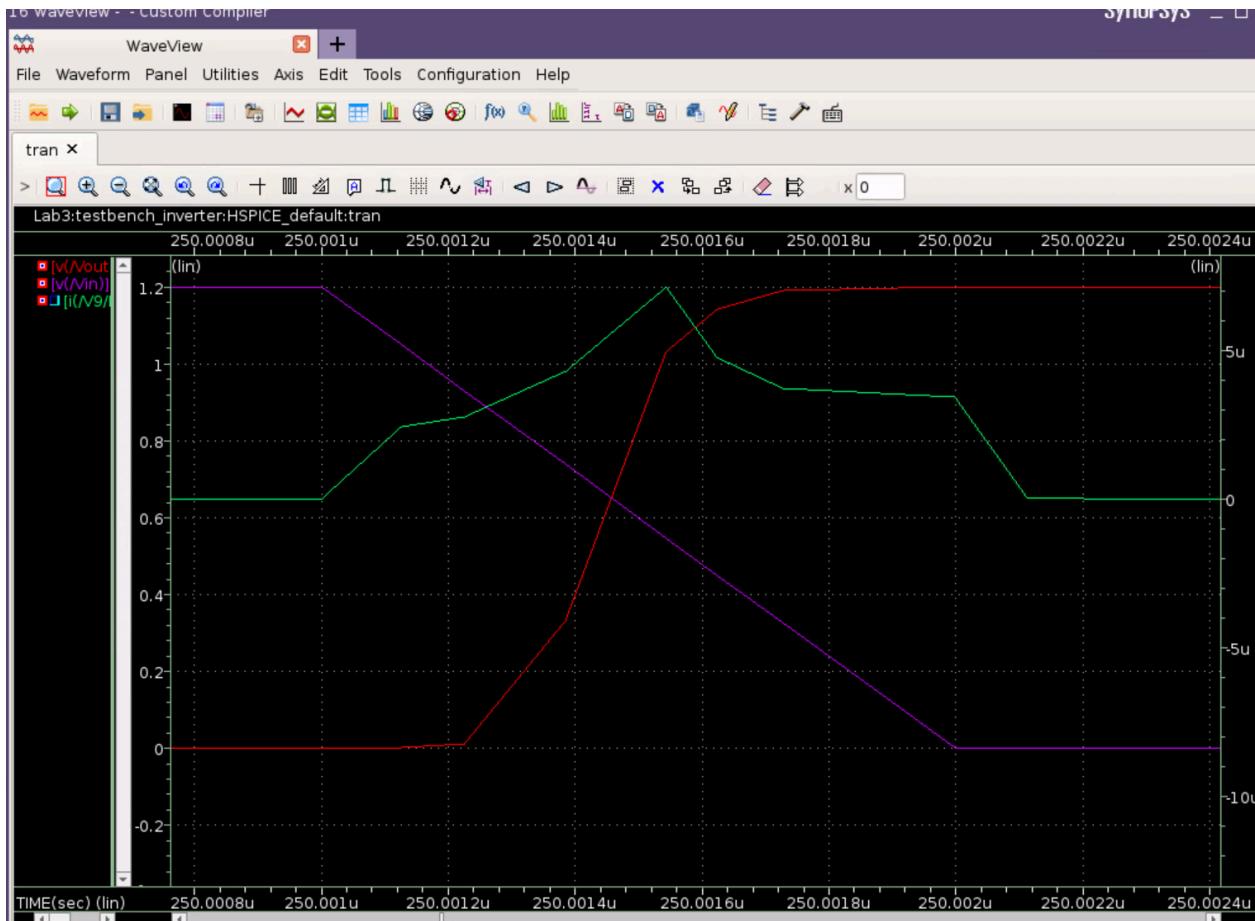
*What device works on pulling the output to VDD and what works on pulling it down to ground?*  
 NMOS pulls down to ground, PMOS pulls up to Vdd.

*What do you notice about the current from VDD? Explain what the various sections are and why this happens.*

When Vout flips from 0 to 1, current from VDD goes through PMOS to charge output capacitance. The area under the curve of this current pulse is actually the charge accumulated at the output node / output voltage.

When Vout flips from 1 to 0, the charge on the output capacitance discharges through the NMOS to GND. No charge is drawn from VDD in the transition, except some short-circuit current when it switches.





Change the rise/fall time to 1ns

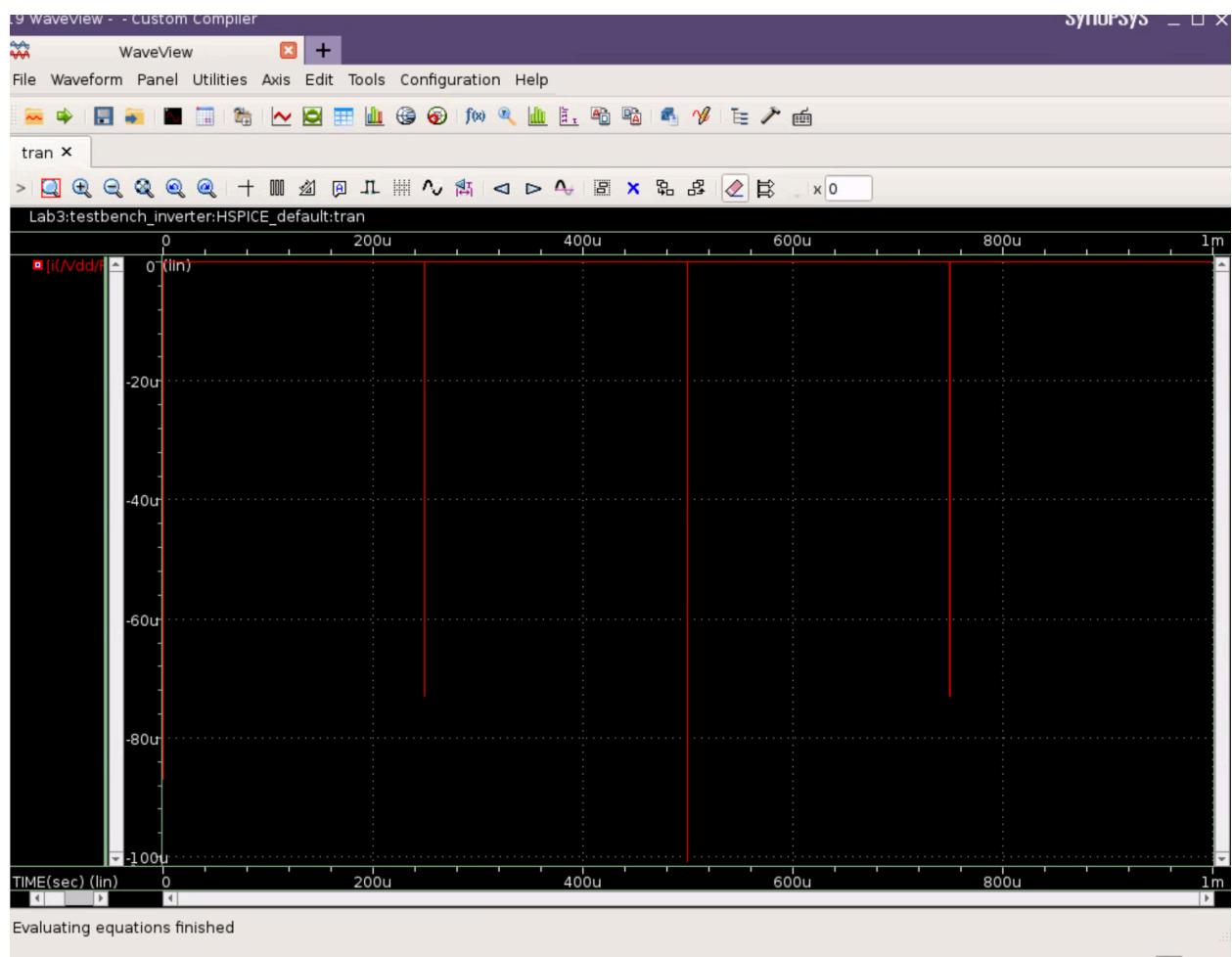
*What device works on pulling the output to VDD and what works on pulling it down to ground?*  
NMOS pulls down to ground, PMOS pulls up to Vdd.

*What do you notice about the current from VDD? Explain what the various sections are and why this happens?*

The current draw from VDD are like short pulses during transitions. When Vout switches from 0 to 1, the PMOS turns on and gives current from VDD. The current rises, reaches its peak, and then falls back to 0 as the output approaches VDD. Because the rise/fall time is 1 ns, there is a time where both PMOS and NMOS are on and a short-circuit current path from VDD to ground is created and that increases peak current.

When Vout switches from 1 to 0, the PMOS is off and the NMOS discharges to ground, so no current is drawn from VDD.

## Part 4: Power



average = -24.1 nA

## **Conclusion**

In this lab the plots helped me so much in understanding CMOS inverters. It made a lot of sense the way we made it into our own custom symbol that we can apply to a simple circuit. All it really needed was the proper voltage source. The most confusing part was getting my graphs to not be flat, but then after about 3.5 hours of troubleshooting it worked all of a sudden. I am unsure why, but I definitely got deeper into the ins and outs of Synopsys Custom Compiler due to that. I also am a lot more comfortable with the measure tool, now that we have used it to do the average, slope, and other measurements.