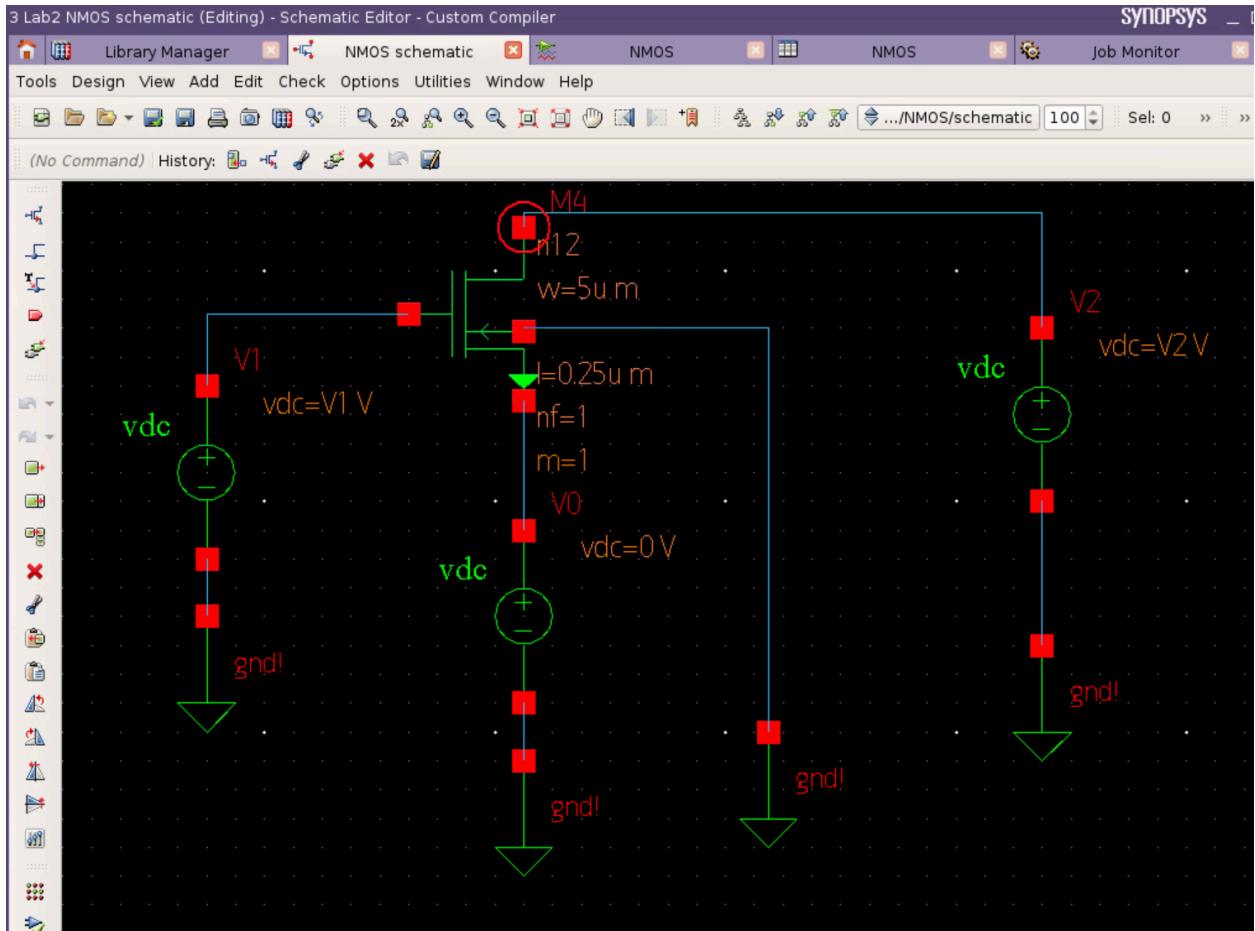


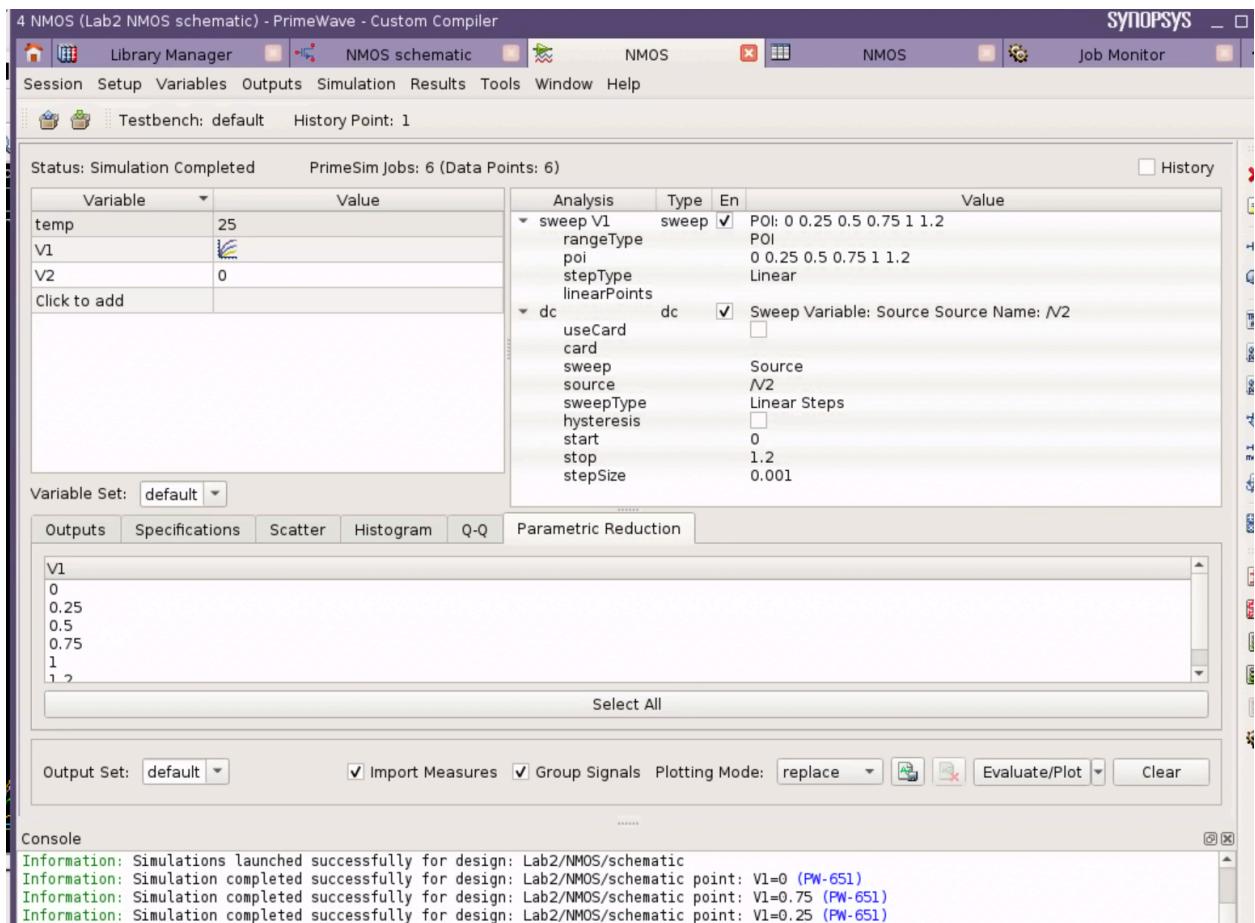
# ECEN 153L Lab 2 Report: MOSFET

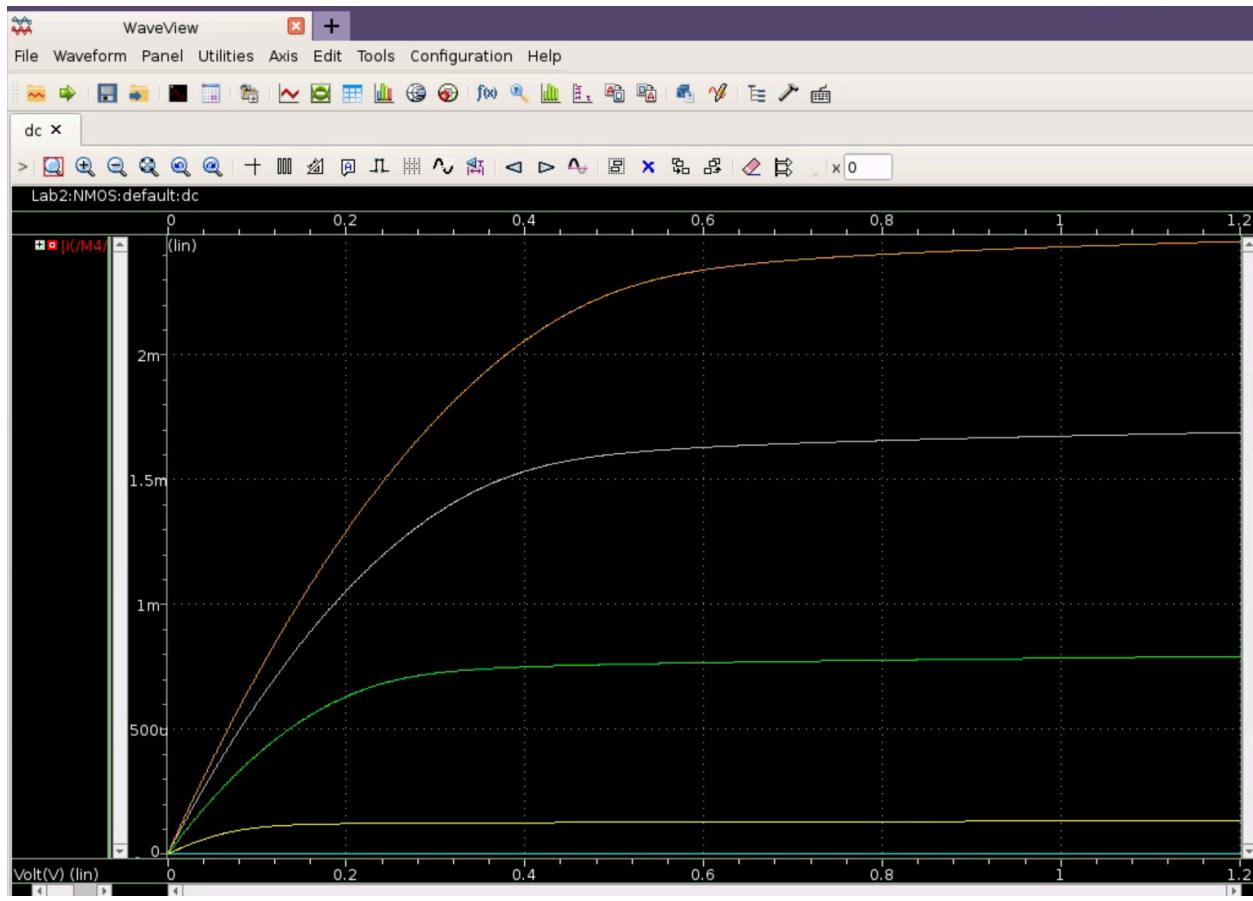
## Characteristics

Aveed Gorji 1/23/26

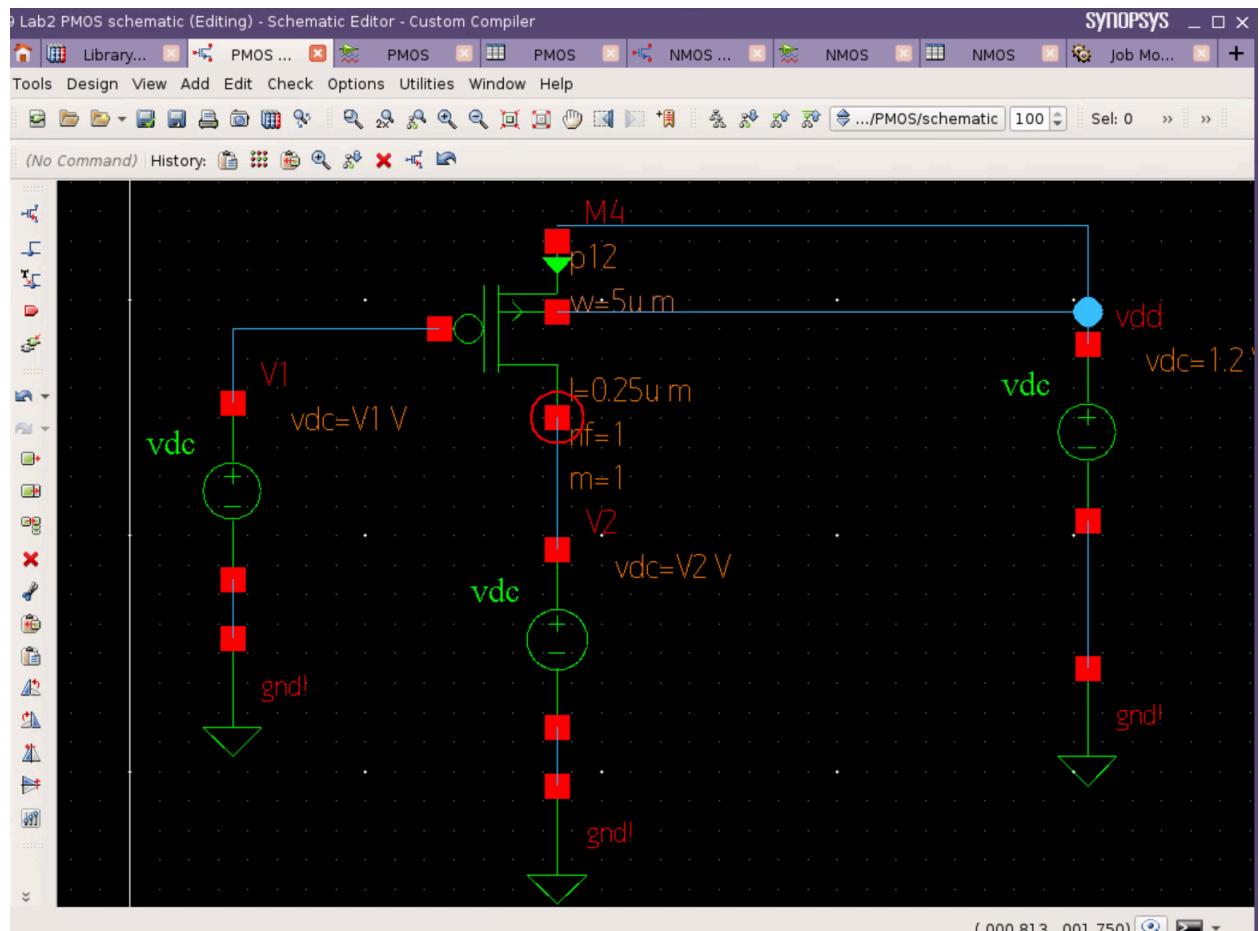
### Part 1B

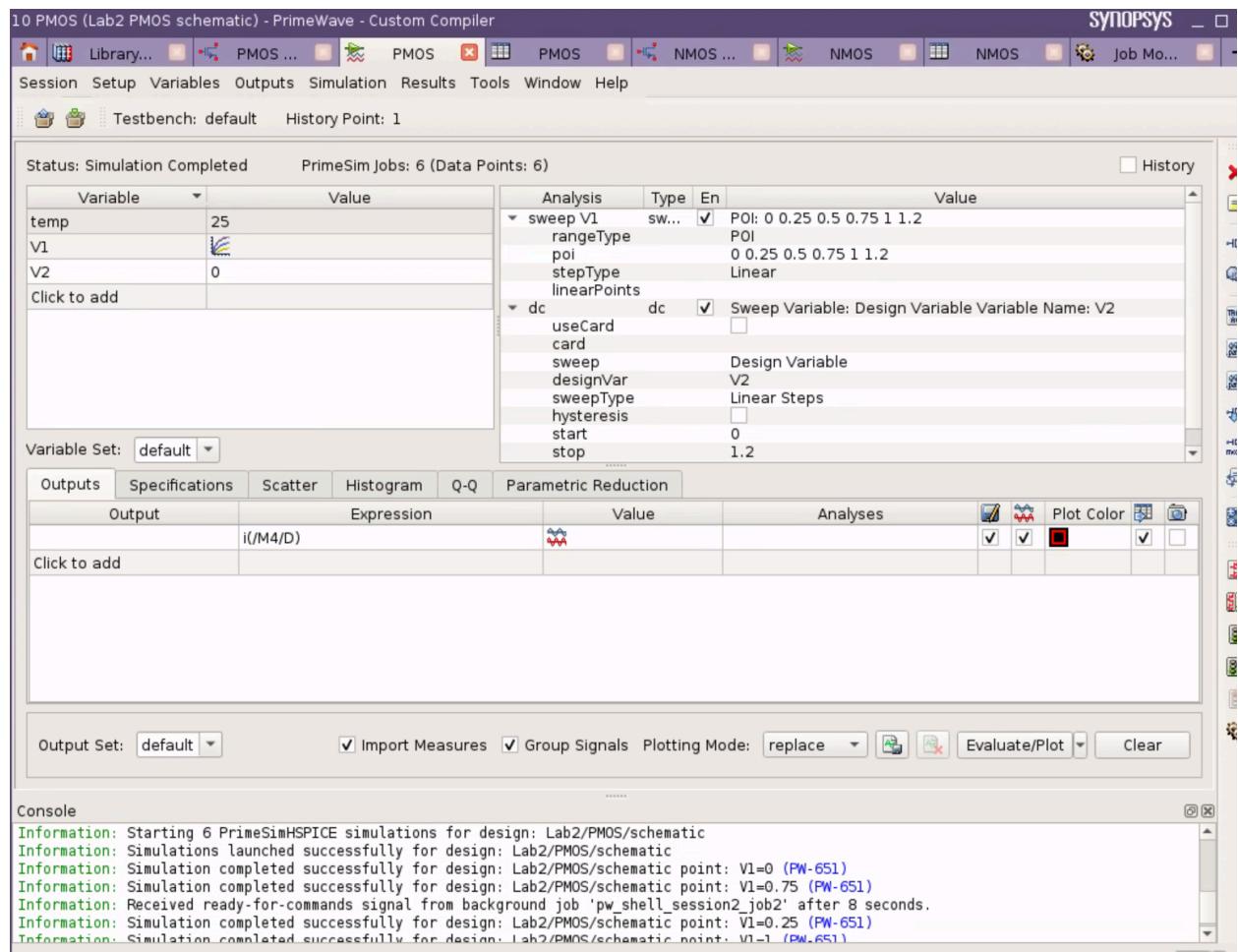


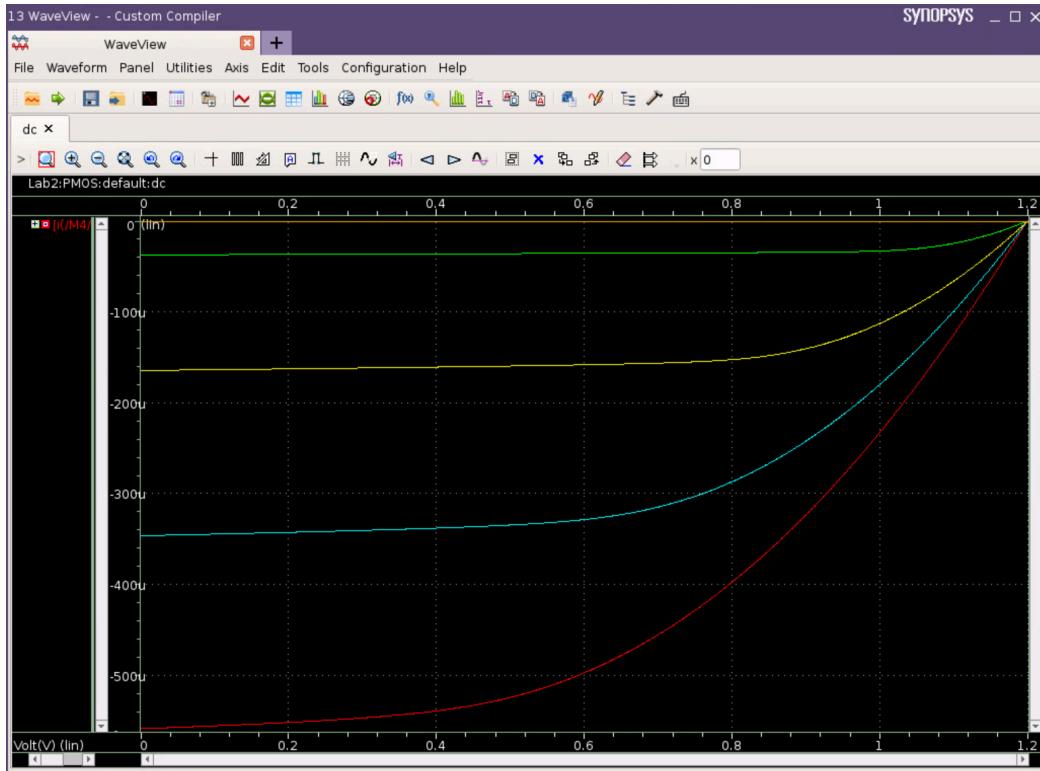




## Part 1C







## Questions

*How do the NMOS I-V curve differ from the PMOS I-V curve?*

The PMOS IV curve is inverted compared to the NMOS curve because of the difference in polarity.

*For the same size NMOS and PMOS devices, what do you observe about the drain current values?*

We can see that the NMOS provides around 2.5mA of current at the peak because it relies on electrons, while the PMOS gets to 500uA since it relies on holes and that is slower. So the NMOS current drive is about 5x stronger than the PMOS.

*Compare your simulation results with your prelab calculations. Are they the same or are they different? Explain your observations.*

There was a difference in current drive power between the two. In simulation the NMOS reached a peak current of 2.5 mA, while the PMOS only reached -500uA. These results are within an order of magnitude with the pre-lab theoretical calculations, so they are close enough. I predicted 1.31 mA for the NMOS and 519 uA for the PMOS. The prelab parameters  $K'n = 200\mu A/V^2$  is more than three times higher than the PMOS  $k'p = 60\mu A/V^2$  so that matches what we noticed with how the electrons have higher mobility when compared to the holes' mobility.

## Part 2

VDS	VGS	Region of operation	Resistance
0.25	0.25	saturation	4.96M
0.25	0.75	saturation	1.1K
0.25	1.2	linear	224
0.75	0.25	saturation	6.16M
0.75	0.75	saturation	21.5K
0.75	1.2	saturation	4.47K
1.2	0.25	saturation	5.66M
1.2	0.75	saturation	27.6K
1.2	1.2	saturation	9.7K

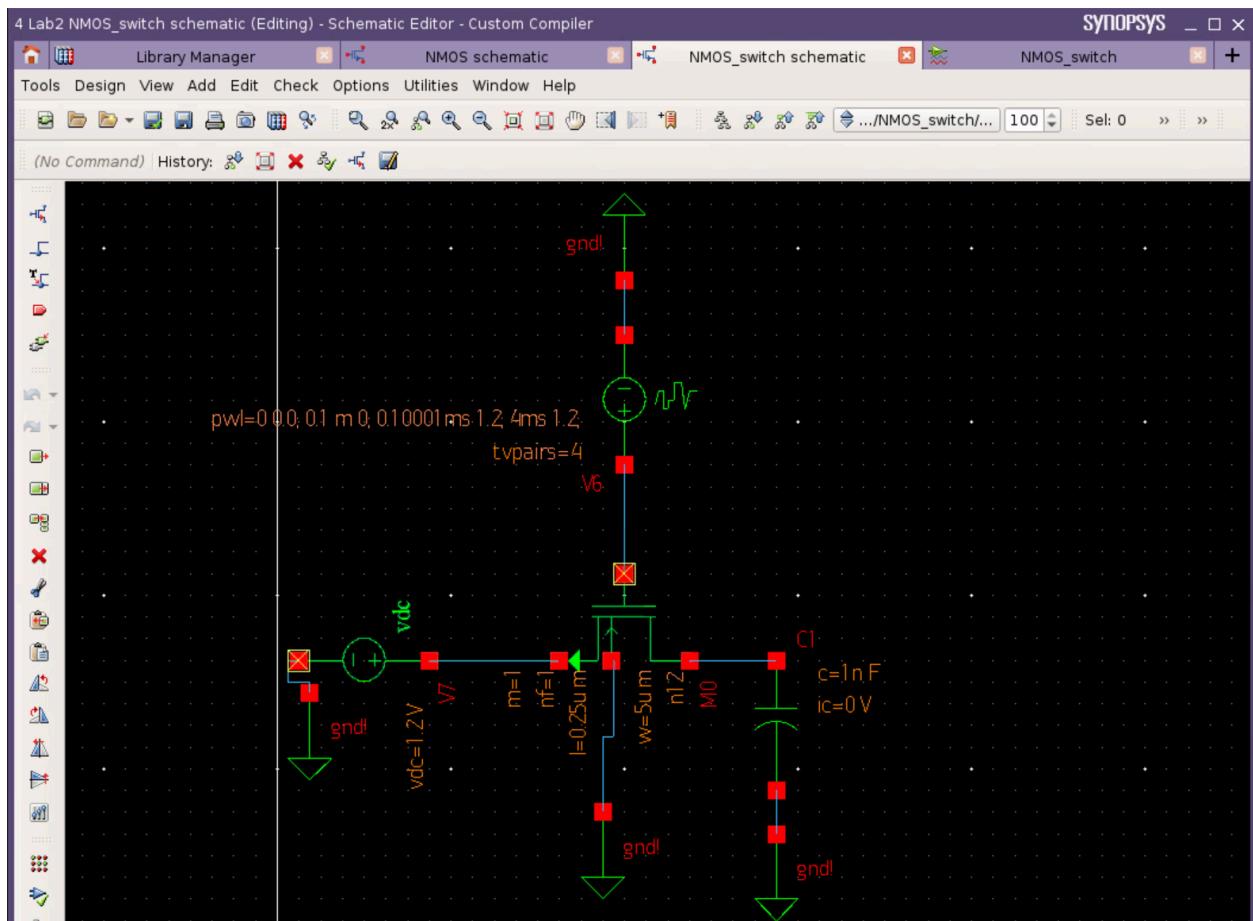
### Questions

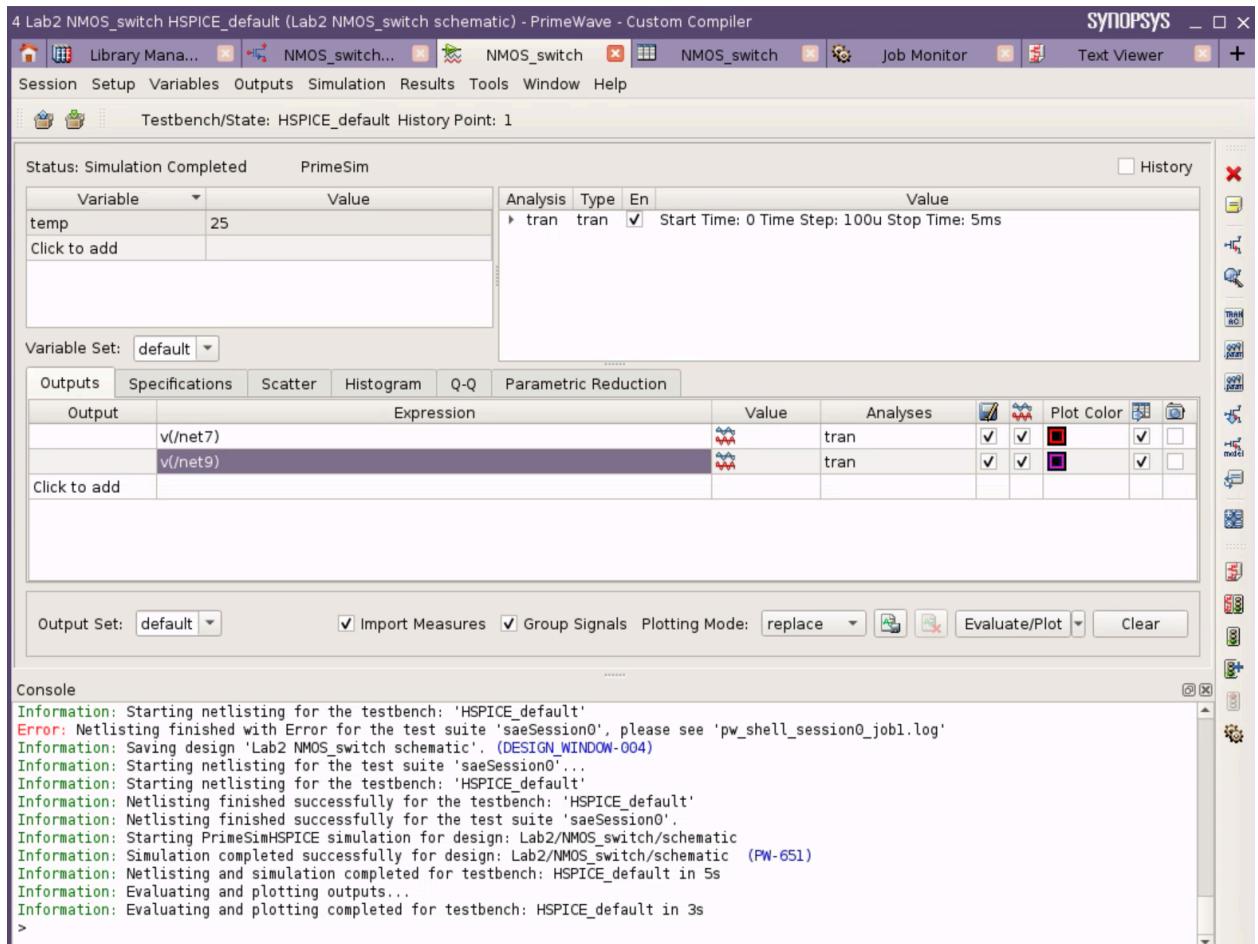
*How does the resistance change with the region of operation?*

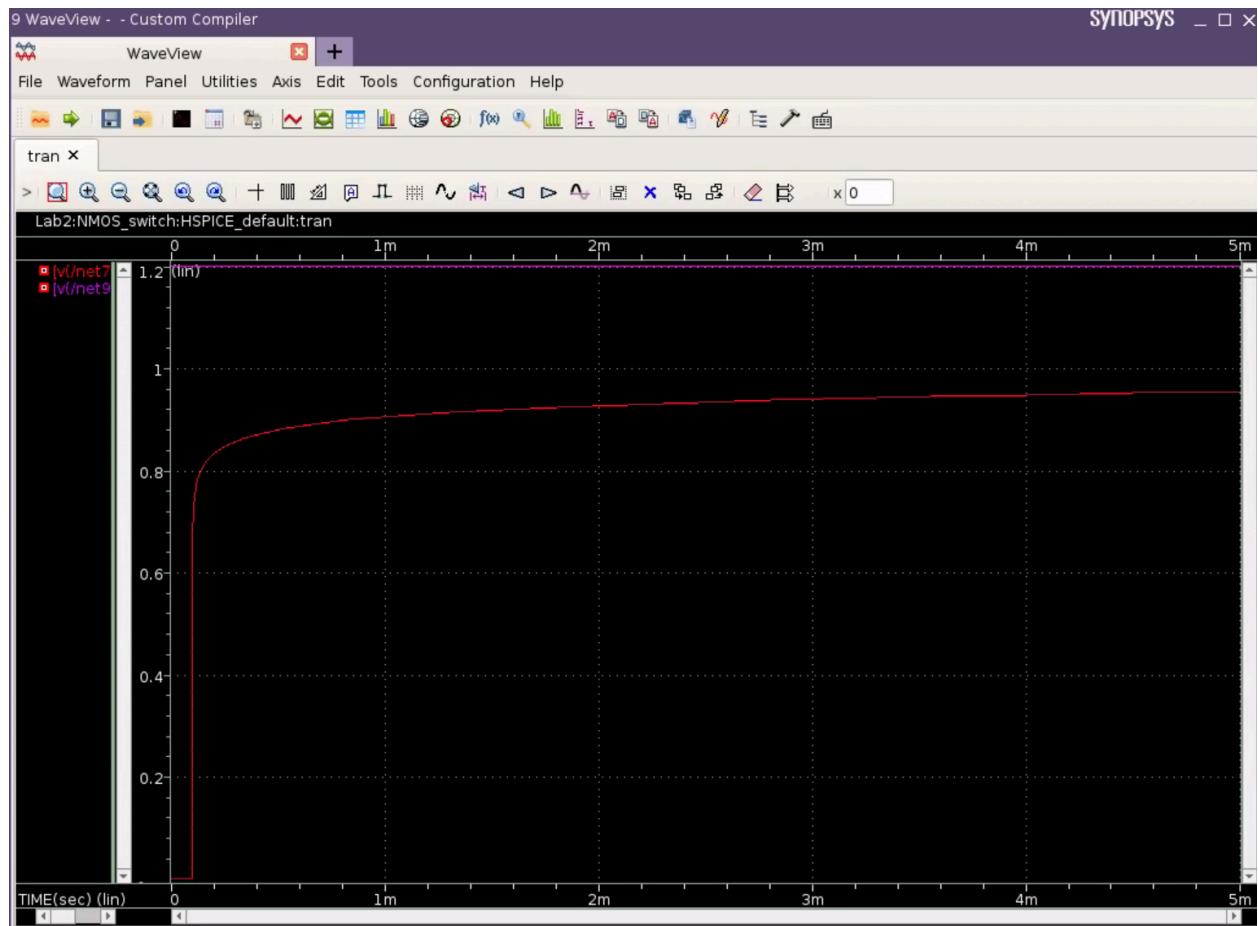
In linear, the mosfet has low resistance with a steep slope and is like a voltage-controlled resistor. In saturation the resistance is extremely high with a flat IV slope because the channel pinches off

In the linear region, how does the resistance change with increasing VGS? Explain why Rds decreases as Vgs increases because the more Vgs the more electric field and attracts carriers and lowers resistance

### Part 3A



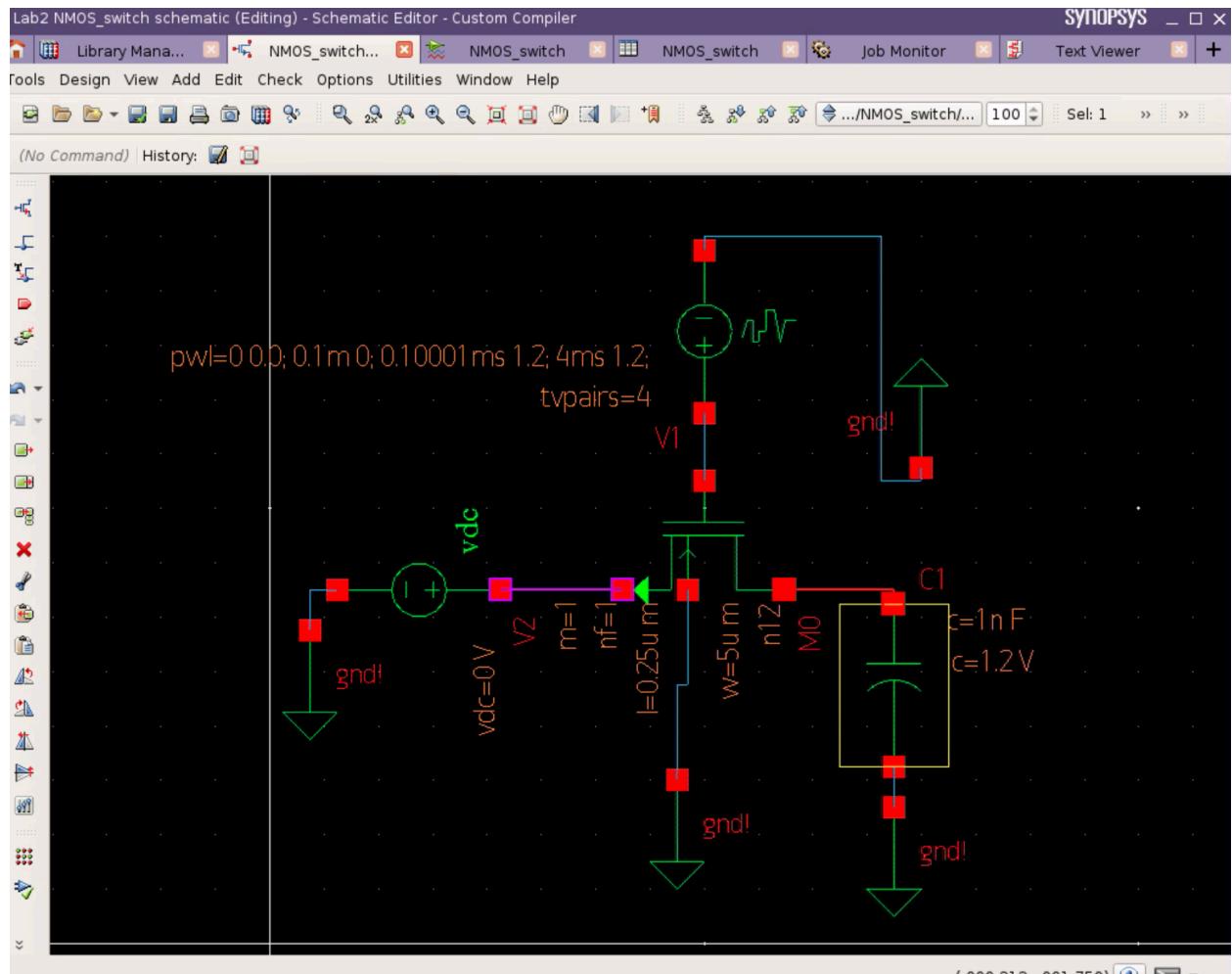


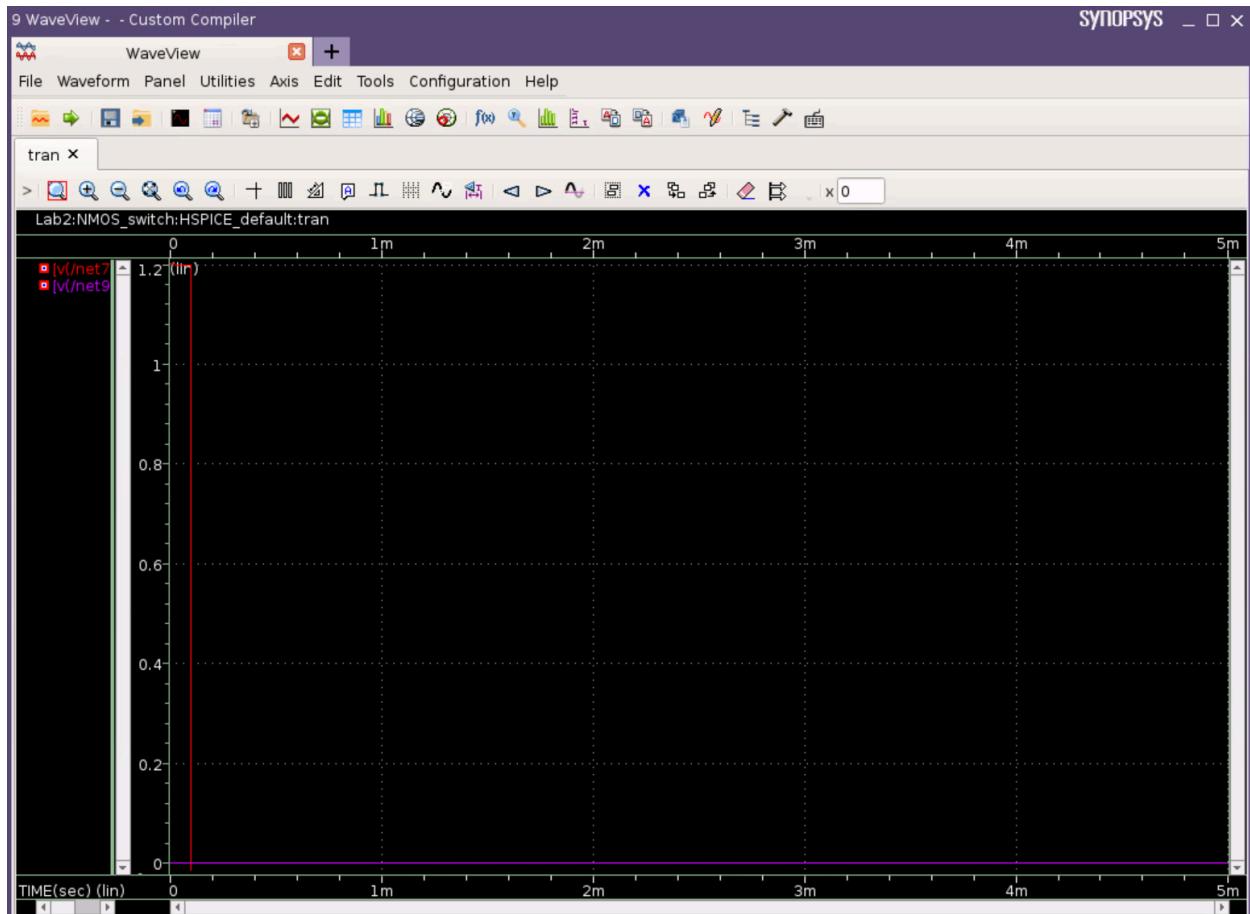


### Question

3A-g Observe the voltage on the capacitor and explain the behavior

The NMOS is a weak pull up, when at 0.1ms it charges the capacitor, then it levels out around 0.95 V since the transistor stops conducting effectively then.



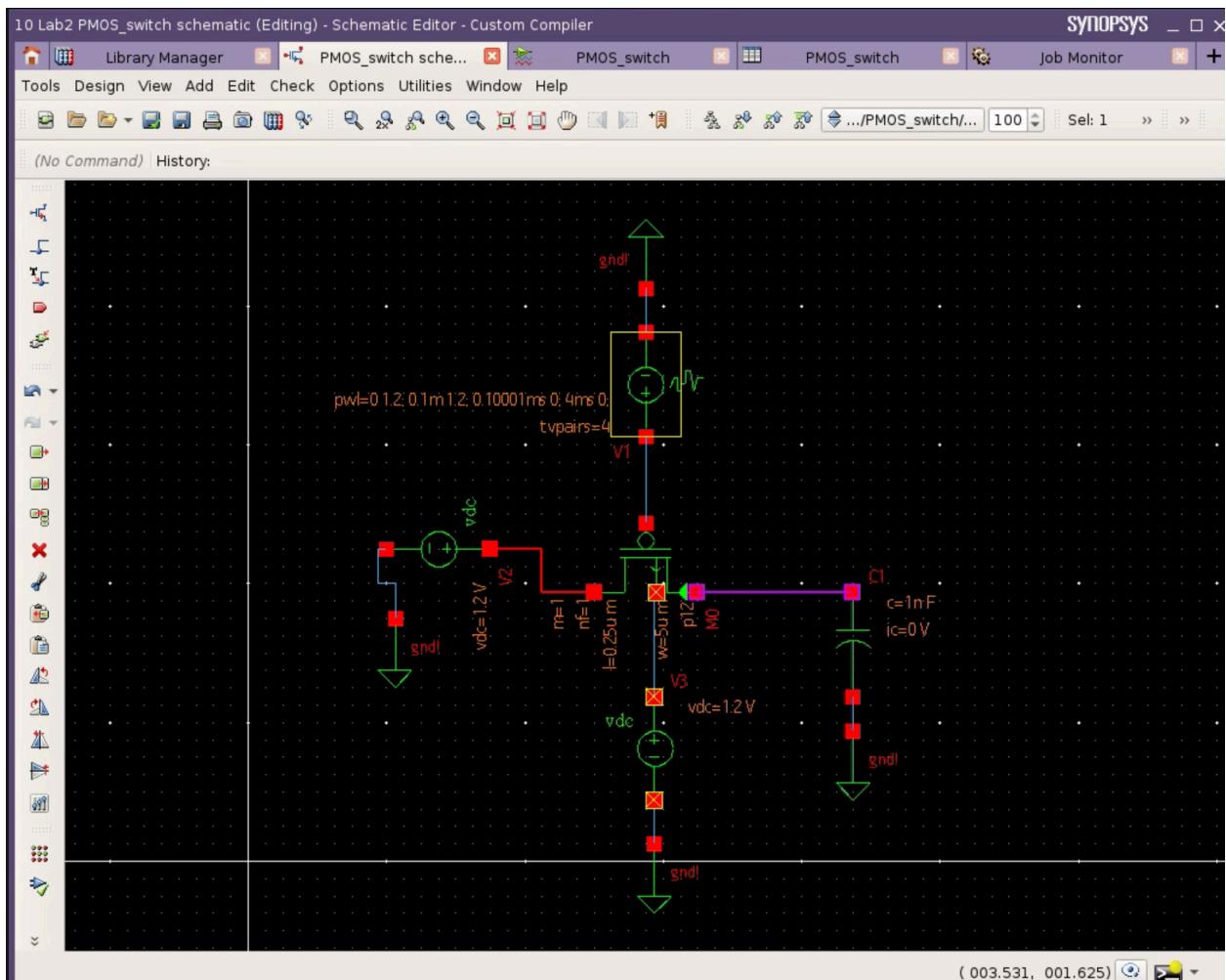


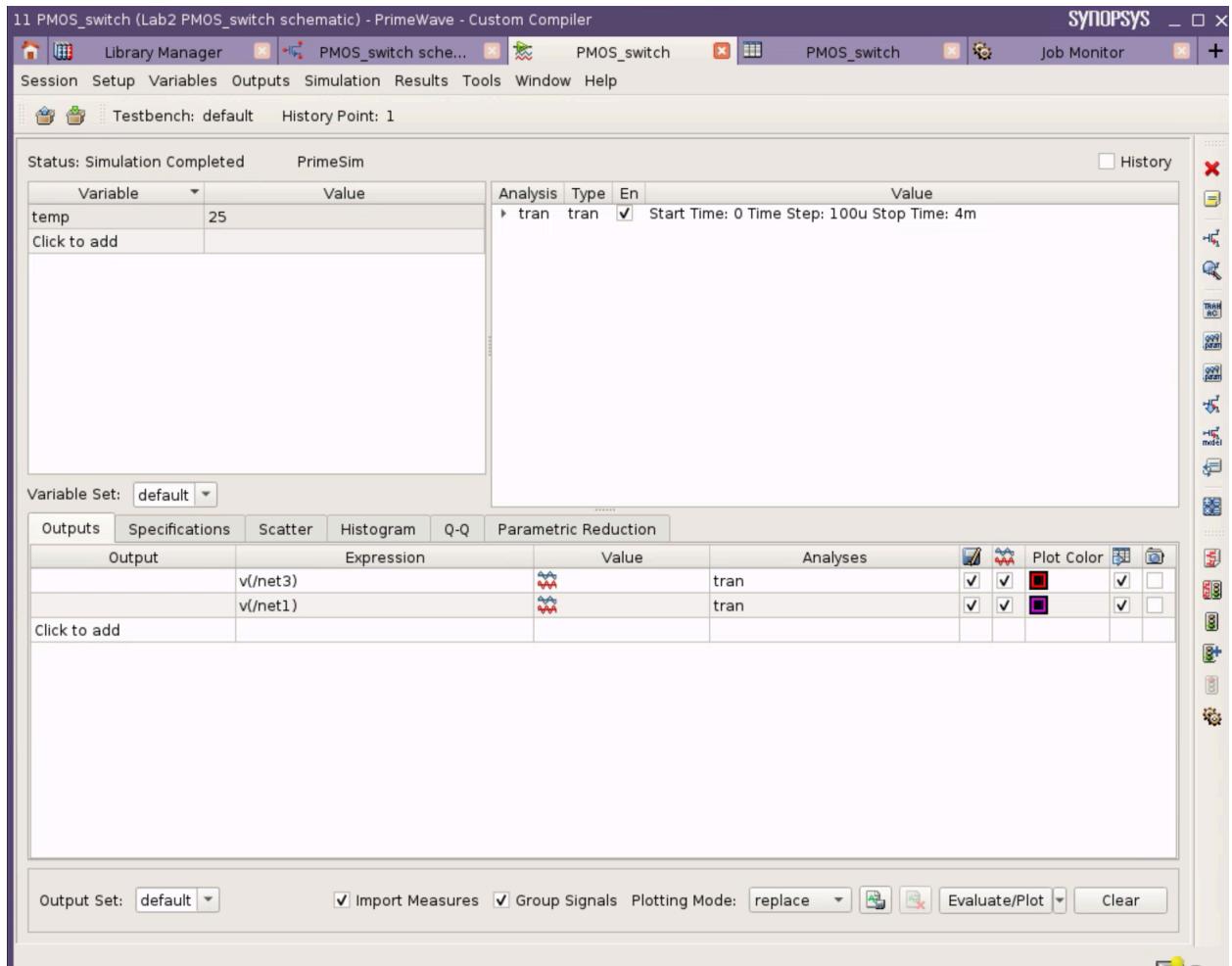
### Question

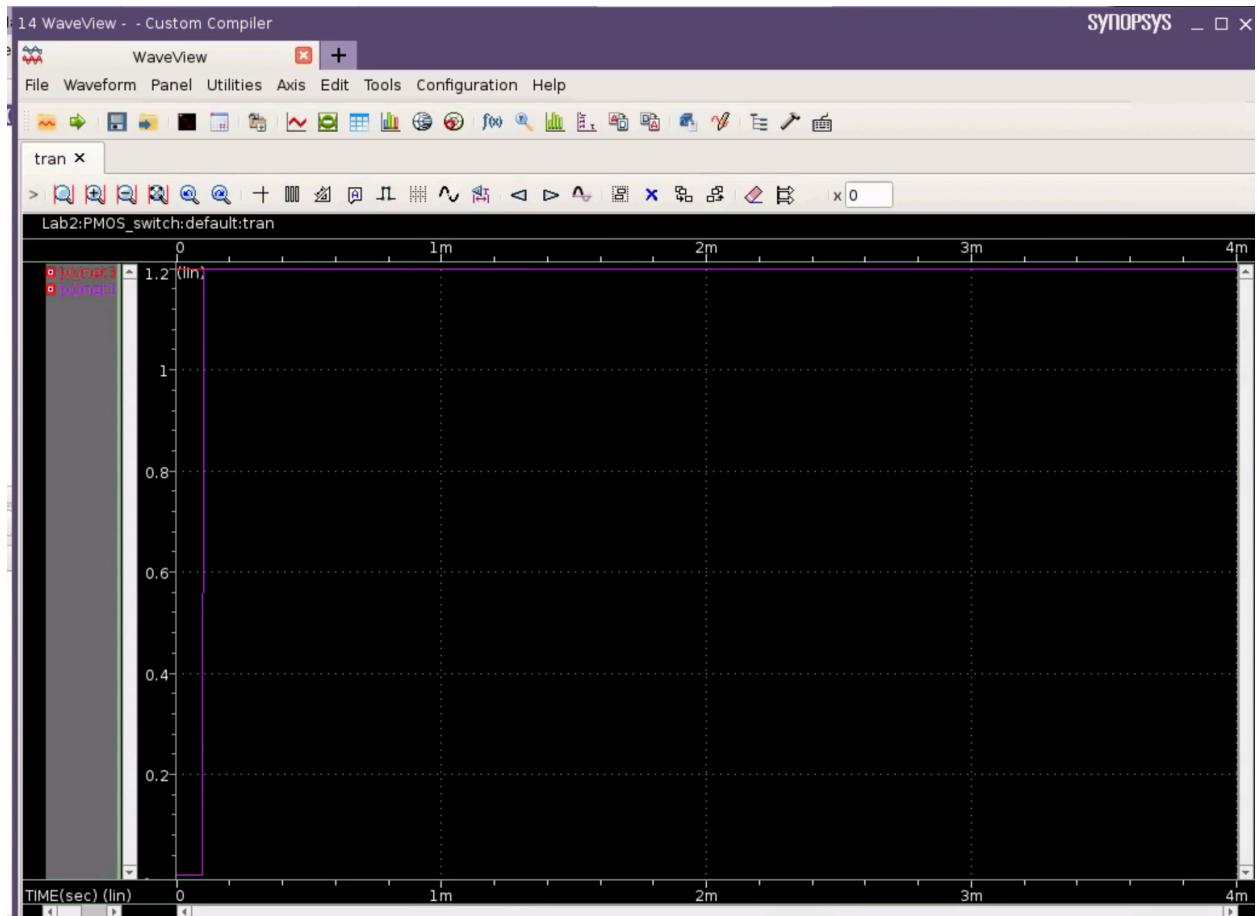
3A-k *Observe the voltage on the capacitor and explain the behavior*

The capacitor being the voltage source for a moment while the other side is not a voltage source anymore caused virtually instant discharging

## Part 3B



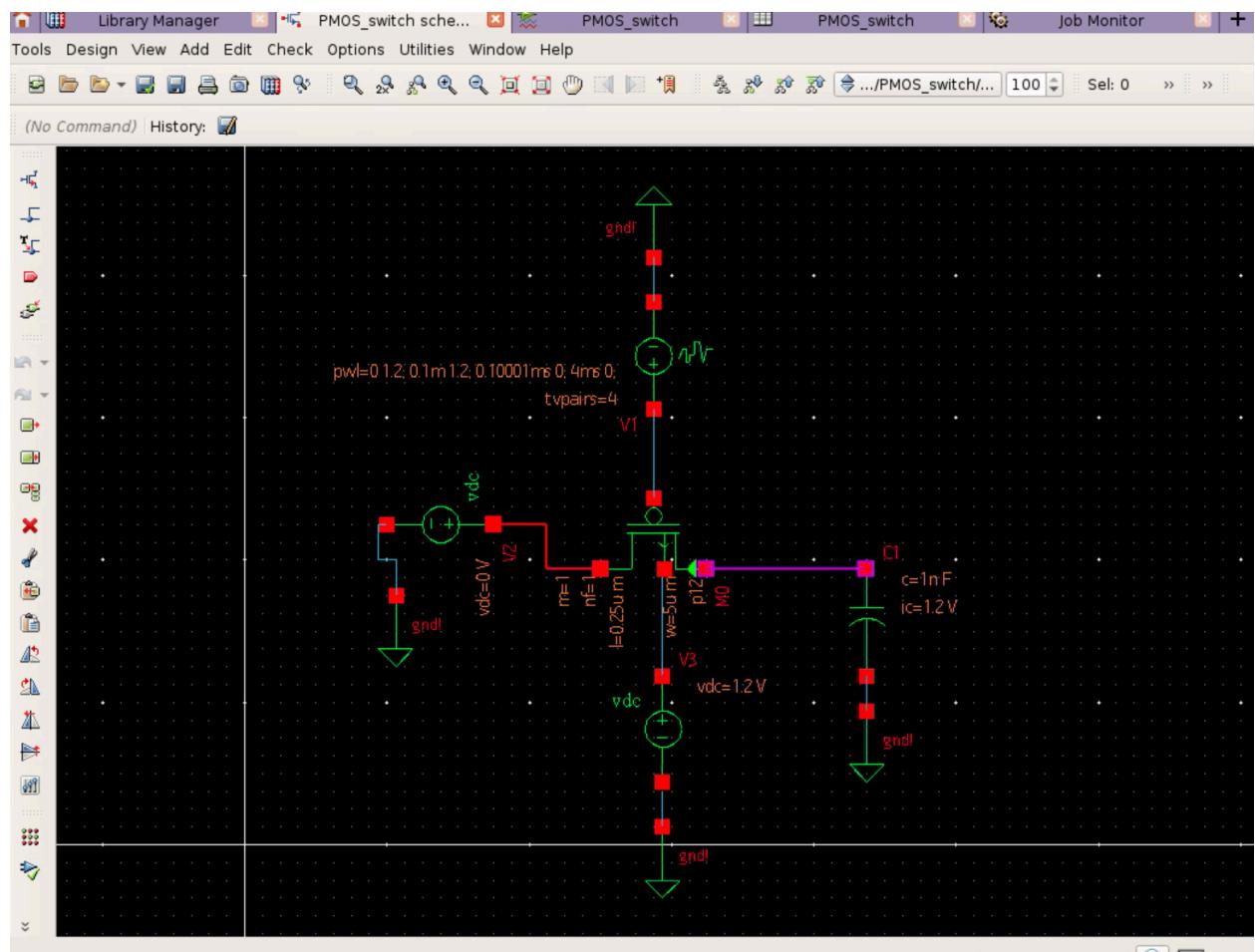


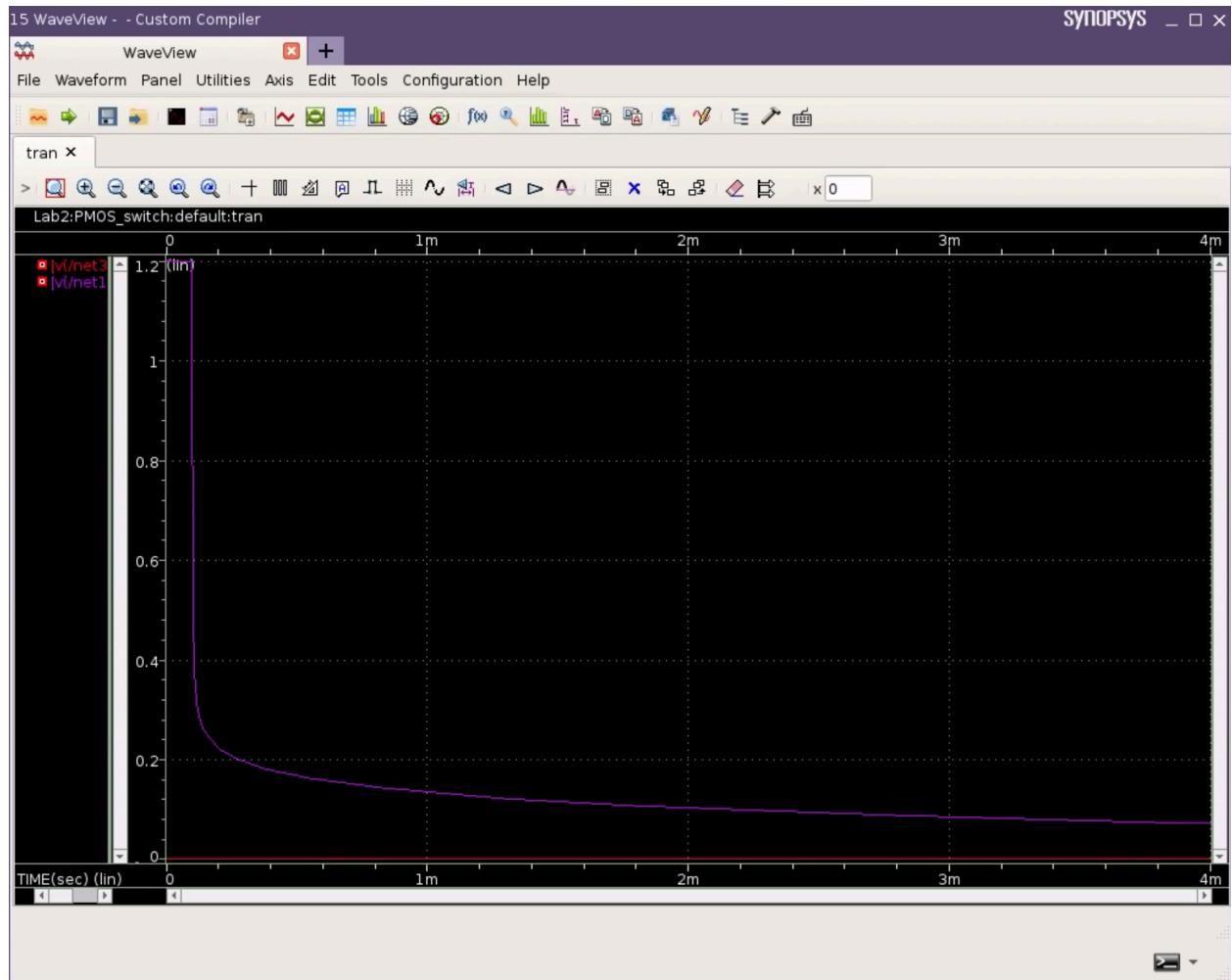


### Question

3B-h Observe the voltage on the capacitor and explain the behavior.

The capacitor's voltage  $V_{out}$  immediately jumps, so this means that the PMOS is a strong pull-up or strong 1 carrier and it does not have a big threshold voltage drop when pulling a high.





### Question

3B-I Observe the voltage on the capacitor and explain the behavior

The voltage of the capacitor is slowly discharging but does not hit 0V. PMOS is a weak pull-down. The V<sub>gs</sub> needs to be over the V<sub>tp</sub>, but as we approach that V<sub>tp</sub> with the capacitor voltage, the transistor is basically turning off, so it is not effectively conducting anymore.

### Question

From the plots, comment on the pull-up and pull-down characteristics of the NMOS and PMOS devices.

As we can see, the NMOS is clearly strong at driving a LOW/0 based on the way that it immediately takes a capacitor's voltage down when set up normally, but when reversed, it struggles to charge it. PMOS is the opposite, the way that it can immediately maximize the voltage of the capacitor, but if we want to instead discharge the capacitor it struggles to get the voltage to 0 unlike the NMOS.

### Conclusion

We can clearly conclude that NMOS devices are properly suited to drive a 0 value, while PMOS devices are made to drive a 1. I can deduce from this lab that in combination, these two devices have the power to control basically all digital circuits. I also learned that the more in the saturation region we are in, the higher the resistance. While as we move into the linear region, the resistance decreases significantly.