ECEN 153L Lab 4 Report: CMOS Inverter Layout

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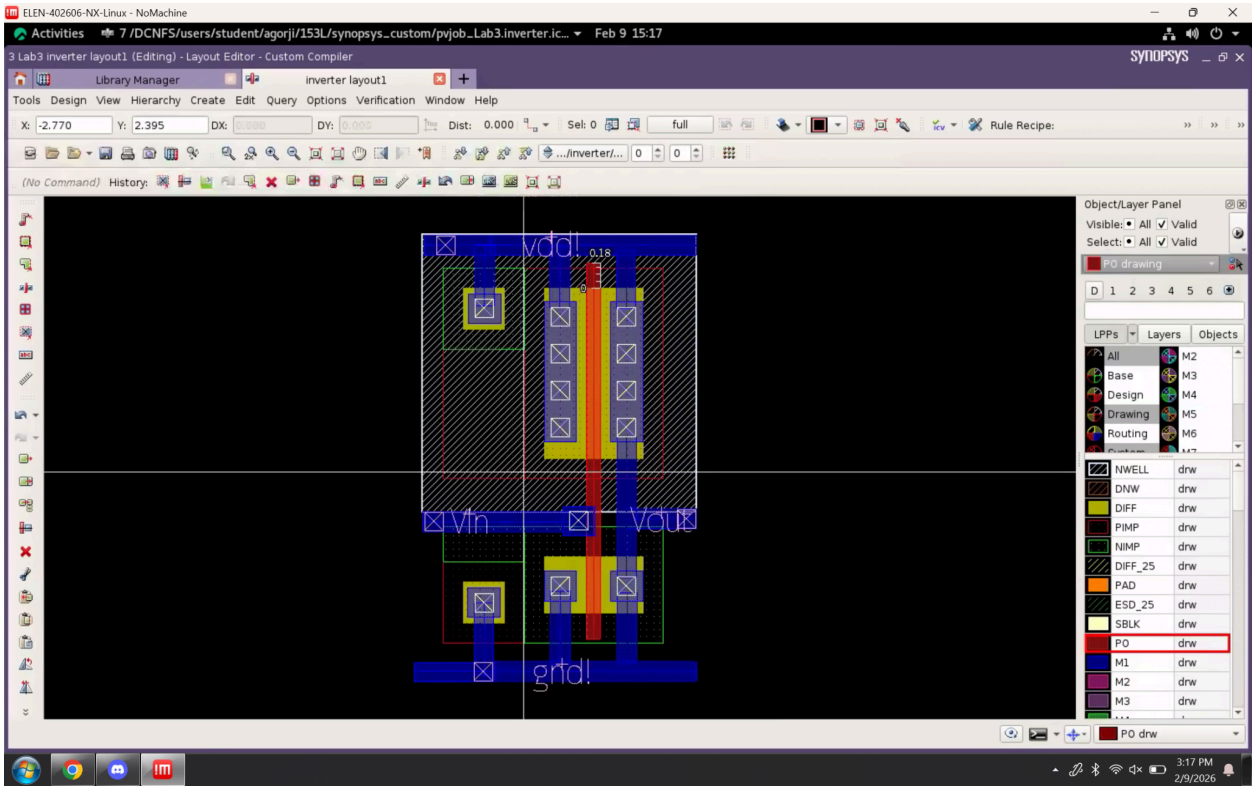
Part 1: Inverter Layout

Image of schematic



1. For your lab report, include a table of all the layout layers along with contact layers you used, and their corresponding names in Synopsys tools (ex. Metal 1 : M1)

Layout layers I used	Corresponding names in Synopsys
N-Well, PMOS well	NWELL
diffusion area	DIFF
P+ implant, PMOS source/drain	PIMP
N+ implant, NMOS source/drain	NIMP
polysilicon gate	PO
metal 1	M1
metal 1 Pin, used as label layer	M1PIN

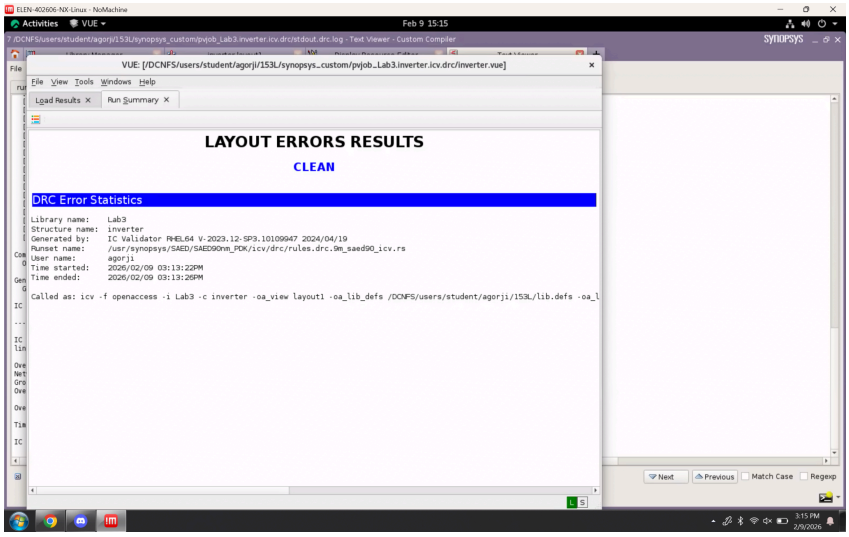
2. Mention the layer that provides PMOS & NMOS channel length and width dimensions. Looking at the 2D image of the layout, mention the axis that determines Length and Width of the transistors. (ex. X-axis : _____)
   Channel length is set by the polysilicon gate dimension over diffusion.
   Channel width is set by the diffusion dimension perpendicular to the gate.
   X-axis corresponds to transistor width
   Y-axis corresponds to transistor length.

Part 2: DRC and LVS

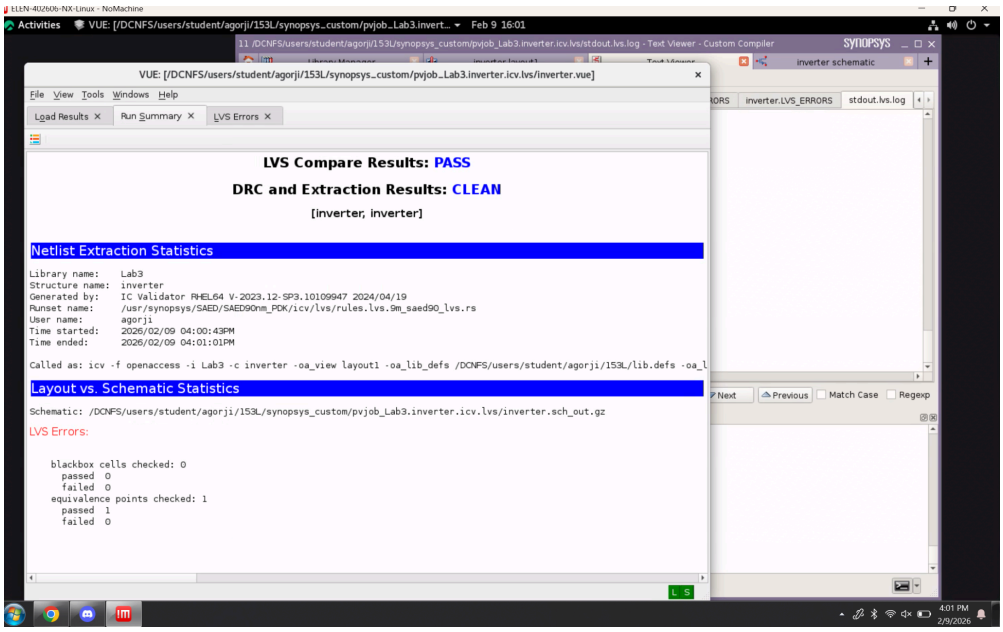
To verify that the layout is correct, a Design Rules Check (DRC) must be performed to verify that the layout complies with design rules for this 90nm process. Furthermore, a Layout vs. Schematic (LVS) check must be performed to verify that layout you created actually matches the schematic of the desired inverter.

- Follow the Layout Verification section in your tutorial, pages 21-28 to perform DRC and LVS. Adjust your layout if necessary to fix any errors. The tutorial includes a troubleshooting guide. Make sure to attach screenshots showing your design passed DRC and LVS.

DRS successful



LVS successful



Conclusion

This lab was very fun in the way that I was able to design my own CMOS inverter. Placing every piece of the system definitely made me understand why we need each one. Because when one piece had an error, I learned exactly what the outcome was. For example, I accidentally added a short to my PMOS and when I removed it, everything started to work. I also was confused in the past about the purpose of wells and taps, but this cleared everything up for me the way we drew the sizes of each for the PMOS and NMOS sides.