ECEN 153L Lab 5 Report: Hierarchical Design: Two-Input XOR Gate

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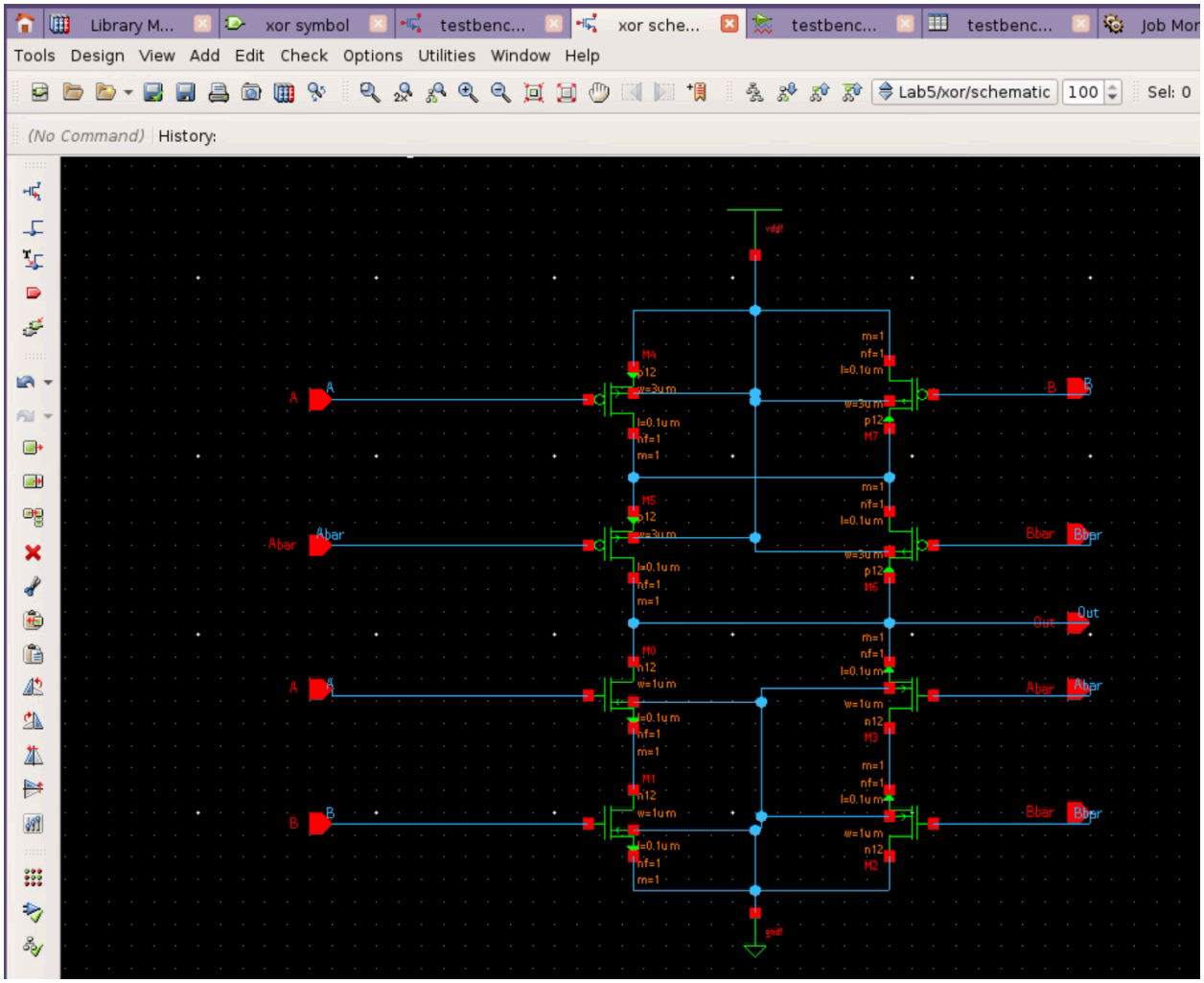
Part A: XOR Logic schematic and Symbol

Question: Explain the transistor sizing of above XOR in your lab report?

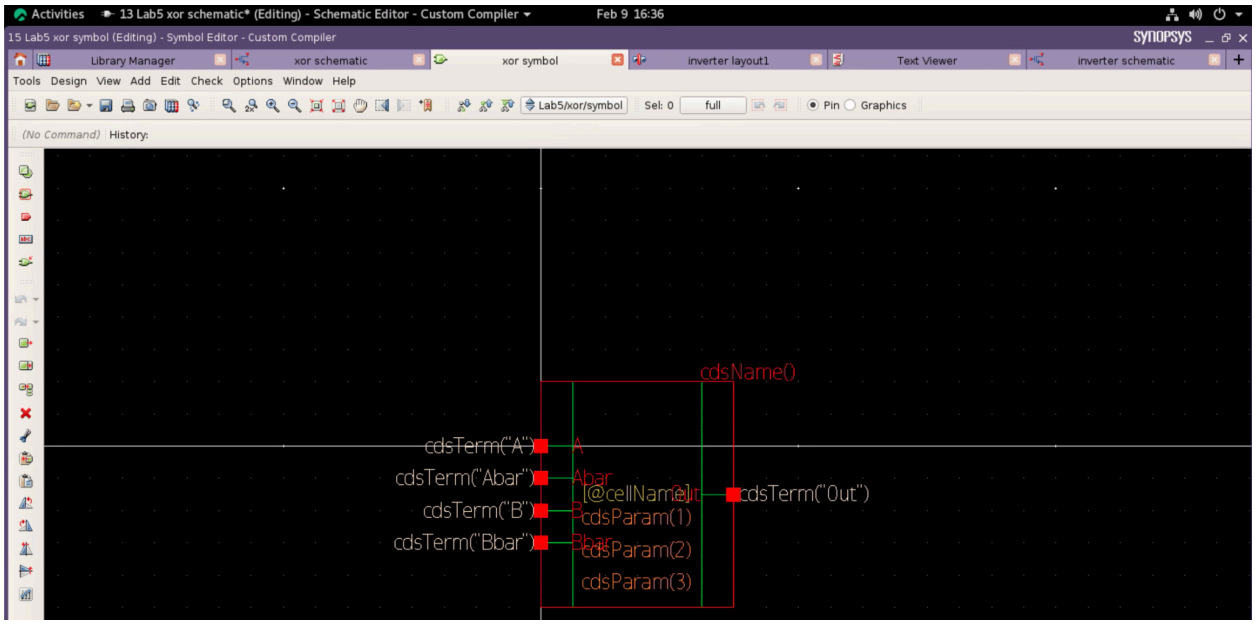
The PMOS was sized to have a W/L that is 3 times greater than the W/L of the NMOS. This is due to the fact that PMOS has more holes. NMOS having electrons are more efficient and faster. The PMOS has more resistance per hole versus the electrons. So we size the PMOS 3 times larger to counteract this and make the resistance equal.

XOR schematic



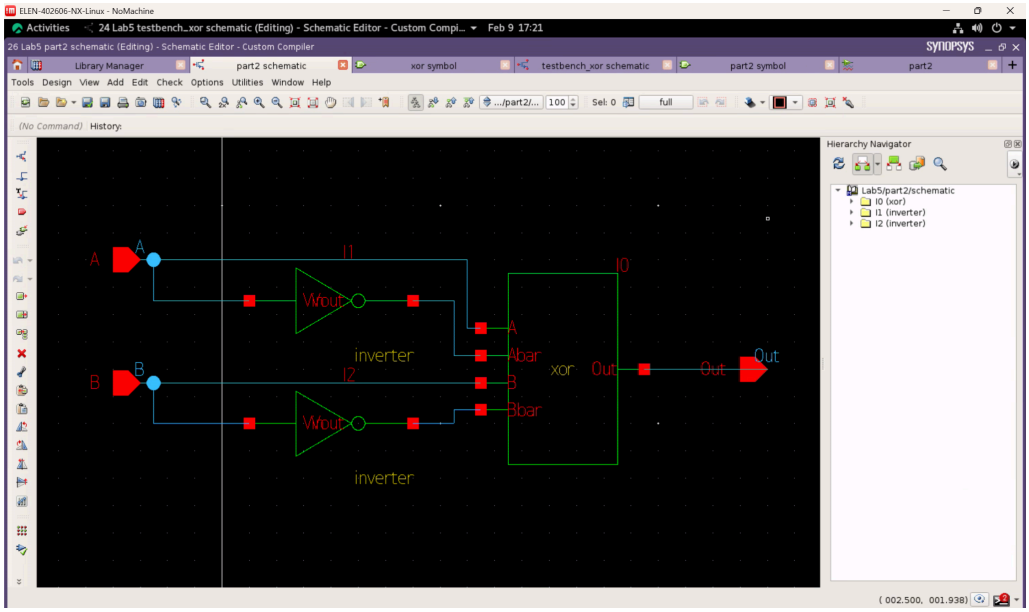
A	B	Out
0	0	0 (gnd)
0	1	1 (Vdd)
1	0	1 (Vdd)
1	1	0 (gnd)

XOR symbol

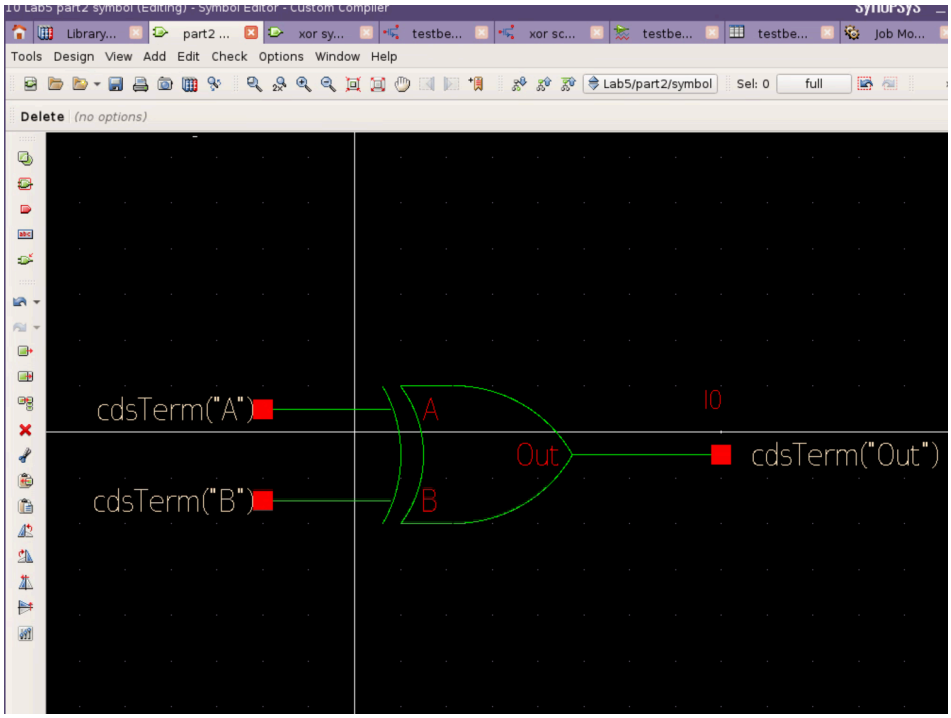


Part B: Four Inputs to Two Inputs using Inverters (Hierarchy)

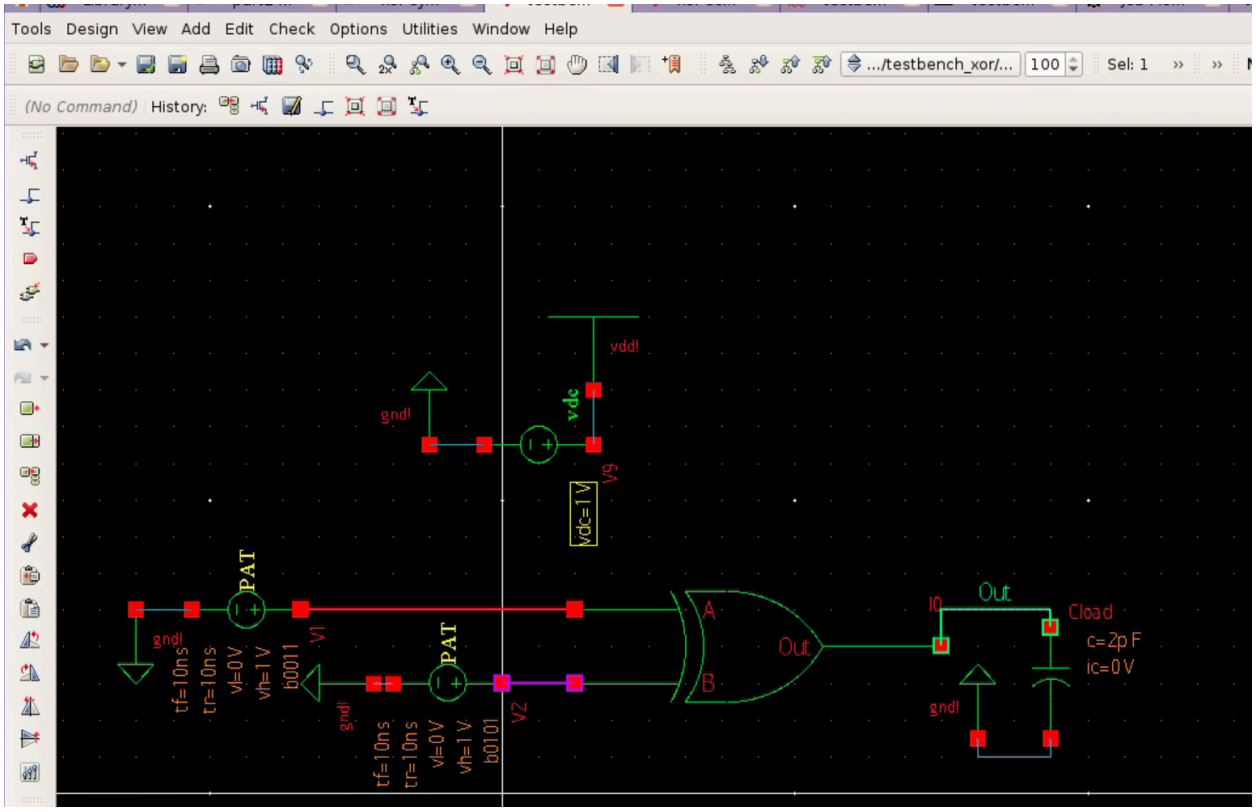
Part 2 schematic

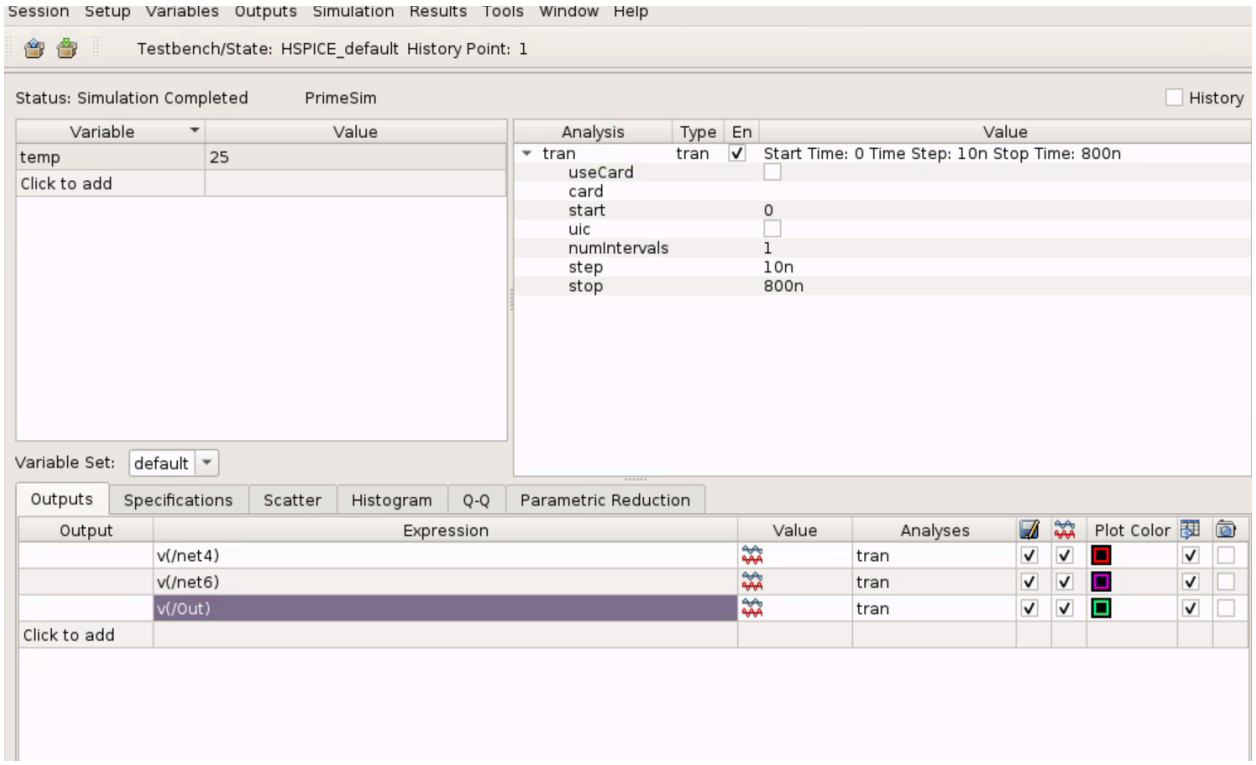


XOR symbol when I put it together

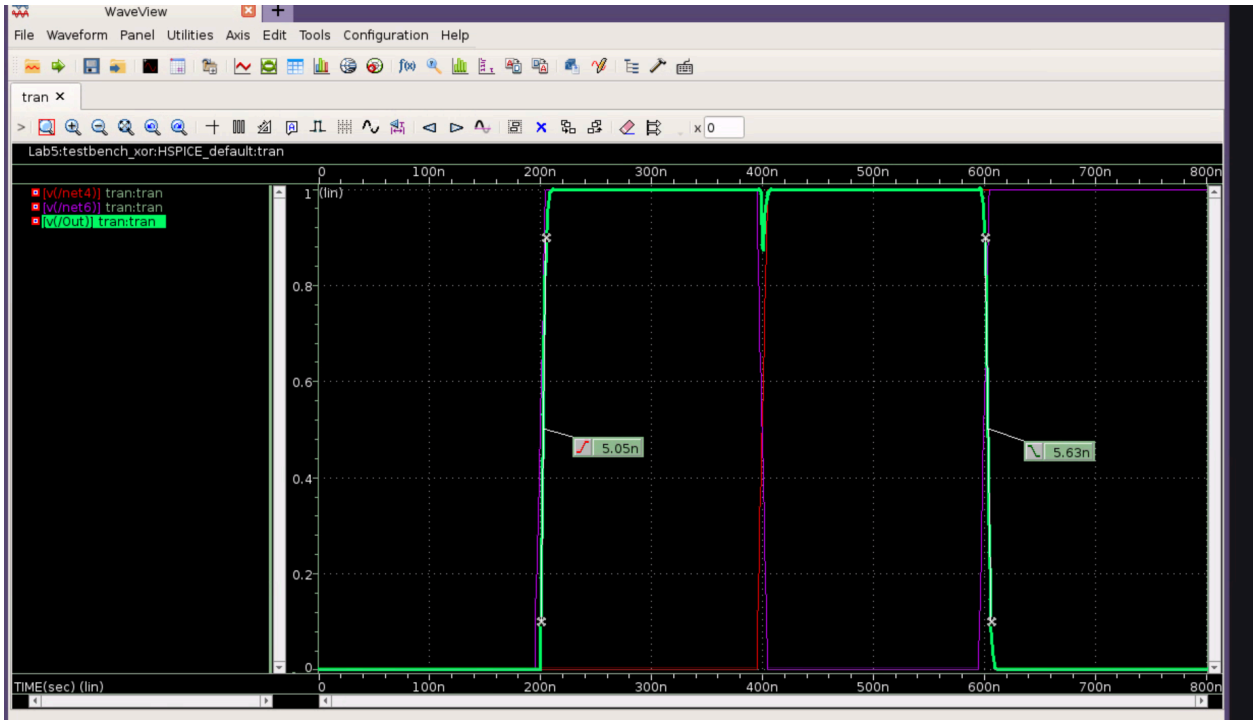


Part C: Transient Simulation





Question: Measure the Rise and Fall time of the output and include the picture with the visible measurements.



Conclusion

It was pretty interesting and a good learning experience creating the XOR gate in HSPICE. I also went even deeper into HSPICE learning the way that I ran into a major bug. I found out that you need to have a separate circuit with a Vdc connected to a Vdd. But it all came together when we graphed the XOR gate and saw how it matched with our logic design.