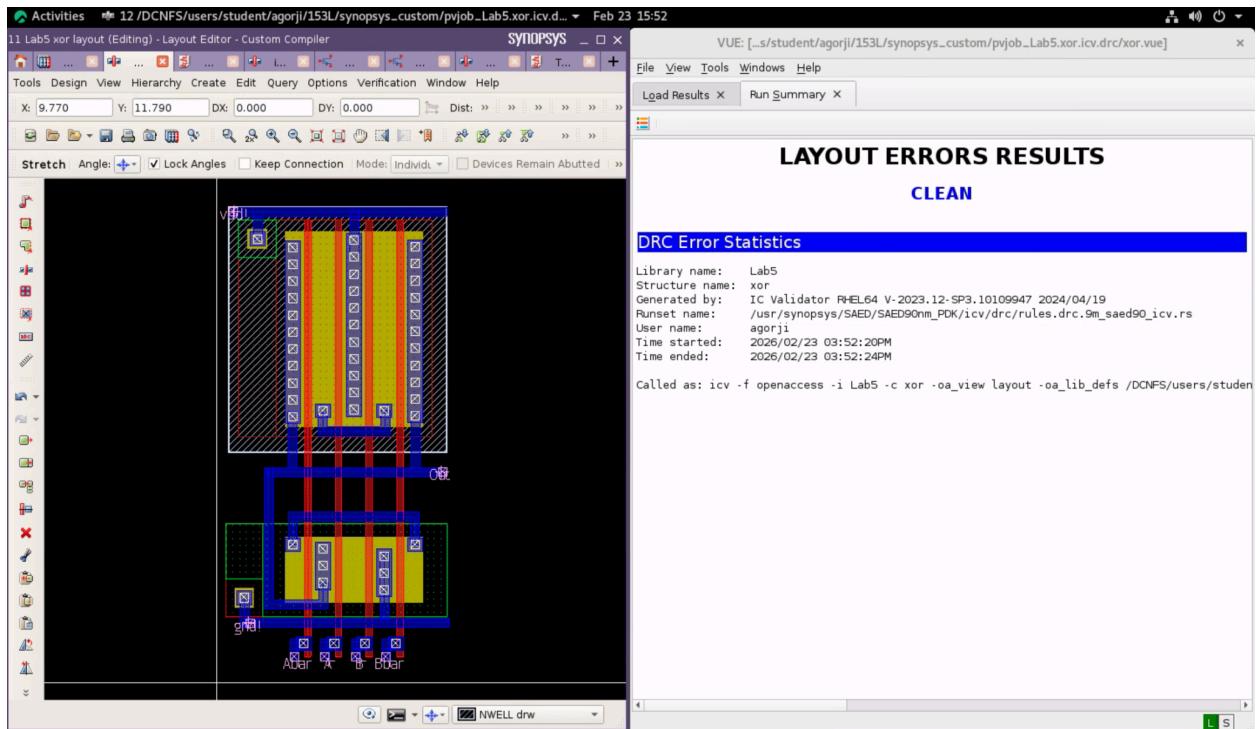


ECEN 153L Lab 6 Report: Hierarchy Layout of an XOR gate

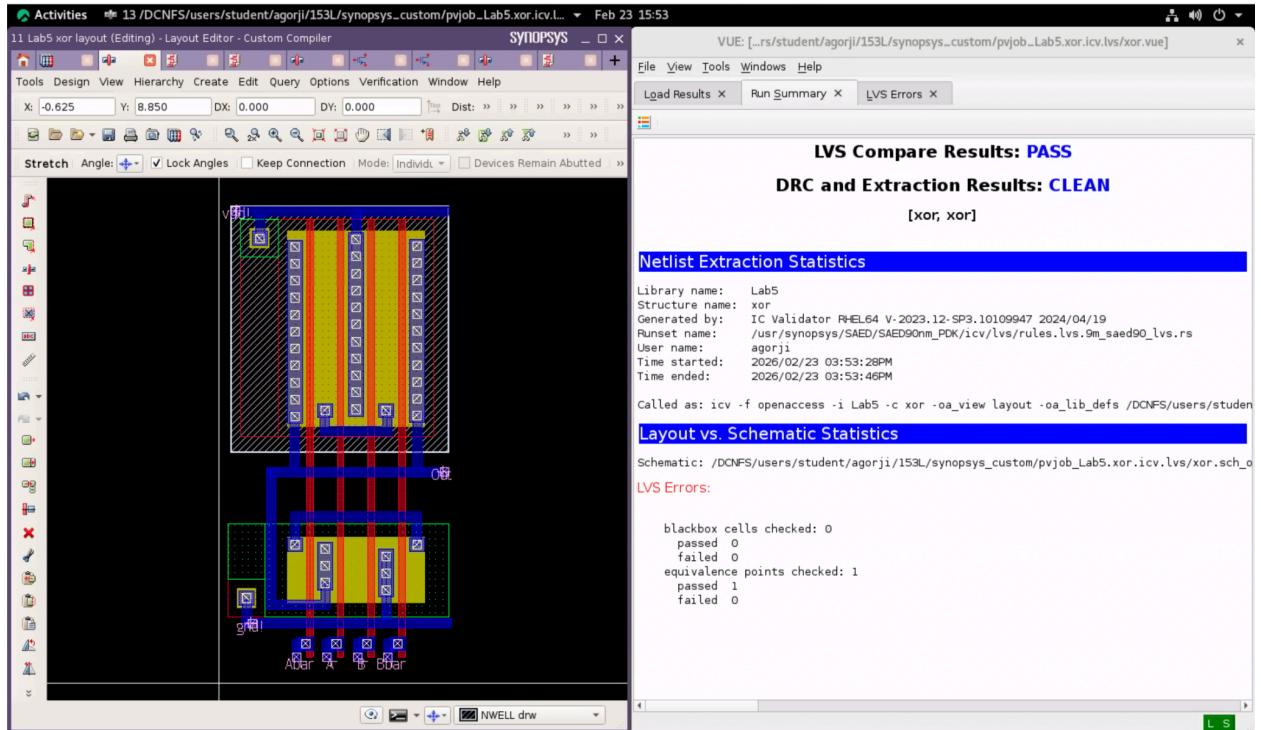
Aveed Gorji 2/20/26

Part 1

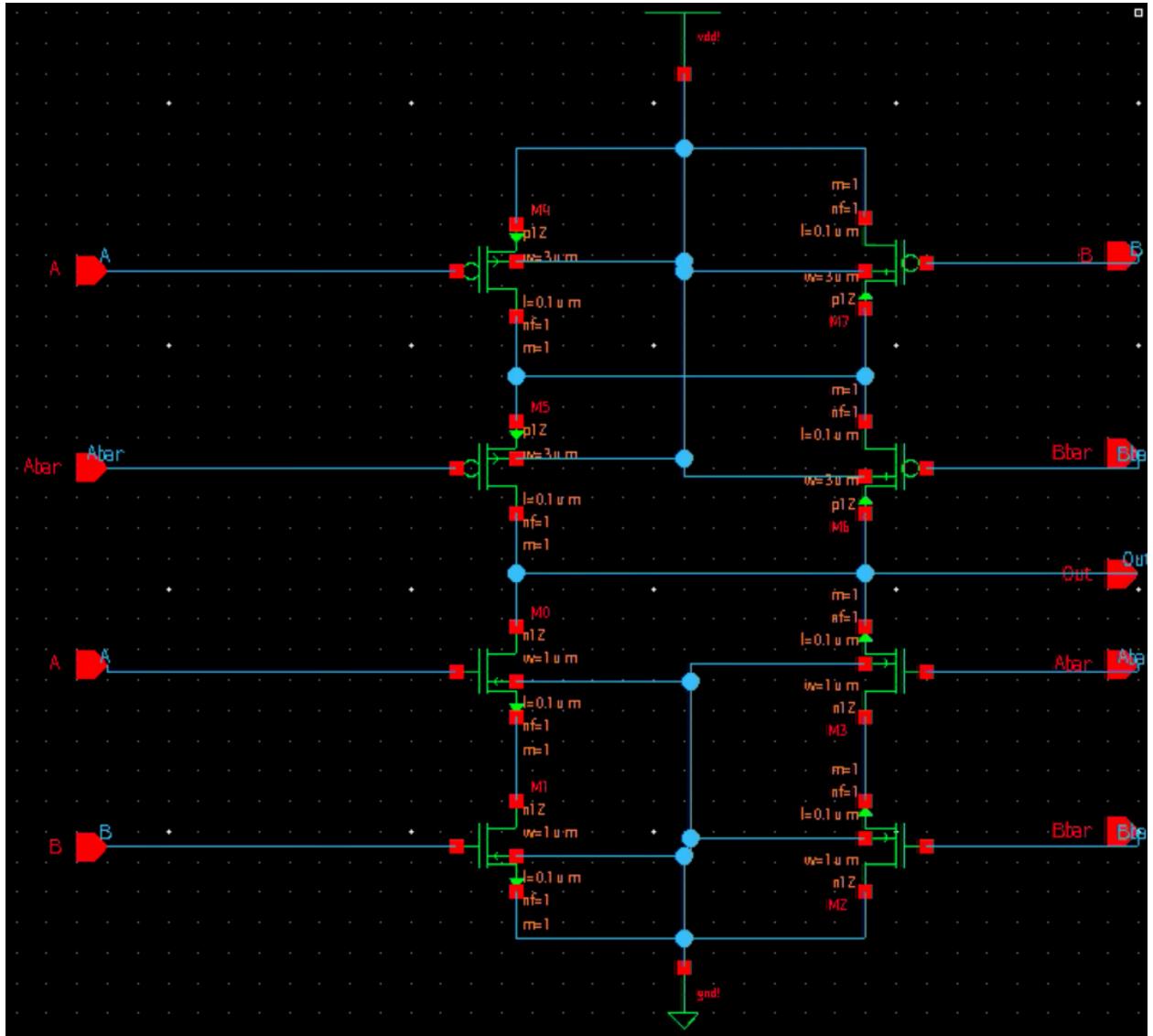
Layout of XOR gate DRC Pass



Layout of XOR gate LVS pass

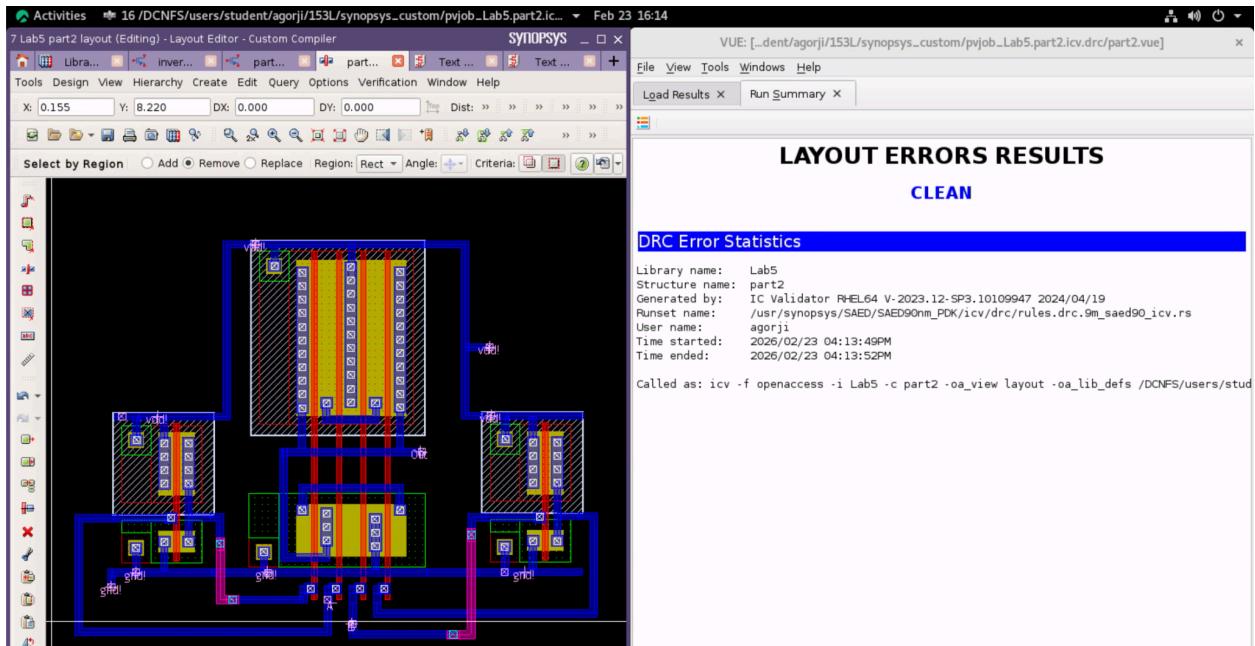


Schematic I used for the XOR gate

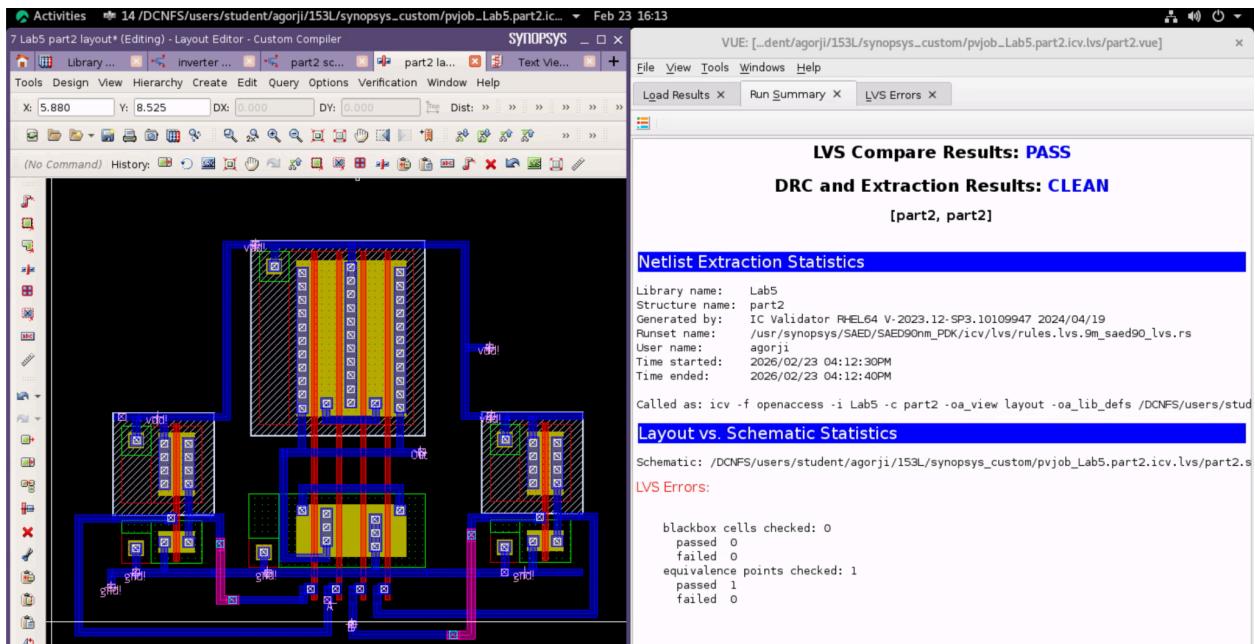


Part 2

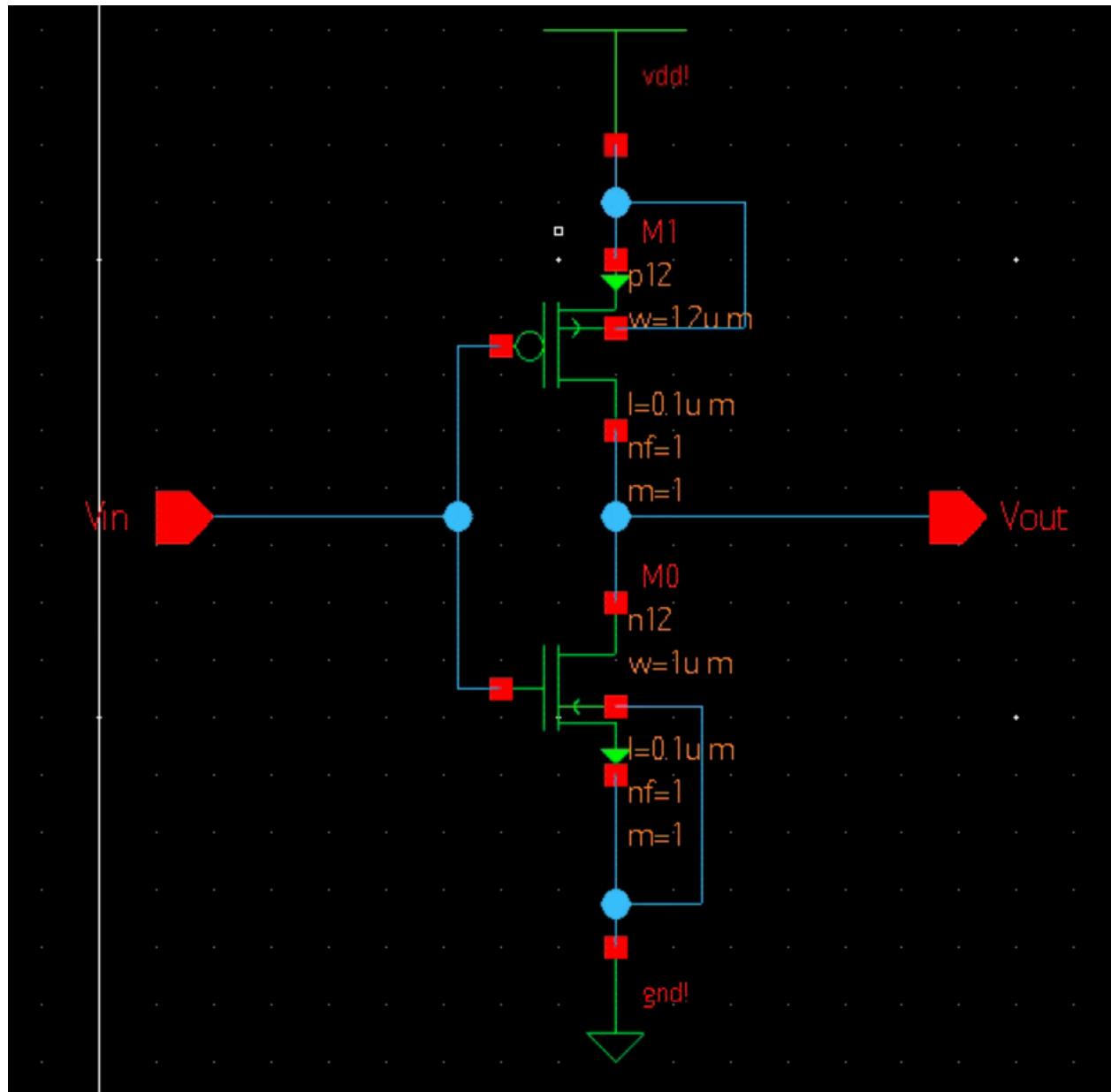
XNOR logic with inverter DRC pass



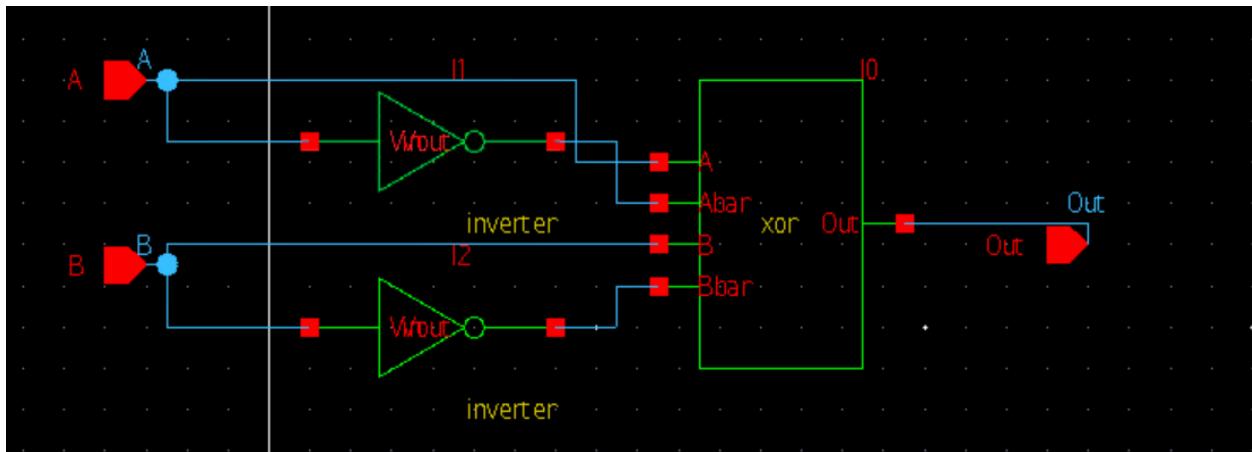
XNOR logic with inverter DRC pass



Schematic I used for the inverter



Schematic I used for the XOR and two inverters



Conclusion

In this lab, I finally felt like I put everything we have learned all together. I was able to understand all the error codes and make the necessary corrections. One problem I ran into was having to add global vdd! and gnd! M1Pin labels, but once I added those some errors went away. Another error I had was that the PMOS width on my original inverter was 3 um while my layout was drawn to 1.2 um. But overall I feel so much more confident in my abilities to navigate HSPICE in terms of troubleshooting and CADing based on design rules.