Signal Name		R-format	I-format(not lw)	LW	SW	beq
Inputs	I6	0	0	0	0	1
	I5	1	0	0	1	1
	I4	1	1	0	0	0
	I3	0	0	0	0	0
	I2	0	0	0	0	0
	I1	1	1	1	1	1
	I0	1	1	1	1	1
Outputs	Memtoreg	0	0	1	X	X
	Regwrite	1	1	1	0	0
	Memread	0	0	1	0	0
	Memwrite	0	0	0	1	0
	branch	0	0	0	0	1