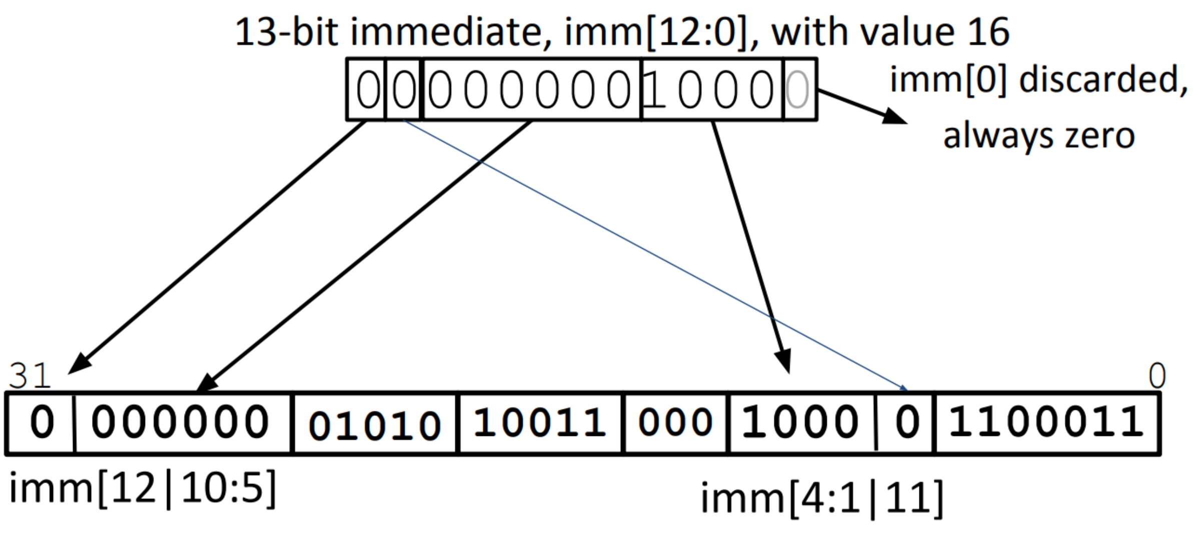
REPORT

Part 4 : Single Cyle Processor

Observations and problems faced:

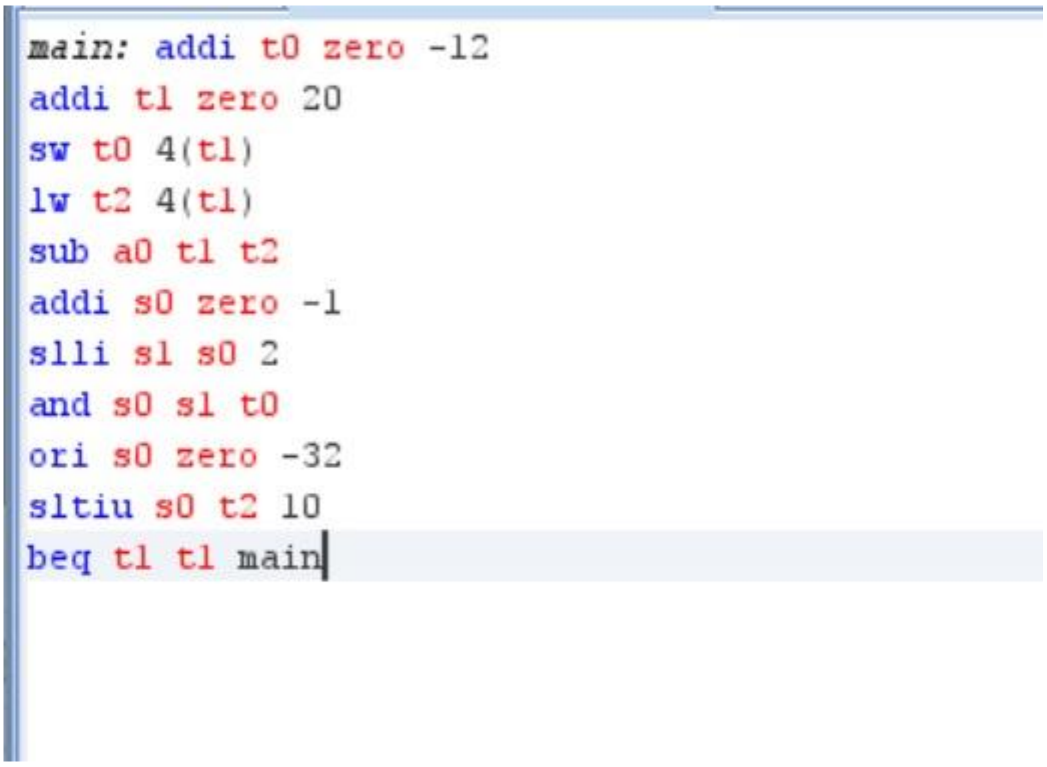
- The Logisim evolution memory has an option to select quad input lines for memory address so we can access 32 bits together when the bit width of the memory is 8 bits. This option is not available in normal Logisim in which 32 bits cannot be accessed simultaneously if the bit width is 8 so previously working in normal Logisim we used 32 bit width memory to access one instruction at once and used pc=pc+1 instead of 4 and used right shift by 2 to handle adding immediates of the branch instruction to the current program counter
- The Logisim evolution memory gives error if addresses are not accessed in multiples of 4. What we mean by this is that is we are currently using 8 bit width memory to store data and quad line mode to access 32 bits in case of load word at once in this case storing operation can only happen at multiples of 4 (0,4,8…). If tried to store something at a memory location lets say 10 which is not a multiple of 4 Logisim gives error which was not the case in normal Logisim
- The maximum size address line of the memory is 24 bits so we had to bit reduce the memory to 24 from 32 wherever addresses were involved.
- We have followed little-endian format in both memory instruction as well as data memory
- The immediate is stored differently in different instruction formats for
    - I type uses the function7 and rs2 field to get a 12 bit immediate
    - S type instruction use function7 and rd field to get a 12 bit immediate
    - SB (branch) type uses immediate like the S type (by using function7 and rd) but it manipulates the immediate to make a 13 bit immediate. It uses the fact that the memory addressing in RISCV uses byte addressing so the first bit(lsb) is always 0 as the addresses would be in multiple of 4 so it drops it and uses it as the 11th bit of the immediate



immediate in case of branch instruction

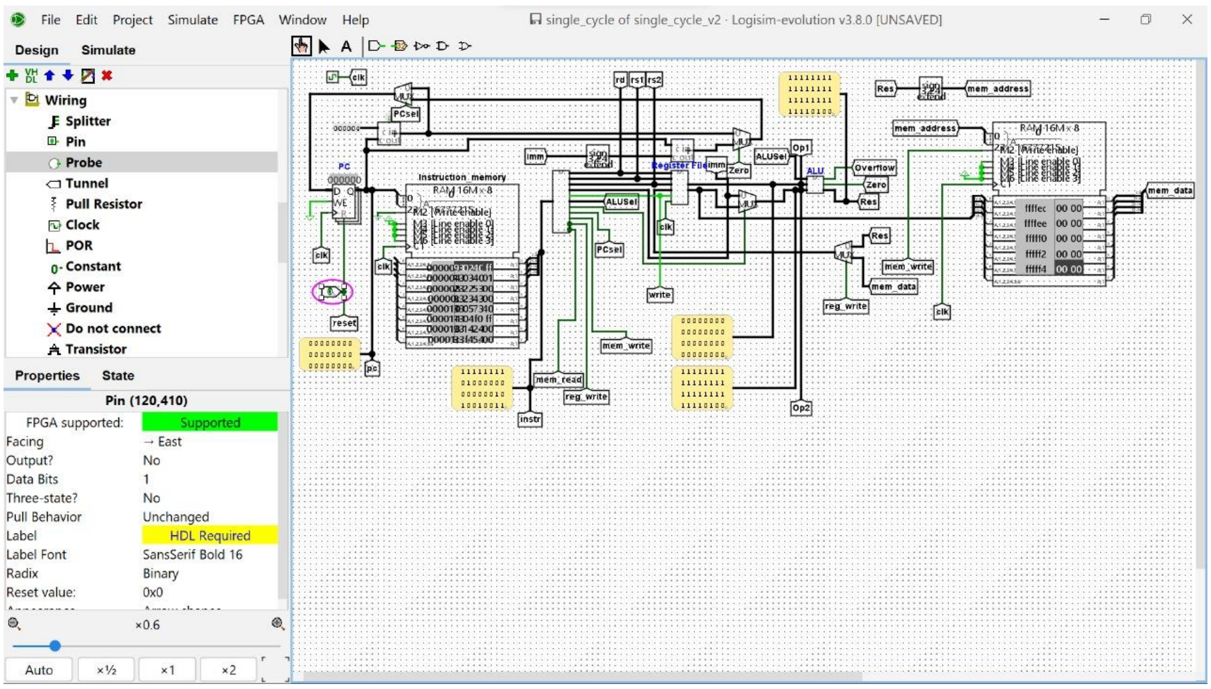
Clips of working programs

Example :



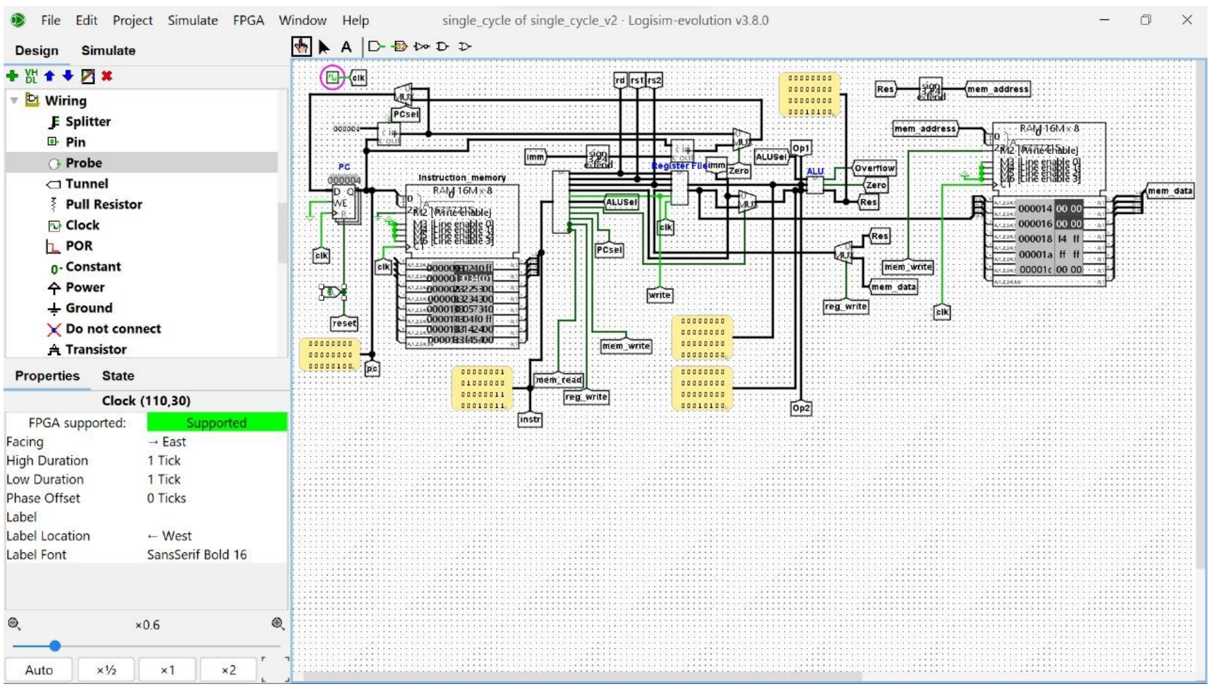
```
main: addi t0 zero -12
addi t1 zero 20
sw t0 4(t1)
lw t2 4(t1)
sub a0 t1 t2
addi s0 zero -1
slli s1 s0 2
and s0 s1 t0
ori s0 zero -32
sltiu s0 t2 10
beq t1 t1 main
```

Instruction for example 1



Pin (120,410)

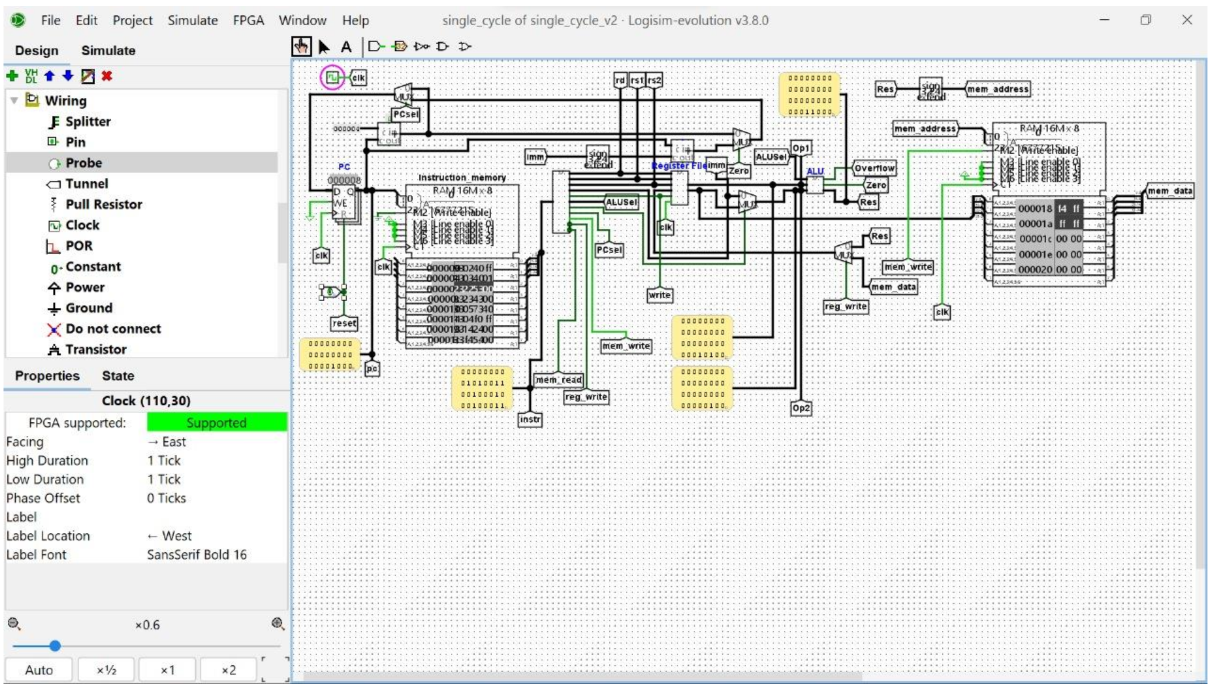
FPGA supported:	Supported
Facing	→ East
Output?	No
Data Bits	1
Three-state?	No
Pull Behavior	Unchanged
Label	HDL Required
Label Font	SansSerif Bold 16
Radix	Binary
Reset value:	0x0



single_cycle of single_cycle_v2 · Logisim-evolution v3.8.0

Clock (110,30)

FPGA supported:	Supported
Facing	→ East
High Duration	1 Tick
Low Duration	1 Tick
Phase Offset	0 Ticks
Label	
Label Location	← West
Label Font	SansSerif Bold 16



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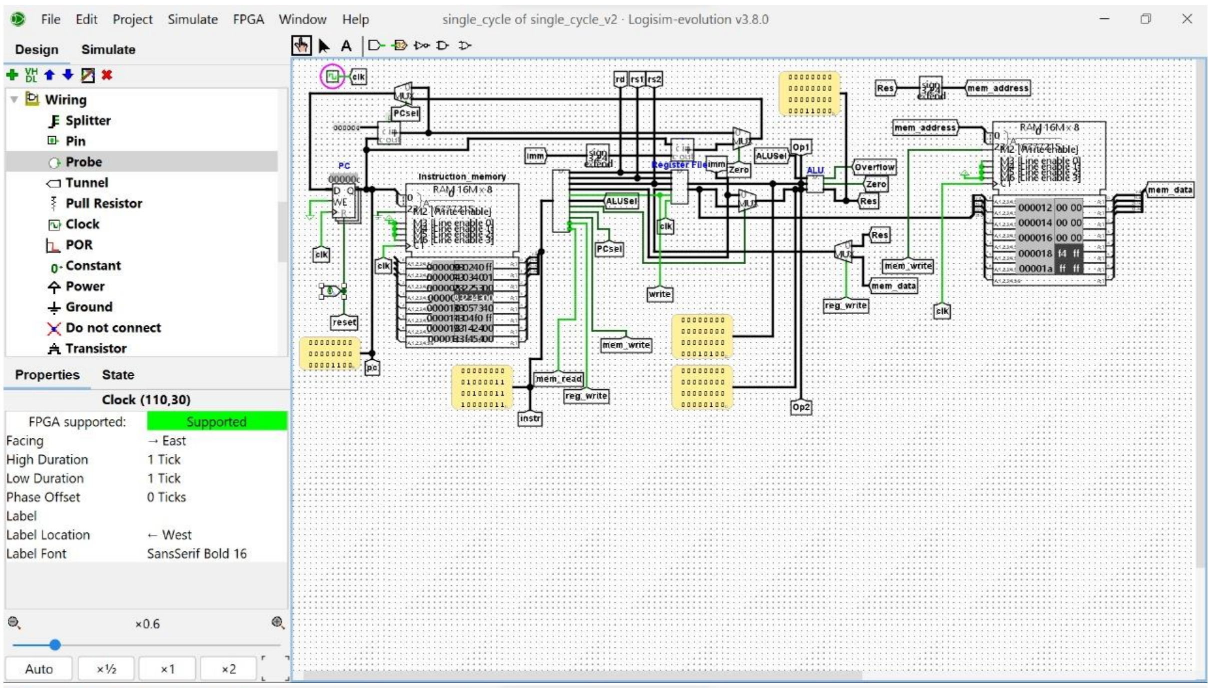

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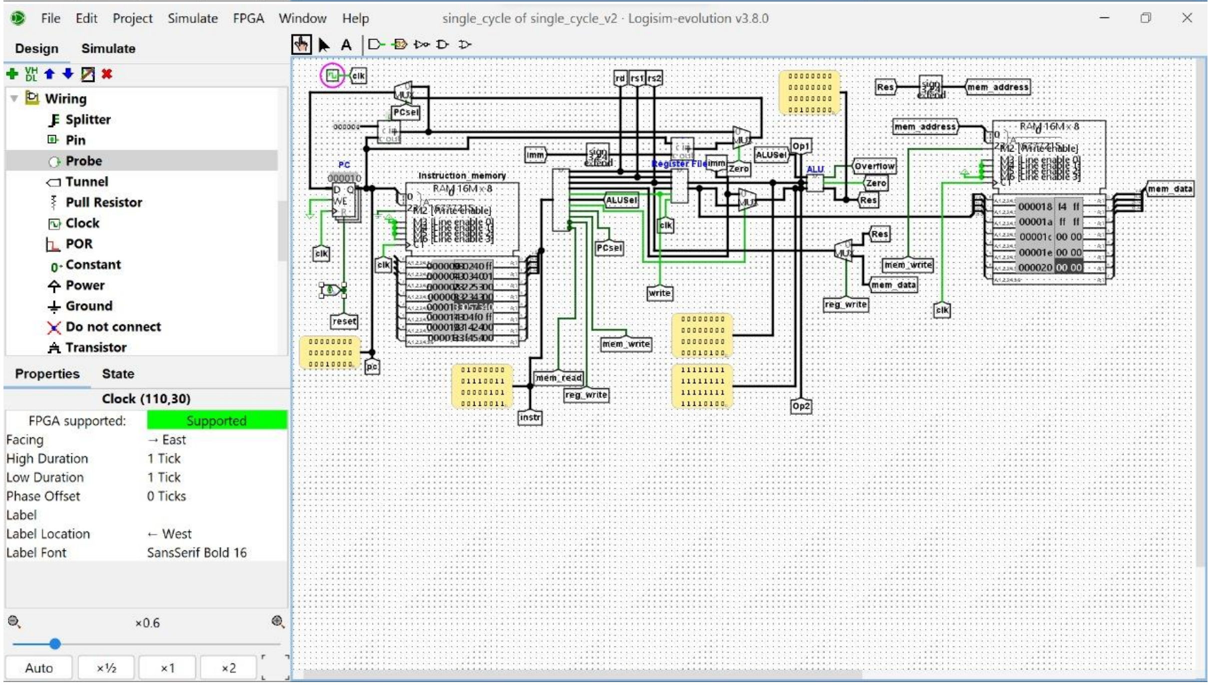

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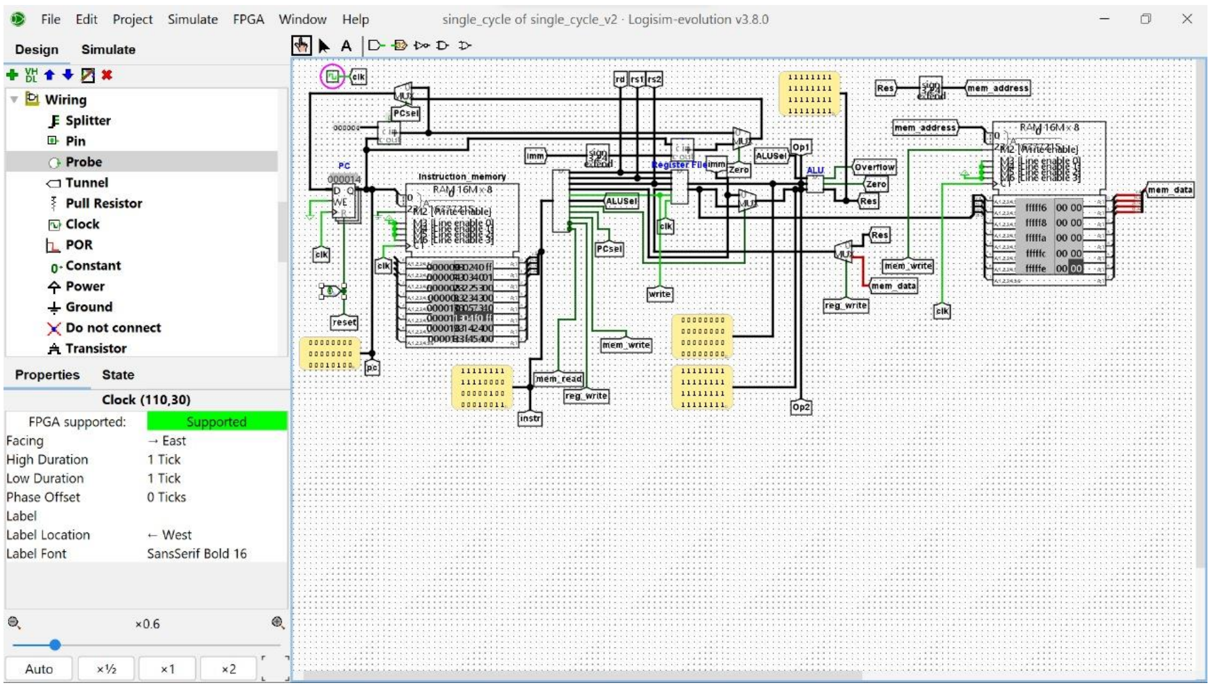

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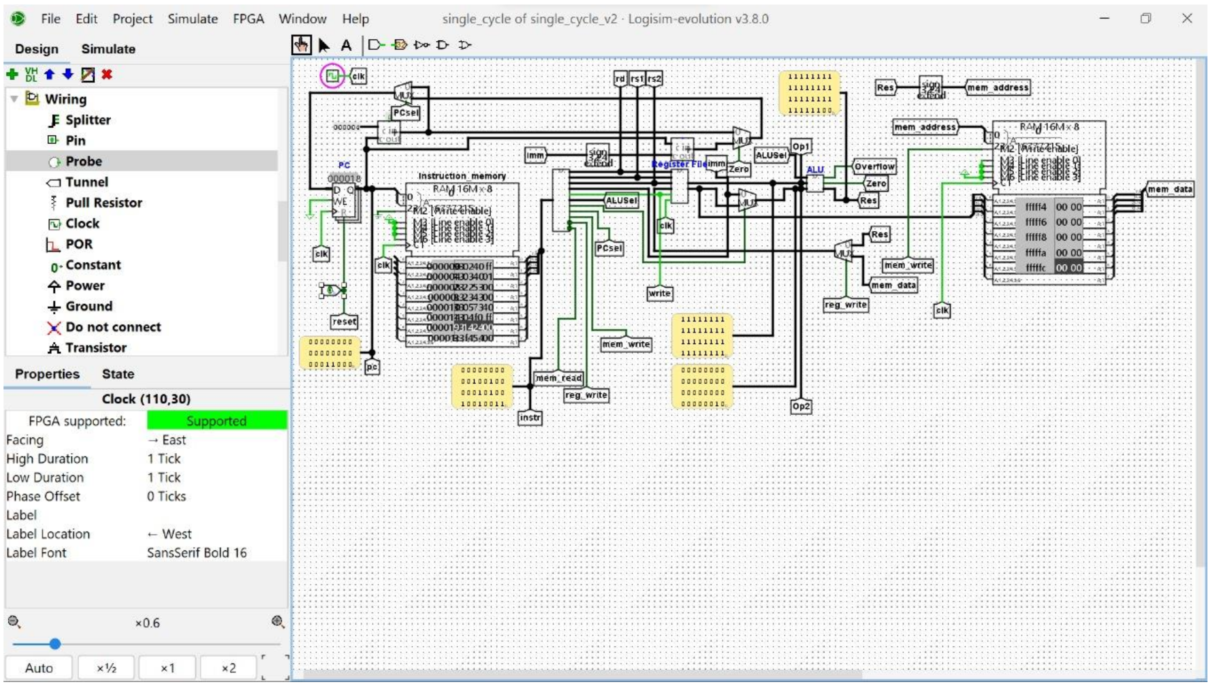

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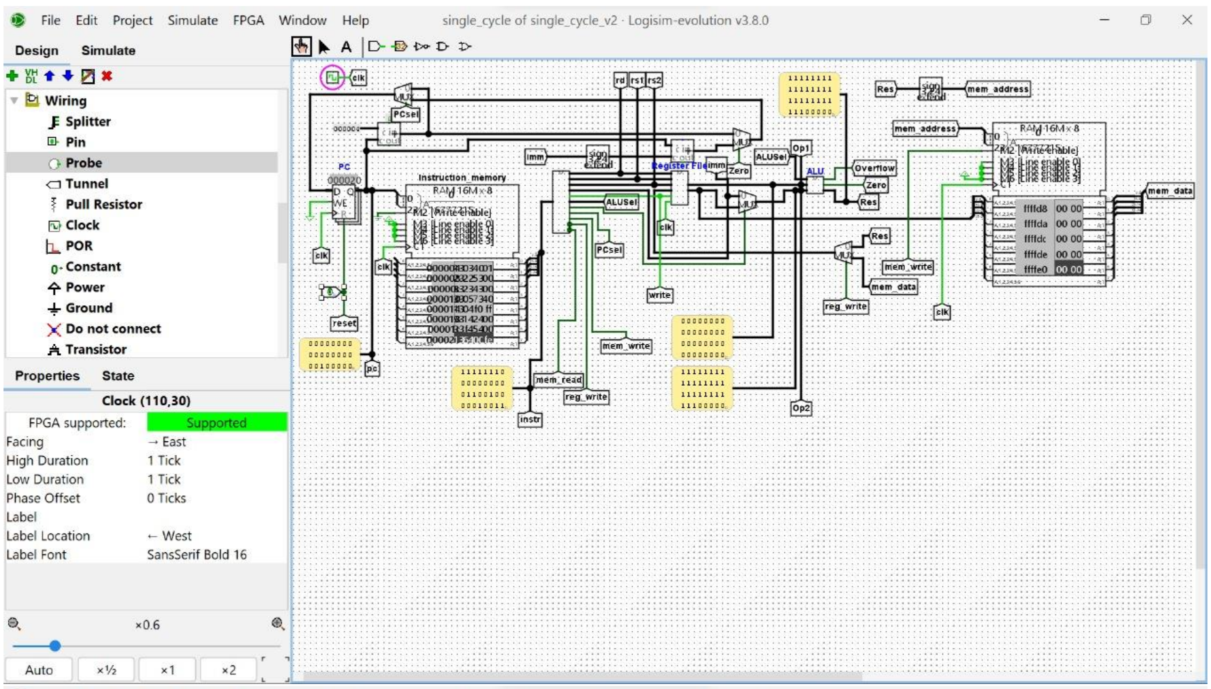

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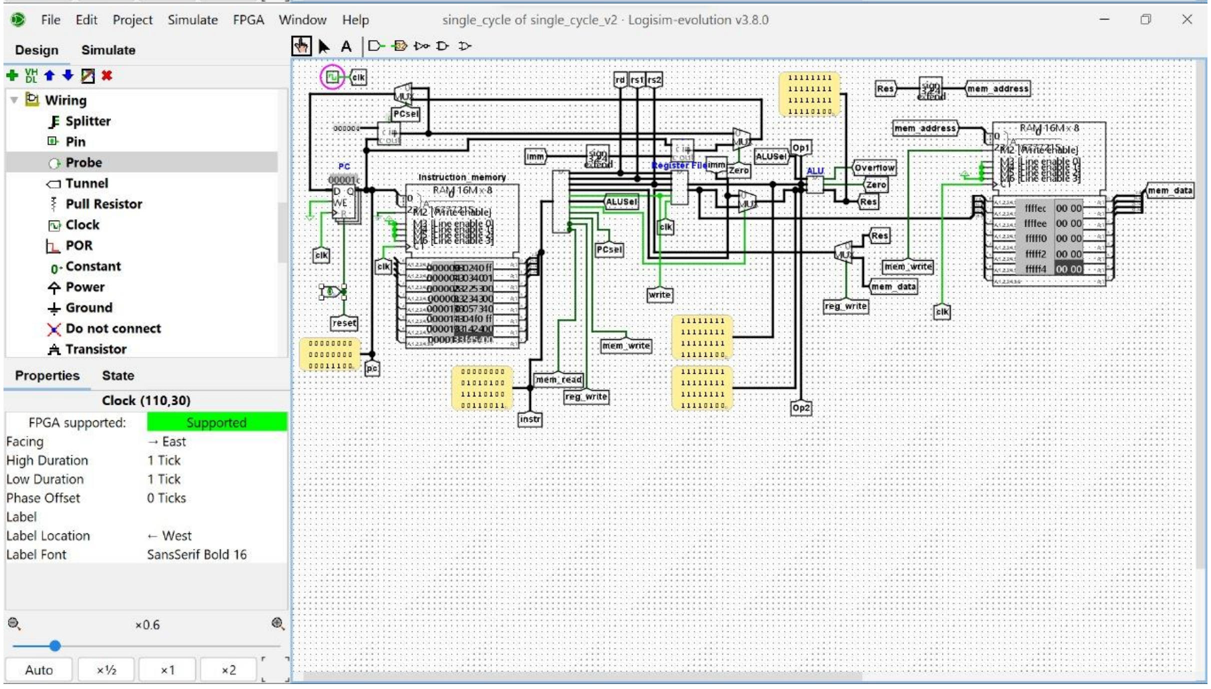

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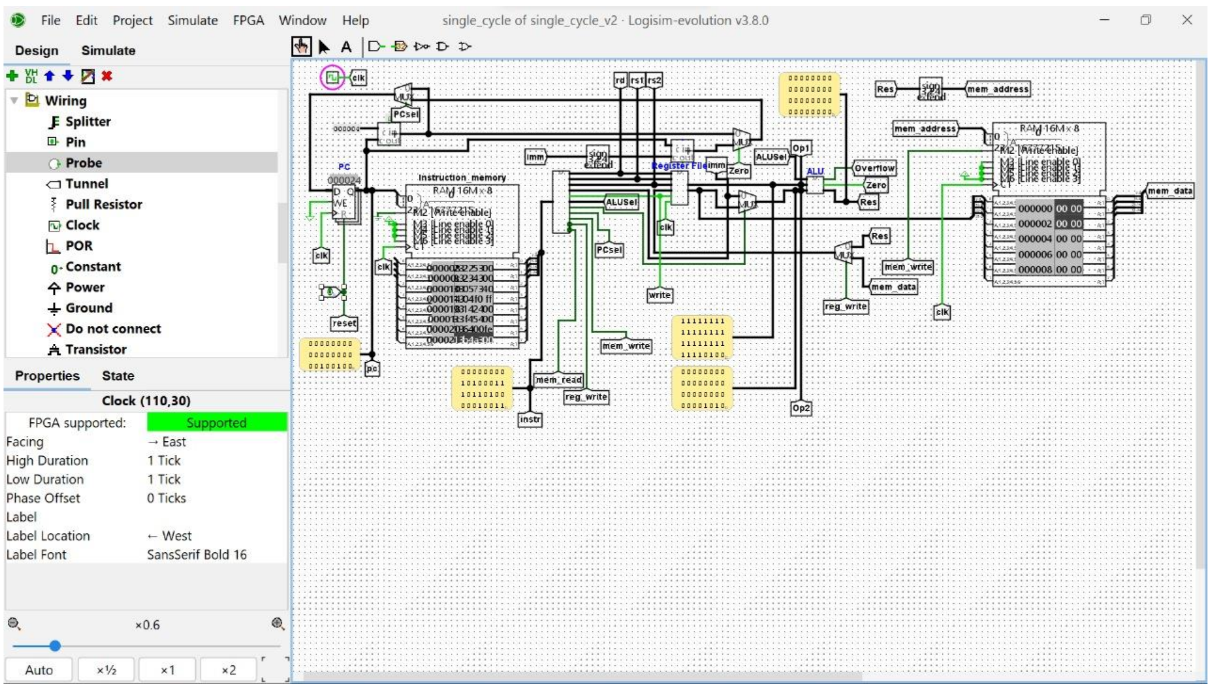

Properties State

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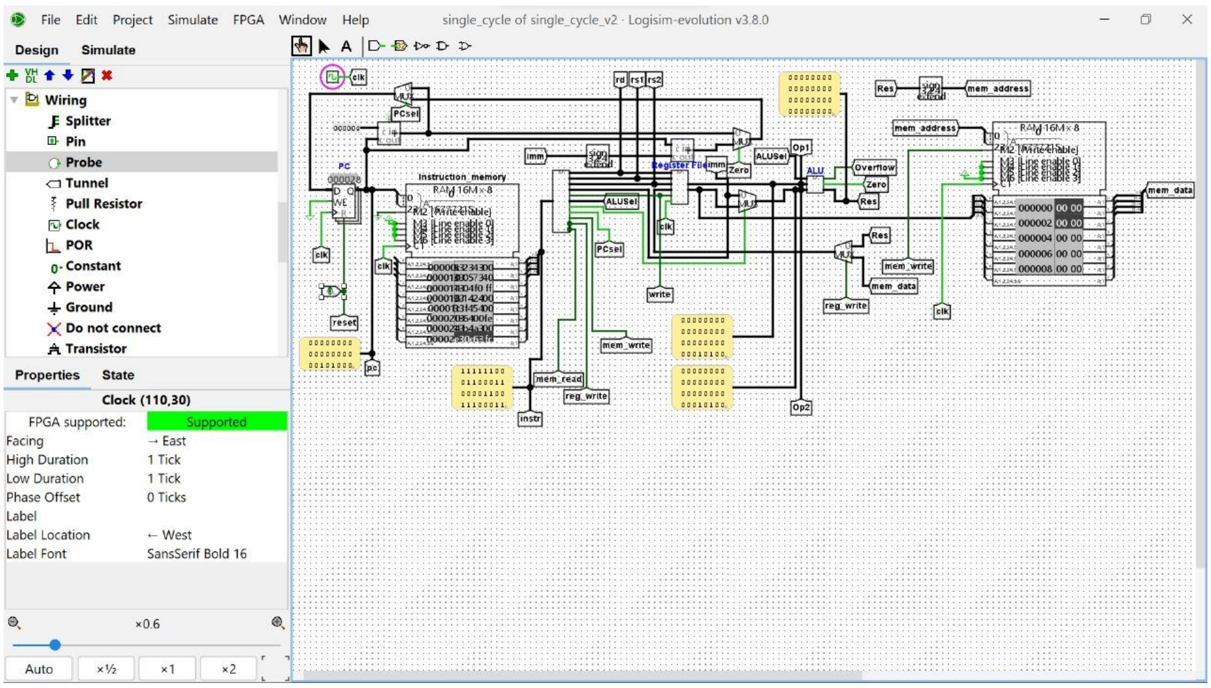

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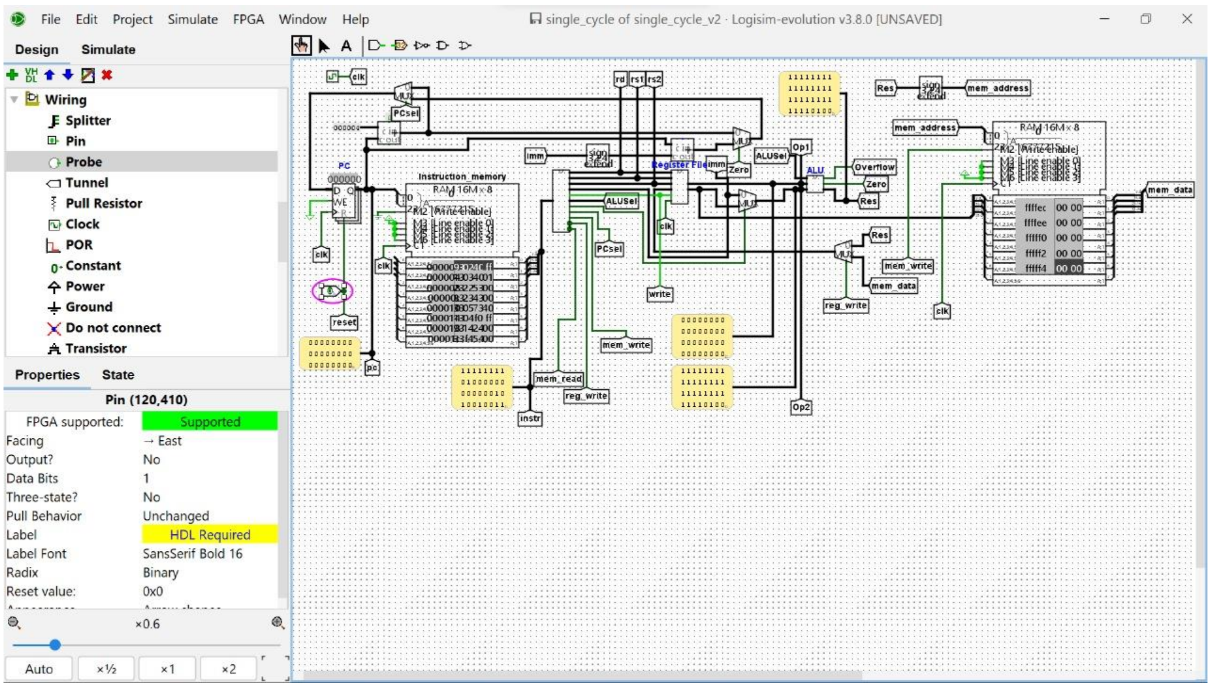

single_cycle of single_cycle_v2 - Logisim-evolution v3.8.0 [UNSAVED]

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