Stephen Alexander Marquis

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EDUCATION

Case Western Reserve University, Cleveland, Ohio **GPA – 3.853 / 4.000**
B.S.E. in Computer Engineering Graduated May 2018

RELEVANT COURSEWORK

Computer Architectures; Computer System Architectures; Very-Large-Scale Integration (VLSI); Computer Design; VLSI/Computer-Aided Design (CAD); Digital Systems Design; Digital Logic Laboratory; Logic Design and Computer Organization; Discrete Mathematics; Statistics for Signal Processing; Signals and Systems; Embedded Systems Laboratory; Data Structures; Circuits 1&2; Semiconductor devices

TECHNICAL KNOWLEDGE

- Static Timing Analysis, Register Transfer Level (RTL) Design, Pipelined Computer Architectures, Digital Logic Design, Object-Oriented Programming, Data Structures

SOFTWARE SKILLS

- Synopsis: Design Compiler, IC Compiler I, IC Compiler II. Mentor Graphics: IC Station, Leonardo, ModelSim. Xilinx ISE, Altera Quartus II
- Verilog, VHDL, Perl, TCL, Python, C, Assembly, Java, Apache Ant, XML, MXML

WORK EXPERIENCE

Cavium Inc., Marlborough, MA Summer 2017
Implementation Intern, *Place and Route Team*

- Worked in 14nm and 28nm Place and Route (PnR) flows; running synthesis, placement, routing, and verification tools.
- Developed scripts to analyze chip power consumption, using tool reports generated during the PnR flow.
- Developed a tool in Python to help designers better understand how timing parameters change at different process corners and as the result of On Chip Variation (OCV), by using multivariate-interpolation and Spice simulation data.
- Updated the 28nm timing ECO flow to work with IC Compiler II in the new 14nm ECO flow.
- Developed TCL processes to place and route RC-delay dominated ring oscillators within IC Compiler II.
- Used IC Compiler to perform cell-level placement, to fix setup violations, and to fix hold violations.
- Worked with in-house tools to perform macro placement, and to analyze block-level progress.

iNet Public Safety, Phoenix, AZ Summers 2015, 2016
Software Engineer, *Development Team*

- Worked in an object-oriented programming environment implementing high-priority features and bug fixes.
- Utilized JIRA bug-tracking to report and resolve critical bugs/features.
- Redesigned the product's mobile GUI, in accordance to Google's Material Design, to provide a more familiar user experience.
- Developed Apache Ant scripts to automate the process of packaging and deploying the product to Android and IOS devices.
- Responded to customer issues/complaints in a fast-paced environment to provide seamless patches to critical errors.

HANDS-ON EXPERIENCE

Lead Programmer and Designer, *Independent and class projects* August 2014 – Present

RISC Processor, *Verilog, ModelSim*

- Wrote a non-pipelined, 32-bit RISC processor that featured a program status register.
- Includes Load, Store, Branch, Xor, Add, Subtract, Rotate, Shift, and Complement.
- Simulated using a test bench in ModelSim, and successfully wrote and executed two programs in machine code.

4-Bit Register Layout, *Design Architect IC, IC Station*

- Created a schematic of a register cell and confirmed proper operation through simulation.
- Created a hierarchical schematic of a 4-bit register, and performed placement and routing using a mixture of automatic tools and manual layout. Passed all Design Rule Checks (DRC) and confirmed proper operation through Layout-versus-Schematic (LVS).

FreeCell Controller, *Verilog, ModelSim*

- Designed a FreeCell controller in Verilog to control the rules and user input for a FreeCell game.
- Successfully executed game 8321, starting from an initial game-state.

Verilog Simulator, *C*

- Wrote a simplified Verilog simulator in C. Successfully simulated a 20,000-gate file.

Motor Speed-Controller, *Altera DE1-SoC, Verilog*

- Created a speed controller with closed-loop feedback in Verilog to drive a motor at a constant speed, even under load.
- The project was uploaded onto an Altera DE1-SoC FPGA, and included an output display of the current motor rpm.

Other Projects, *Verilog, VHDL, ModelSim*

- Traffic light controller, cache controller, Handshake checker.

LEADERSHIP

Phi Kappa Theta Fraternity, Case Western Reserve University January 2014 – Present
Vice President of Fraternity, *Executive Council*
House Improvement, Public Relations, Historian, *Committee Chairs*