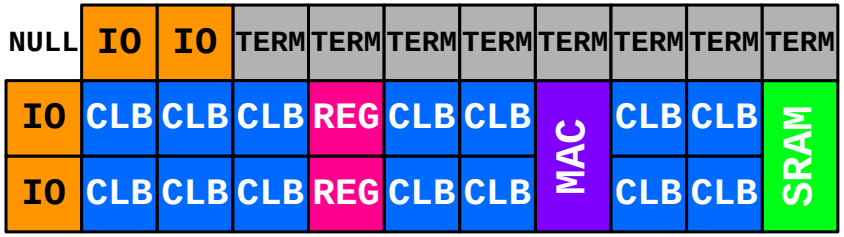
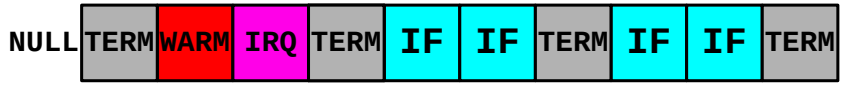
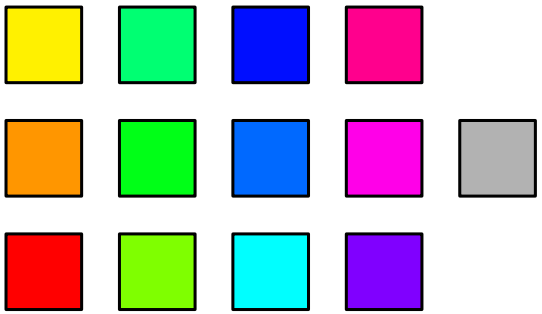
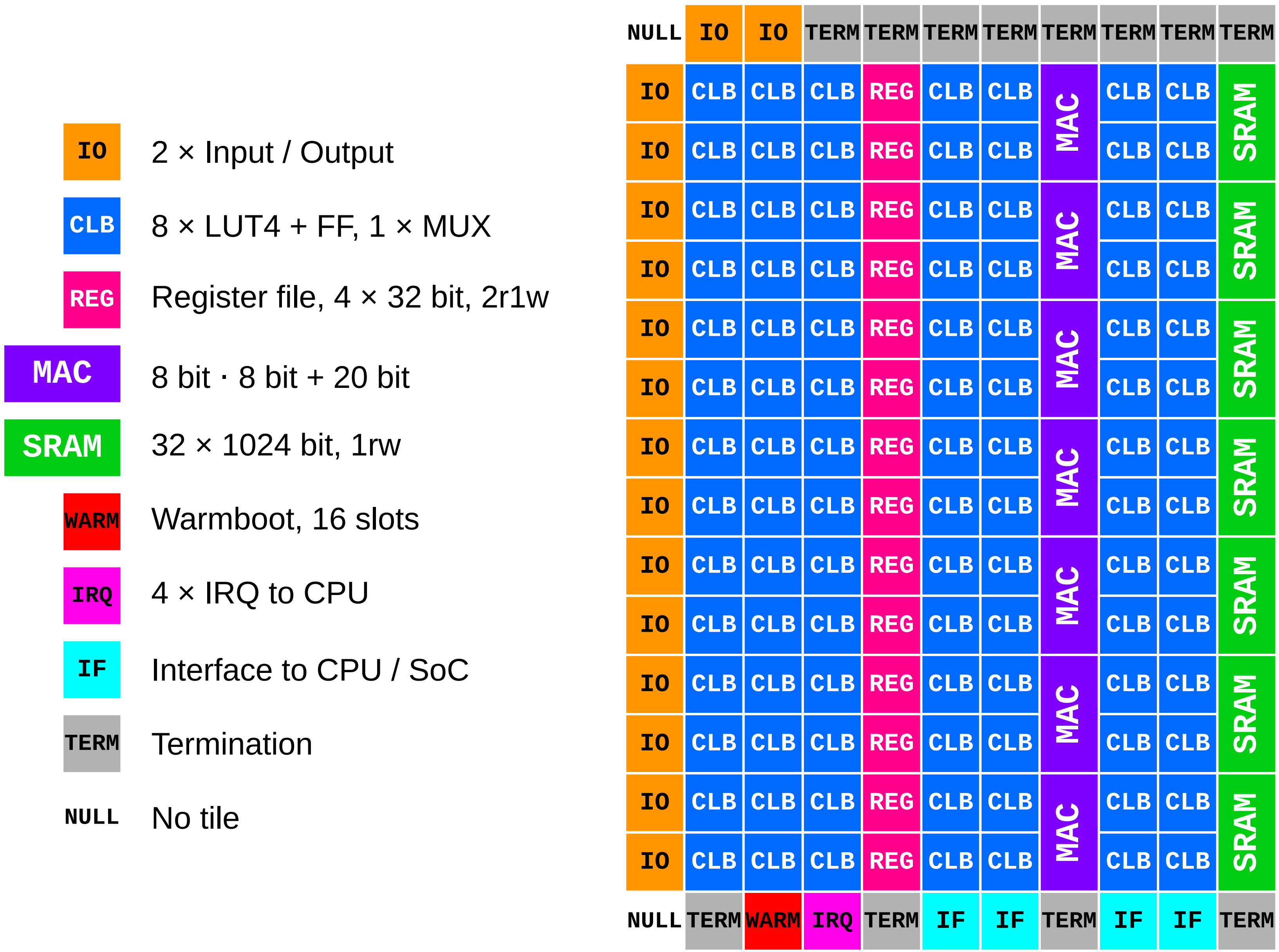

NULL IO IO TERM TERM TERM TERM TERM TERM TERM TERM
IO CLB CLB CLB REG CLB CLB MAC CLB CLB SRAM
IO CLB CLB CLB REG CLB CLB CLB CLB


NULL TERM WARM IRQ TERM IF IF TERM IF IF TERM




REG
REG


IO 2 × Input / Output
CLB 8 × LUT4 + FF, 1 × MUX
REG Register file, 4 × 32 bit, 2r1w
MAC 8 bit · 8 bit + 20 bit
SRAM 32 × 1024 bit, 1rw
WARM Warmboot, 16 slots
IRQ 4 × IRQ to CPU
IF Interface to CPU / SoC
TERM Termination
NULL No tile
NULL IO IO TERM TERM TERM TERM TERM TERM TERM TERM
IO CLB CLB CLB REG CLB CLB MAC CLB CLB SRAM
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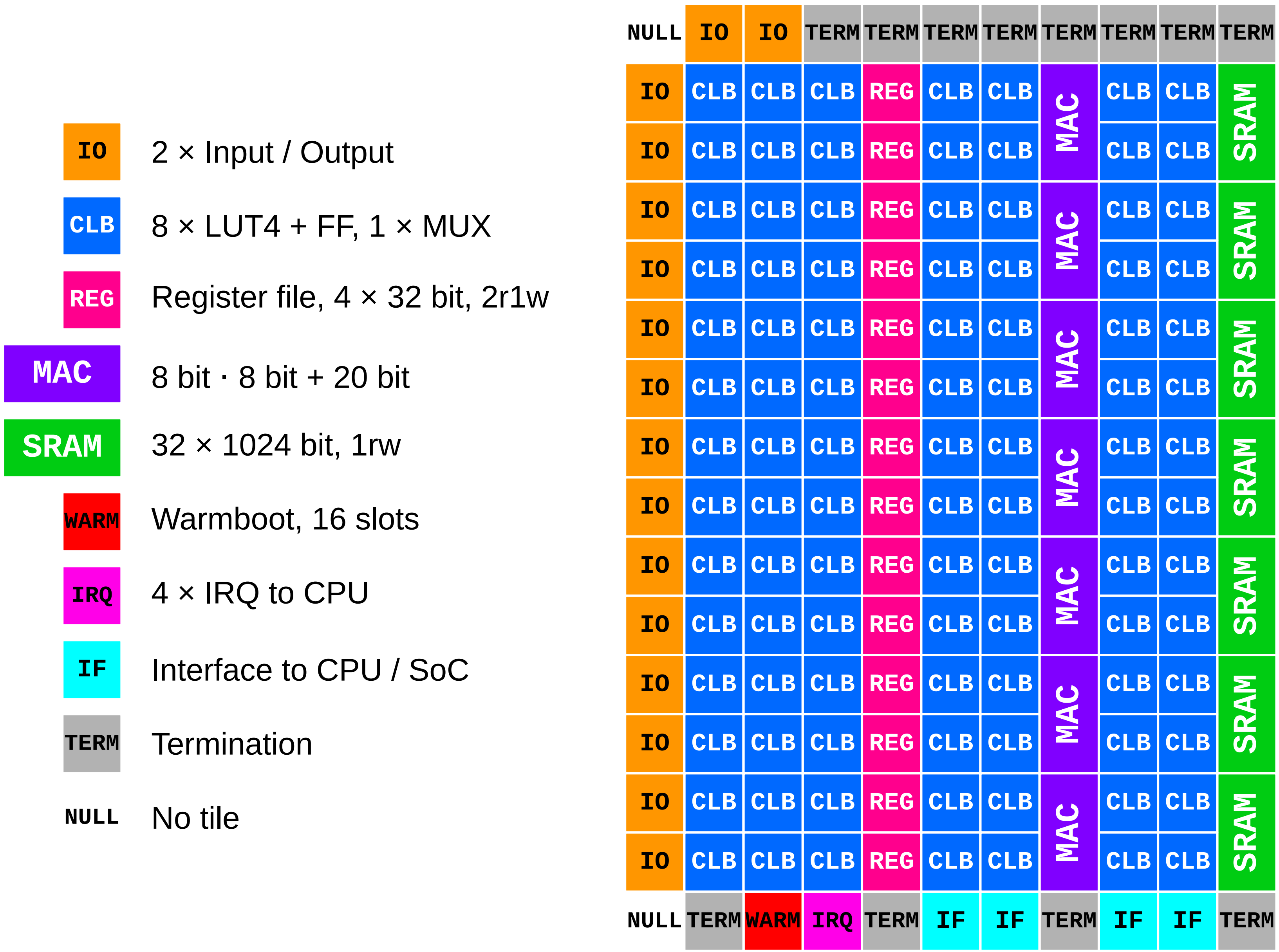
NULL TERM WARM IRQ TERM IF IF TERM IF IF TERM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NULL TERM WARM IRQ TERM IF IF TERM IF IF TERM