CS 31007 Autumn 2020

COMPUTER ORGANIZATION AND ARCHITECTURE

Instructors

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Lecture 02

Indian Institute of Technology Kharagpur

Computer Science and Engineering

Agenda

- Model for computation and Turing Machine
- von Neumann Architecture
- Basic Features of Instruction Set Architecture (ISA)
- Die yield
- CPU Performance Equation
- Amdahl’s Law; Gustavson-Barsis Law
- RISC *versus* CISC

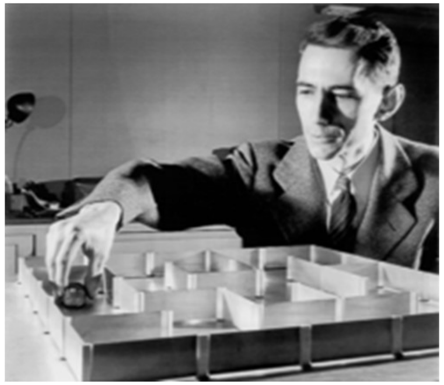
Three Challenges

1. How to design efficient hardware (logic)?

2. What is the simplest, yet all powerful computer (computability)?

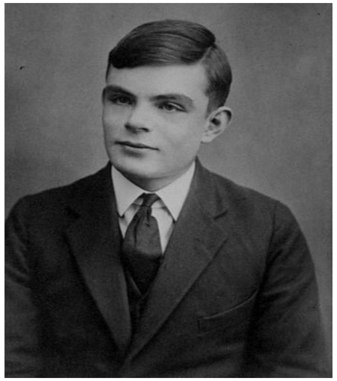
3. How should the basic computer architecture be conceived?

Pioneers who answered these three questions



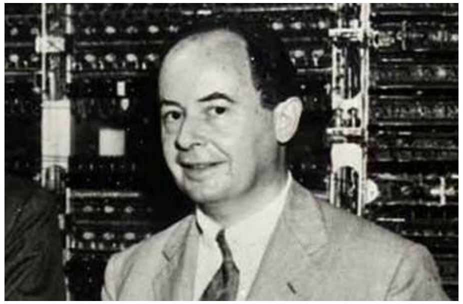
Claude E. Shannon
(1916-2001)

Logic design (basis of computer organization; hardware cost/ circuit delay/power optimization)



Alan Turing
(1912-1954)

Theory of computability (basis for the fundamental requirement in computation)



John von Neumann
(1903-1957)

Blueprint for basic computer architecture

Turing Machine

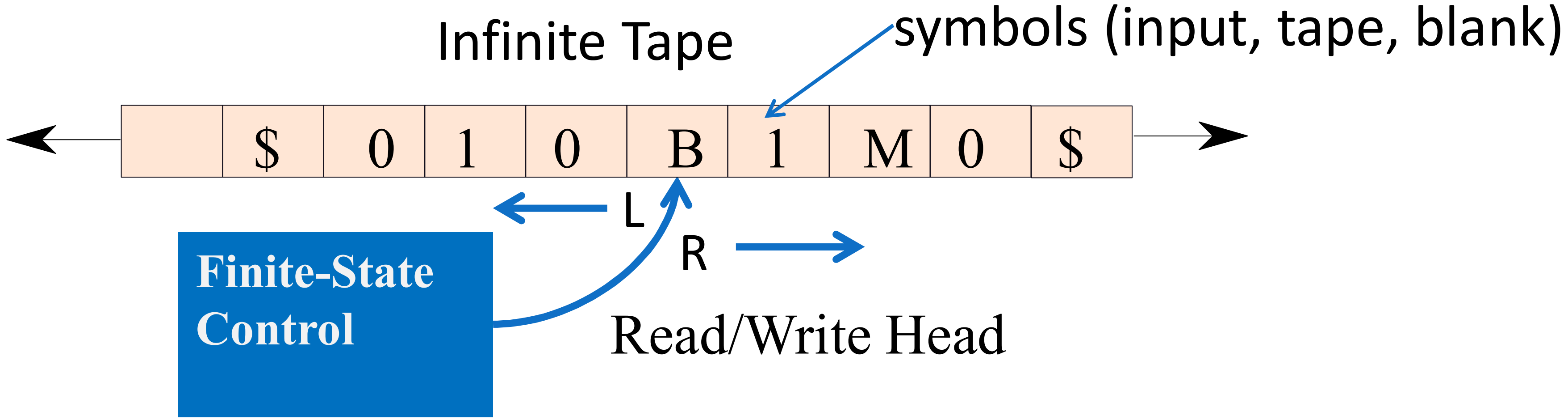
❖ Alan Turing, who gave the fundamental abstraction of a computing machine, was an excellent long distance runner

❖ Pioneer of theoretical computer science and artificial intelligence

❖ His father served Indian Civil Service and worked in Odisha

What is the simplest yet all powerful computer?

Alan Turing (1936): Conceived a machine that introduces a model for computation (Turing Machine)



The tape head can only move left or right

Actions: (present state, current symbol) →
(new state, write symbol, move one cell left/right);

-- The machine halts when an “accept”/”reject” state is reached

Example

- Start with a blank tape and create a pattern 0b1b0b1b . . .
- Define symbols: b (blank), 0, 1

Present state	Symbol on tape	Operation	Next state
S0 (begin)	blank	Write 0 and move right	S1
S1	blank	Move right	S2
S2	blank	Write 1 and move right	S3
S3	blank	Move right	S0

http://en.wikipedia.org/wiki/Turing_machine_examples

Turing Machine

- ❖ Very simple mechanism:
  -- memory, control, read/write, shift, accept/reject

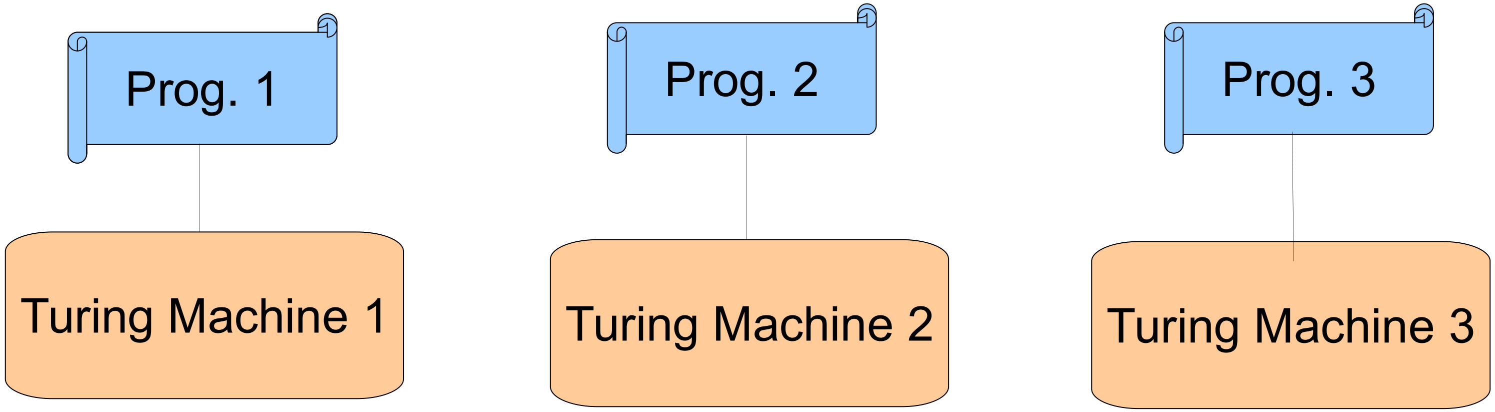
A. M. Turing (1936) , On Computable Numbers with an Application to the Entscheidungsproblem, *Proc. Royal Math. Soc.*, Ser. 2, Vol. 42, pp. 230-265, 1936.

- ❖ Extremely powerful

Church-Turing Conjecture (1936): A function on natural numbers can be calculated by an effective method *if and only if* it is computable by a Turing machine
Any procedure that is computable by paper-and-pencil methods (algorithm) can be solved by a Turing machine

Universal Turing Machine

Church-Turing Conjecture (1936): Any procedure that is computable by paper-and-pencil method (algorithm) can be solved by a Turing machine.

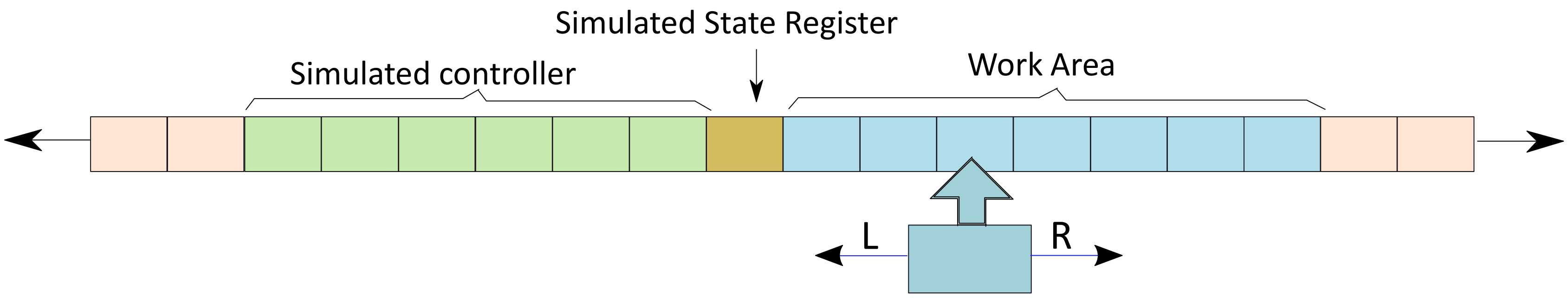


More general question:

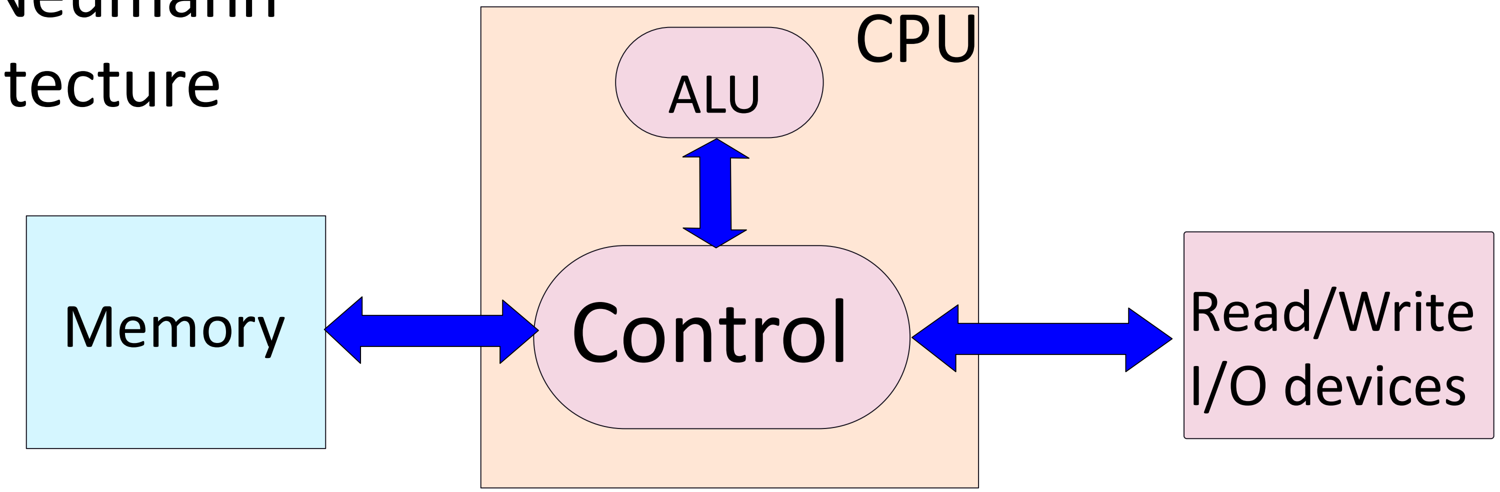
Can we design a Universal Turing machine (UTM) that can simulate any Turing machine?

Universal Turing Machine

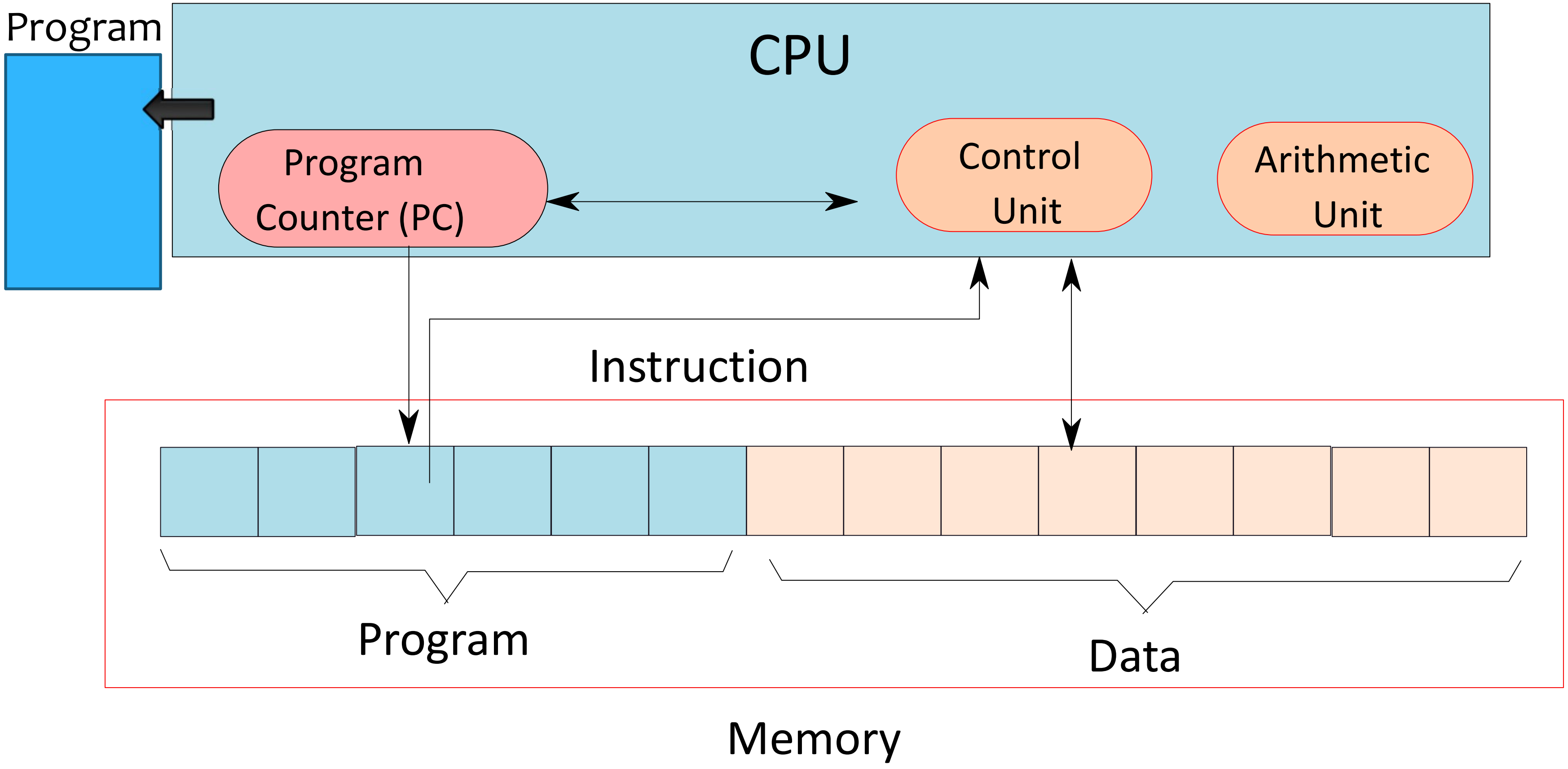
Controller and states are simulated on tape



Von Neumann Architecture



Computer mimicing Turing machine



Turing Undecidability?

Halting Problem: Can we write a program *Q*, which given any arbitrary program *P* as input, will decide whether on not *P* terminates or falls into an infinite loop on input data?

Halting problem is Turing undecidable

Gödel's Incompleteness Theorem

Kurt Gödel
1906-1978

- In 1931, Gödel demonstrated that within any given branch of mathematics, there would always be some propositions that cannot be proven either true or false using the rules and axioms

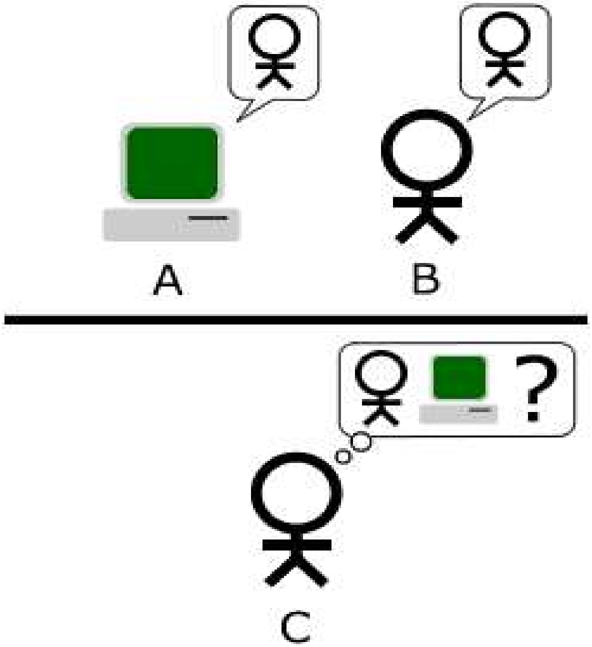
Father of AI/Machine Learning?

“What we want is a machine that can learn from experience”

- Alan Turing

Turing Test

- Can a computer think? (Turing, 1950)
- A. P. Saygin, I. Cicekli and V. Akman, “Turing Test: 50 Years Later,” *Minds and Machines*, vol. 10, no. 4, pp. 463-518, 2000.



Can a person *C* discriminate between a machine *A* and human *B* by asking questions and getting written answers?

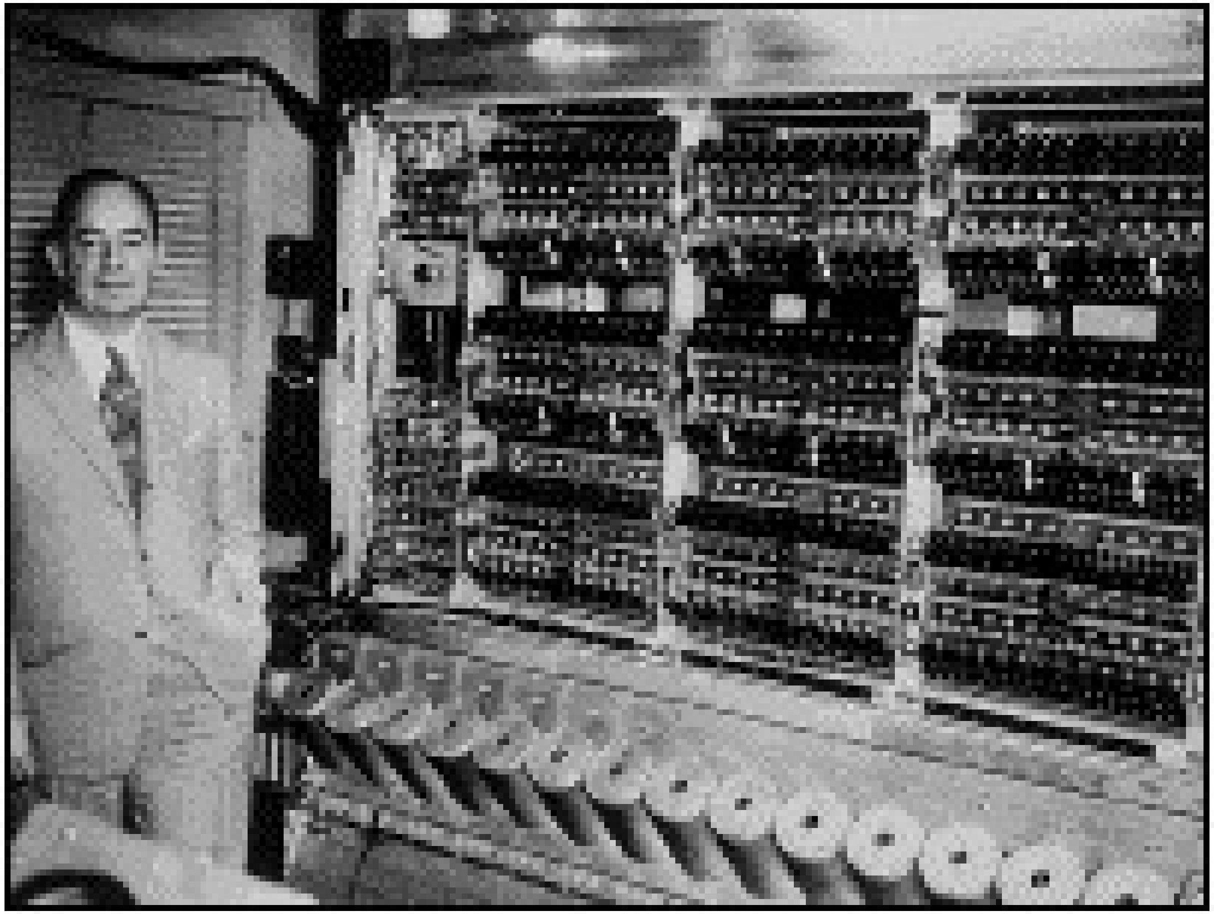
http://www.engadget.com/2011/01/13/ibms-watson-supercomputer-destroys-all-humans-in-jeopardy-pract/

Turing Test

- In 2014, The 65 year-old Turing Test was passed for the very first time by computer program Eugene Goostman during Turing Test held at the Royal Society in London
- 'Eugene' simulates a 13 year old boy and was developed in Saint Petersburg, Russia. The development team includes Vladimir Veselov and Eugene Demchenko
- A program wins the Turing Test if it is mistaken for a human more than 30% of the time.

http://www.reading.ac.uk/news-and-events/releases/PR583836.aspx

John Von Neumann



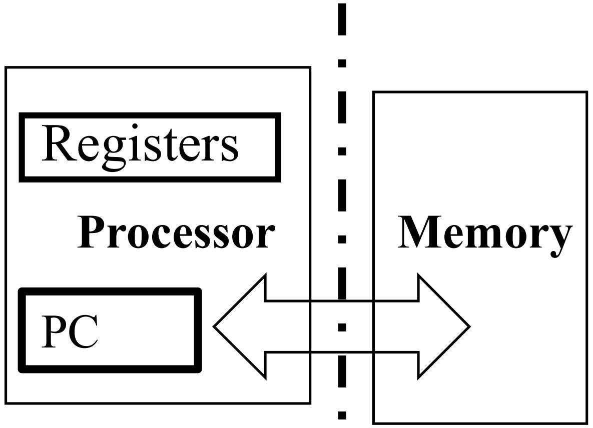
von Neumann Architecture (1945): Princeton Architecture

° Stored program concept

° Serves as the basis for almost all modern computers

° Instructions and data are just bits

° Programs (sequence of machine instructions) are stored in memory to be read or written just like data



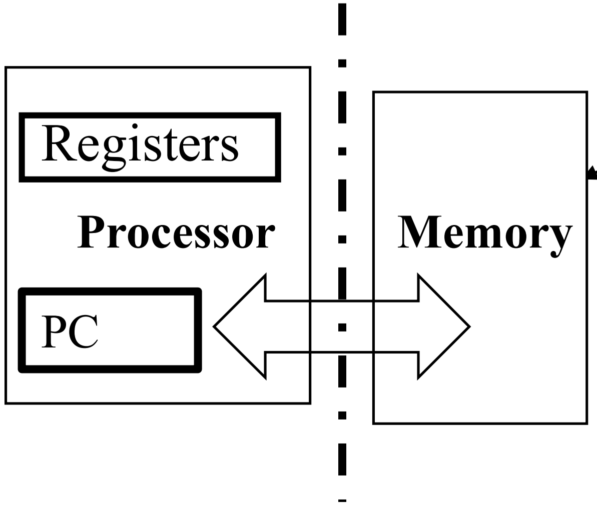
memory for data, programs, compilers, systems programs

° **Fetch & Execute Cycle**

- Program Counter (PC) points to the present Instruction to be fetched
- Bits in the register "control" the subsequent actions
- Fetch the “next” instruction and continue

Binary String Stored in Computer: Who am I?

- X = - 1,880,113,152 (if X is a 2's complement binary number)
- X = 2,414,854,144 (if X is an unsigned binary number)
- X = - 1.873 × 2^{-96} (if X is a floating-point number)
- X ⇨ `lw $t7, -16384 ($ra)` (if X is a MIPS instruction)



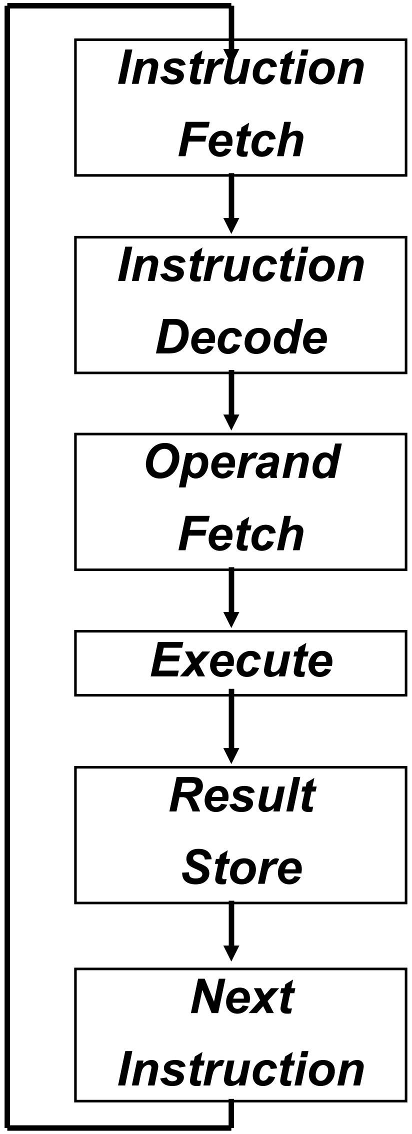
Let the content (X) of a memory location be:

X: 0x 8FEFC000

X: 1000 1111 1110 1111 1100 0000 0000 0000

- Need execution cycles to interpret the binary strings properly – whether it is instruction or data, and if data, what type?

Execution Cycle



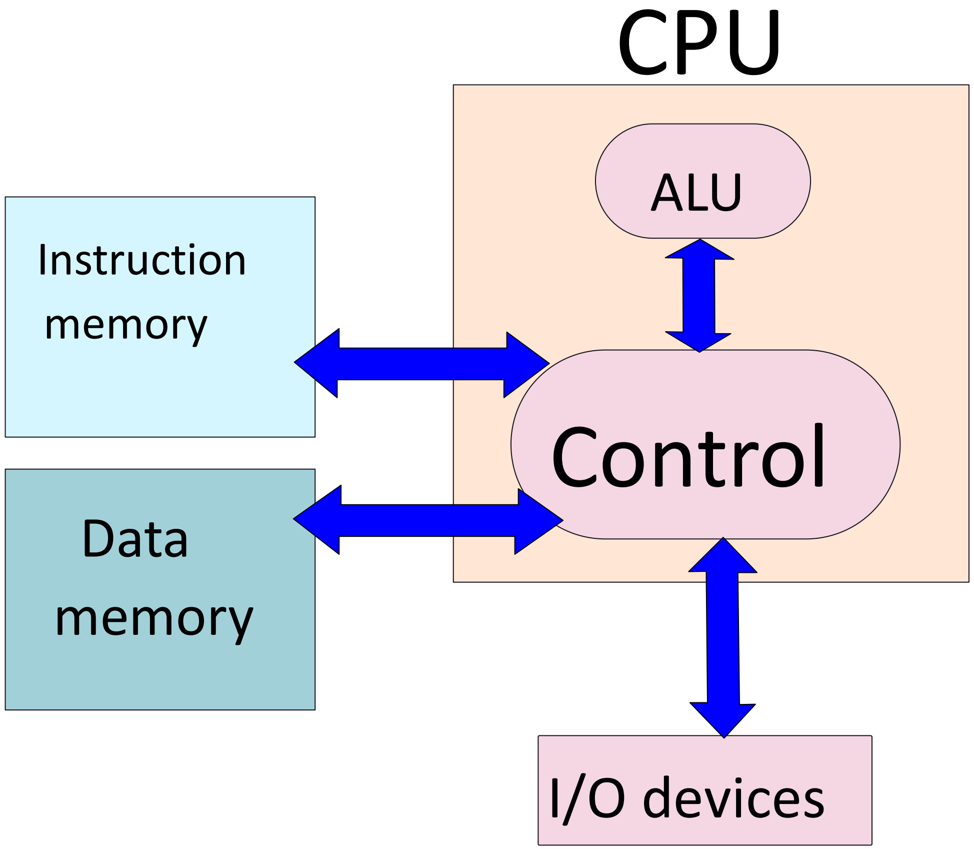
Instruction Fetch	Obtain instruction from memory
Instruction Decode	Determine required actions and instruction size
Operand Fetch	Locate and obtain operand data from memory/register
Execute	Compute result value or status
Result Store	Deposit results in register/memory for later use
Next Instruction	Determine successor instruction

Features of von Neumann Architecture

- Same physical memory to save instructions and data
- Instruction fetch and data transfer cannot be done concurrently; they need two clock cycles
- Simple architecture

- Harvard Architecture: Separate instruction and data memory

Harvard Architecture

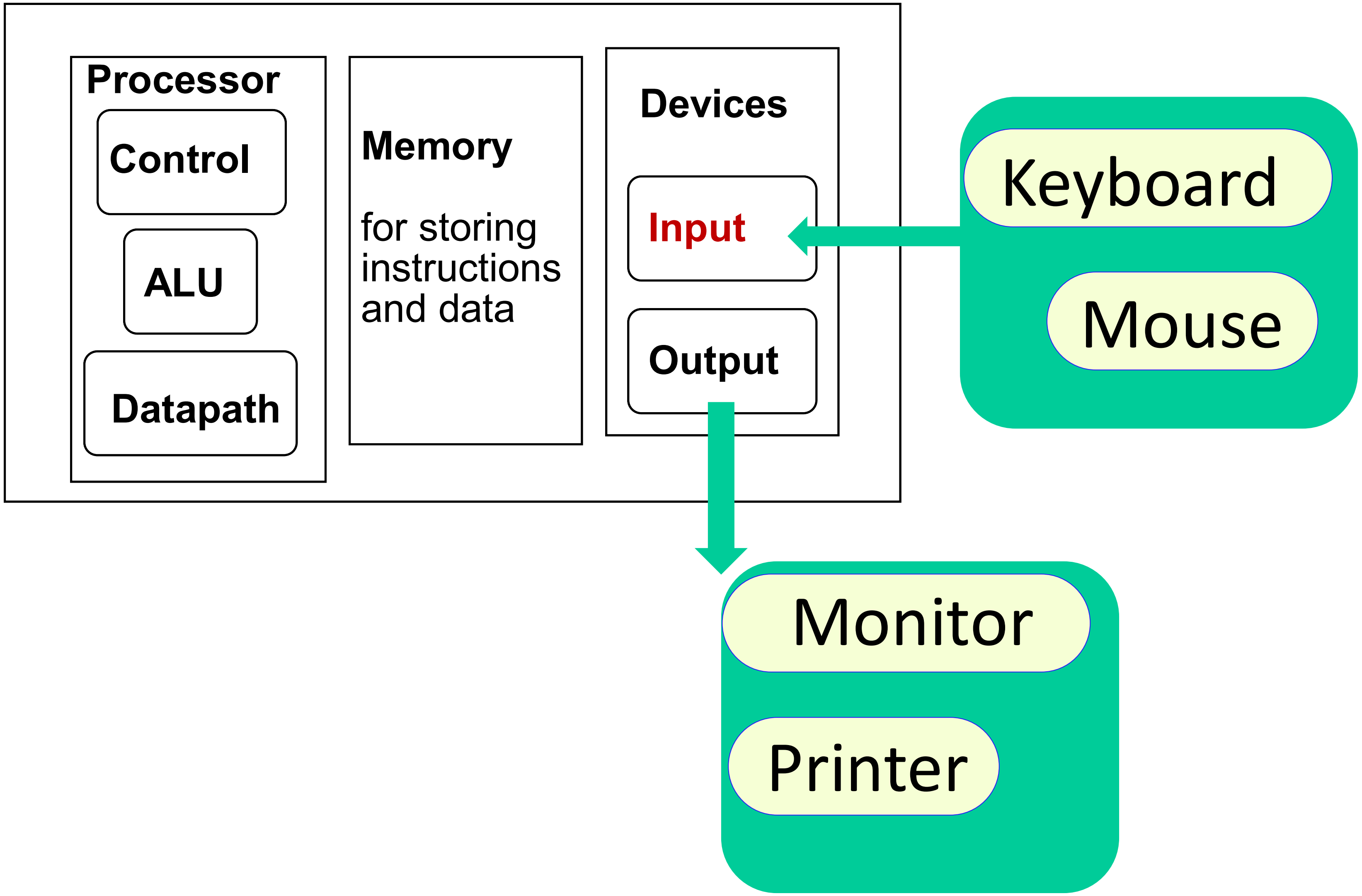


- ➢Based on Harvard Mark I relay-based computer model
- ➢Separate signal pathways for instruction and data; can be accessed concurrently

Von Neumann Bottleneck

- Von Neumann architecture uses the same memory for instructions (program) and data.
- The time spent in memory accesses can limit the performance. This phenomenon is referred to as *von Neumann bottleneck*.
- To avoid the bottleneck, later architectures allow frequently used operands to reside in on-chip registers

Full Picture



What You Will Learn

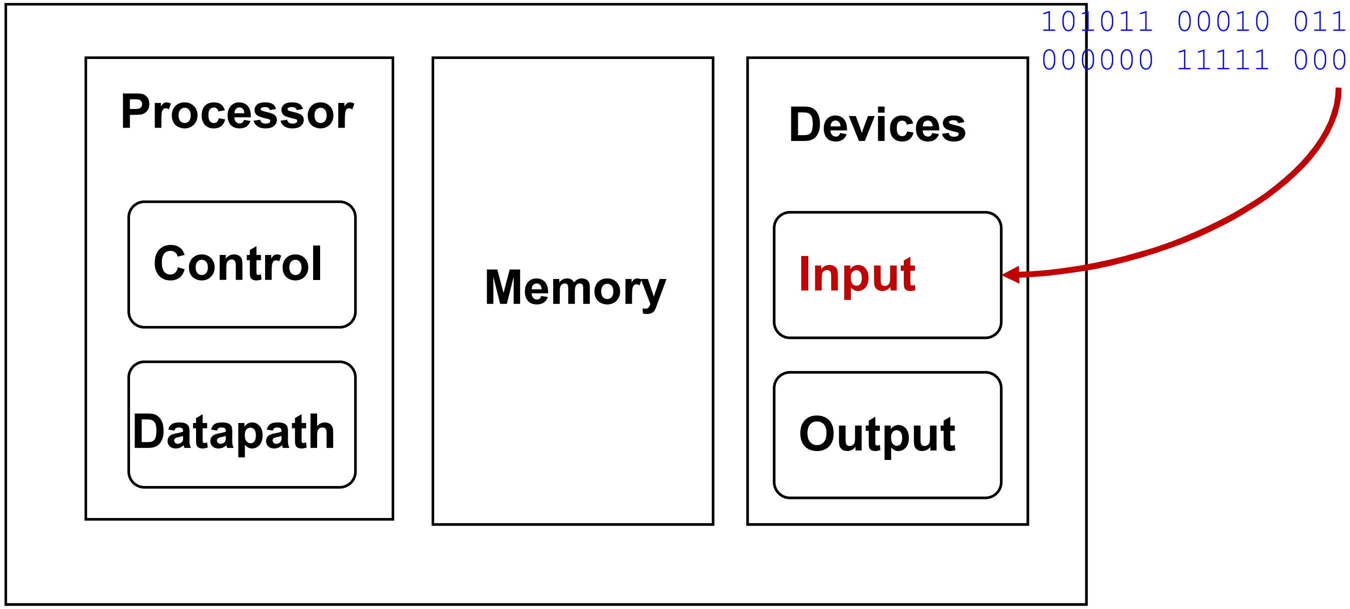
- How programs are translated into the machine language
  - And how the hardware executes them
- The hardware/software interface
- What determines program performance
  - And how it can be improved
- How hardware designers improve performance
- What is parallel processing

Understanding Performance

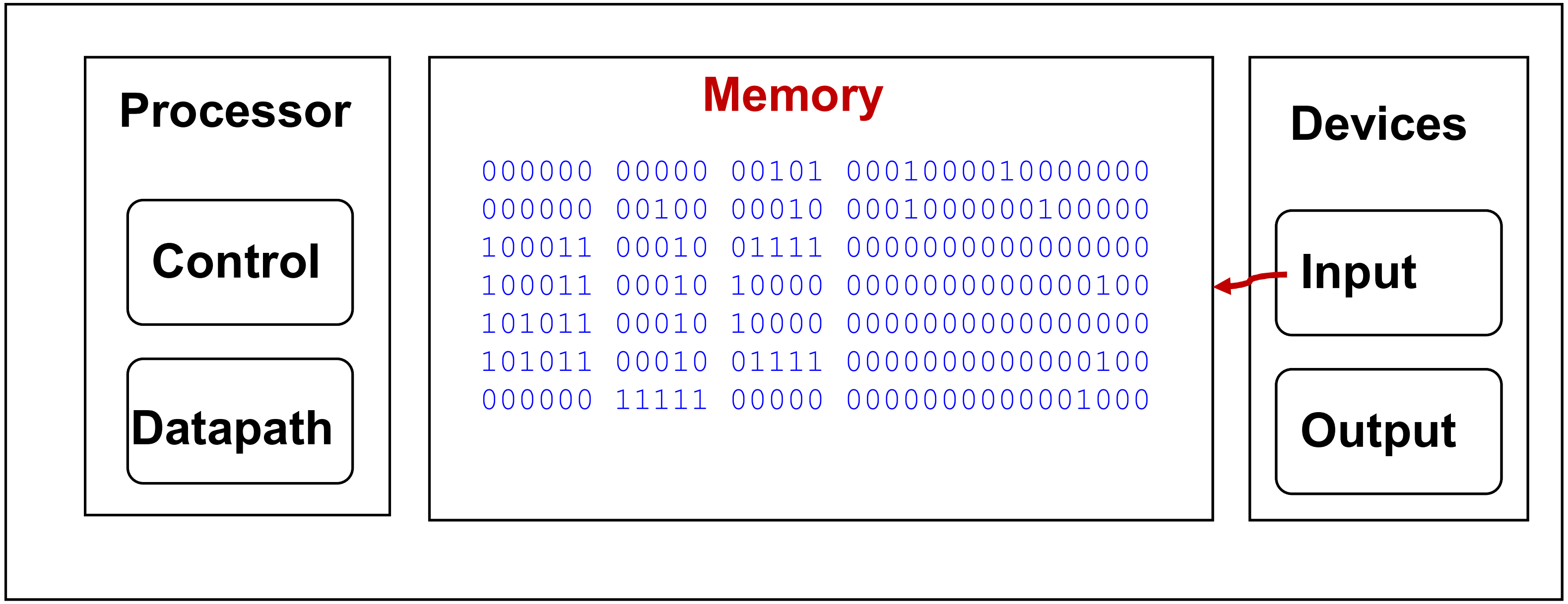
- Algorithm
  - Determines number of operations executed
- Programming language, compiler, architecture
  - Determine number of machine instructions executed per operation
- Processor and memory system
  - Determine how fast instructions are executed
- I/O system (including OS)
  - Determines how fast I/O operations are executed

Load Input Binary

```
000000 00000 00101 0001000010000000
000000 00100 00010 0001000000100000
100011 00010 01111 0000000000000000
100011 00010 10000 0000000000000100
101011 00010 10000 0000000000000000
101011 00010 01111 0000000000000100
000000 11111 00000 0000000000001000
```



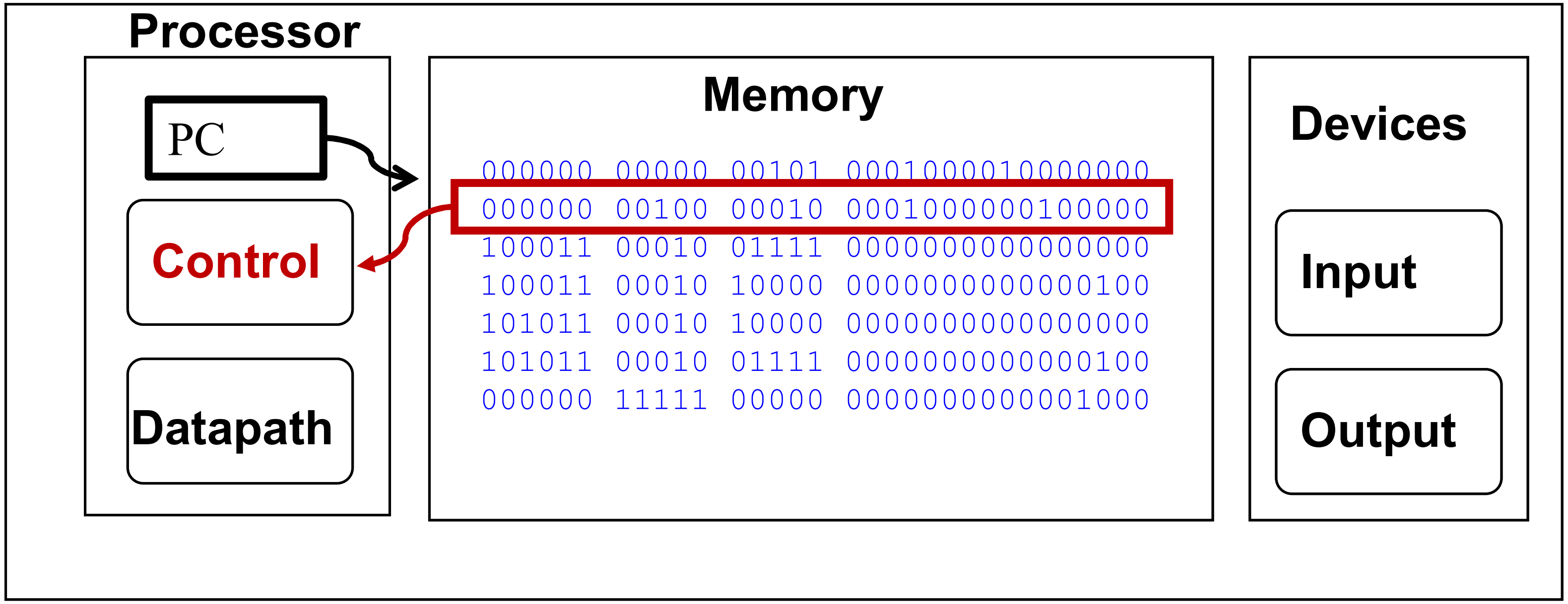
Code Stored in Memory



```
000000 00000 00101 0001000010000000
000000 00100 00010 0001000000100000
100011 00010 01111 0000000000000000
100011 00010 10000 0000000000000100
101011 00010 10000 0000000000000000
101011 00010 01111 0000000000000100
000000 11111 00000 0000000000001000
```

Processor Fetches an Instruction

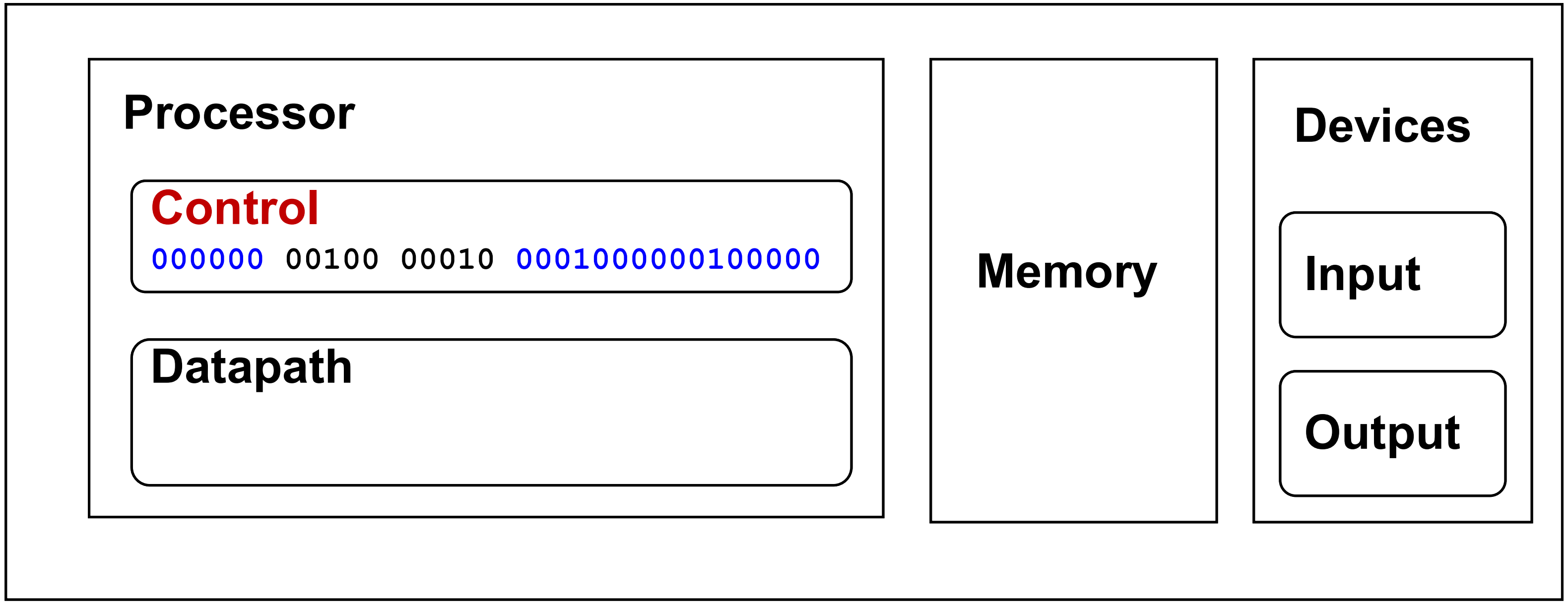
Processor fetches an instruction from memory pointed by Program Counter PC



```
000000 00000 00101 0001000010000000
000000 00100 00010 0001000000100000
100011 00010 01111 0000000000000000
100011 00010 10000 0000000000000100
101011 00010 10000 0000000000000000
101011 00010 01111 0000000000000100
000000 11111 00000 0000000000001000
```

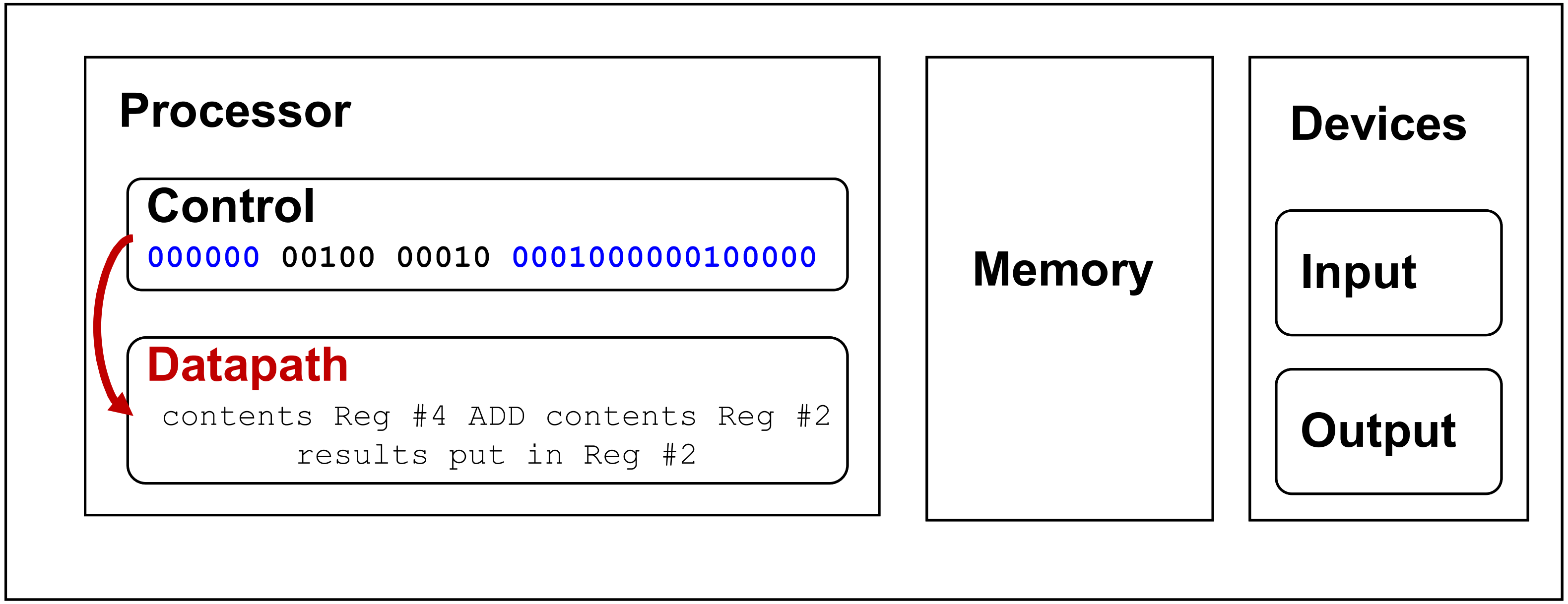
Where does it fetch from?

Control Decodes the Instruction



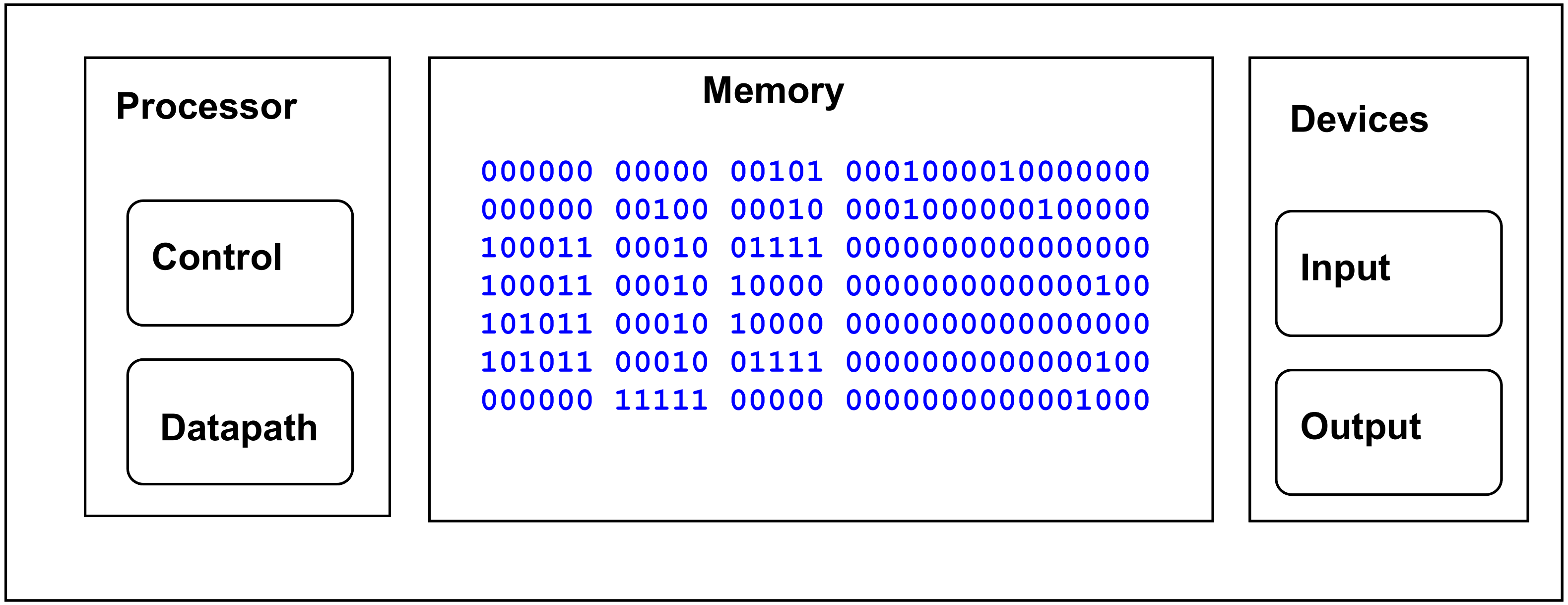
Control decodes the instruction to determine what to execute

Datapath Executes the Instruction

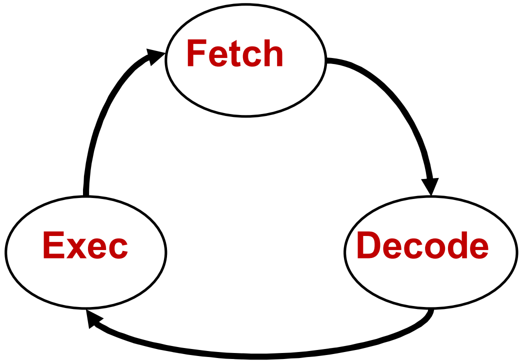


Datapath executes the instruction as directed by control

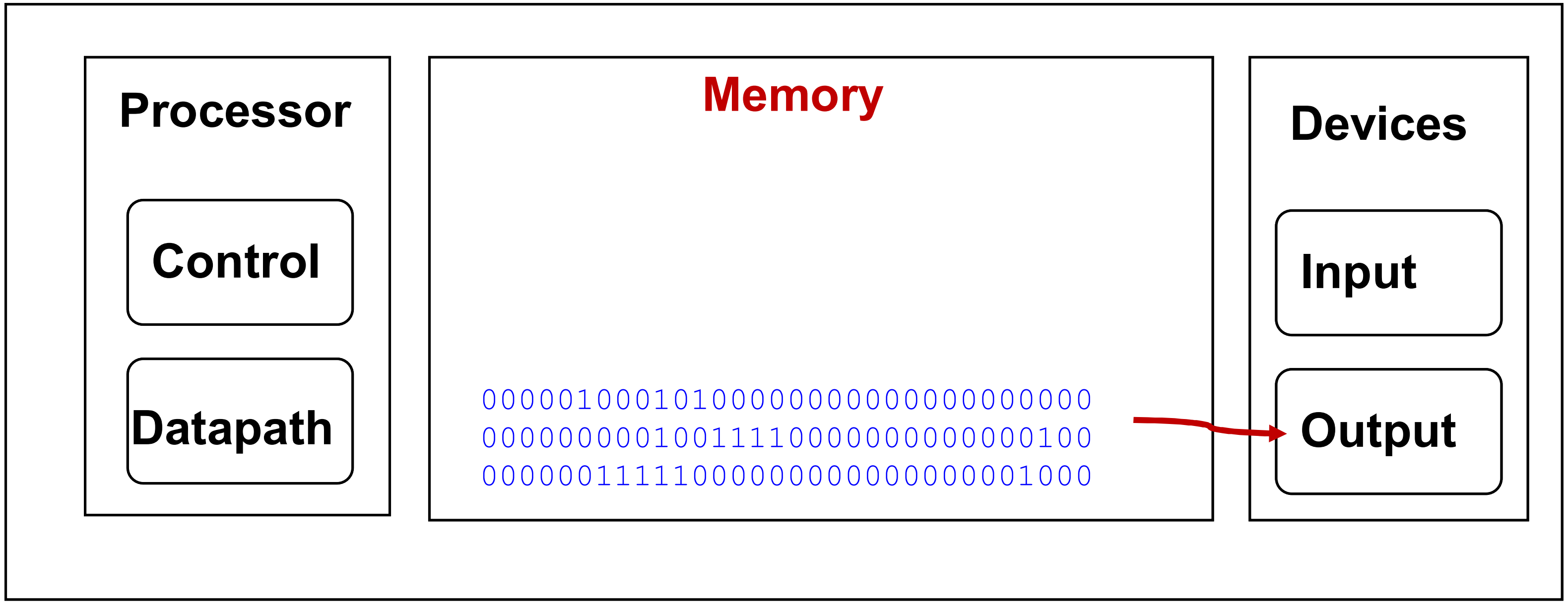
What Happens Next?



```
000000 00000 00101 0001000010000000
000000 00100 00010 0001000000100000
100011 00010 01111 0000000000000000
100011 00010 10000 0000000000000100
101011 00010 10000 0000000000000000
101011 00010 01111 0000000000000100
000000 11111 00000 0000000000001000
```



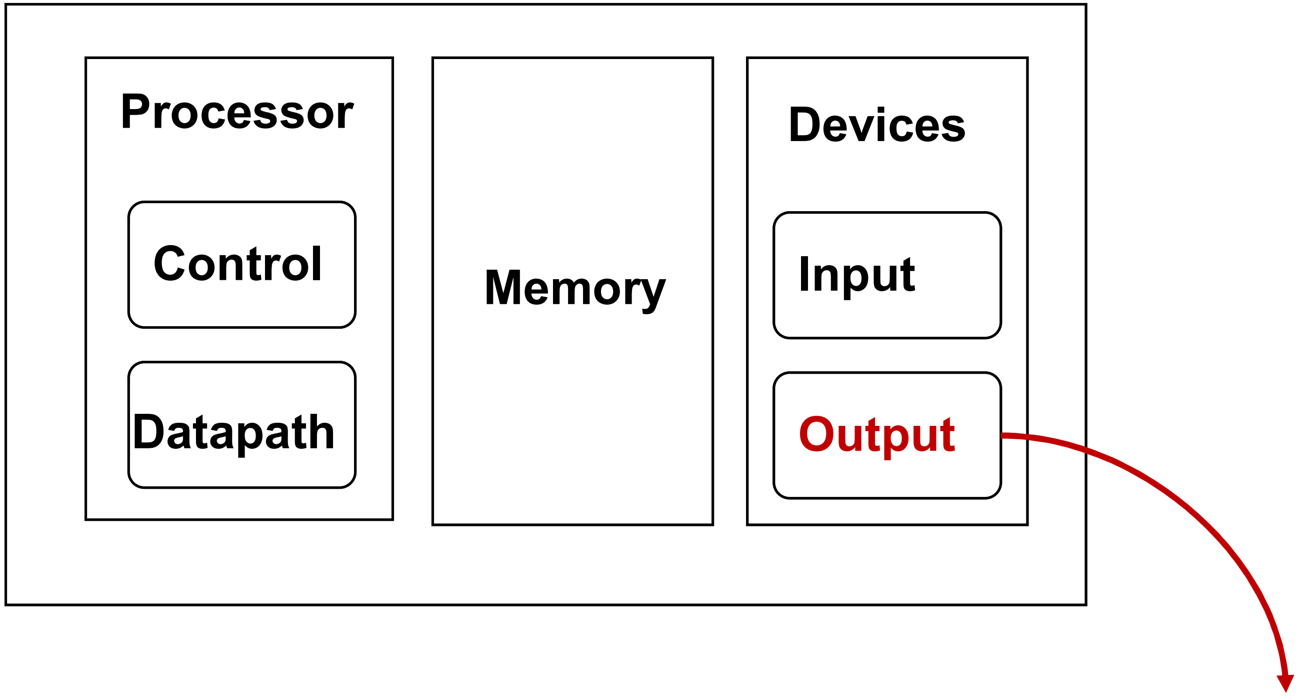
Output Data Stored in Memory



```
00000100010100000000000000000000
00000000010011110000000000000100
00000011111000000000000000001000
```

On program completion, results reside in memory

Output Device Outputs Data

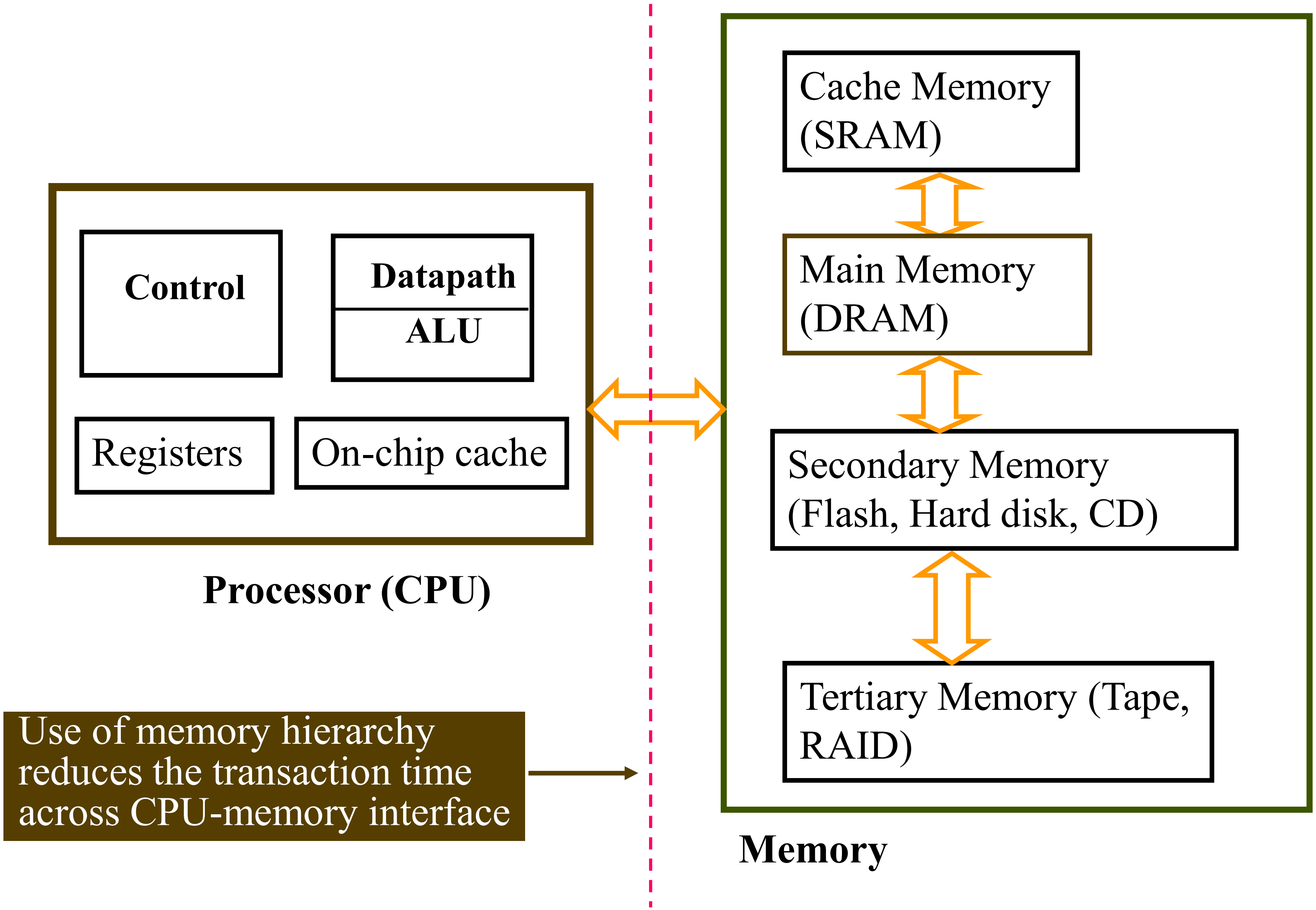


```
00000100010100000000000000000000
00000000010011110000000000000100
00000011111000000000000000001000
```

von Neumann Bottleneck

- von Neumann architecture uses the same memory for instructions (program) and data
- The time spent in memory accesses can limit the performance. This phenomenon is referred to as *von Neumann bottleneck*.
- To avoid the bottleneck, later architectures restrict operands to registers (temporary storage in processor).

Complete View of Computer Architecture



Control

Datapath

ALU

Registers

On-chip cache

Processor (CPU)

Cache Memory (SRAM)

Main Memory (DRAM)

Secondary Memory (Flash, Hard disk, CD)

Tertiary Memory (Tape, RAID)

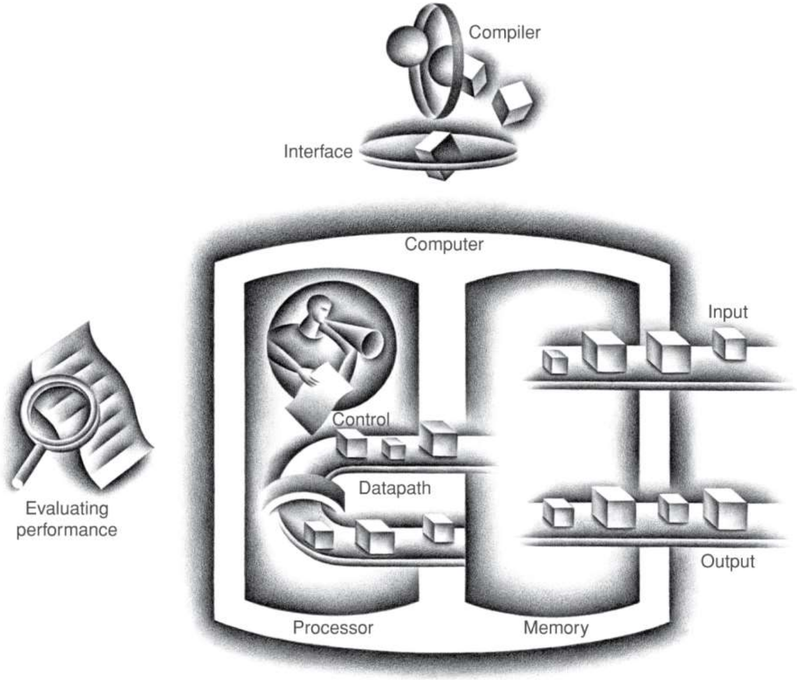
Memory

Use of memory hierarchy reduces the transaction time across CPU-memory interface

Components of a Computer

§1.4 Under the Covers

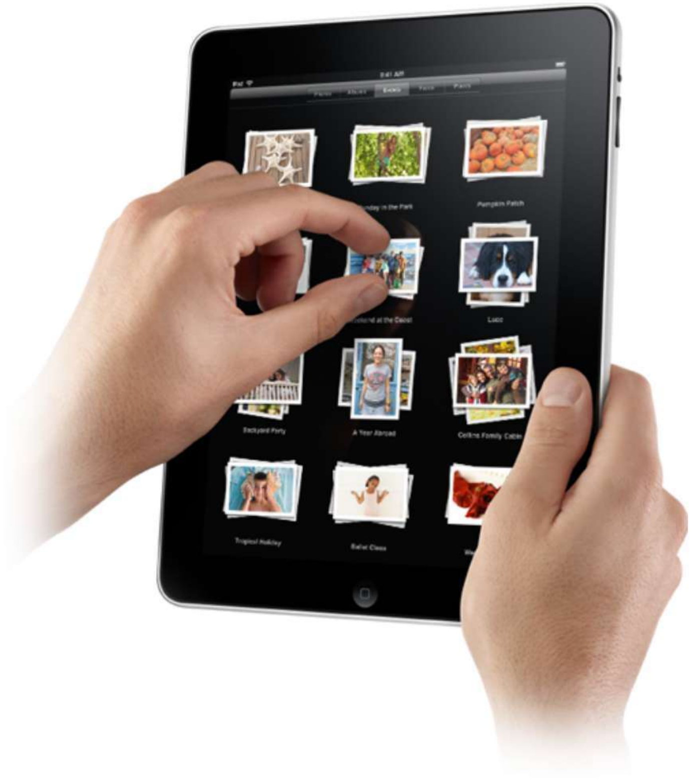
The BIG Picture



- Same components for all kinds of computer
  - Desktop, server, embedded
- Input/output includes
  - User-interface devices
    - Display, keyboard, mouse
  - Storage devices
    - Hard disk, CD/DVD, flash
  - Network adapters
    - For communicating with other computers

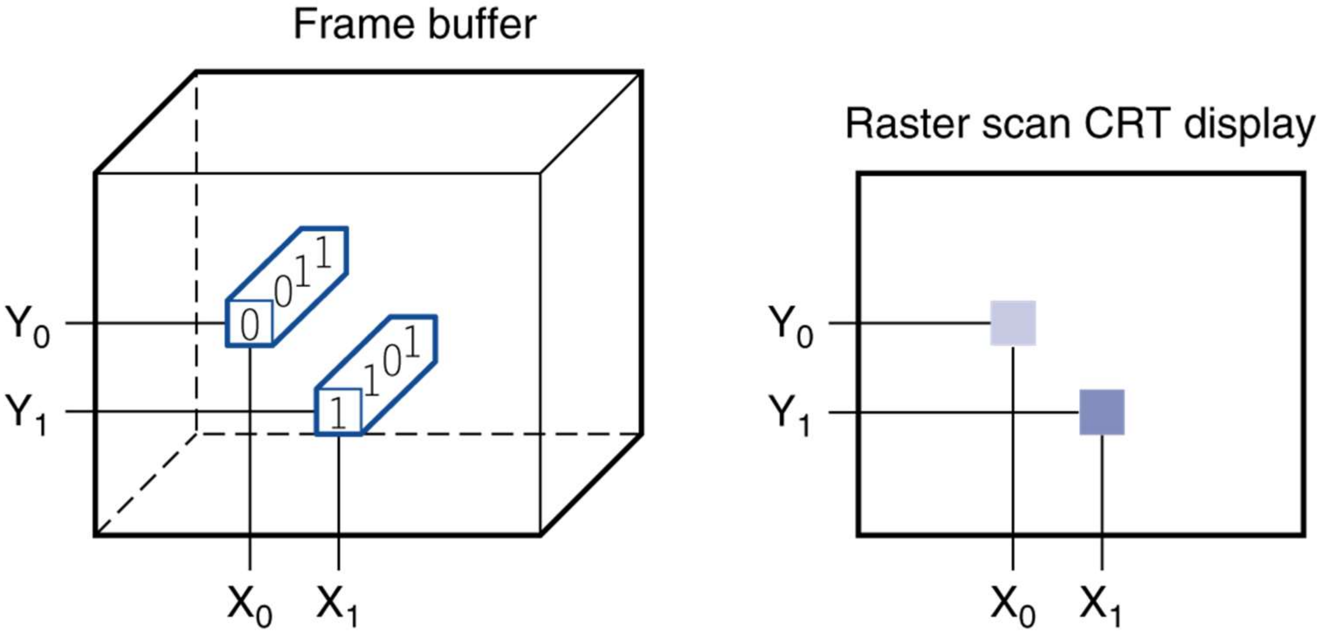
Touchscreen

- PostPC device
- Supersedes keyboard and mouse
- Resistive and Capacitive types
  - Most tablets, smart phones use capacitive
  - Capacitive allows multiple touches simultaneously

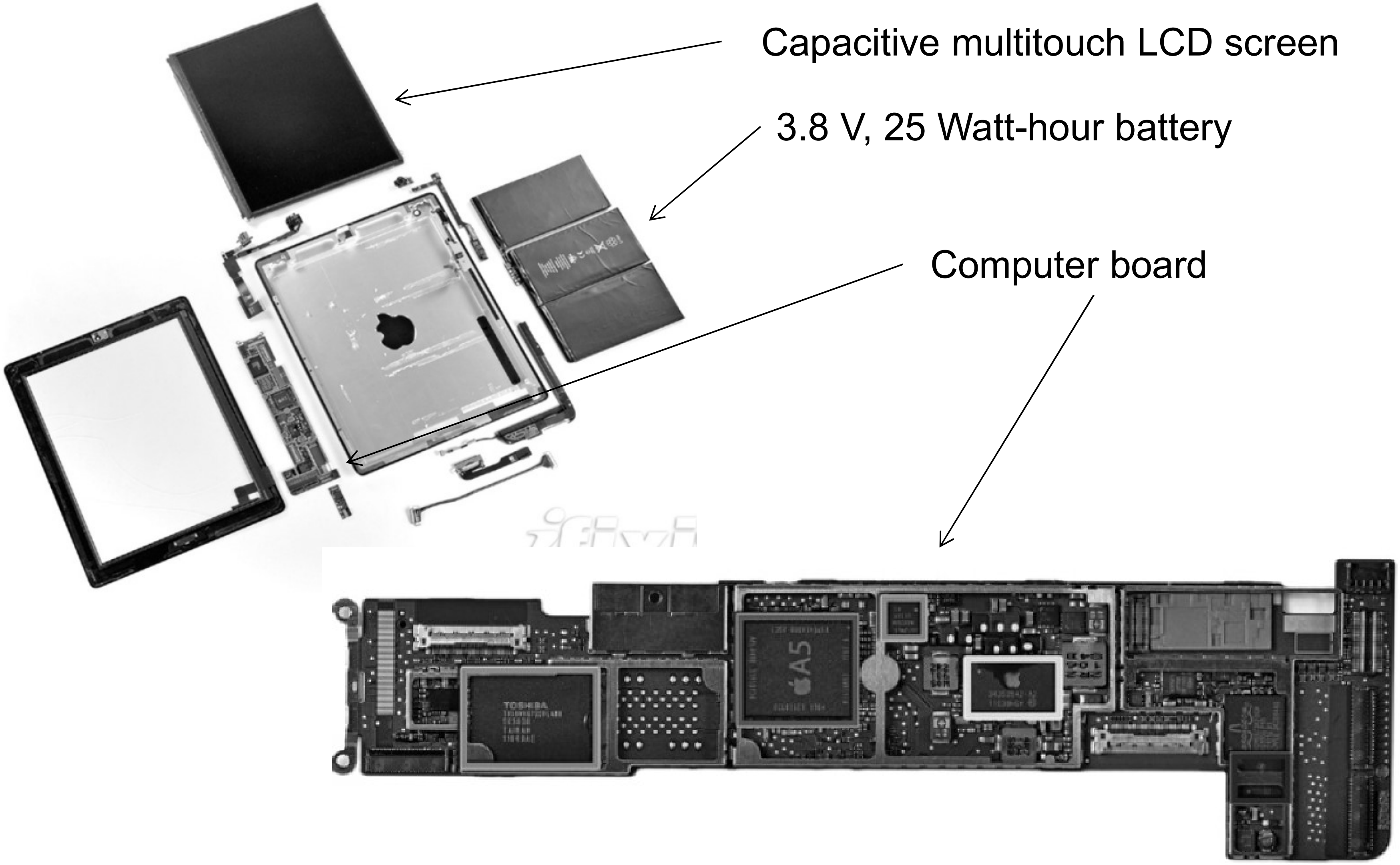


Through the Looking Glass

- LCD screen: picture elements (pixels)
  - Mirrors content of frame buffer memory



Opening the Box



Capacitive multitouch LCD screen

3.8 V, 25 Watt-hour battery

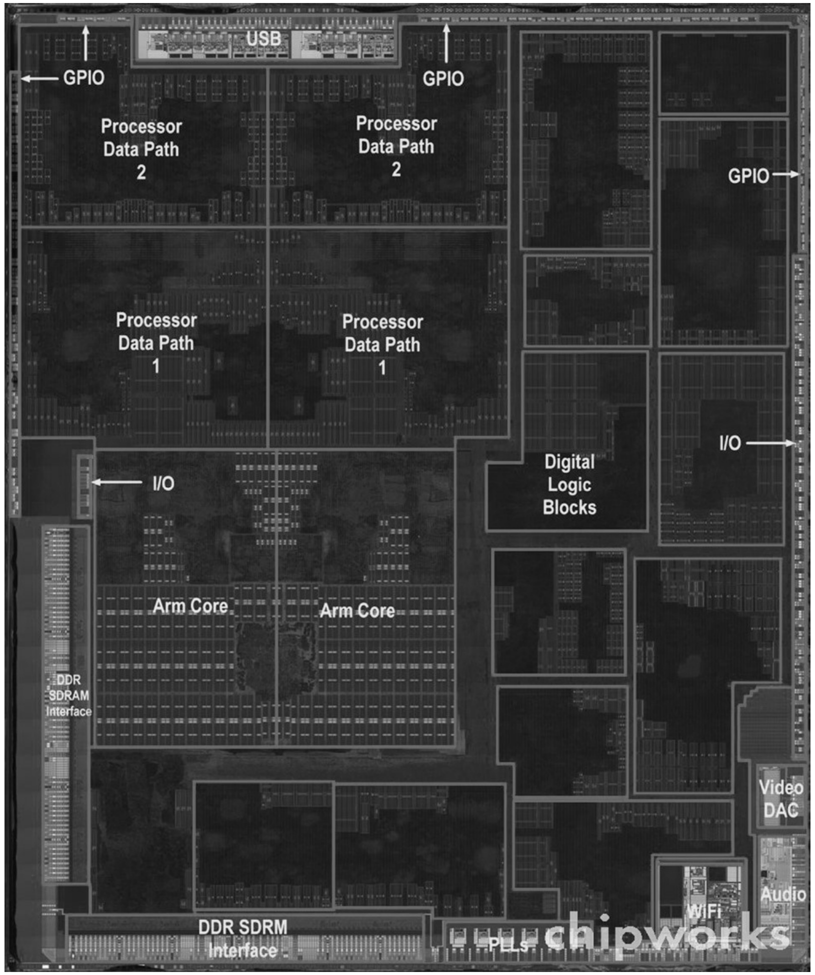
Computer board

Inside the Processor (CPU)

- Datapath: performs operations on data
- Control: sequences datapath, memory, ...
- Cache memory
  - Small fast SRAM memory for immediate access to data

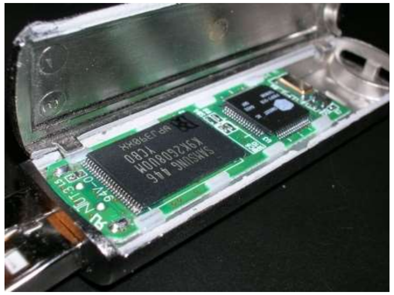
Inside the Processor

- Apple A5



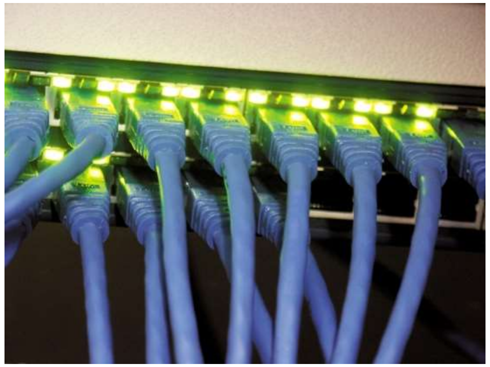
A Safe Place for Data

- Volatile main memory
  - Loses instructions and data when power off
- Non-volatile secondary memory
  - Magnetic disk
  - Flash memory, SSD
  - Optical disk (CDROM, DVD)



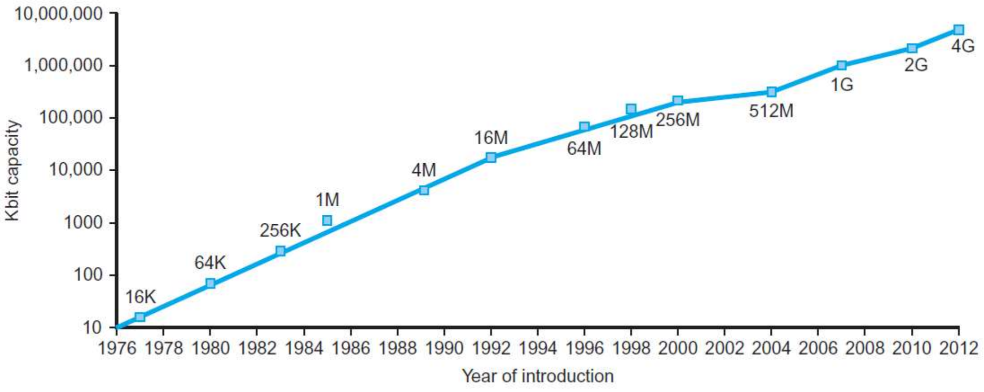
Networks

- Communication, resource sharing, nonlocal access
- Local area network (LAN): Ethernet
- Wide area network (WAN): the Internet
- Wireless network: WiFi, Bluetooth



Technology Trends

- Electronics technology continues to evolve
  - Increased capacity and performance
  - Reduced cost



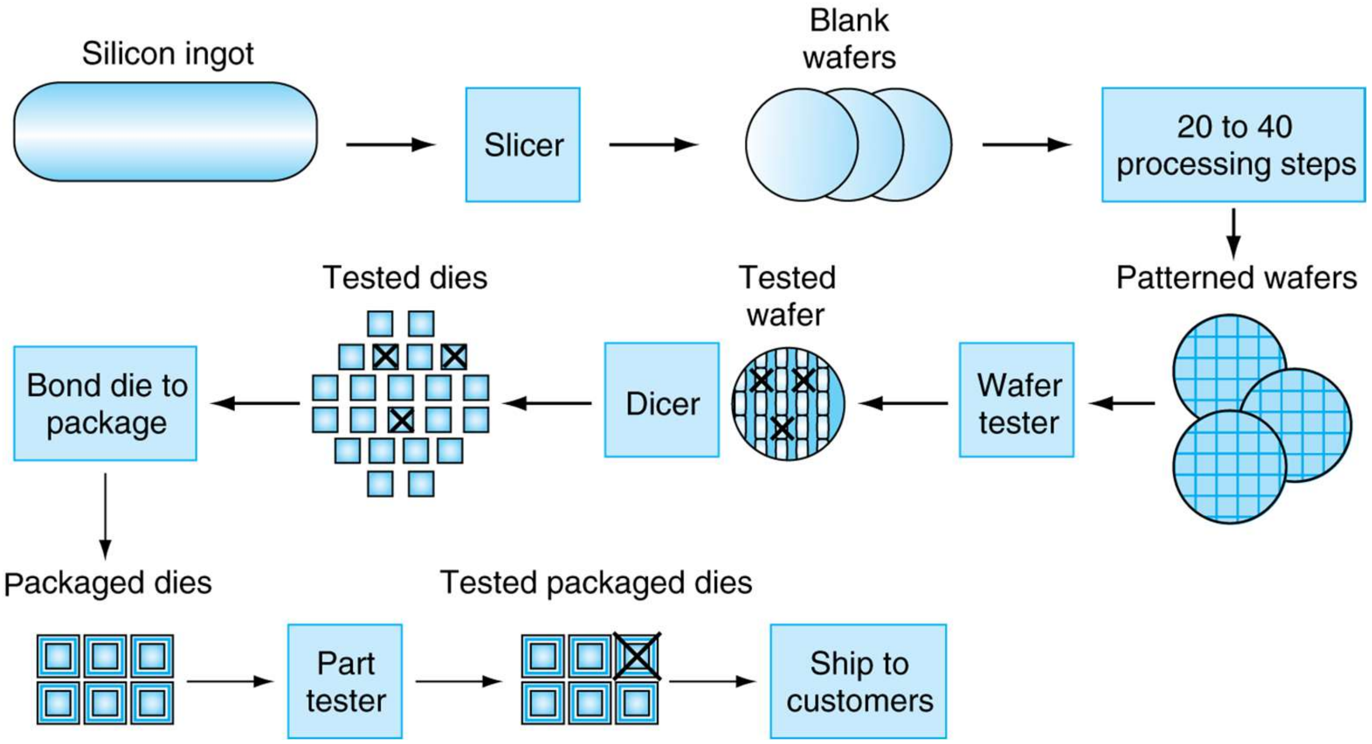
DRAM capacity

§1.5 Technologies for Building Processors and Memory

Semiconductor Technology

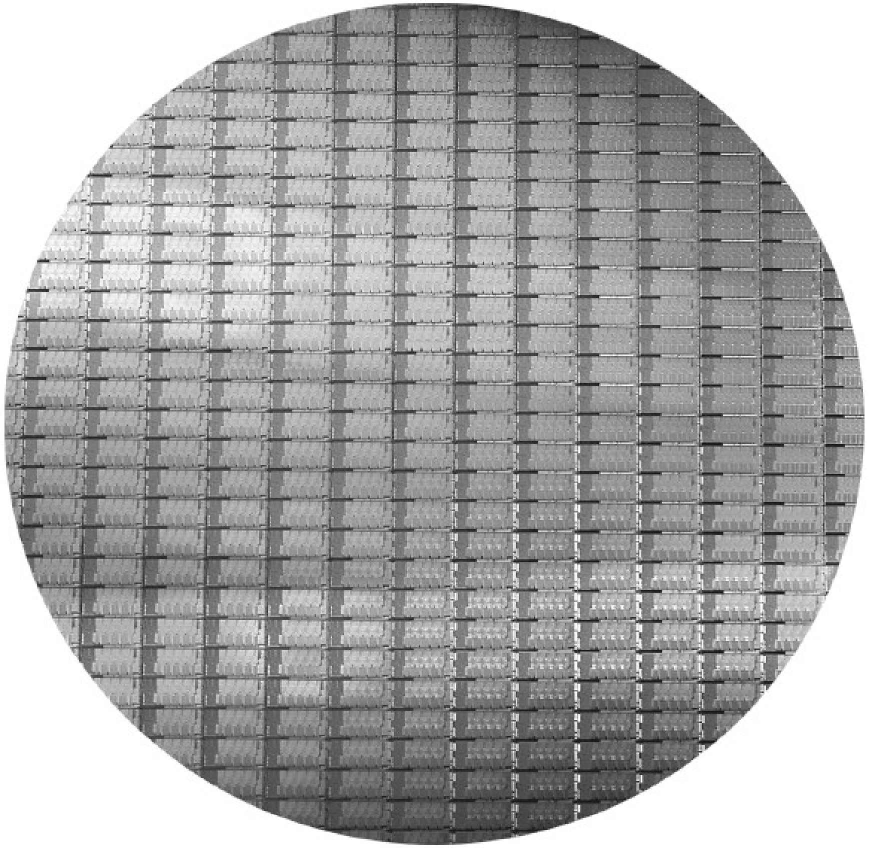
- Silicon: semiconductor
- Add materials to transform properties:
  - Conductors
  - Insulators
  - Switch

Manufacturing ICs



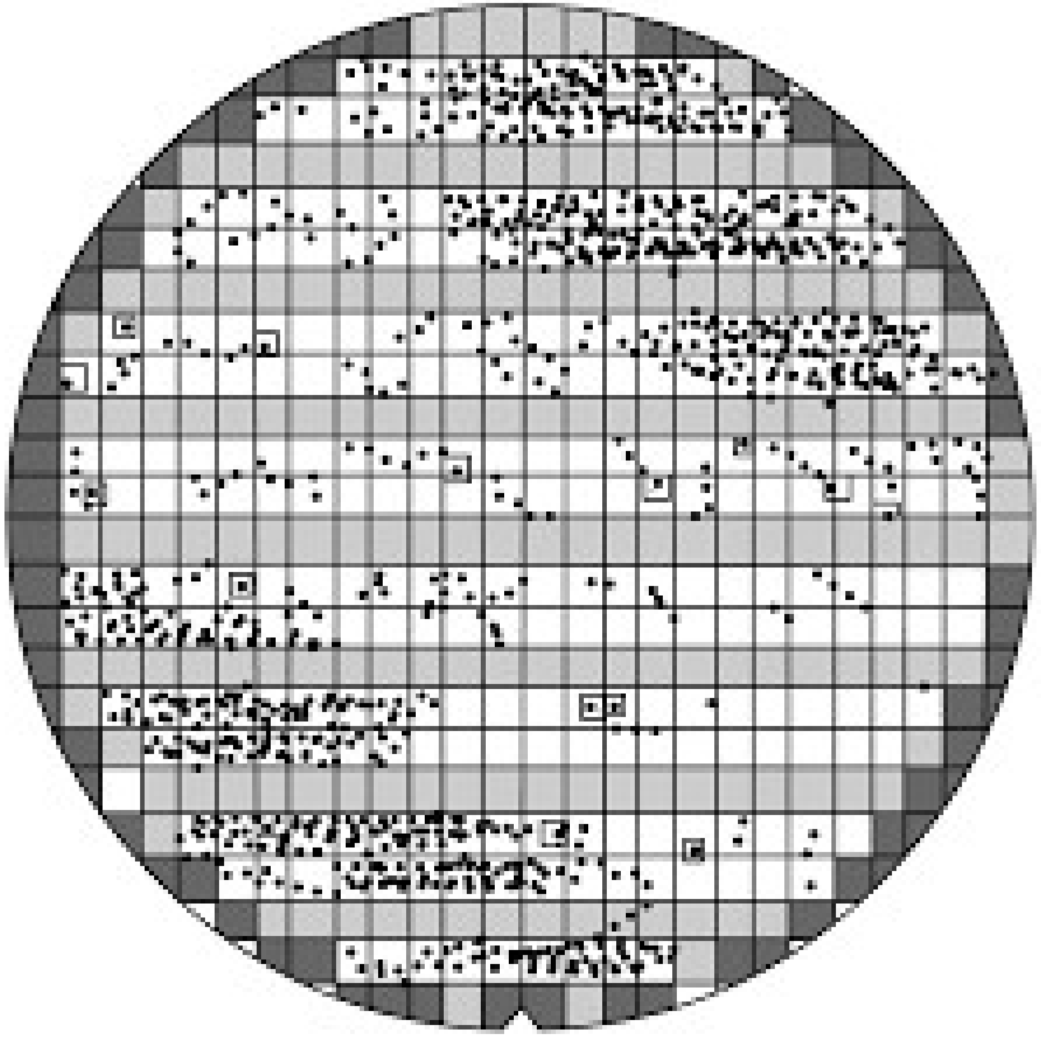
- Yield: proportion of working dies per wafer

Intel Core i7 Wafer



- 300mm wafer, 280 chips, 32nm technology
- Each chip is 20.7 x 10.5 mm

Defects in IC's and Yield



Integrated Circuit Cost

$$\text{Cost per die} = \frac{\text{Cost per wafer}}{\text{Dies per wafer} \times \text{Yield}}$$

$$\text{Dies per wafer} \approx \text{Wafer area} / \text{Die area}$$

$$\text{Yield} = \frac{1}{[1 + \{(\text{Defects per unit area of chip} \times \text{chip area})/\alpha\}]^{\alpha}}$$

chip-cost ~ $(\text{die-area})^4$

This is an empirical estimation of yield; α is a parameter that roughly captures the complexity of the manufacturing process

- Nonlinear relation to area and defect rate
  - Wafer cost and area are fixed
  - Defect rate determined by manufacturing process
  - Die area determined by architecture and circuit design

Summary: Elements of a Computer

- Memory (array of bytes) contains
  - The program, which is a sequence of instructions
  - The program data → variables and constants
- The program counter (PC) points to an instruction in a program
  - After executing an instruction, it points to the next instruction by default
  - A branch instruction makes the PC point to another instruction (not in sequence)
- CPU (Central Processing Unit) contains
  - Program counter, instruction execution units, arithmetic logic unit (ALU)

Instruction Set Architecture (ISA)

- The set of machine-level instructions in a particular CPU implementation is called *Instruction Set*
- Goals of Instruction Set:
  - Software must be able to compute anything in a reasonable number of steps using the instructions in the instruction set
- Different CPUs implement different sets of instructions

Features of Instruction Set Archiecture (ISA)

Collection of Assembly-level or Machine-level (M/L) instructions, which are executable by the hardware

An example of M/L instruction: `addi $t0, $s1, 5`

op	s1	t0	Immediate
6 bits	5 bits	5 bits	16 bits
001000	10001	01000	0000000000000101

Total length of the instruction – 16 bits; opcode: 6 bits; $t0, $s1 -> CPU registers;

Add 5 to the content of $s1 and save the result in $t0

Features of Instruction Set Archiecture (ISA)

Instruction format: length (how many bits – fixed or variable?), format, fields, opcodes, register specifications, how many operands/memory addresses specified?
Size of the logical address space?
Number of instructions? – determines #bits in op-code.
Instruction types? – arithmetic (integer/floating point), logical, data transfer, branch, procedure calls, bit-shifting
Addressing modes: immediate, direct, register, displacement, scaled, indirect; addressing granularity (word-level, byte-level?)
Others: Orthogonality, Completeness, Alignment (Big-Endian/Little-Endian)

ISA governs both hardware implementation (below) and compiler design (up)

Performance Issues

-- CPU-Performance Equation

-- Amdahl’s Law

What Affects Performance?

- Algorithm
  - Determines number of operations executed
- Programming language, compiler, architecture
  - Determine number of machine instructions executed per operation →depends on ISA
- Processor and memory system
  - Determine how fast instructions are executed
- I/O system (including OS)
  - Determines how fast I/O operations are executed

Response Time and Throughput

- Response time
  - How long it takes to do a task
- Throughput
  - Total work done per unit time
    - e.g., tasks/transactions/… per hour
- How are response time and throughput affected by
  - Replacing the processor with a faster version?
  - Adding more processors?
- We'll study their estimation

- **Response time:** time between submission of a job (program P) and its completion (depends on overall system load)

This includes

--- I/O

--- Operating system time for managing programs, compile time, etc.

--- **CPU-time** that includes time for executing the machine code for P, memory access time, procedure calls, and system time spent on P.

- Performance is proportional to the *inverse* of the CPU time.

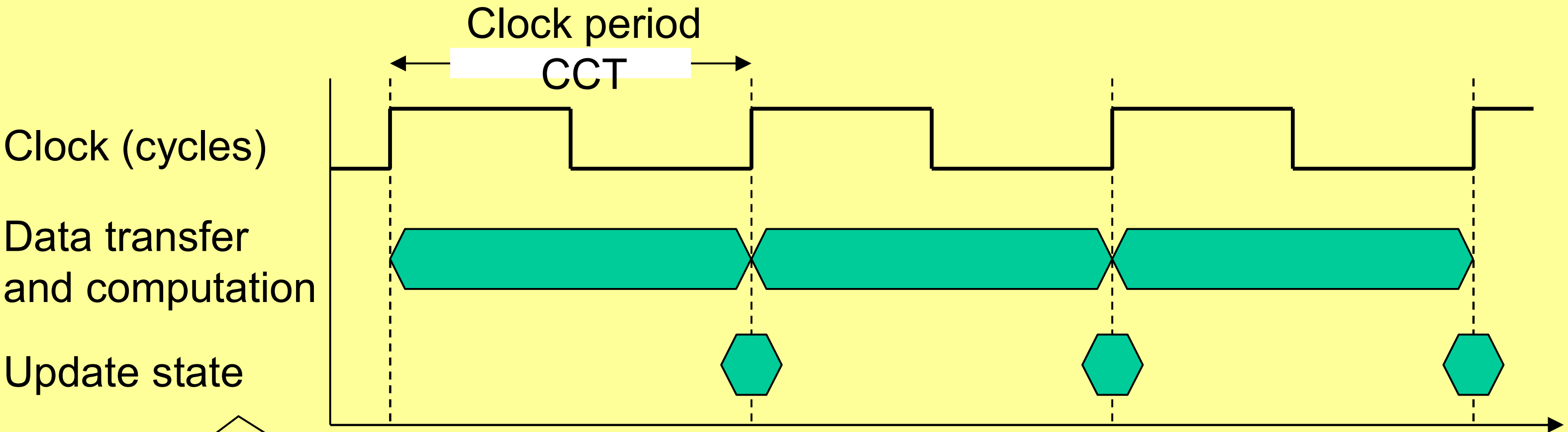
What determines the execution time of a machine/assembly-level program P when run on a machine M?

- P consists of a number of machine-level instructions (IC – instruction count);
- Each machine instruction requires several clock cycles to complete (CPI – average number of clock cycles per instruction);
- Each clock cycle has certain time period (CCT – clock cycle time)

Thus, CPU-time = IC × CPI × CCT

CPU Clocking

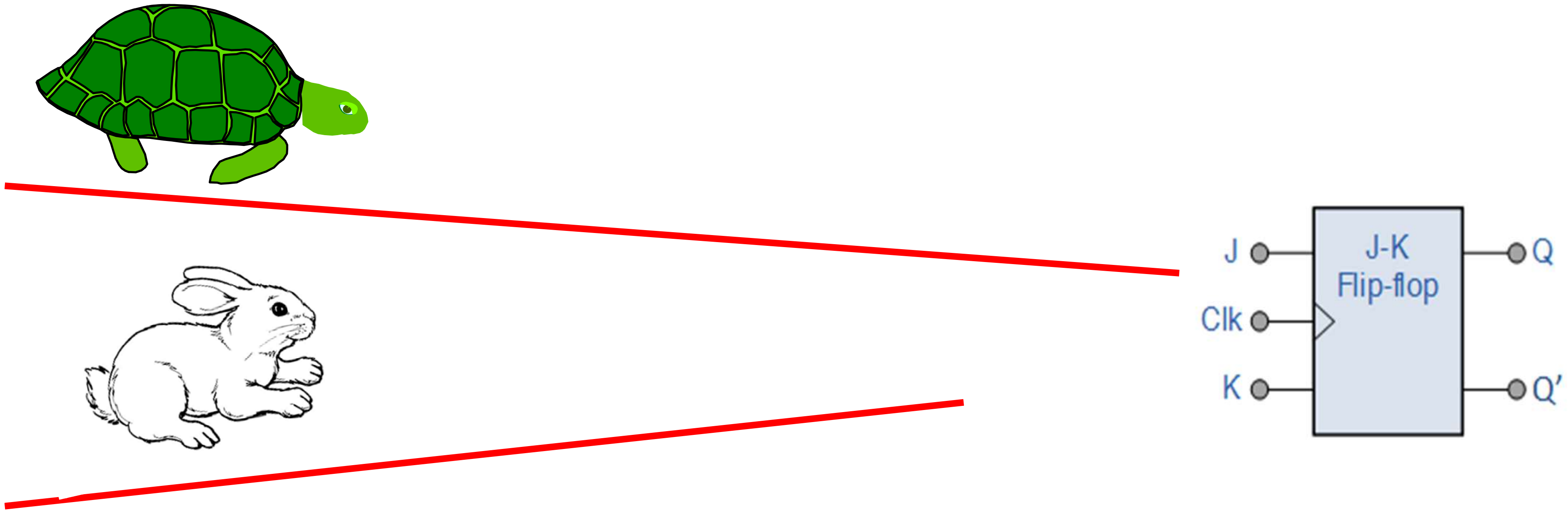
- CPUs are driven by constant-rate system clocks:
  - 100 MHz clock frequency (*f*) means the system clock ticks 100 million times every second:



One Clock Cycle Time ("Tick"), i.e., CCT
= 1/100,000,000 *sec*
=1/100 *microsec* = 10 *nanosec*

CCT = 1/*f*

Clock Timing



Clock period should be large enough to accommodate delays along critical paths in the circuit (longest ones); but not too large – system slows down unnecessarily

CPU Time

$$\text{CPU Time} = \text{CPU Clock Cycles} \times \text{Clock Cycle Time}$$

$$= \frac{\text{CPU Clock Cycles}}{\text{Clock Rate}}$$

- Performance improved by
  - Reducing number of clock cycles
  - Increasing clock rate
  - Hardware designer must often trade off clock rate against cycle count

CPU Time Example

- Computer A: 2GHz clock, 10s CPU time
- Designing Computer B
  - Aim for 6s CPU time
  - Can do faster clock, but causes 1.2 × clock cycles
- How fast must Computer B clock be?

$$\text{Clock Rate}_B = \frac{\text{Clock Cycles}_B}{\text{CPU Time}_B} = \frac{1.2 \times \text{Clock Cycles}_A}{6\text{s}}$$

$$\begin{aligned}\text{Clock Cycles}_A &= \text{CPU Time}_A \times \text{Clock Rate}_A \\ &= 10\text{s} \times 2\text{GHz} = 20 \times 10^9\end{aligned}$$

$$\text{Clock Rate}_B = \frac{1.2 \times 20 \times 10^9}{6\text{s}} = \frac{24 \times 10^9}{6\text{s}} = 4\text{GHz}$$

Instruction Count and CPI

$$\text{Clock Cycles} = \text{Instruction Count} \times \text{Cycles per Instruction}$$

$$\text{CPU Time} = \text{Instruction Count} \times \text{CPI} \times \text{Clock Cycle Time}$$

$$= \frac{\text{Instruction Count} \times \text{CPI}}{\text{Clock Rate}}$$

- Instruction Count for a program
  - Determined by program, ISA and compiler
- Average cycles per instruction
  - Determined by CPU hardware
  - If different instructions have different CPI
    - Average CPI affected by instruction mix

CPI Example

- Computer A: Cycle Time = 250ps, CPI = 2.0
- Computer B: Cycle Time = 500ps, CPI = 1.2
- Same ISA
- Which is faster, and by how much?

$$\begin{aligned}
\text{CPU Time}_A &= \text{Instruction Count} \times \text{CPI}_A \times \text{Cycle Time}_A \\
&= \text{I} \times 2.0 \times 250\text{ps} = \text{I} \times 500\text{ps}
\end{aligned}$$

A is faster…

$$\begin{aligned}
\text{CPU Time}_B &= \text{Instruction Count} \times \text{CPI}_B \times \text{Cycle Time}_B \\
&= \text{I} \times 1.2 \times 500\text{ps} = \text{I} \times 600\text{ps}
\end{aligned}$$

$$\frac{\text{CPU Time}_B}{\text{CPU Time}_A} = \frac{\text{I} \times 600\text{ps}}{\text{I} \times 500\text{ps}} = 1.2$$

…by this much

CPI in More Detail

- If different instruction classes take different numbers of cycles

$$\text{Clock Cycles} = \sum_{i=1}^{n} (\text{CPI}_i \times \text{Instruction Count}_i)$$

  - Weighted average CPI

$$\text{CPI} = \frac{\text{Clock Cycles}}{\text{Instruction Count}} = \sum_{i=1}^{n} \left(\text{CPI}_i \times \underbrace{\frac{\text{Instruction Count}_i}{\text{Instruction Count}}}_{\text{Relative frequency}} \right)$$

CPI Example

- Alternative compiled code sequences using instructions in classes A, B, C

Class	A	B	C
CPI for class	1	2	3
IC in sequence 1	2	1	2
IC in sequence 2	4	1	1

- Sequence 1: IC = 5
  - Clock Cycles
    = 2×1 + 1×2 + 2×3
    = 10
  - Avg. CPI = 10/5 = 2.0

- Sequence 2: IC = 6
  - Clock Cycles
    = 4×1 + 1×2 + 1×3
    = 9
  - Avg. CPI = 9/6 = 1.5

Performance Summary

The BIG Picture: CPU Performance Equation

$$\text{CPU-time} = \text{IC} \times \text{CPI} \times \text{CCT}$$

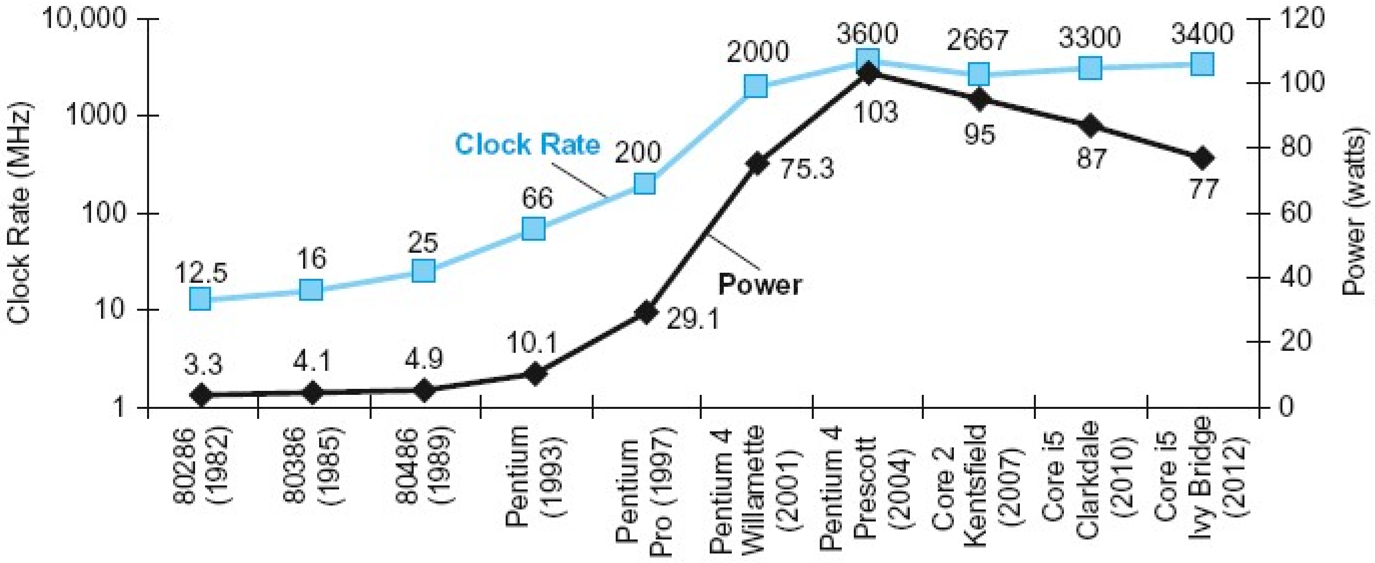
- Performance depends on
  - Algorithm: affects IC, possibly CPI
  - Programming language: affects IC, CPI
  - Compiler: affects IC, CPI
  - Instruction set architecture: affects IC, CPI, CCT
  - CPI is also affected by memory hierarchy, pipelining; CCT is affected by logic design, technology

MIPS as Performance Measure

MIPS = Millions of Instructions per Second

$$= \frac{\text{Instruction Count (IC) of a program P}}{\text{Execution time of P in seconds} \times 10^6}$$

Power Trends



- In CMOS IC technology

$$\text{Power} = \text{Capacitive load} \times \text{Voltage}^2 \times \text{Frequency}$$

×30

5V → 1V

×1000

Reducing Power

- Suppose a new CPU has
  - 85% of capacitive load of old CPU
  - 15% voltage and 15% frequency reduction

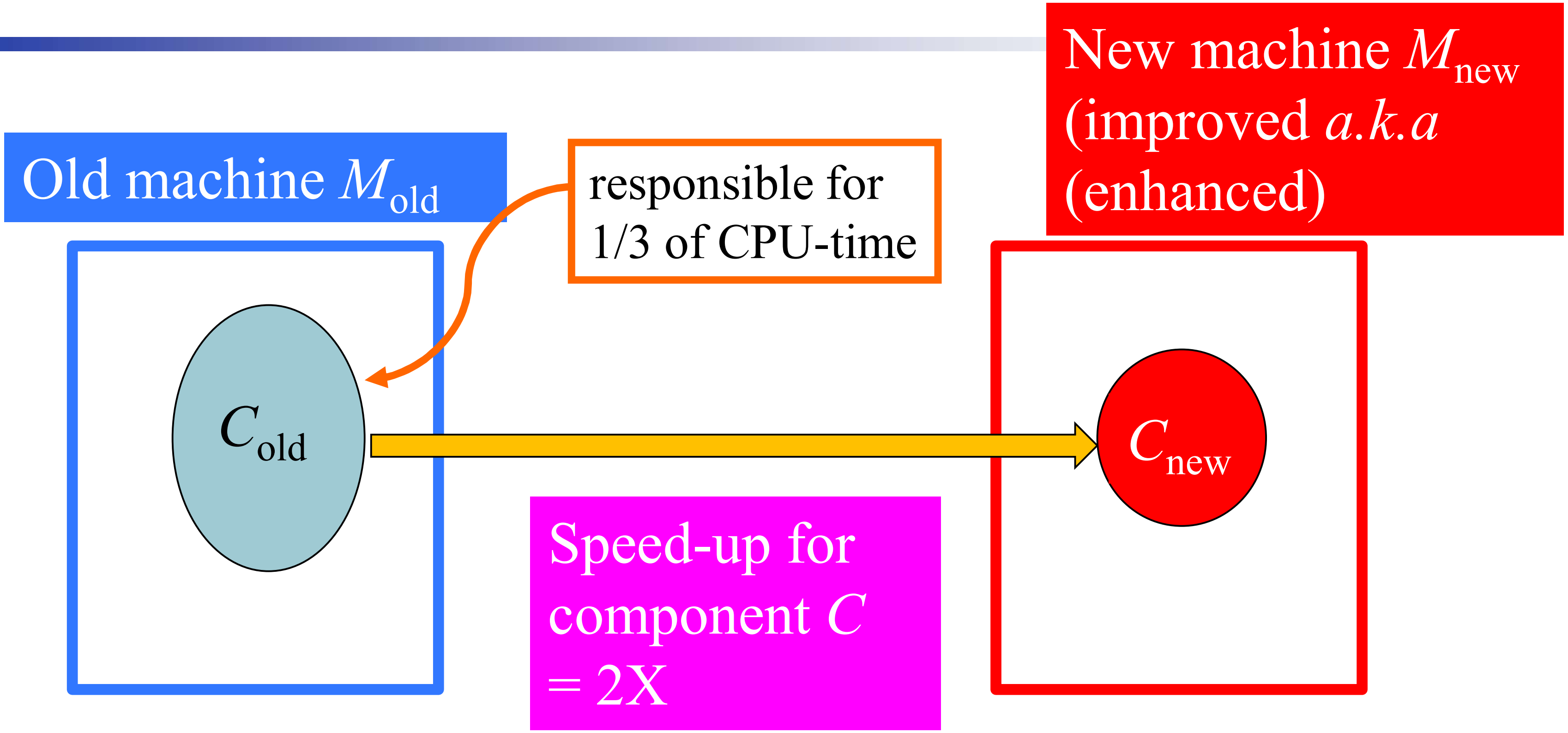
$$\frac{P_{new}}{P_{old}} = \frac{C_{old} \times 0.85 \times (V_{old} \times 0.85)^2 \times F_{old} \times 0.85}{C_{old} \times V_{old}{}^2 \times F_{old}} = 0.85^4 = 0.52$$

- The power wall
  - We can’t reduce voltage further
  - We can’t remove more heat
- How else can we improve performance?

How to enhance performance of a machine by “Enhancement”?

→ Amdahl’s Law

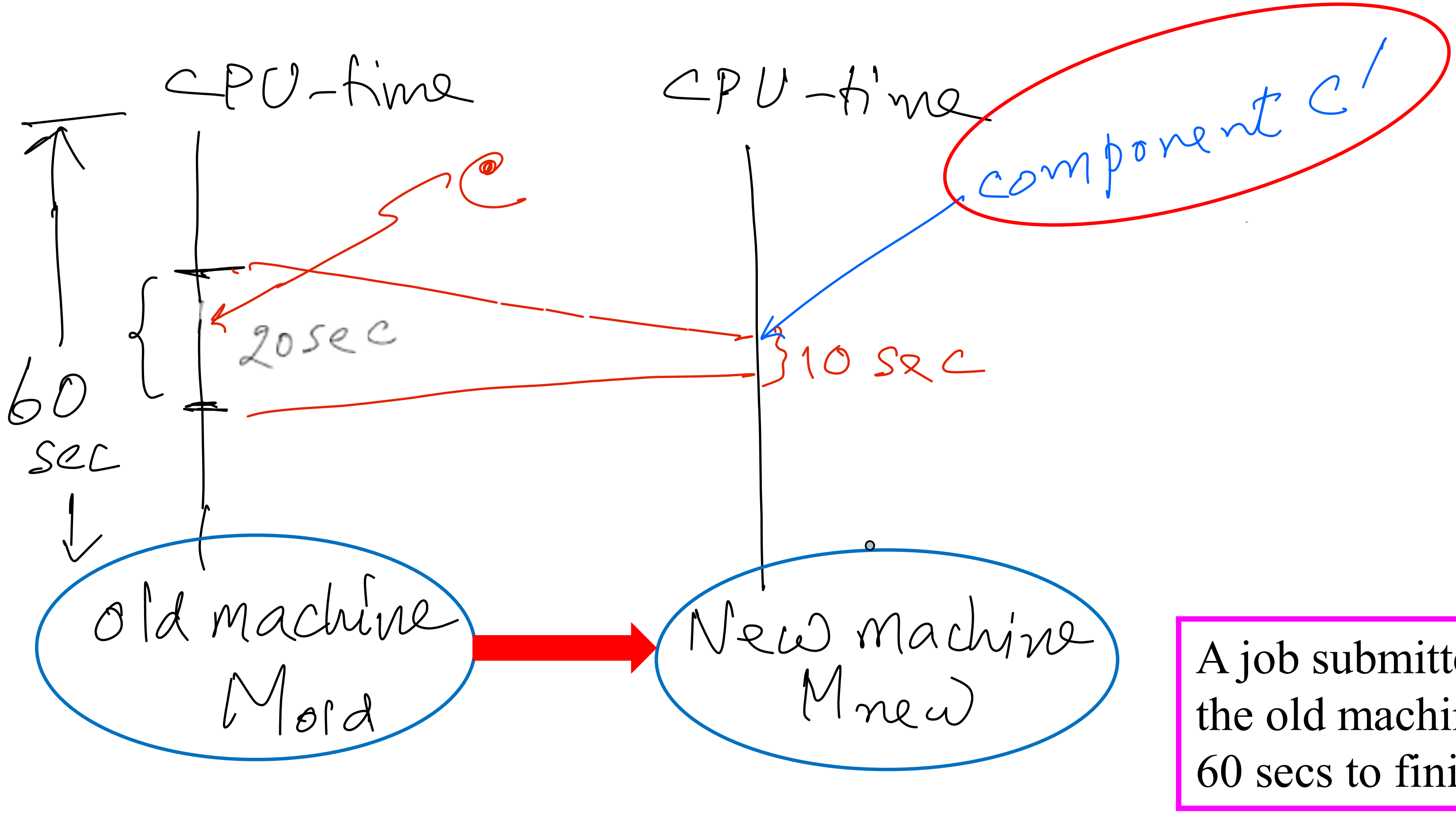
Example: Improving performance in steps


Old machine M_{old}
responsible for 1/3 of CPU-time
New machine M_{new} (improved *a.k.a* (enhanced)
C_{old}
C_{new}
Speed-up for component C = 2X

Question: What is the overall speed-up of M_{new} *w.r.t.* M_{old}?

Gradual enhancement of resources for speed-up

Let C be a component (e.g., adder) of an old machine, which is improved to C' in a new machine

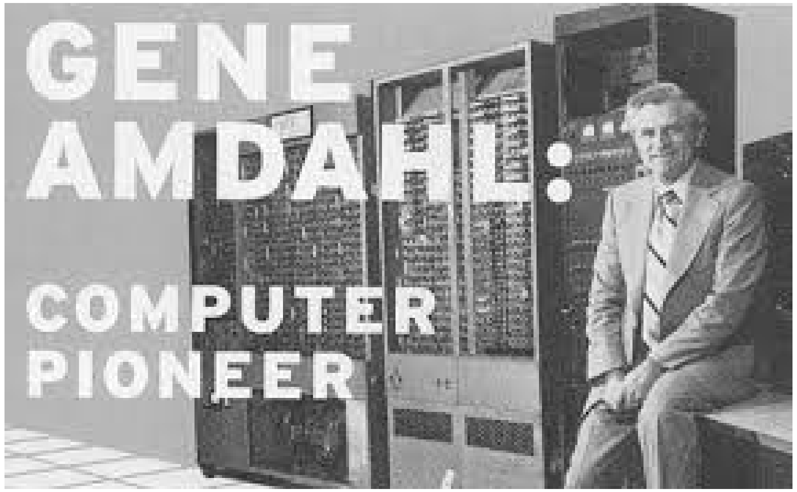


A job submitted to the old machine takes 60 secs to finish

Gradual enhancement of resources for speed-up

Question : What is the overall speed-up ?

The general result concerning the overall speed-up, when a component of the old machine is enhanced is captured in "Amdahl's Law"

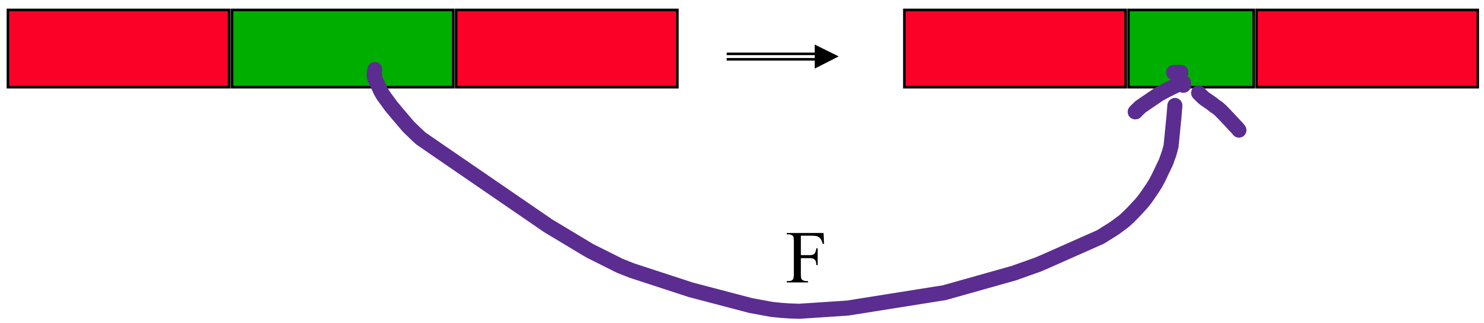


Gene Amdahl
(1922-2015)

Amdahl's Law

Speed-up due to enhancement E:

$$\text{Speed-up}(E) = \frac{\text{CPU-time w/o E}}{\text{CPU-time w/E}} = \frac{\text{Performance w/E}}{\text{Performance w/o E}}$$



Suppose that enhancement E accelerates a fraction F of the task by a factor S, and the remainder of the task is unaffected

Amdahl’s Law

- Law of diminishing return: unaffected fraction will determine the limiting case!
- Improvement of larger fraction will yield higher overall speed-up → Make the common case faster

Example: Amdahl’s Law

- Floating-point (FP) instructions are improved to run 2X in a new machine
- 10% of actual instructions are FP

Example: Amdahl's Law

- Floating-point (FP) instructions are improved to run 2X in a new machine
- 10% of actual instructions are FP

$$\text{CPU-time}_{\text{new}} = \text{CPU-time}_{\text{old}} \times (0.9 + 0.1/2) = 0.95 \times \text{CPU-time}_{\text{old}}$$

$$\text{Speed-up}_{\text{overall}} = \frac{1}{0.95} = 1.053$$

- For FP Speed-up 100X, $\text{Speed-up}_{\text{overall}} = 1.109$

Pitfall: Amdahl's Law

§1.10 Fallacies and Pitfalls

- Improving an aspect of a computer and expecting a proportional improvement in overall performance

$$T_{\text{improved}} = \frac{T_{\text{affected}}}{\text{improvement factor}} + T_{\text{unaffected}}$$

- Example: multiply accounts for 80s/100s
  - How much improvement in multiply performance to get 5× overall?

$$20 = \frac{80}{n} + 20$$

  - Can't be done!

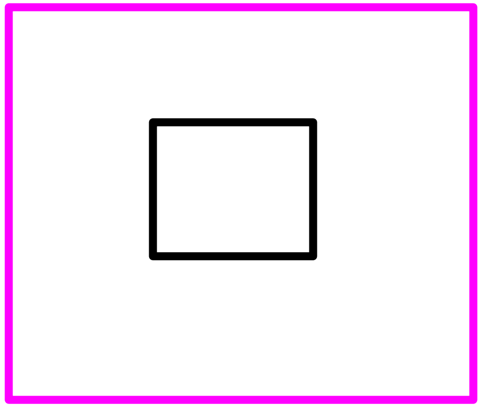
- Corollary: make the common case fast

Multiprocessors

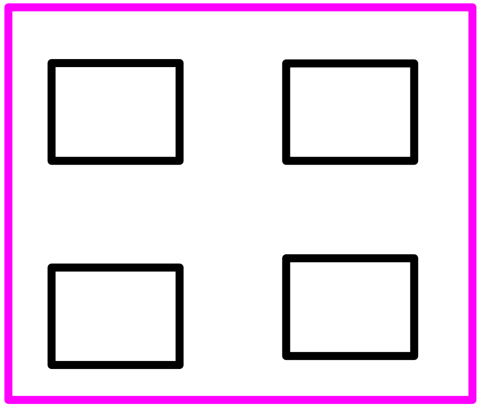
- Multicore microprocessors
  - More than one processor per chip
  - Clock frequency limited
- Requires explicitly parallel programming
  - Compare with instruction level parallelism
    - Hardware executes multiple instructions at once
    - Hidden from the programmer
  - Hard to do
    - Programming for performance
    - Load balancing
    - Optimizing communication and synchronization

Parallelism: Adding multiple processors

Pessimistic view



Single processor



Multi-processor

1. X:= A + B
2. Y:= X * C
3. D:= B + C

Statement 1 & 2 cannot be executed in parallel (serial);
1 and 3 can be executed in parallel;

What kind of *speed-up* is expected?

s: time needed by a single processor on serial parts of *P*;
p: time needed by a single processor on the parts of *P* that can be parallelized; $s + p = 1$
By **Amdahl's Law**, the speed-up in the multi-core processor $= 1/(s + p/N) \Longrightarrow$ If $s = 10\%$, the maximum speed-up is 10X

Parallelism: Adding multiple processors
Amdahl's Law *versus* Gustavson-Barsis Law

By *Amdahl's Law*, the speed-up in the multi-core processor = $1/(s + p/N)$, i.e., it is limited by s, increasing N does not help.

In Amdahl's Law, the size of the job is assumed to be constant; however, multi-cores can solve a large job in the same time. This leads to Gustavson-Barsis Law:

Let s and p represent serial and parallel time on N-core system; The single core processor would take $s + (p \times N)$ to perform the same job P.

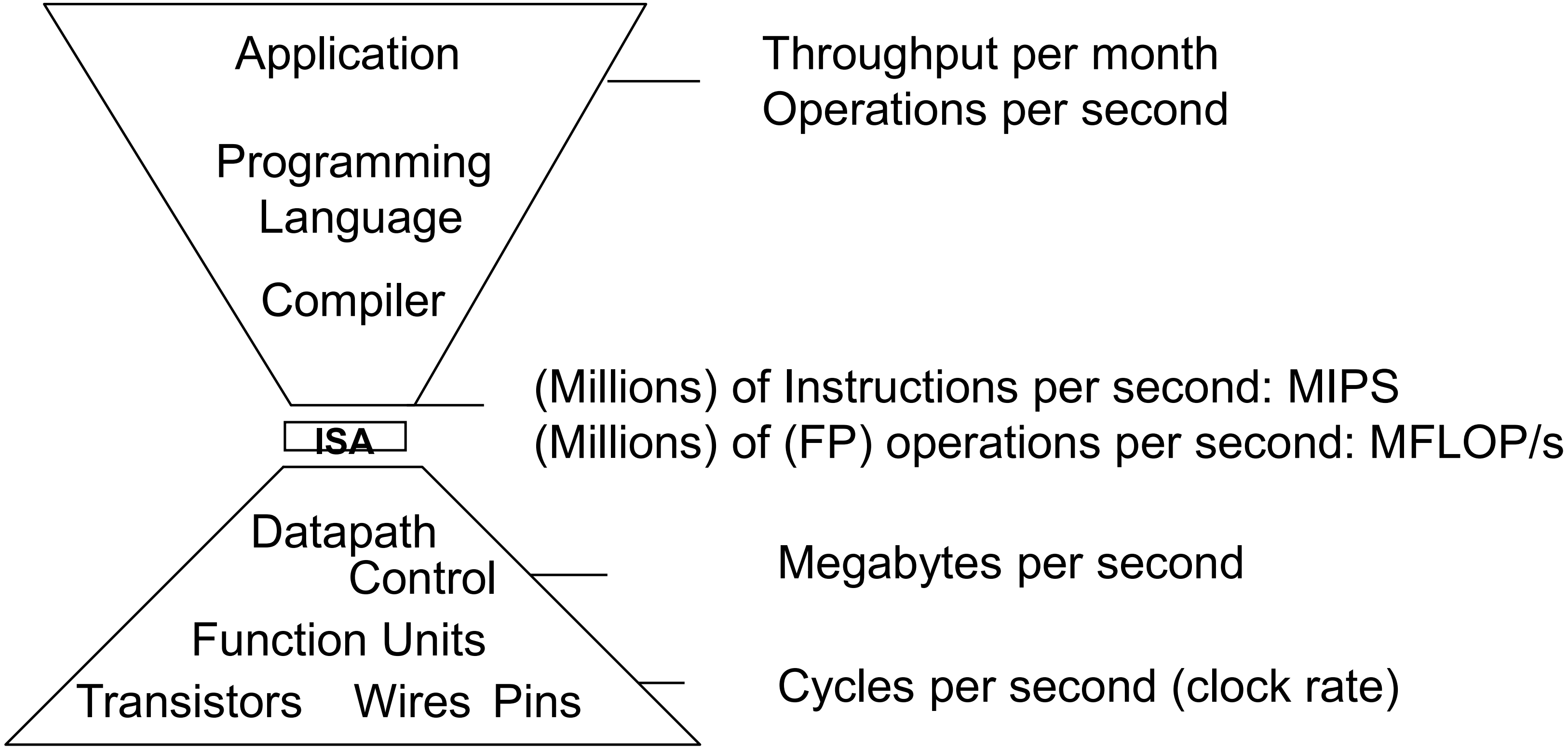
Hence, Speed-up = $(s + (p \times N))/(s + p) = (s + (p \times N))$

Thus, by *Gustavson-Barsis Law*, speed-up **grows** with N

Optimistic view

J.L. Gustavson, Reevaluating Amdahl's Law, *CACM*, M ay 1988

Metrics of Performance



Application

Programming Language

Compiler

ISA

Datapath

Control

Function Units

Transistors Wires Pins

Throughput per month
Operations per second

(Millions) of Instructions per second: MIPS
(Millions) of (FP) operations per second: MFLOP/s

Megabytes per second

Cycles per second (clock rate)

ISA: RISC *versus* CISC

- RISC (Reduced Instruction Set Computing)
  - Keep the instruction set small and simple
  - Fixed instruction lengths
  - Load-store instruction sets
  - Limited addressing modes
  - Limited operations
  - CPI low

  Advantage: makes the hardware simple and fast; decoding simple; pipelining easy

  Performance is optimized focused on software

RISC Example: MIPS, Sun SPARC, HP PA-RISC, IBM PowerPC, Alpha, RISC-V, ARM

- **CISC - Complex Instruction Set Computer**
  - complex instructions
  - different lengths
  - can handle multiple operands
  - complex functionalities

Code size becomes smaller; pipelining becomes harder; compiler design is more involved

- Examples of CISC processors are Intel x86 CPUs, System/360, VAX, AMD

Eight Great Ideas

- Design for ***Moore's Law***
- Use ***abstraction*** to simplify design
- Make the ***common case fast***
- Performance *via* ***parallelism***
- Performance *via* ***pipelining***
- Performance *via* ***prediction***
- ***Hierarchy*** of memories
- ***Dependability*** *via* redundancy

Amdahl's law

Gustavson-Barsis law

§1.2 Eight Great Ideas in Computer Architecture

Concluding Remarks

- Cost/performance is improving
  - Due to underlying technology development
- Hierarchical layers of abstraction
  - In both hardware and software
- Instruction set architecture
  - The hardware/software interface
- Execution time: the best performance measure
- Power is a limiting factor
  - Use parallelism to improve performance

Next Class

-
- Introducing MIPS Assembly Language