**Birla Institute of Technology and Science Pilani , Pilani Campus**
**CS F342 Computer Architecture**
**General Instructions**

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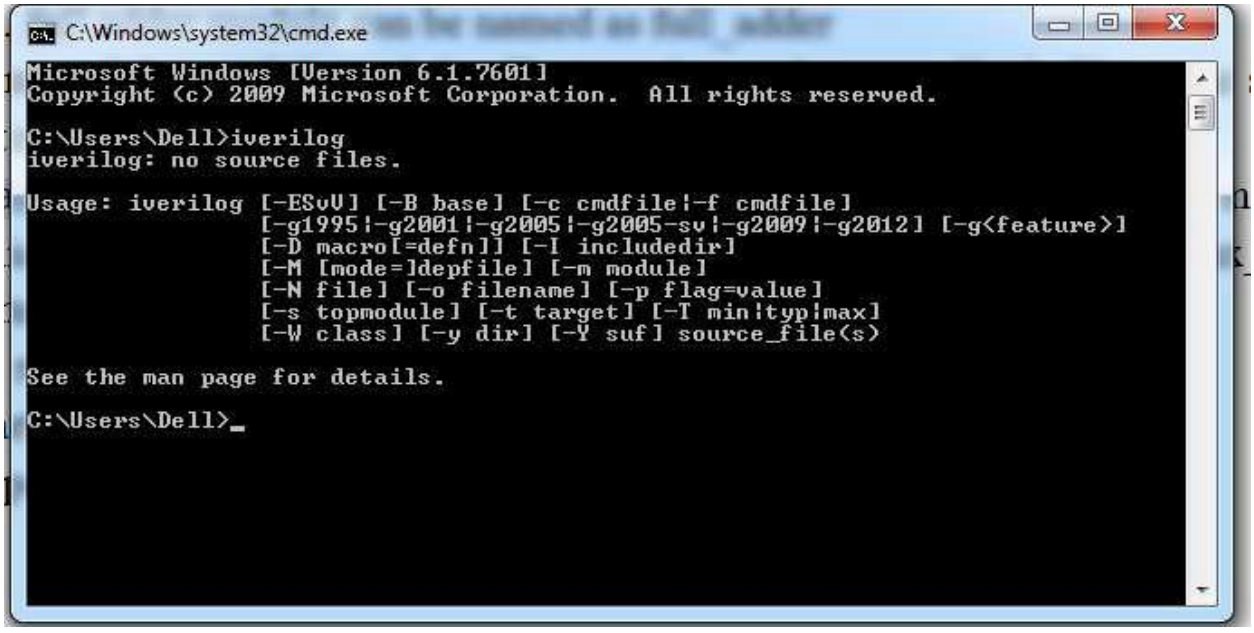
**General Guidelines:**

1. Create a new folder (if it doesn't exist) with the name Computer_Architecture in E or D drive and in that create a folder with your name followed by id no. and save all the codes in them. Ex: if your id is 2014A3PS125P and name Sarath Chandra create a folder with the name sarath_125
2. Use the same system for all the lab sessions. This allows reusability of the codes you have made in the previous lab sessions.
3. Create the input files using note-pad-plus-plus software. The extension for the filename should be .v
4. Have a backup of your work regularly through google drive after every lab.
5. Use only relevant names for each module. Use comment lines wherever necessary
   Ex. full adder module can be named as full_adder
6. Name of the module and the file is to be made same. Each file name should have an extension .v
7. Name of the test bench modules should start with tb_ followed by the module name for which it is being used as a test vector generator. Ex test bench for mux_4x1 should be named as tb_mux_4x1
8. To run icarus verilog you need to go to the command prompt.
   Start - → Run - → cmd
9. Type *iverilog* and press enter. You should see the following screen if the installation is done properly.



10. Change the working directory to the folder you have created in step-1. Ex. to change to E drive in command prompt type E: (press enter)
    *cd Computer_Architecture\name_idno.* (press enter)
11. To simulate any verilog file use the command
    *iverilog –o filename.vvp filename.v*
12. If there are no syntax errors, then you can check in the directory a file filename.vvp will appear.
13. Now use the following command to see the output using $monitor statements. *vvp filename.vvp*
    to exit from the interactive mode type *finish*
14. To see the graphical waveform use the command
    *gtkwave filename.vcd*

**Note :**

1. while using icarus verilog make sure that the following lines of code are added in every test bench. The .vcd file generated goes as an input to a wave form viewer

```
initial
    begin
        $dumpfile("filename.vcd");
        $dumpvars;
    end
```

2. If you want to instantiate any module in any other module then the first line in the new module should have *`include "modulename.v"* ex. the full_adder.v which calls half_adder module which is in file half_adder.v then the full_adder.v should have the line *`include "half_adder.v"* in it. This is exclusive to icarus verilog only.

**Most Common Mistakes in Verilog**

1. All keywords should be in lower case.
2. Upper case and lower case are distinct in verilog, it is case sensitive,
3. Make sure that the wires are properly declared before usage.
4. Unwanted spaces will put you in trouble ex. endmodule doesn't have any space in between.
5. Module declaration is a statement terminate it with a semicolon.
6. Module name can't start with a number and can't have a special charcters in it.
7. The output 'x' indicates that the signal is still unkown and being evaluated.
8. In combinational circuits 'z' in the output means the signals are not connected properly.