

# The Design and Implementation of a Scanning Fabry-Perot Interferometer for Use in Measuring Multiple Modes in Lasers

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**Abstract**—A scanning mirror Fabry-Perot Interferometer (sFPI) was designed, built, and implemented to measure the modes of a laser beam. It has an estimated finesse of 155 and free spectral range of 3.75 GHz with a resolution bandwidth of 24 MHz. A piezoelectric device will change the spacing of the mirrors, allowing scanning across multiple free spectral ranges. A voltage-source driver provides a controllable signal to a piezoelectric device. The spectral frequency content will be captured by a photo-detector and amplified by a trans-impedance amplifier. This can be analyzed one of two ways. Either sent to a micro-controller-computer pair which processes, displays, and stores this data locally on a hard disk, or sampled by an oscilloscope which can take the place of the micro-controller.

**Index Terms**—FSR, sFPI, Python

## I. INTRODUCTION

The current sFPI (Spectra-Physics SP-470-06) is bulky and requires various appendages in order to operate. It requires a separate photodiode and data collection device (i.e. oscilloscope). This makes it cumbersome to use. The new model has been constructed to reduce the overall real estate and make the operation more user friendly. It has a pre-installed photodiode as well as an integrated application which communicates directly with an on-board micro-controller to process and display the spectral content of the cavity. The computer application increases the functionality of the device by calibrating the incoming signal based on user input of the free spectral range of the cavity which prompts the application to mathematically scale the output for analysis. While the newly development sFPI seems to be superior to the other it has its disadvantages. The frequency of the driver is only 2.35 Hz, making it much slower than real-time analysis. It also requires more than one individual to design and build all of the necessary components to make the design successful.

## II. BACKGROUND

In order to understand how the sFPI works, a fundamental principle must be explained. In its static state, a cavity<sup>1</sup> can hold a specific number longitudinal modes, proportional to the length of the cavity ( $L$ ). Verheyen's book on laser electronics gives an adequate definition for a cavity mode:

A cavity mode is a field distribution that reproduces itself in relative shape and in relative phase after a round trip through the system [6]

Each mode has an order of the form  $(m,n,q)$ , where  $m$ ,  $n$ , and  $q$  are integers. The transverse modes are represented by  $m$  and  $n$ , and the longitudinal modes are represented by  $q$ . Typically only the  $TEM_{0,0,q}$  modes are examined because it makes the math easier, however higher order transverse modes are prevalent in the system. For our purposes we will only be examining the longitudinal modes. However, when the length of the cavity changes ( $\Delta L$ ), so does the orders of the modes which can occupy length  $L + \Delta L$ . In order to achieve a maximum transmission,  $\Delta L$  must be on the order of a wavelength, corresponding to a  $q+1$  increase in the mode order. Any other change in length ( $\Delta L$ ) not on that order will result in little to no transmission of the cavity beam. The separation of the maximum transmission peaks is defined as the free spectral range (FSR) and can be expressed by  $FSR = c/2L$ , where  $c$  is the speed of light in a vacuum. The FSR is described by a frequency, however it can also be related to spacial frequency as well. Figure 1 graphically describes the free spectral range.

Since this is not a perfect cavity, the photon-lifetime is described by an exponential decay rate,

<sup>1</sup>Define what a cavity is

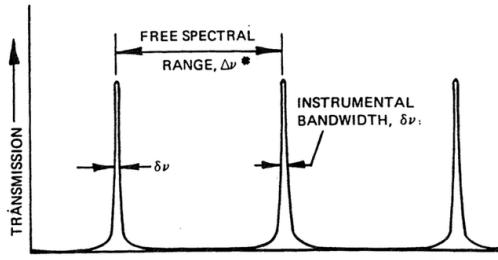


Figure 2-2 Transmission vs. Frequency of a Fabry-Perot Interferometer

Fig. 1. Spectral Frequency Content of a sFPI [4]

$e^{-t/\tau}$ . The line shape of the cavity, which has the shape of a Lorentzian, is the Fourier transform of the photon-lifetime. The line shape is the transmission intensity of the deviations of frequencies from the fundamental. The full-width at half maximum of the line shape is the bandwidth of the cavity. Typically bandwidth is not expressed, but rather the finesse of the cavity. The finesse is defined as the ratio of the free spectral range to the bandwidth of the cavity (Eq. 1).

$$\mathcal{F} = \frac{\pi}{2\sin^{-1}(1/\sqrt{F})} \quad (1)$$

The finesse is related by a factor defined as the coefficient of finesse ( $F$ ) which is proportional to reflectivity of the mirrors used (Eq. 2).

$$F = \frac{4R}{(1-R)^2} \quad (2)$$

Dielectrically coated mirrors with high reflectivity, at the principle wavelength, are used to increase the finesse and overall performance of the Fabry-Perot cavity. The reflectivity of these mirrors is typically  $> 90\%$ . Since the reflectivity is greater than 50% the simplified Eq. 3 can be used to approximate the finesse. This is because at small values of  $x$  for  $\sin^{-1}(x)$  the relationship is 1 to 1.

$$\mathcal{F} = \frac{\pi R^{1/2}}{1-R} \quad (3)$$

We have discussed what happens when we change the length of the cavity, but we must further dive into the movement of the cavity. The length of the cavity must be on the order of the principle wavelength to achieve resonance. Thusly, a position change of one wavelength will constitute resonance

in the cavity. This insinuates that  $\Delta L = n\lambda$ , where  $\lambda = 632.8\text{nm}$ . A piezoelectric device (PED) can generate a  $\Delta L$  of that magnitude. While other forms of precision motion control can be used (i.e. pressurized air), a PED's real estate is ideal for the application. A PED's deformation is directly proportional to the electric field applied across it and is related by the following equation, where  $x$  is the strain of the PED,  $d_{33}$  is the piezoelectric strain constant, and  $E$  is the applied electric field [5].

$$x = d_{33}E \quad (4)$$

Since strain ( $x$ ) is the ratio of the change in length by the length ( $\Delta L/L$ ) of the material and the applied electric ( $E$ ) is the ratio of the applied voltage ( $V$ ) to the length ( $L$ ) over which it is applied ( $V/L$ ), Equation 4 can be expressed as  $\Delta L = d_{33}V$ , directly relating the change in length to the change in applied voltage [5]. For our applications a saw-tooth voltage signal will be applied across the PZT. This will allow for scanning of the mirrors through the modes of the resonant cavity by systematically controlling  $\Delta L$  for reproducible output.

The transmission intensity resulting from the scanning of the cavity by means of the PZT is incident on a photodiode. Photodiodes have a unique characteristic where light incident upon the semiconductor ( $h\nu$ ) produces a current. This can be done in the photo-voltaic or photo-conductive regions of operation; however, the photo-conductive region, which operates in reverse bias, has a much higher responsivity. The responsivity of a photodiode ( $R_\lambda$ ) is the ratio of current ( $I_{P_n}$ ) in amperes to the incident power ( $P_n$ ) in watts, where  $n$  is an integer describing the different levels of incident power (Fig. 2). The responsivity can be calculated by Equation 5, where  $\eta$  is the quantum efficiency,  $h$  is Plank's constant,  $\nu$  is the frequency of the light, and  $e$  is the elementary charge (Eq. 5).

$$R = \eta \frac{e}{h\nu} \quad (5)$$

A trans-impedance amplifier can be implemented to convert the current signal into a voltage signal making it quite easy to collect the resulting data using an analog-to-digital converter. However, since the analog-to-digital converter has a limit on the conversion rate, the frequency of the PZT must match this rate to achieve maximum resolution.

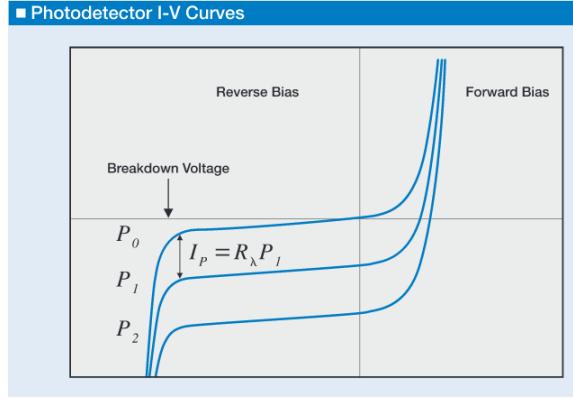


Fig. 2. Photo-conductive Diode Curve [3]

### III. sFPI DESCRIPTION

The scanning Fabry-Perot interferometer as discussed in Section II has three main design components: the optical design, the mechanical design, and the electrical design. The cavity design was chosen based on the typical construction for a Fabry-Perot interferometer. The mechanical design was designed for simplicity, with the majority of construction done by a 3D printer. The electrical design was based on the operation of the Spectra Physics Scanning Interferometer Driver which consisted of a signal generator with the ability to tune the amplitude of the signal. This was coupled with a analog-to-computer interface to sample the output of the cavity through a photodiode.

### IV. OPTICAL DESIGN

The optical design component, as illustrated in the block diagram, is a Fabry-Perot interferometer. This resonant cavity consists of two spherical mirrors with a radius of curvature equal to  $40 \text{ mm} \pm 2 \text{ mm}$ . In order to have a stable cavity the following equation applies.

$$0 \leq \left(1 - \frac{L}{R_1}\right) \left(1 - \frac{L}{R_2}\right) \leq 1 \quad (6)$$

Given that  $R_1 = R_2 = 40 \text{ mm} \pm 2 \text{ mm}$ , the range of the length of the cavity ( $L$ ), for a stable resonator, is:

$$0 \leq L \leq 40 \text{ mm} \pm 2 \text{ mm} \quad (7)$$

The surface of the mirrors are coated with a dielectric material, which has a reflectivity ranging from 99.4–99.8% for 632.8 nm light. The finesse of

this cavity, as explained in Section II, is expected to be within the range of 522 – 1569 for the respective reflectivity. The resonant cavity for the device is represented in Figure 3.

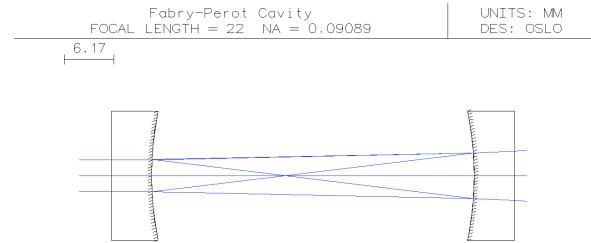


Fig. 3. The resonant cavity is comprised of two dialectically coated spherical mirrors, which reflect 632.8 nm light with 98% reflectivity

A 75 mm PCX lens, minimizing spherical aberrations, is used to couple the system and account for any misalignment (Figure 4). By adding in the auxiliary lens the spot size of the output is decreased as well as the divergence angle of the Gaussian beam leaving the cavity. This allows more of the cavity to be used, increasing the photon-lifetime of the cavity. Figures 5 and 6 show the direct improvement of adding in an auxiliary lens to the system. This is done assuming a confocal resonant cavity with the focal point of the auxiliary lens matching the center of the resonant cavity.

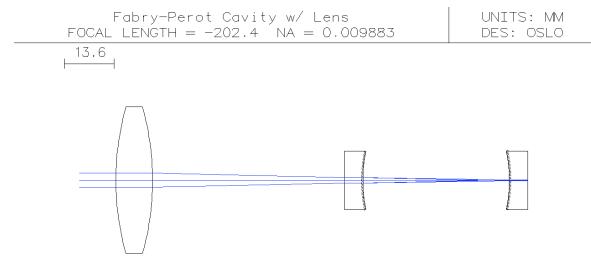


Fig. 4. The auxiliary lens couples the incoming beam to the resonant cavity by increasing the photon-lifetime of the cavity

### V. MECHANICAL DESIGN

The first surface mirror is mounted in a milled disk which is counter sunk, to keep the mirror from falling out (see Figure 7). This is held in place by a set screw.

The second surface mirror is attached to the piezoelectric device, which is described in more detail in the next subsection. This is done by the clear adhesive Gorilla Glue. The piezo-mirror combination is mounted to a plastic appendage

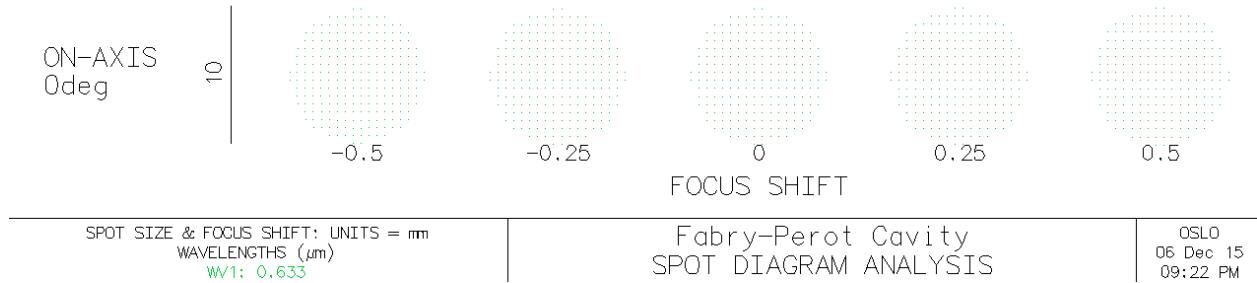


Fig. 5. The spot size of the light exiting the resonant cavity after 1 pass

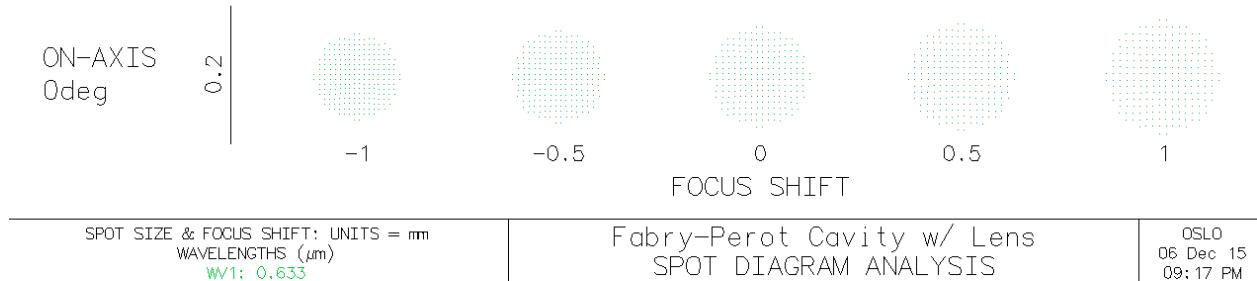


Fig. 6. The spot size of the light exiting the resonant cavity after 1 pass with an auxiliary lens of 75 mm focal length

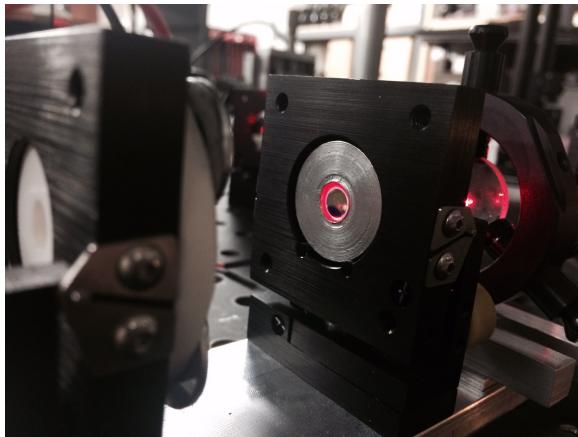


Fig. 7. Milled Disk for first surface mirror

(Figure 9). When properly aligned, this plastic appendage is designed to keep the limiting aperture within the cavity. It is designed such that 4 washers hold the Piezo-Mirror combination in place, without grounding the plates, and so that it fits inside the adjustable mounts (see Figure 8).

The entire cavity is held in place by dual-axis adjustable mounts for aligning purposes (See Figure 11). These are attached to an aluminum base with adjustable distances between the mirrors (Figure 10).

The photodiode is mounted on the back of

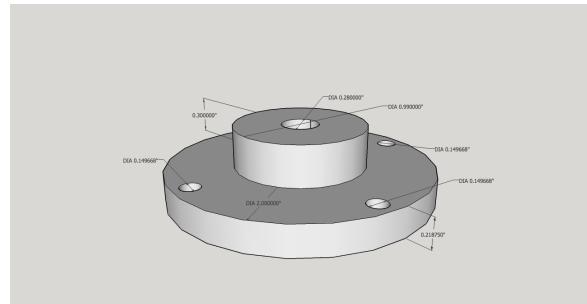


Fig. 8. Piezo-Mirror Holder

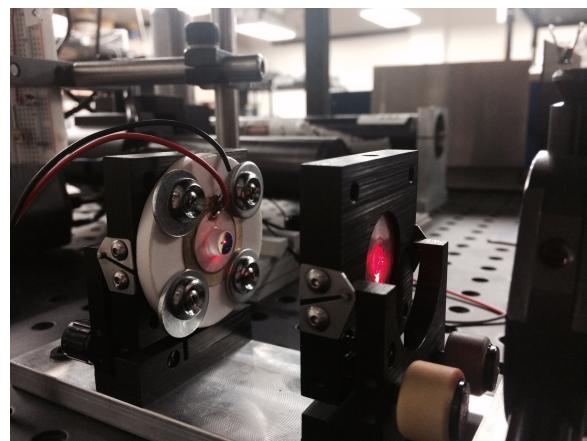


Fig. 9. Piezo-Mirror Holder Dimensions

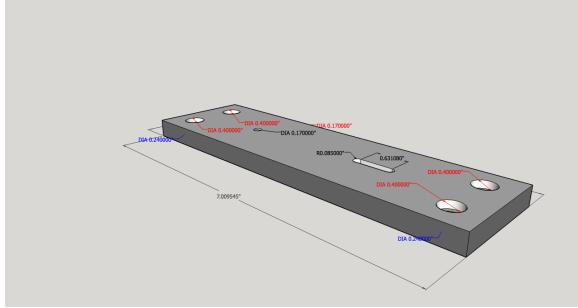


Fig. 10. Aluminum base for the sFPI cavity system. Full layout drawings with measurements can be found on page 11

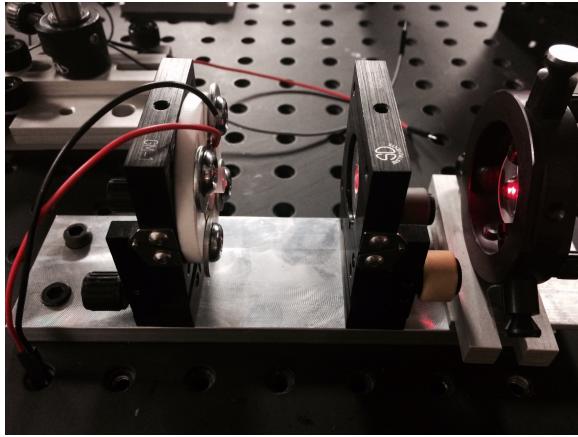


Fig. 11. Adjustable mounts for entire cavity setup

the adjustable mounts by the specially made holder (Figure 12). A set screw is taped post-3D-print in order to secure the photodiode. This is done with a 4-40 drill and tap for a 4-40 set screw.

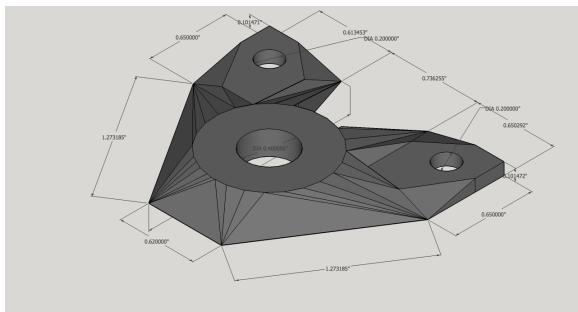


Fig. 12. The mounting device for the photodiode with all measurements and outlays specified on page 12

## VI. INTERFEROMETER DRIVER DESIGN

## A. Piezo-Electric Device

As stated in the previous sections, when a voltage difference is applied across a piezoelectric device a deformation occurs. This results in an

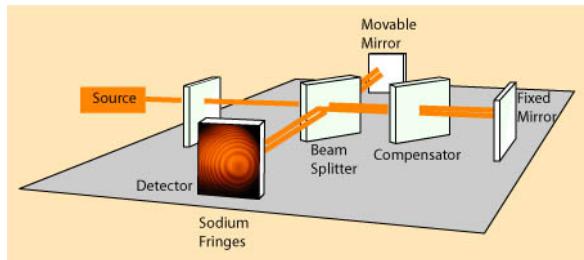


Fig. 14. Michelson Interferometer used for precisely measuring the change in distance of the piezoelectric device per voltage differential placed across it [1]

overall change in length ( $\Delta L$ ) of the piezo. In order to properly design the function generator, which will be driving the PZT, a Michelson Interferometer was constructed (see Figure 14) to determine the strain coefficient of the material.

The PZT was supplied with an adjustable voltage supply ranging from 0-30V. When cycling from 0 to 30 V, seven individual fringe movements occurred. The distance moved was calculated to be:

$$d = \frac{m\lambda}{2} = 2.2\mu\text{m} \quad (8)$$

Where  $\lambda$  is the wavelength of the light (632.8 nm) and  $m$  is the number of fringe changes observed. This resulted in the piezoelectric strain constant ( $d_{33}$ ) equivalent to 73nm/V. With a voltage scan from 0-30V will produce roughly 3.5 free spectral ranges when used in the sFPI. Based on this data, the PZT is adequate for this application.

### *B. Function Generator*

The micro-controller for the driver setup is constructed using an Arduino UNO (see Data Sheet on page 113). The Arduino UNO has firmware in which it communicates with a MCP4725 (see Data Sheet on page 109) 12-bit Digital-to-Analog Converter (DAC) via the I2C communication protocol (see Figure 15).

The DAC attenuates the +5V 10% voltage supply from the Arduino UNO with  $2^{12}$  individual output values. A peak-to-peak sawtooth voltage signal is the result, with a bit resolution of 1.2 mV/bit at a frequency of 2.5 Hz (see Figure 16). The MCP4725 signal-generator acts as a near-perfect voltage source with a series impedance of  $1\Omega$  when in normal operations. This will not affect input resistances for the analog design.

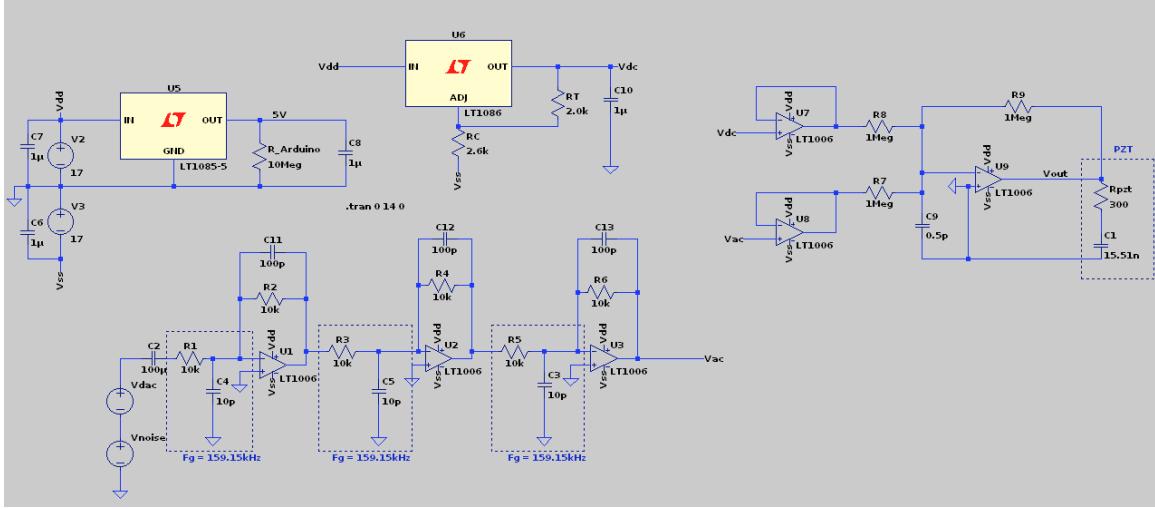


Fig. 13. The three-stage negative feedback amplifier configuration provides a range of 0.2 V/V up to 7.716 V/V of amplification to the input signal by changing resistors R3 and R5 from  $3.6\text{ k}\Omega$  to  $10\text{ k}\Omega$ .  $V_{DD}$  and  $V_{SS}$  are the respective positive and negative voltage rails +17V and -17V. For more clarification the full LTSpice model is Figure ?? in Section ??

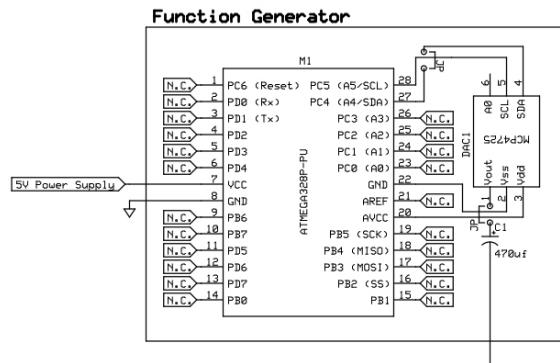


Fig. 15. Function generator design

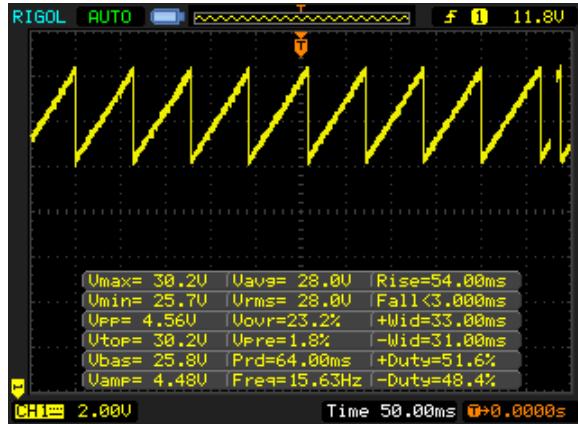


Fig. 16. The output of the MCP4725 DAC from the I2C communication with the Arduino which has 4096 individual steps from  $0 - 5 \pm 10\%V$

### C. Analog-Amplifier Circuit

The sawtooth waveform is sourced to a three-stage negative feedback amplifier, using LT1006

OpAmps, configuration (Figure 18). The amplification ( $A_v$ ) is adjustable from 0.1V/V up to 9V/V. This is done through three stages: the dispersion stage and the two magnitude stages. The dispersion stage allows for small adjustments, 0.1x to 1x of the original signal based on  $R_{in,min} = 10\text{k}\Omega$  and  $R_{in,max} = 50\text{k}\Omega$ . The magnitude stage allows for roughly 1x to 3x of the original signal based on  $R_{in,min} = 3.6\text{k}\Omega$  and  $R_{in,max} = 10\text{k}\Omega$ . Resistors R1, R2, and R3 are representation a resistor in series with a potentiometer. R1 is a  $10\text{k}\Omega$  resistor in series with a  $100\text{k}\Omega$  potentiometer. R2 and R3 are simply a  $3.3\text{k}\Omega$  resistor in series with a  $10\text{k}\Omega$  potentiometer. This was done for simplicity as the precision of the range was not a high priority.

The overall gain ( $A_v$ ) is adjustable because of these resistors and is governed by Eq. 9.

$$A_v = (R_f)^3 \left( \frac{1}{R_1} \right) \left( \frac{1}{R_2} \right) \left( \frac{1}{R_3} \right) \quad (9)$$

A LTSpice Netlist program was developed (see code on page ??). This provided the expected output of the signal given a specified input signal. This input signal is generated by a python-shell script which generates a PWL file for LTSpice based on a series of user inputs (see code on page ??).

This is sourced to a buffer which uses a single LT1006 (see Datasheet on page ??) operation amplifier. This gives the AC signal an infinite output impedance, preventing impedance mismatching. Figure 17 denotes the circuit construction.

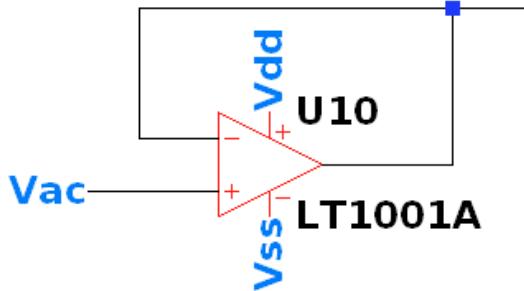


Fig. 17. The voltage follower (unity buffer amplifier) configuration for an OpAmp for circuit isolation and prevention of impedance mismatching.

To change the offset biasing of the sawtooth voltage signal an NTE957 (see Datasheet on page 101) adjustable DC voltage regulator is added using a summation circuit to the AC signal with the following configuration (Figure ??).

#### D. Power Distribution

A VELLEMAN PSINO2512N 12-VOLT 25-WATT DC SWITCHING POWER SUPPLY (see Datasheet on page ??) was complimented with a DROK Micro Electric DC/DC Boost Converter LM2577 Step-up Voltage Transformer (see Datasheet on page ?? for specifications of the DROK component and on page ?? for the LM2577 data sheet) to provide the power to the system. A LT1129 5 VDC  $\pm 1\%$  fixed voltage regulator (see Datasheet on page 99) and an MAX737 inverting buck-boost converter (see Datasheet on page ??).

The 12VDC PSIN02512N voltage supply is sourced to LM2577, boosting the voltage to 17 VDC. The 17 VDC is sourced to the LT1129 5-VDC producing +5 volts supplying power to the boot-loaded Arduino and the MCP4725 DAC.

Since the design calls for a signal with a max peak-to-peak voltage of approximately 34V, the rails must have a range +17 VDC to -17 VDC. Since the constraint that  $V_s - V_{out} \leq 22V_DC$  holds for the buck converter, if the 5VDC rail is used,  $V_{out_{max}} = -17V$  [?]. This is achieved by using values for  $R_3 = 82 k\Omega$  and  $R_4 = 1.06 M\Omega$  (Figure ??).

The current design of the board, which will be discussed later in this section, was simulated in LTspice for power consumption calculations. The

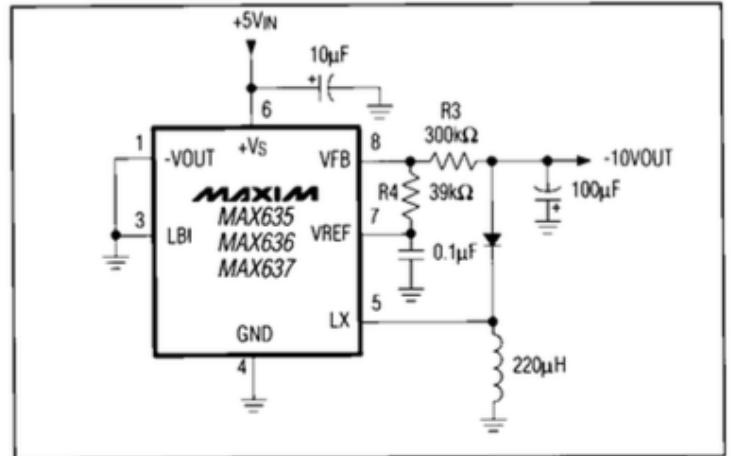


Figure 3. Adjustable Output Operation

Fig. 19. Adjustable Output Operation [?]

negative power supply was sinking 22.69 mA of current. In order to calculate the range of inductance and capacitance necessary for operations Eqs 10 and 11 were used.

$$L_{min} = \frac{(1 - D)^2 * R_{min}}{2 * f} \quad (10)$$

$$C_{min} = \frac{D}{R_{min} * f * v_r} \quad (11)$$

Where  $D = \frac{V_o}{V_o + V_s} = 0.77$  (duty cycle),  $f = 50\text{kHz}$  (switching frequency),  $R_{min} = 850\Omega$  (maximum load resistor), and  $v_r = 0.01$  (ripple voltage). The minimum inductance was found to be  $440\mu H$  and the minimum capacitance was found to be  $1.82\mu F$ .

#### VII. ANALOG DATA CONVERSION PROCESSOR

The photodiode is mounted to an adjustable plate at the rear of the sFPI for calibration, for maximum transmission of the spectral content. The photodiodes resulting current is reverse biased by an Arduino UNO (#2), which is supplying the 5V. Based on the IV curve of the photodiode, the voltage stays within the photo-conductive range while remaining far enough away from the breakdown voltage.

A recent Ph.D. thesis details the quantum efficiency of doped GaAs being between 30% and 22% [2]. This means at 632.8 nm a good approximation for the responsivity is 154 mA/W. The incident

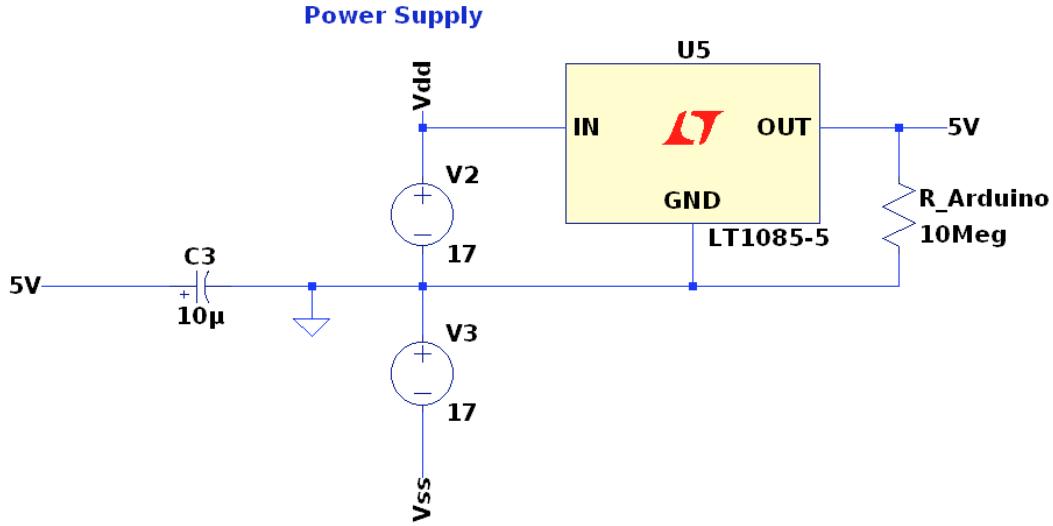


Fig. 18. The three-stage negative feedback amplifier configuration provides a range of 0.2 V/V up to 7.716 V/V of amplification to the input signal by changing resistors  $R_3$  and  $R_5$  from  $3.6\text{ k}\Omega$  to  $10\text{ k}\Omega$ .  $V_{DD}$  and  $V_{SS}$  are the respective positive and negative voltage rails +17V and -17V. For more clarification the full LTSpice model is Figure ?? in Section ??

power on the detector can be approximated based on the losses in the cavity. Section IV explained that the reflectivity of the mirrors was between 99.4% – 99.8%. From this the transmitted power of the beam can be calculated for one pass through the cavity:

$$P_{out} = T_1 T_2 * P_{in} \quad (12)$$

Given the ranges for reflectivity given above, that  $T = 1 - R$ , and  $P_{in} = 3\text{mW}$ , the output power of the cavity was found to be  $P_{max} = 0.108\mu\text{W}$  and  $P_{min} = 120\text{nW}$ . With an optical output of approximately  $1\text{ }\mu\text{W}$  results in a current of roughly  $0.154\text{ }\mu\text{A}$ . However, sound this might be it is wrong! This could be due to the photodiode not being consistent with the model or that my measurement of the optical power was incorrect. Whatever the case may be the diode current was experimentally determined to be roughly  $1\text{nA}$ .

A trans-impedance negative-feedback amplifier with a voltage booster (TAV) converts the AC-current signal to a AC-voltage signal, which uses a AD8672 (see Datasheet on page ??), The voltage gain of this amplifier setup is adjustable for tuning the sFPI, when the signal-to-noise ratio is small, to increase the intensity of the output of the cavity (Figure ??). This corresponding output is sampled

by an analog-to-digital converter (ADC). Since the Arduino, the micro-controller used for storing the data, uses a prescaler of 128, the ADC clock speed is set at 125 kHz. Given that it takes 13 ADC clocks for a conversion the ADC can sample data at a rate of 9615 Hz. Since our we have 4096 individual steps, to match the rate of the ADC a frequency of 2.35 Hz in used for the driver.

## VIII. DIGITALLY ANALYZED OUTPUT

The content captured by the ADC (Figure ??) is transmitted to a computer to process, display (by a graphical representation), and stores the data by user command.

### A. ADC-Computer Interface

The voltage signal from the TAV is sampled by the Arduino Uno, as discussed in Section VII. This is converted to a 512 byte array. The array is then encoded to send to the computer upon request (see code in Section B-B).

### B. Data Analysis

This data will be combined in conjunction with the 5V sawtooth signal to plot the photodiode signal as a function of the geometrical change of the resonant cavity, which is proportional to the wavelength

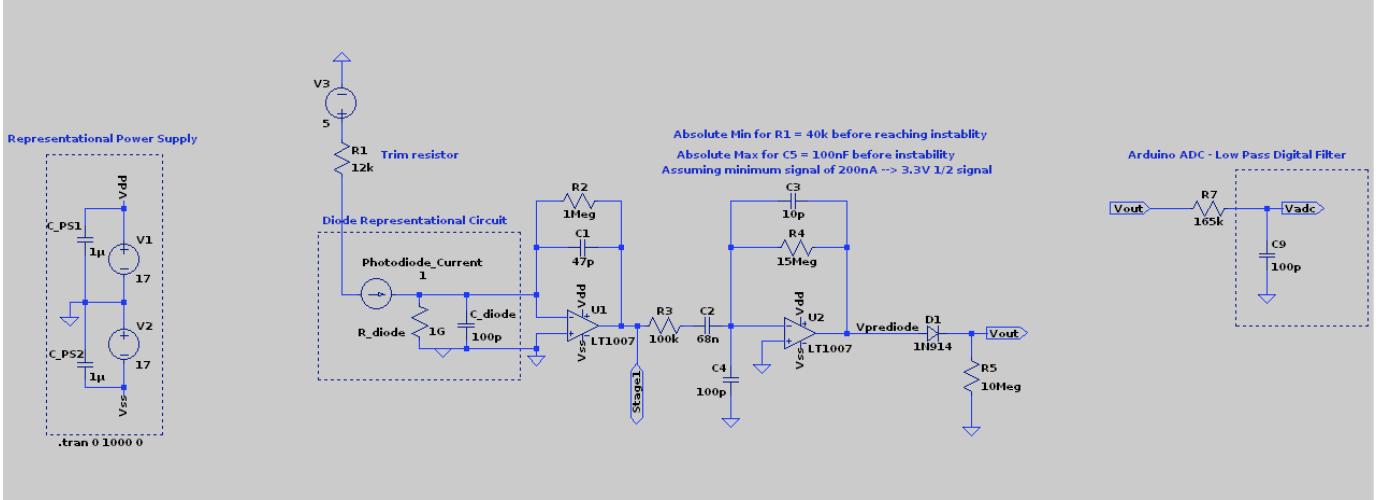


Fig. 20. Transimpedance amplifier design

of the light. This will be done via a GUI model with a language that possesses the capability for universal interfacing. Python will be the base model for programming; however, other languages will be tested for user interface and compared based on speed, cross-platform configuration, and simplicity.

## IX. DISCUSSION AND CONCLUSION

While the project in whole was not finished, the crucial parts of the design were completed as well as the optical and mechanical construction of the cavity and the sFPI driver. The resonant cavity was successfully integrated with mechanical design using adjustable mounting brackets and CNCed aluminum based and 3D printed parts. This allowed the user to align or misalign the cavity as desired. The mirrors can be separated from 18mm to 50mm  $\pm$  3mm. The construction of the sFPI driver was successful on the second iteration of the design. The result being a sawtooth waveform output with amplitude ranging from 500mV to 32V and a DC offset ranging from 0 to 32V  $\pm$  2V. The third design iteration was not constructed, but the design was complete. It eliminated noise issues by creating a bandpass filter of the system.

## X. ACKNOWLEDGMENTS

I could not have had the success I did without the help of my professors' and academic colleges. Thanks go out to Dr. Scott Prahl for mentoring me on this project as well as suggesting the idea to me. I would like to thank the Optoelectronics program

at OIT for making this project possible by providing all of the necessary parts that I needed for prototyping and construction. Thanks to Brandon Clarno for providing me with precision milling of the designs I provided him. He was instrumental in bringing the aluminum base to life as well as the first iteration of the piezo-mirror holder milled out of PVC plastic. Thanks go out to Caleb Schlamp for moral support and advisement of the electrical design. Thanks to Frank Rykoten and Neils Williams for helping me construct

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## APPENDIX A MECHANICAL ASSEMBLY DRAWINGS

### A. PZT-Mirror Holder

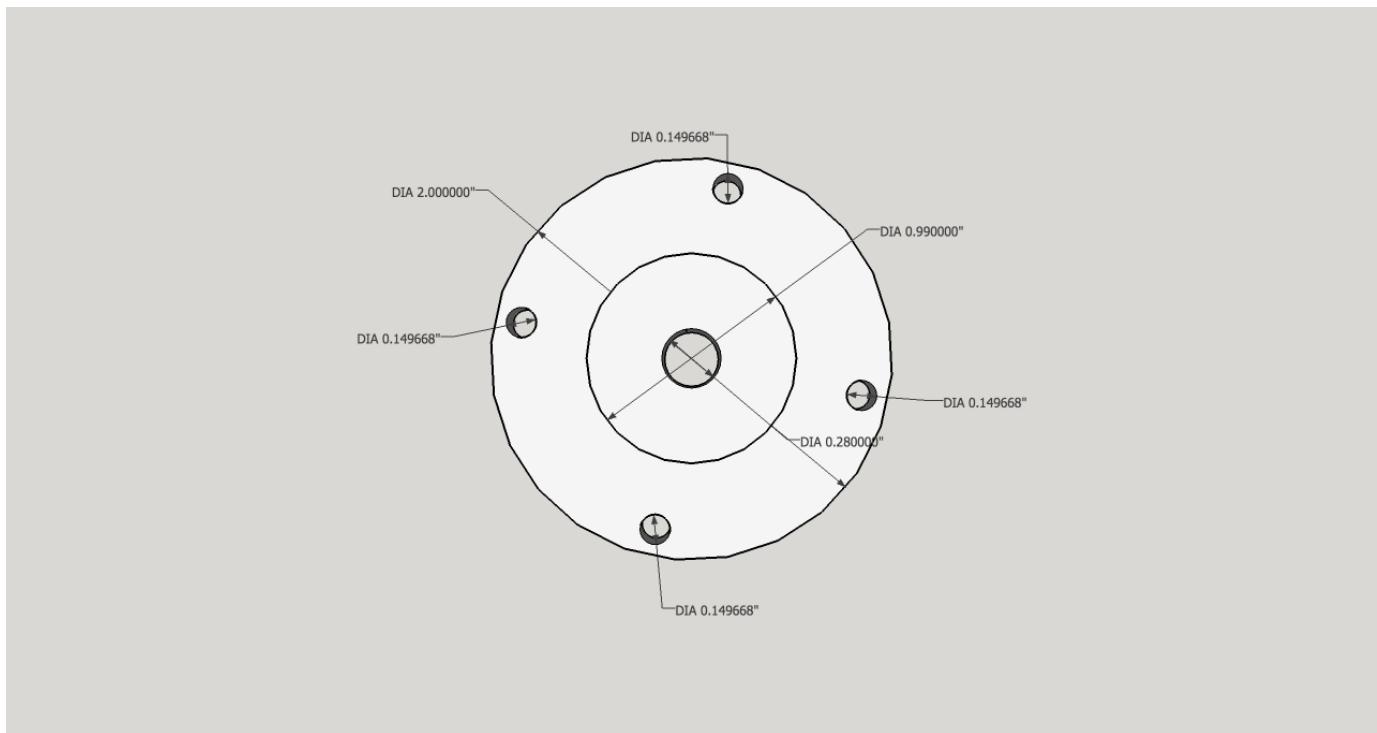


Fig. 21. The top down view and measurements of the PZT-Mirror holder

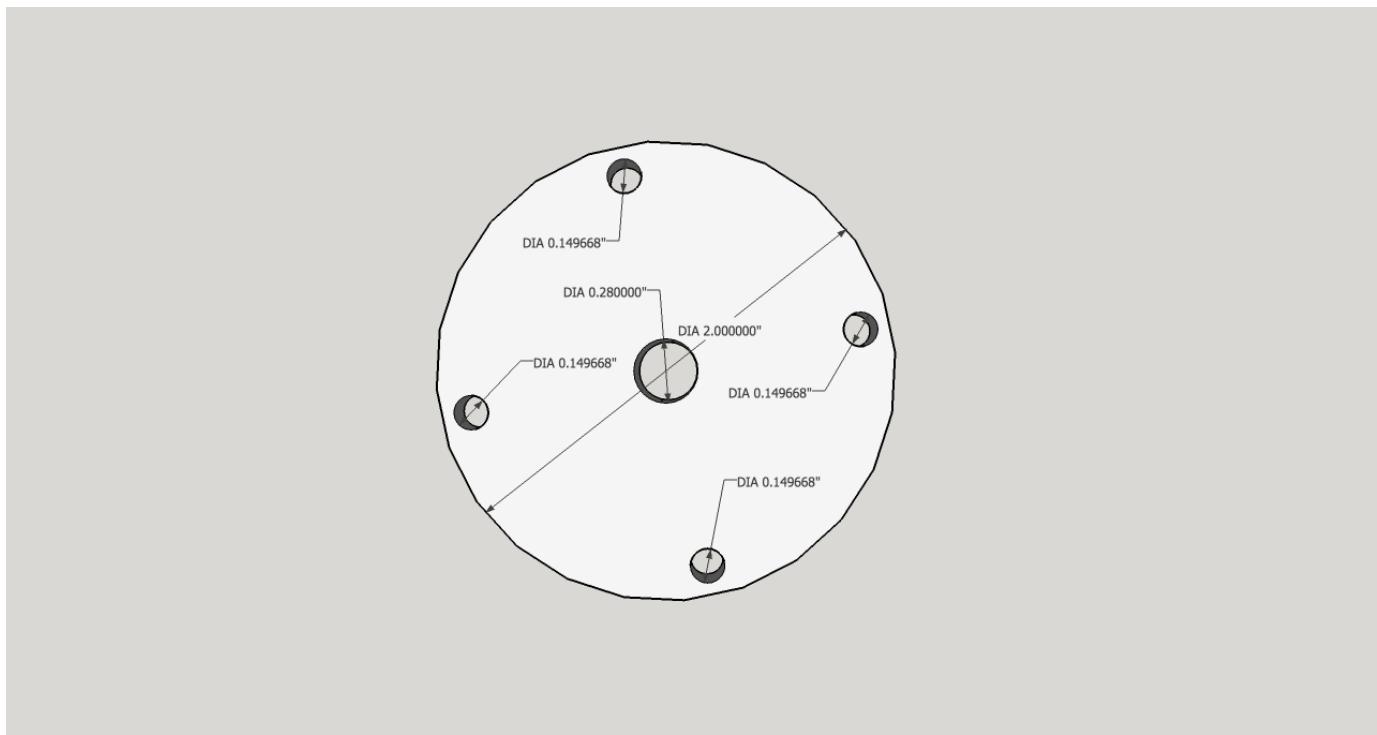


Fig. 22. The bottom up view and measurements of the PZT-Mirror holder

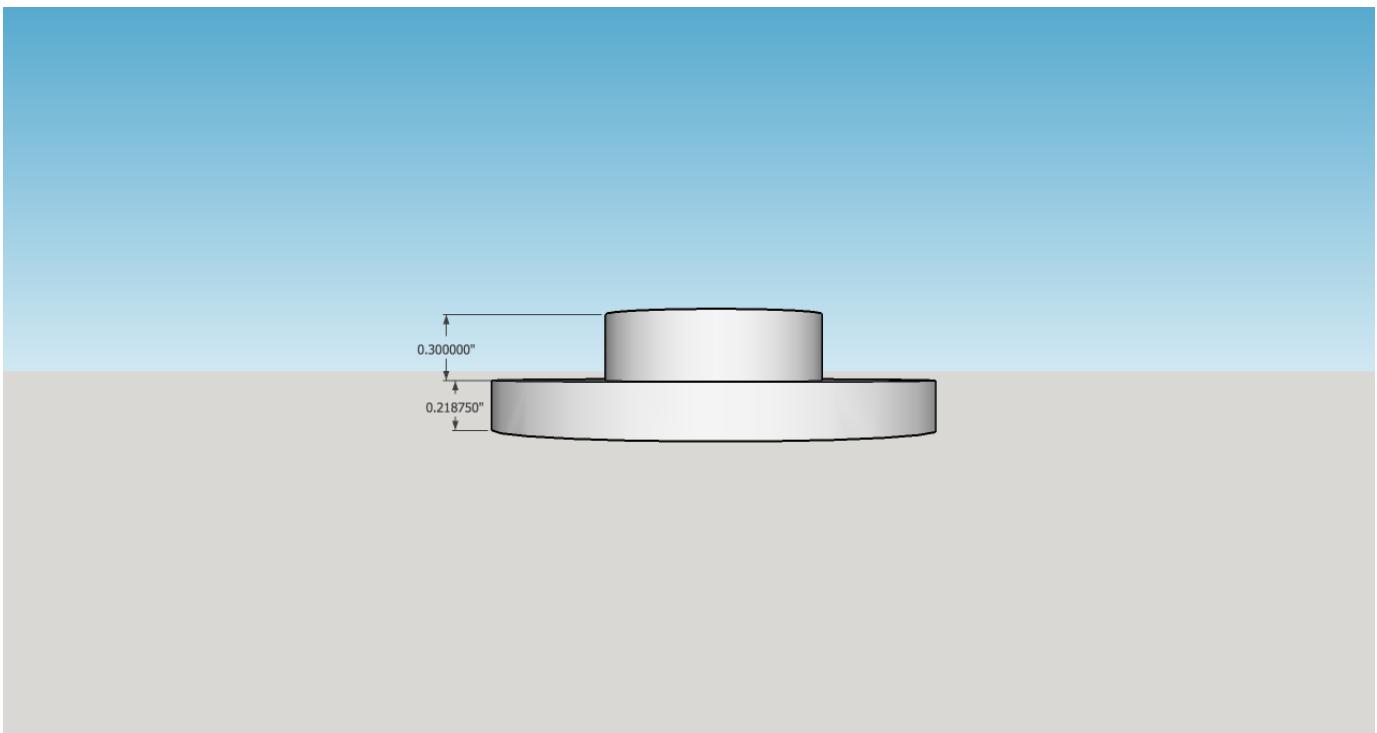


Fig. 23. The side view and measurements of the PZT-Mirror holder

#### B. sFPI Aluminum Base

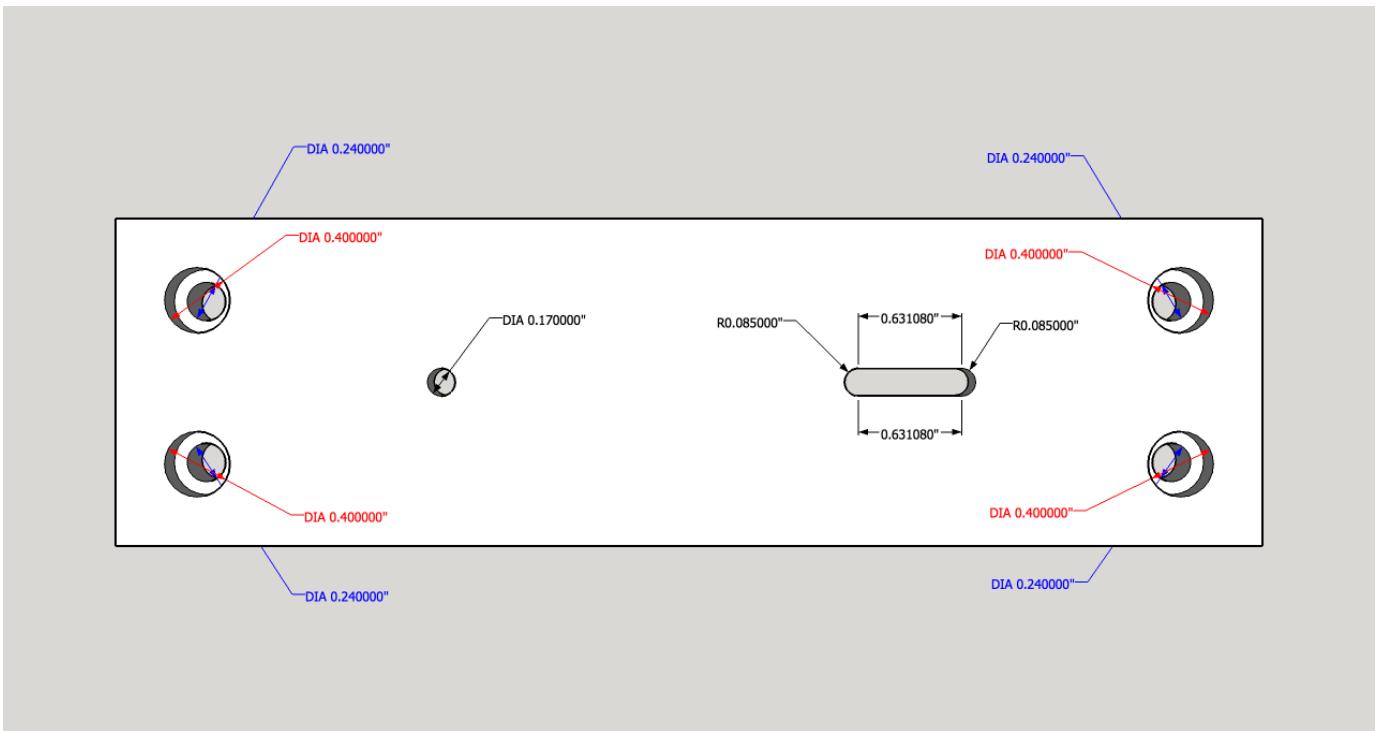


Fig. 24. The top down view and measurements of the sFPI aluminum base

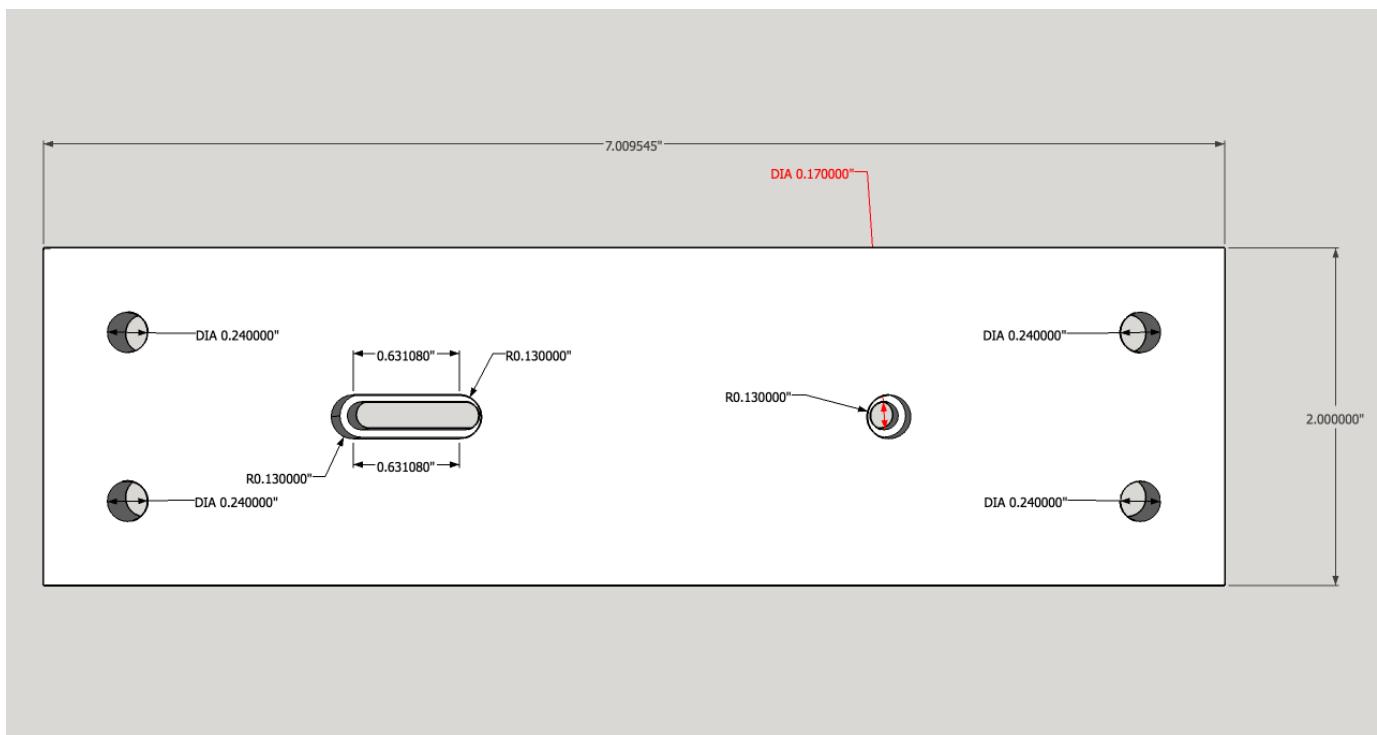


Fig. 25. The bottom up view and measurements of the sFPI aluminum base

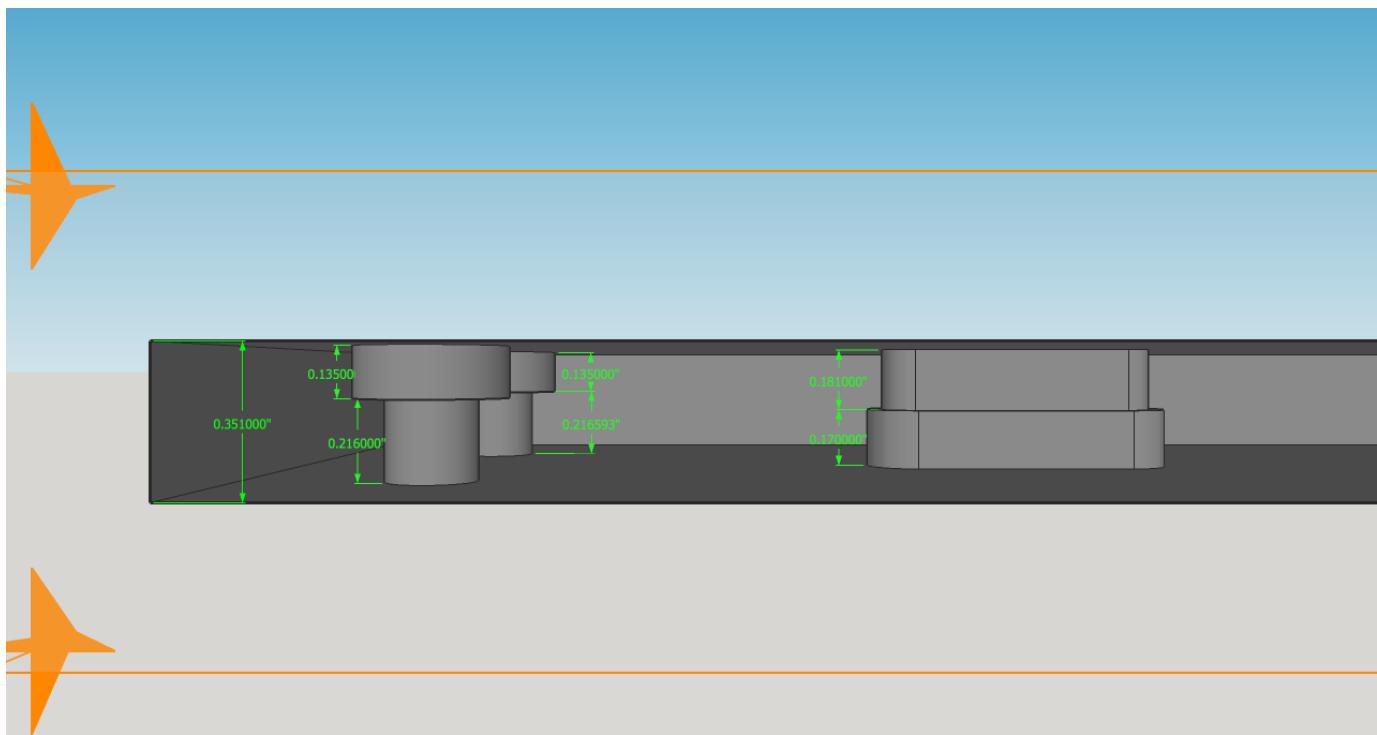


Fig. 26. The front cross section view and measurements of the sFPI aluminum base

### C. Photodiode Holder

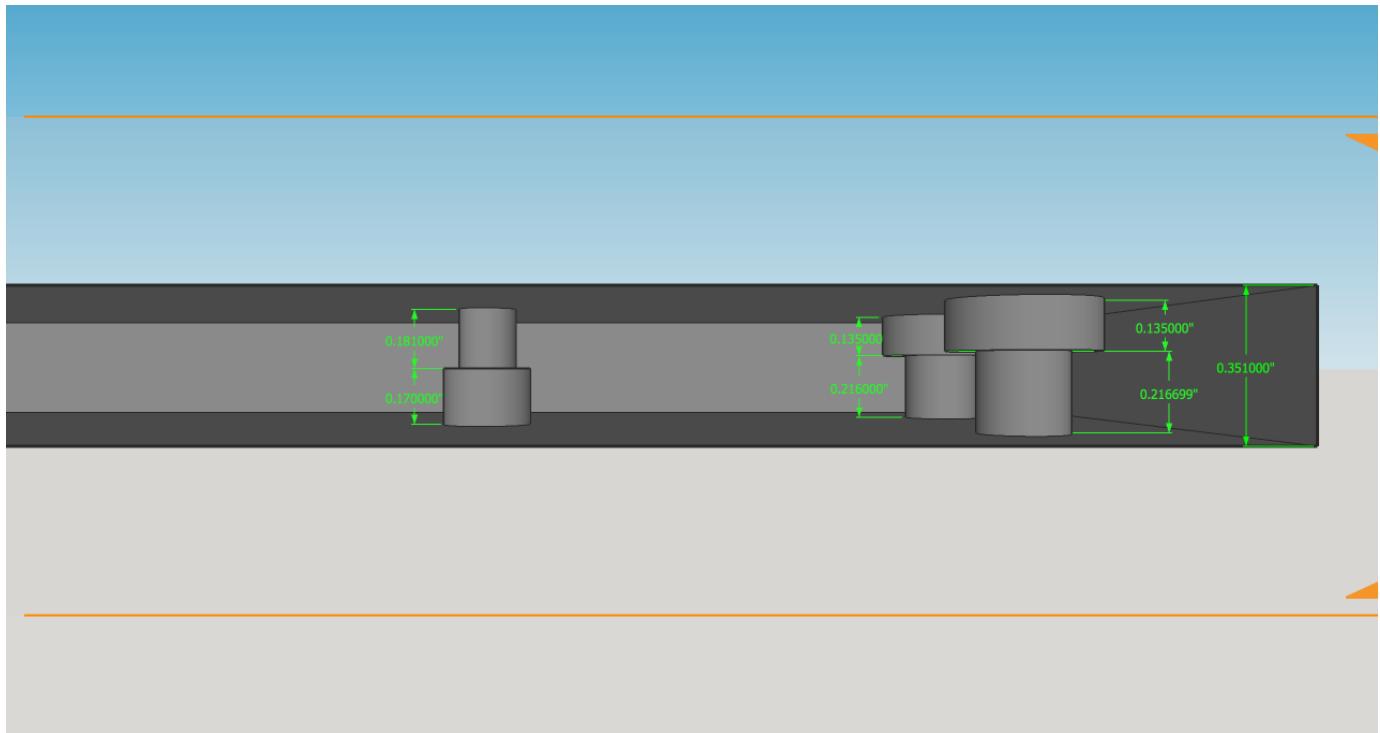


Fig. 27. The back cross section view and measurements of the sFPI aluminum base

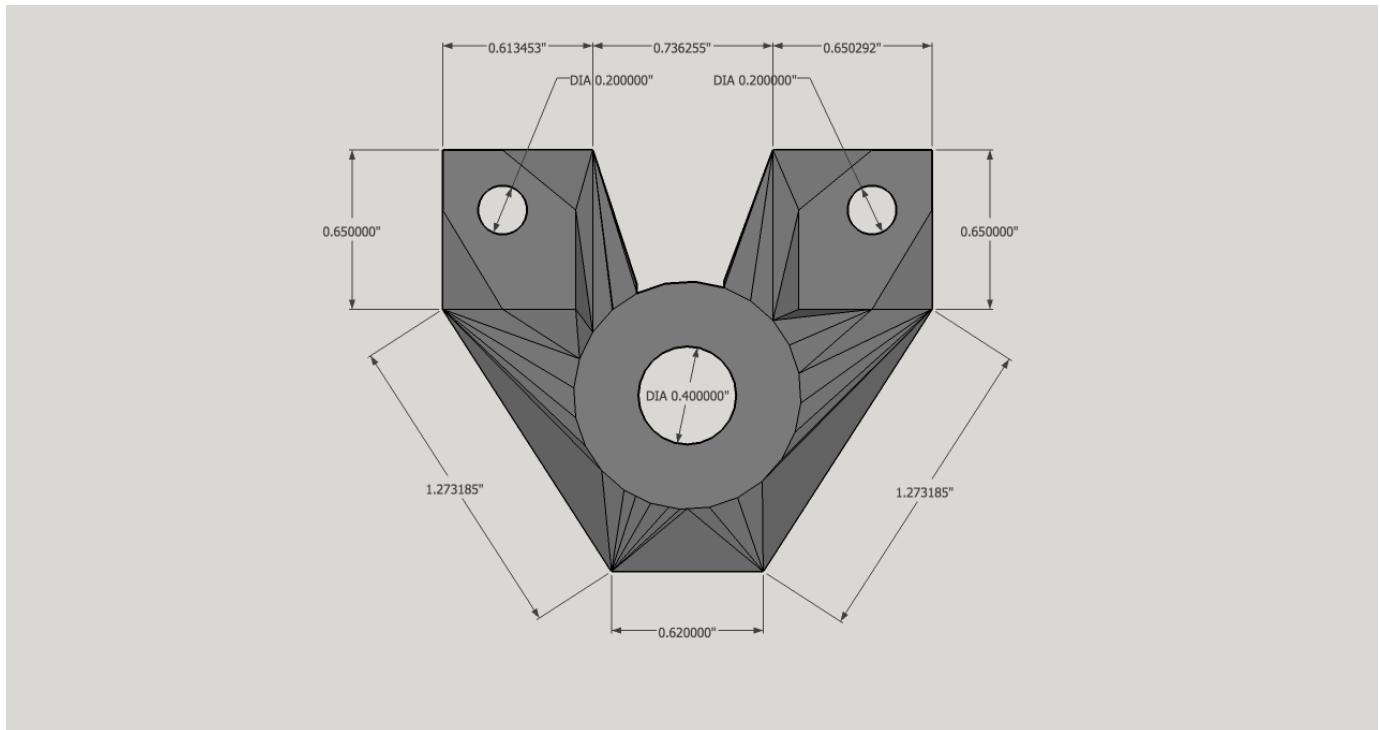


Fig. 28. The top down view and measurements of the sFPI aluminum base

## APPENDIX B ARDUINO PROGRAMS

### A. Writing to the MCP4725 12-bit DAC via I2C

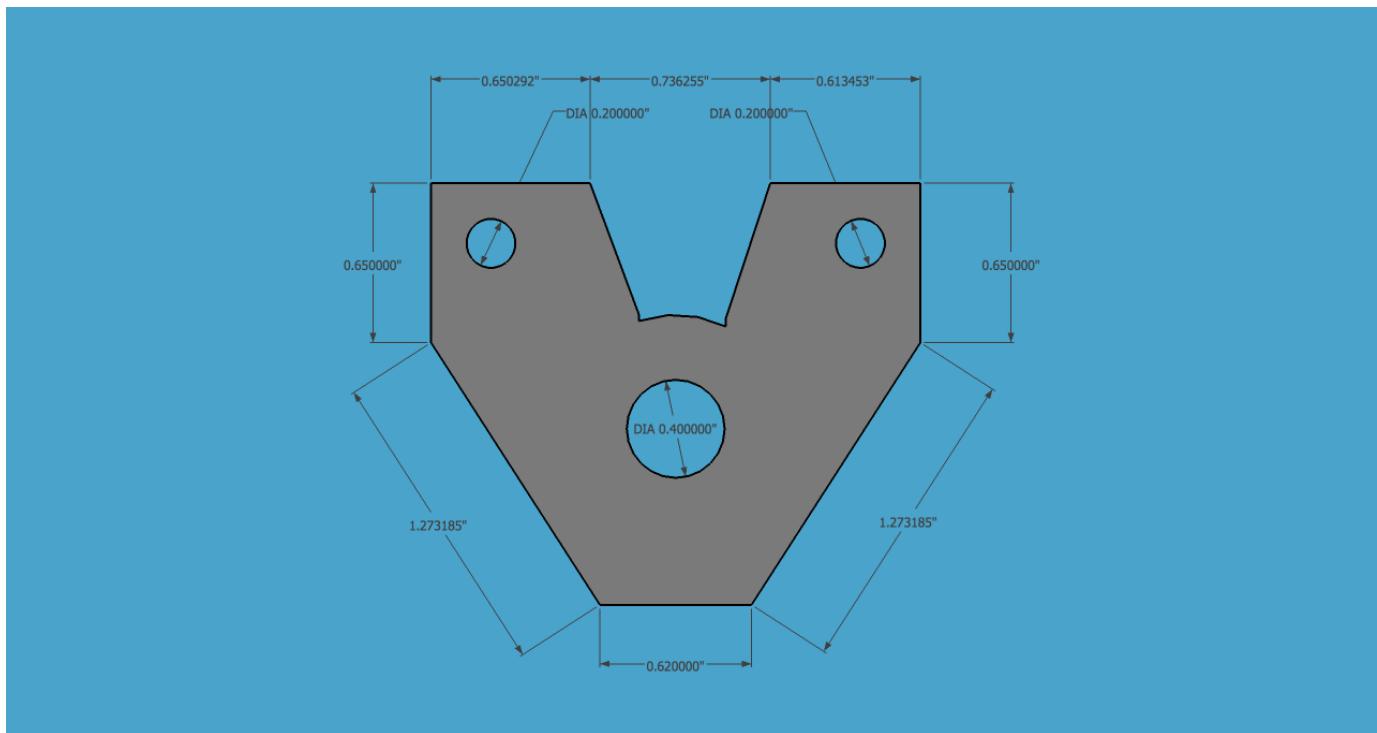


Fig. 29. The bottom up view and measurements of the sFPI aluminum base

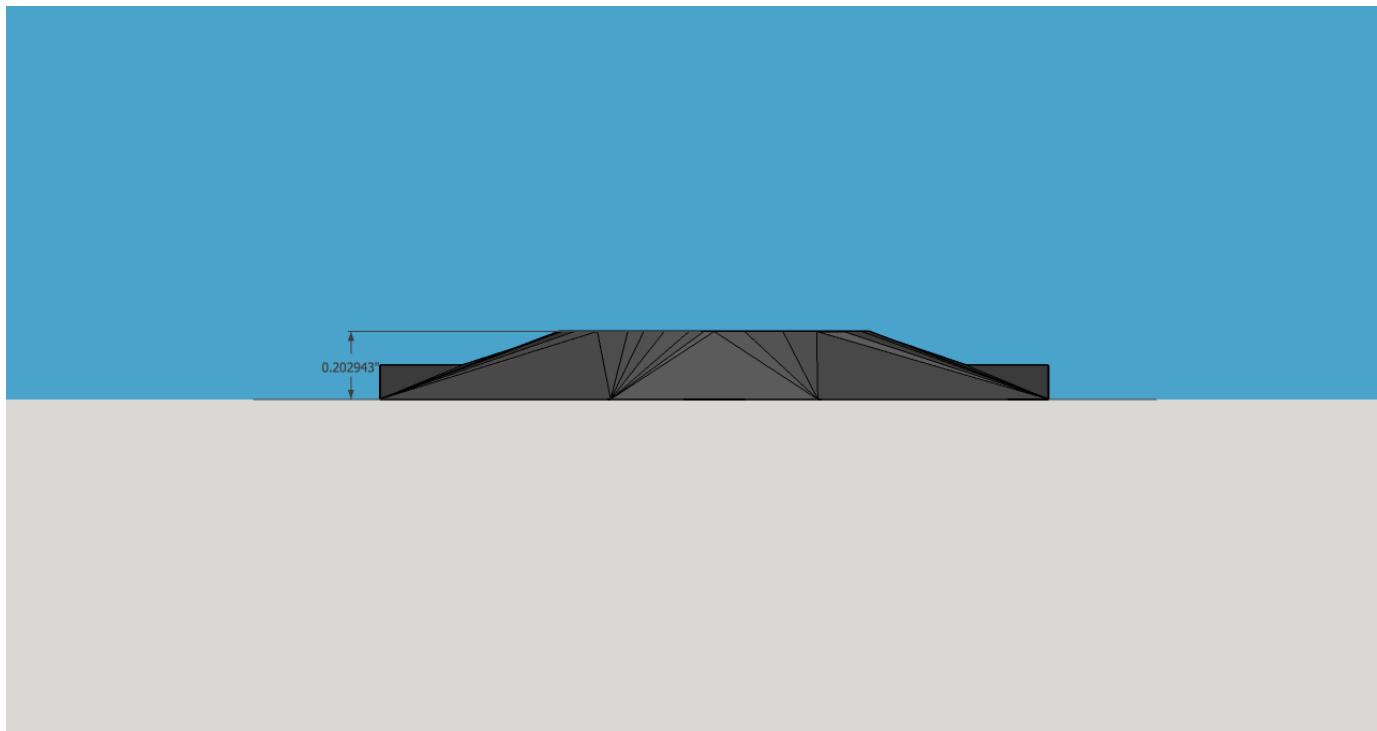


Fig. 30. The front cross section view and measurements of the sFPI aluminum base

---

```
/* sFPI Driver version 1.5
Copyright (c) 2015 David Miles Houston
```

This sketch uses the following associated

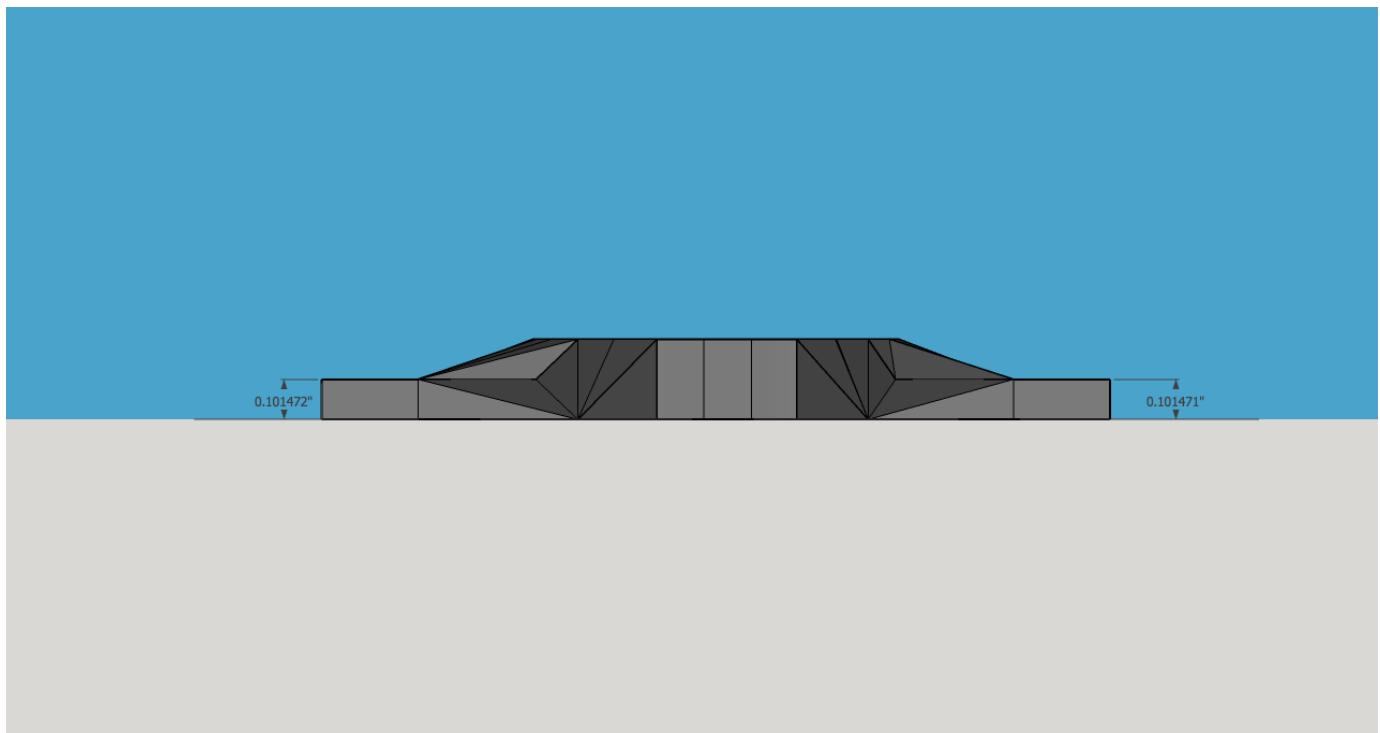


Fig. 31. The back cross section view and measurements of the sFPI aluminum base

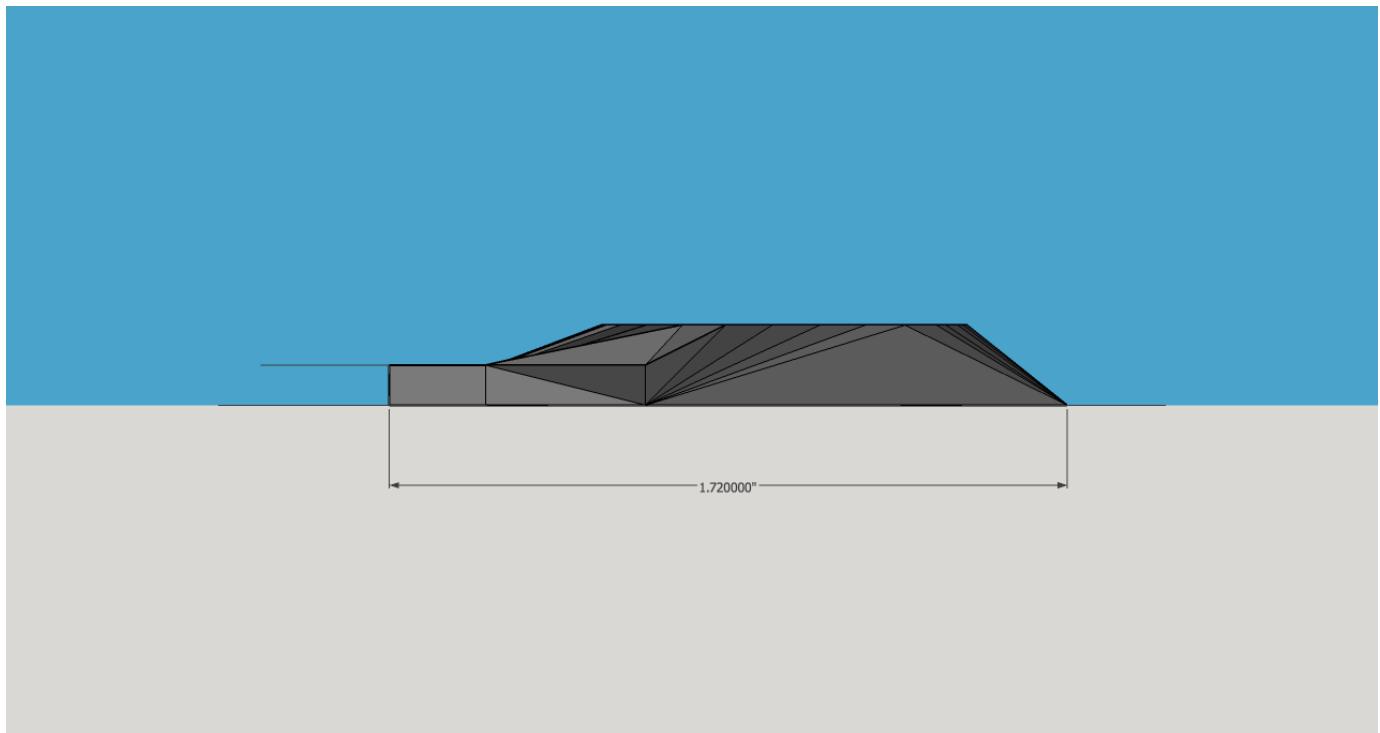


Fig. 32. The back cross section view and measurements of the sFPI aluminum base

pins in conjunction with the ,  
for the use of a sawtooth signal generator.

Developers Note: Current Pin out is as follows

```

Pin Name      Pin Location
-----  -----
SDA           A5
SCL           A4
*/
#include <Wire.h>
#include "Adafruit_MCP4725.h"

// use layout from the Adafruit Header File
Adafruit_MCP4725 dac;

#define bitres 1024;
// Number of tunable bits at one time
const int numbits = 1024;
// Number of bits in the period of the signal
const int wave_bits = 4096;
const int DP1 = 9;
//Number of bits to skip each time to increase speed
uint32_t skip = 1;

// Setup Loop
void setup()
{
    // Setup for Serial Communication
    // Pin Assignments
    pinMode(DP1,OUTPUT);
    dac.begin(0x62);
}

// Infinite Loop
void loop()
{
    digitalWrite(DP1,HIGH);
    for (uint32_t i = 0; i < wave_bits -1; i = i + skip) {
        dac.setVoltage(i, false);
        if (i==0) {
            digitalWrite(DP1,LOW);
        }
    }
}

```

---

### B. Program for capturing and sending serial data to the computer

```

/*
 * Title: Data Collection for sFPI
 * Authors: Scott Prahl & David Houston
 * Version: 1.0
 * Date: November 2015
 *
 * Description: This program accepts a byte of data
 * from the computer and then determines what ADC
 * pin to sample data from. It then sends the 512 bytes
 * to the computer via USB.
 */

// Arduino Pin A0 connected to photodiode output
const int PIN = A0;
// Arduino Pin A1 connected to ramp function output
const int SIN = A1;
// Pin connected to the other Arduino for communication
const int DP1 = 9;

```

```

const int PULSE = 10;
boolean run = false;
unsigned int data[257];

void setup()
{
    Serial.begin(57600);
    pinMode(PIN, INPUT);
    pinMode(SIN, INPUT);
    pinMode(DP1, INPUT);
}

void loop()
{
    // If data is requested by computer
    if (Serial.available() > 0) {
        char incomingByte = Serial.read();
        Serial.flush();
        /*
        while (run != true) {
            if (digitalRead(DP1) == HIGH){
                run = true;
            }
        }*/
        if (incomingByte == '0') {
            TakeData(SIN);
        }
        else
        {
            TakeData(PIN);
        }
    }
}

void TakeData(const int P)
{
    for (int i=0; i<256; i++) {
        data[i] = analogRead(P);
    }

    // send 512 bytes of data over serial interface
    // this is probably slowest of everything
    for (int i=0; i<256; i++) {
        Serial.write(byte(0x00FF & data[i]));
        Serial.write(byte(data[i] >> 8));
    }
}

```

---

## APPENDIX C PYTHON GUI

### A. Main program

---

```

from Tkinter import *
import sys, os
from Application import GUI

# The backbone Application Class

def main():

```

```

app = GUI(master=root)
mods = app.master

# Modify GUI features
mods.title("GUI - Scanning Fabry-Perot Interferometer")
app.mainloop()
# send to GUI Application and display accordingly

if __name__ == "__main__":
    root = Tk()
    main()
    sys.exit()

```

---

## B. Application Class

```

import csv, os
import numpy as np
import datetime
import FileDialog
import matplotlib
matplotlib.use("TkAgg")
from matplotlib.backends.backend_tkagg \
    import FigureCanvasTkAgg, NavigationToolbar2TkAgg
from matplotlib.figure import Figure
from USBInterface import SerialPort as SP
from Tkinter import *
# from GUIErrors import *

class GUI(Frame):
    def __init__(self,directory="/Applications/sFPI-GUI",
                 master=None,port=None,data=None,go=None):
        Frame.__init__(self,master, bd=1)
        # Initialize Class Variables and Functions
        self.cwd = directory
        self.master = master
        self.calibrated = False
        self.max_screenwidth = 1200
        self.max_screenheight = 690
        self.start_time = None

        # Set the geometry of the main windowing
        self.set_geometry()

        # Data Variables
        self.driver = [1]
        self.pdiode = [1]
        self.preferences_pause = False
        filename = self.cwd + "/docs/info.bin"

```

```

if not os.path.exists(os.path.dirname(filename)):
    self.port_name = "New Port Address"
else:
    self.port_name = open(filename, 'r').read()
# Set Port variable
self.port = port
# Execute Initialization Functions for Operation
self.pack()
self.clock()
self.tell_time()
self.create_menu_bar()
self.preferences()
self.display_port()
self.update()

def create_menu_bar(self):
    menu = Menu(self.master)
    self.master.config(menu=menu)

    # File Menu
    fileMenu = Menu(menu)
    menu.add_cascade(label="File", menu=fileMenu)
    fileMenu.add_command(label="New Project...", command=self.save_project())
    fileMenu.add_command(label="Save Project", command=self.save_project())
    fileMenu.add_separator()
    fileMenu.add_command(label="Exit", command=self.master.destroy)

    # Edit Menu
    editMenu = Menu(menu)
    menu.add_cascade(label="Edit", menu=editMenu)
    editMenu.add_command(label="Copy Image", command=self.save_project())

    # Tools Menu
    toolsMenu = Menu(menu)
    menu.add_cascade(label="Tools", menu=toolsMenu)
    toolsMenu.add_command(label="Change Serial Port", command=self.serial_window)
    toolsMenu.add_command(label="Calibrate", command=self.fsr_calibration)
    toolsMenu.add_command(label="Preferences", command=self.preferences())
    toolsMenu.add_separator()
    toolsMenu.add_command(label="Pause", command=self.pause())
    toolsMenu.add_command(label="Start", command=self.resume())
    toolsMenu.add_command(label="Get Ramp", command=self.get_ramp())

```

```

def graph_data(self):
    if bool(self.preferences_twoplot_var.get()) is False:
        f = Figure(figsize=(15,6), dpi=100,)
        self.graph = f.add_subplot(111)
        self.plot_data, = self.graph.plot(0,0)

        self.graph_canvas = FigureCanvasTkAgg(f, self)
        self.graph_canvas.show()
        self.graph_canvas.get_tk_widget().pack(side=BOTTOM,
                                              fill=BOTH, expand=True)

        toolbar = NavigationToolbar2TkAgg(self.graph_canvas, self)
        toolbar.update()
        self.graph_canvas._tkcanvas.pack(side=TOP,
                                         fill=BOTH, expand=True)

    else:
        f = Figure(figsize=(15,6), dpi=100,)
        self.graph1 = f.add_subplot(211)
        self.graph2 = f.add_subplot(212)
        self.plot_data_1, = self.graph1.plot(0,0)
        self.plot_data_2, = self.graph2.plot(0,0)

        self.graph_canvas = FigureCanvasTkAgg(f, self)
        self.graph_canvas.show()
        self.graph_canvas.get_tk_widget().pack(side=BOTTOM,
                                              fill=BOTH, expand=True)

        toolbar = NavigationToolbar2TkAgg(self.graph_canvas, self)
        toolbar.update()
        self.graph_canvas._tkcanvas.pack(side=TOP,
                                         fill=BOTH, expand=True)

    self.update_graph()

def update_graph(self):
    if bool(self.preferences_twoplot_var.get()) is False:
        self.graph.clear()
        self.graph.plot(np.array(self.driver),
                        np.array(self.pdiode),"r")
        self.graph.set_title('Spectral Plot of Cavity')
        self.graph.set_xlabel('Frequency (GHz)')
        self.graph.set_ylabel('Normalized Intensity')
        self.graph_canvas.draw()

    else:
        self.graph1.clear()
        self.graph1.plot(np.array(self.driver),"r")
        self.graph1.set_title('Ramp Function')

        self.graph2.clear()

```

```

    self.graph2.plot(np.array(self.pdiode), "r")
    self.graph2.set_title('Photodiode Output')
    self.graph_canvas.draw()

if self.preferences_pause is False:
    self.after(500, self.update_graph)

def save_project(self):
    filename = self.cwd + '/Logs/' + \
        datetime.datetime.now().strftime("%m-%d-%Y-%H_%M_%S") + \
        '.csv'
    if not os.path.exists(os.path.dirname(filename)):
        os.makedirs(os.path.dirname(filename))
    with open(filename, 'wb') as csvfile:
        spamwriter = csv.writer(csvfile, delimiter=',',
                               quotechar='|',
                               quoting=csv.QUOTE_MINIMAL)
        spamwriter.writerow(self.driver)
        spamwriter.writerow(self.pdiode)
    csvfile.close()

def pause(self):
    self.preferences_pause = True

def resume(self):
    self.preferences_pause = False
    self.update_graph()
    self.serial = SP(port=self.port_name)
    self.serial_read()

def get_ramp(self):
    self.serial = SP(port=self.port_name, get_ramp=True)
    self.serial_read(run_once=True)

def set_geometry(self):
    if self.master.winfo_screenwidth() > self.max_screenwidth:
        self.screen_width = self.max_screenwidth
    else:
        self.screen_width = self.master.winfo_screenwidth()

    if self.master.winfo_screenheight() > self.max_screenheight:
        self.screen_height = self.max_screenheight
    else:
        self.screen_height = self.master.winfo_screenwidth()

    self.master.geometry('{0}x{1}'.format(self.screen_width,
                                          self.screen_height))
    self.master.minsize(self.screen_width, self.screen_height)
    self.master.maxsize(self.screen_width, self.screen_height)

```



```

self.Plot2.pack()

self.Submit = self.GET = Button(iframe, text="Submit",fg="black",
                                command=self.close_window,
                                relief=SUNKEN)
self.Submit.pack(fill=X)

iframe.pack(expand=1, fill=X, pady=10, padx=5)
self.preferences.attributes("-topmost", True)
self.preferences.title("Preferences")
self.preferences.geometry('{}x{}'.format(170, 90))
self.preferences.minsize(170,90)

self.preferences.update_idletasks()
w = self.preferences.winfo_screenwidth()
h = self.preferences.winfo_screenheight()
size = tuple(int(_) for _ in
             self.preferences.geometry().split('+')[0].split('x'))
x = w/2 - size[0]/2
y = h/2 - size[1]/2
self.preferences.geometry("%dx%d+%d+%d" % (size + (x, y)))

def serial_window(self):
    self.serial_window = Toplevel(self.master)
    iframe1 = Frame(self.serial_window, bd=2)
    self.serial_window.title("Enter Serial Port")

    # Get Port Button
    self.GET = Button(iframe1, text="Store Port",fg="black",
                      command=self.get_port)
    self.GET.pack(side=RIGHT, padx=5)

    self.e = Entry(iframe1)
    self.e.pack(side=RIGHT, padx=0)

    self.e.delete(0, END)
    self.e.insert(0, self.port_name)

    iframe1.pack(expand=1, fill=X, pady=10, padx=5)

def get_port(self):
    self.port = self.e.get()
    filename = self.cwd + "/docs/info.bin"
    if not os.path.exists(os.path.dirname(filename)):
        os.makedirs(os.path.dirname(filename))
    info = open(filename, 'w')
    string = self.port
    info.write(string)
    info.close()
    self.port_name = string

```

```

self.serial_window.destroy()
self.update_port()

def display_port(self):
    try:
        filename = self.cwd + "/docs/info.bin"
        if not os.path.exists(os.path.dirname(filename)):
            os.makedirs(os.path.dirname(filename))
        info = open(filename, 'w')
        self.port_name = info.read()
        self.name_label = Label(self.master, text=self.port_name,
                               bd=1, relief=SUNKEN, anchor=SE)
        self.name_label.pack(fill=X)

    except IndexError as ie:
        port = "No Port Selected"
        self.name_label = Label(self.master, text=port,
                               bd=1, relief=SUNKEN, anchor=SE)
        self.name_label.pack(fill=X)

    except IOError as INOUT:
        port = "No Port Selected"
        self.name_label = Label(self.master, text=port,
                               bd=1, relief=SUNKEN, anchor=SE)
        self.name_label.pack(fill=X)

def update_port(self):
    self.name_label.configure(text=self.port_name)
    self.serial = SP(port=self.port_name)

def close_window(self):
    self.preferences.destroy()
    if bool(self.preferences_test_var.get()) is True:
        data = {}
        filename = self.cwd + "/test/photodiode_output.csv"
        if not os.path.exists(os.path.dirname(filename)):
            os.makedirs(os.path.dirname(filename))
        with open(filename, 'r') as csvdata:
            data_reader = csv.reader(csvdata)
            i = 0
            for row in data_reader:
                if i == 0:
                    data['driver'] = row
                    i = i + 1
                else:
                    data['pdiode'] = row
        for num in range(len(data['driver'])):
            data['driver'][num] = float(data['driver'][num])
            data['pdiode'][num] = float(data['pdiode'][num])
        self.driver = data['driver']

```

```

        self.pdiode = data['pdiode']
    self.graph_data()

def clock(self):
    self.time = Label(self.master, bd=1, relief=SUNKEN, anchor=SE)
    self.time.pack(fill=X)

def tell_time(self):
    time = datetime.datetime.now().strftime("Time: %H:%M:%S")
    self.time.config(text=time)
    #lab['text'] = time
    self.after(1000, self.tell_time) # run itself again after 1000 ms

def serial_read(self, run_once=False):
    data = self.serial.Get_Data()
    if data is not False:
        if data['get_ramp'] is False:
            self.pdiode = data['values']
        else:
            self.driver = data['values']

        if self.calibrated == True:
            self.set_calibration()

        if run_once is False:
            self.after(1000, self.serial_read)
    else:
        self.name_label.configure(text="Communication Failed")

```

---

### C. USB Interface Class

```

import serial, time, itertools
from GUIErrors import *

class SerialPort():
    def __init__(self, port=None, get_ramp=False):
        try:
            self.get_ramp = get_ramp
            self.error = False
            self.ser = serial.Serial(port, 57600, timeout=1)
        except OSError as Bad_Port:
            self.error = True

    def Get_Data(self):
        try:
            arduino_data = []
            data = []
            if self.error is not True:

```

```

# VERY IMPORTANT!!!
time.sleep(1/1000)
self.ser.setDTR(level=0)
time.sleep(1/1000)
if self.get_ramp == True:
    self.ser.write("0")
else:
    self.ser.write("1")
self.bits = 256
for i in range(0,(self.bits*2)):
    arduino_data.append(self.ser.read())
if arduino_data[0] == '':
    raise DataError(arduino_data[0])
arduino_data = self.deArduinoify(arduino_data)
self.ser.flush()
for i in range(0,self.bits-1):
    data.append(self.add_hex(arduino_data[2*i],
                            arduino_data[2*i+1]))
else:
    data = []
raise DataError('No Data')

output = {'values':data,'get_ramp':self.get_ramp}
return output
except DataError as Bad_comm:
    return False

def deArduinoify(self,data):
    values = []
    for k in range(len(data)):
        d = data[k].encode('hex')
        dnew = int(d,16)
        values.append(dnew)
    return values

def add_hex(self,A,B):
    conv = B*256 + A
    return conv

```

---

#### D. GUI Errors Class

---

```

class Error(Exception):
    pass

class DataError(Error):
    def __init__(self,data):
        self.data = data
    def __str__(self):

```

---

```

    return repr(self.data)

class ImageError(Error):
    def __init__(self,data):
        self.data = data
    def __str__(self):
        return repr(self.data)

```

---

### E. Setup Function

---

```

"""
This is a setup.py script generated by py2applet

Usage:
    python setup.py py2app
"""

from setuptools import setup

APP = ['GUI.py']
DATA_FILES = []
OPTIONS = {
    'iconfile': 'GUI.icns',
    'plist': {'CFBundleShortVersionString': '1.0.0',}
}

setup(
    app=APP,
    name='GUI',
    data_files=DATA_FILES,
    options={'py2app': OPTIONS},
    setup_requires=['py2app'],
)
```

---

## APPENDIX D

### LTSPICE NETLISTS

#### A. Interferometer Driver LTSpice Netlist for Simulation

```

* Z:\Users\aviatorblue\Documents\sFPI\Electrical Design\Amplifier_Design\amplifier_setup_rev2.asc
* The LT1001 component is used in place of the NTE941M
XU1 0 N011 Vdd Vss N012 LT1001
XU2 0 N006 Vdd Vss N007 LT1001
XU3 0 N009 Vdd Vss N010 LT1001
XU4 0 N008 Vdd Vss Vac LT1001
R1 N011 N013 10k
R2 N012 N011 10k
R3 N006 N012 5k
R4 N007 N006 10k
R5 N009 N007 5k
R6 N010 N009 10k
R7 N008 N010 10k
R8 Vac N008 10k
* The sawtooth_current.txt file is generated using a python script located in the same directory
V1 N013 0 PWL file=sawtooth_current.txt
V2 Vdd 0 17
V3 0 Vss 17
* The LT1086 component is used in place of the NTEXXX (5 V regulator)
XU5 0 5V Vdd LT1085-5
R_Arduino 5V 0 10Meg
* The LT1086 component is used in place of the NTE956
XU6 N003 Vdc Vdd LT1086
R10 N003 Vss 2.6k
R11 Vdc N003 1.5k
XU9 0 N002 Vdd Vss Vout LT1001
XU10 Vac N004 Vdd Vss N004 LT1001
XU11 Vdc N001 Vdd Vss N001 LT1001
R19 N002 N001 100k
R20 N002 N004 100k
R12 Vout N002 100k
R13 Vout N005 300
C1 N005 0 15.51n
.tran 0 0.01 0
.lib LT1083.lib
.lib LTC.lib
.backanno
.end

```

## APPENDIX E DATASHEETS

## Features

- High Performance, Low Power AVR® 8-Bit Microcontroller
  - Advanced RISC Architecture
    - 131 Powerful Instructions – Most Single Clock Cycle Execution
    - 32 x 8 General Purpose Working Registers
    - Fully Static Operation
    - Up to 20 MIPS Throughput at 20 MHz
    - On-chip 2-cycle Multiplier
  - High Endurance Non-volatile Memory Segments
    - 4/8/16/32K Bytes of In-System Self-Programmable Flash program memory (ATmega48PA/88PA/168PA/328P)
    - 256/512/512/1K Bytes EEPROM (ATmega48PA/88PA/168PA/328P)
    - 512/1K/1K/2K Bytes Internal SRAM (ATmega48PA/88PA/168PA/328P)
    - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
    - Data retention: 20 years at 85°C/100 years at 25°C<sup>(1)</sup>
    - Optional Boot Code Section with Independent Lock Bits
      - In-System Programming by On-chip Boot Program
      - True Read-While-Write Operation
    - Programming Lock for Software Security
  - Peripheral Features
    - Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode
    - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
    - Real Time Counter with Separate Oscillator
    - Six PWM Channels
    - 8-channel 10-bit ADC in TQFP and QFN/MLF package
      - Temperature Measurement
    - 6-channel 10-bit ADC in PDIP Package
      - Temperature Measurement
    - Programmable Serial USART
    - Master/Slave SPI Serial Interface
    - Byte-oriented 2-wire Serial Interface (Philips I²C compatible)
    - Programmable Watchdog Timer with Separate On-chip Oscillator
    - On-chip Analog Comparator
    - Interrupt and Wake-up on Pin Change
  - Special Microcontroller Features
    - Power-on Reset and Programmable Brown-out Detection
    - Internal Calibrated Oscillator
    - External and Internal Interrupt Sources
    - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
  - I/O and Packages
    - 23 Programmable I/O Lines
    - 28-pin PDIP, 32-lead TQFP, 28-pad QFN/MLF and 32-pad QFN/MLF
  - Operating Voltage:
    - 1.8 - 5.5V for ATmega48PA/88PA/168PA/328P
  - Temperature Range:
    - -40°C to 85°C
  - Speed Grade:
    - 0 - 20 MHz @ 1.8 - 5.5V
  - Low Power Consumption at 1 MHz, 1.8V, 25°C for ATmega48PA/88PA/168PA/328P:
    - Active Mode: 0.2 mA
    - Power-down Mode: 0.1 µA
    - Power-save Mode: 0.75 µA (Including 32 kHz RTC)



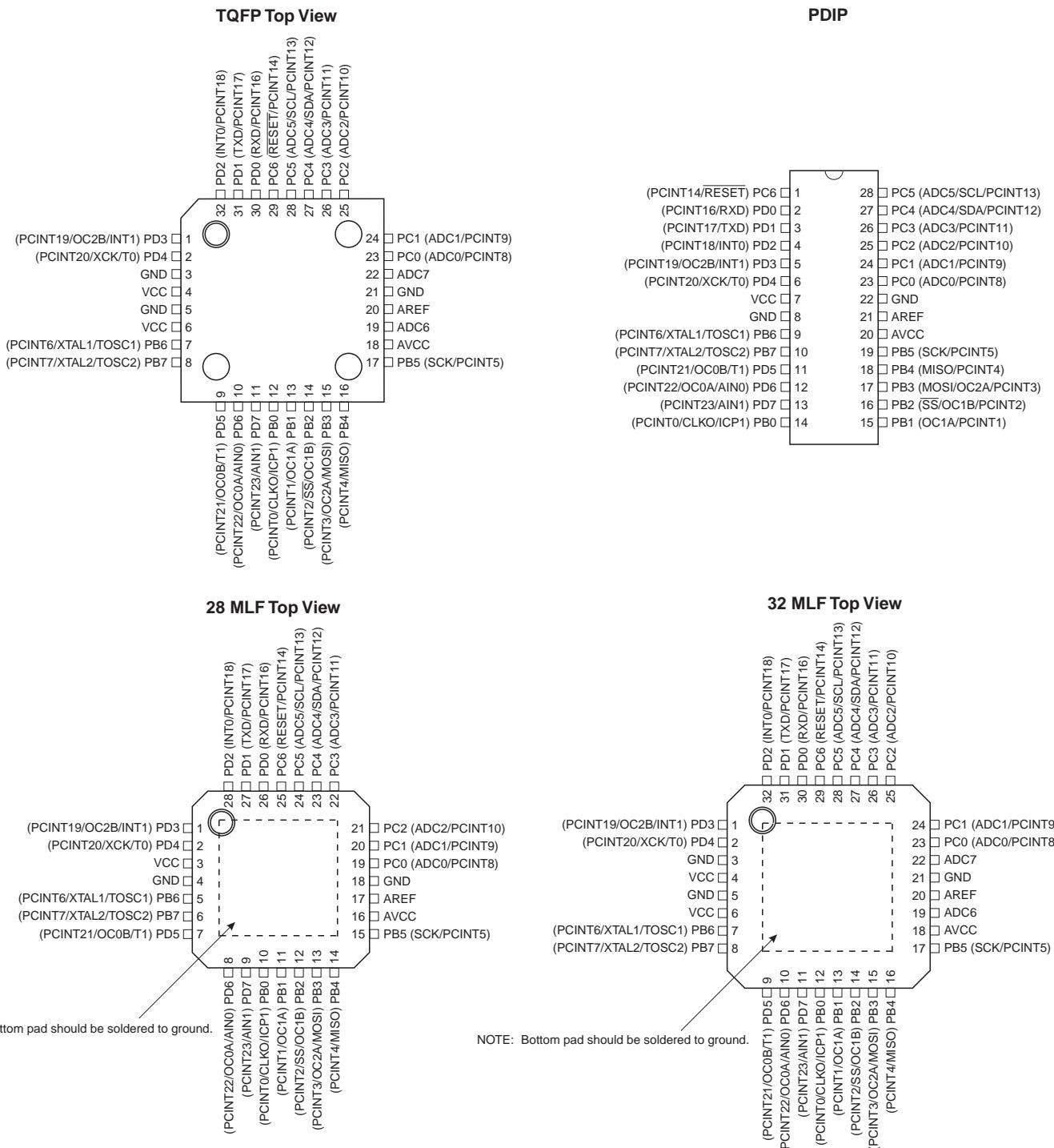
## 8-bit AVR® Microcontroller with 4/8/16/32K Bytes In-System Programmable Flash

**ATmega48PA**  
**ATmega88PA**  
**ATmega168PA**  
**ATmega328P**



## 1. Pin Configurations

**Figure 1-1.** Pinout ATmega48PA/88PA/168PA/328P



## 1.1 Pin Descriptions

### 1.1.1 VCC

Digital supply voltage.

### 1.1.2 GND

Ground.

### 1.1.3 Port B (PB7:0) XTAL1/XTAL2/TOSC1/TOSC2

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Depending on the clock selection fuse settings, PB6 can be used as input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

Depending on the clock selection fuse settings, PB7 can be used as output from the inverting Oscillator amplifier.

If the Internal Calibrated RC Oscillator is used as chip clock source, PB7..6 is used as TOSC2..1 input for the Asynchronous Timer/Counter2 if the AS2 bit in ASSR is set.

The various special features of Port B are elaborated in "[Alternate Functions of Port B](#)" on page [82](#) and "[System Clock and Clock Options](#)" on page [26](#).

### 1.1.4 Port C (PC5:0)

Port C is a 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The PC5..0 output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

### 1.1.5 PC6/RESET

If the RSTDISBL Fuse is programmed, PC6 is used as an I/O pin. Note that the electrical characteristics of PC6 differ from those of the other pins of Port C.

If the RSTDISBL Fuse is unprogrammed, PC6 is used as a Reset input. A low level on this pin for longer than the minimum pulse length will generate a Reset, even if the clock is not running. The minimum pulse length is given in [Table 28-3 on page 318](#). Shorter pulses are not guaranteed to generate a Reset.

The various special features of Port C are elaborated in "[Alternate Functions of Port C](#)" on page [85](#).

### 1.1.6 Port D (PD7:0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.



The various special features of Port D are elaborated in "[Alternate Functions of Port D](#)" on page 88.

## 1.1.7 AV<sub>CC</sub>

AV<sub>CC</sub> is the supply voltage pin for the A/D Converter, PC3:0, and ADC7:6. It should be externally connected to V<sub>CC</sub>, even if the ADC is not used. If the ADC is used, it should be connected to V<sub>CC</sub> through a low-pass filter. Note that PC6..4 use digital supply voltage, V<sub>CC</sub>.

## 1.1.8 AREF

AREF is the analog reference pin for the A/D Converter.

## 1.1.9 ADC7:6 (TQFP and QFN/MLF Package Only)

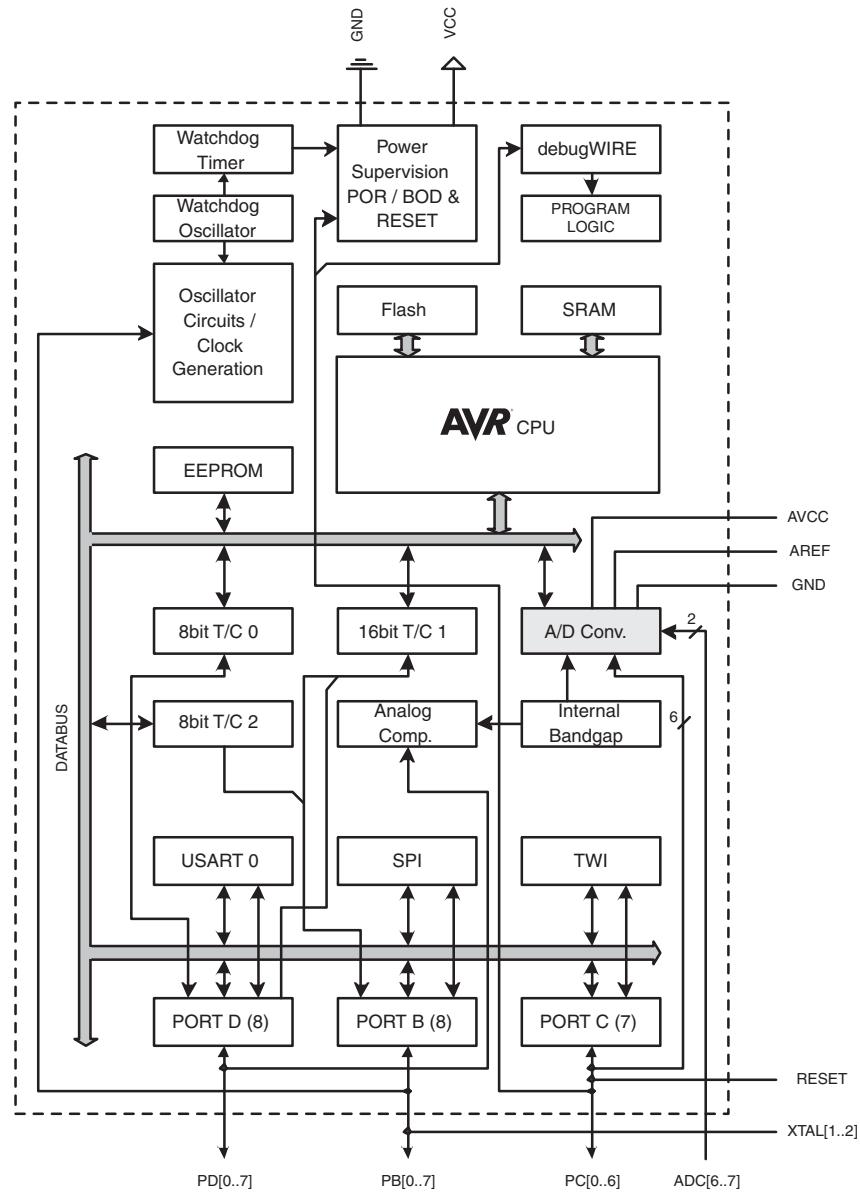
In the TQFP and QFN/MLF package, ADC7:6 serve as analog inputs to the A/D converter. These pins are powered from the analog supply and serve as 10-bit ADC channels.

## 2. Overview

The ATmega48PA/88PA/168PA/328P is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega48PA/88PA/168PA/328P achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

### 2.1 Block Diagram

**Figure 2-1.** Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting

# ATmega48PA/88PA/168PA/328P

architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega48PA/88PA/168PA/328P provides the following features: 4K/8K bytes of In-System Programmable Flash with Read-While-Write capabilities, 256/512/512/1K bytes EEPROM, 512/1K/1K/2K bytes SRAM, 23 general purpose I/O lines, 32 general purpose working registers, three flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, a byte-oriented 2-wire Serial Interface, an SPI serial port, a 6-channel 10-bit ADC (8 channels in TQFP and QFN/MLF packages), a programmable Watchdog Timer with internal Oscillator, and five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, USART, 2-wire Serial Interface, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, by a conventional non-volatile memory programmer, or by an On-chip Boot program running on the AVR core. The Boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega48PA/88PA/168PA/328P is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega48PA/88PA/168PA/328P AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation kits.

## 2.2 Comparison Between ATmega48PA, ATmega88PA, ATmega168PA and ATmega328P

The ATmega48PA, ATmega88PA, ATmega168PA and ATmega328P differ only in memory sizes, boot loader support, and interrupt vector sizes. [Table 2-1](#) summarizes the different memory and interrupt vector sizes for the three devices.

**Table 2-1.** Memory Size Summary

Device	Flash	EEPROM	RAM	Interrupt Vector Size
ATmega48PA	4K Bytes	256 Bytes	512 Bytes	1 instruction word/vector
ATmega88PA	8K Bytes	512 Bytes	1K Bytes	1 instruction word/vector
ATmega168PA	16K Bytes	512 Bytes	1K Bytes	2 instruction words/vector
ATmega328P	32K Bytes	1K Bytes	2K Bytes	2 instruction words/vector

ATmega88PA, ATmega168PA and ATmega328P support a real Read-While-Write Self-Programming mechanism. There is a separate Boot Loader Section, and the SPM instruction can only execute from there. In ATmega48PA, there is no Read-While-Write support and no separate Boot Loader Section. The SPM instruction can execute from the entire Flash.



## 3. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on <http://www.atmel.com/avr>.

## 4. Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

## 5. About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

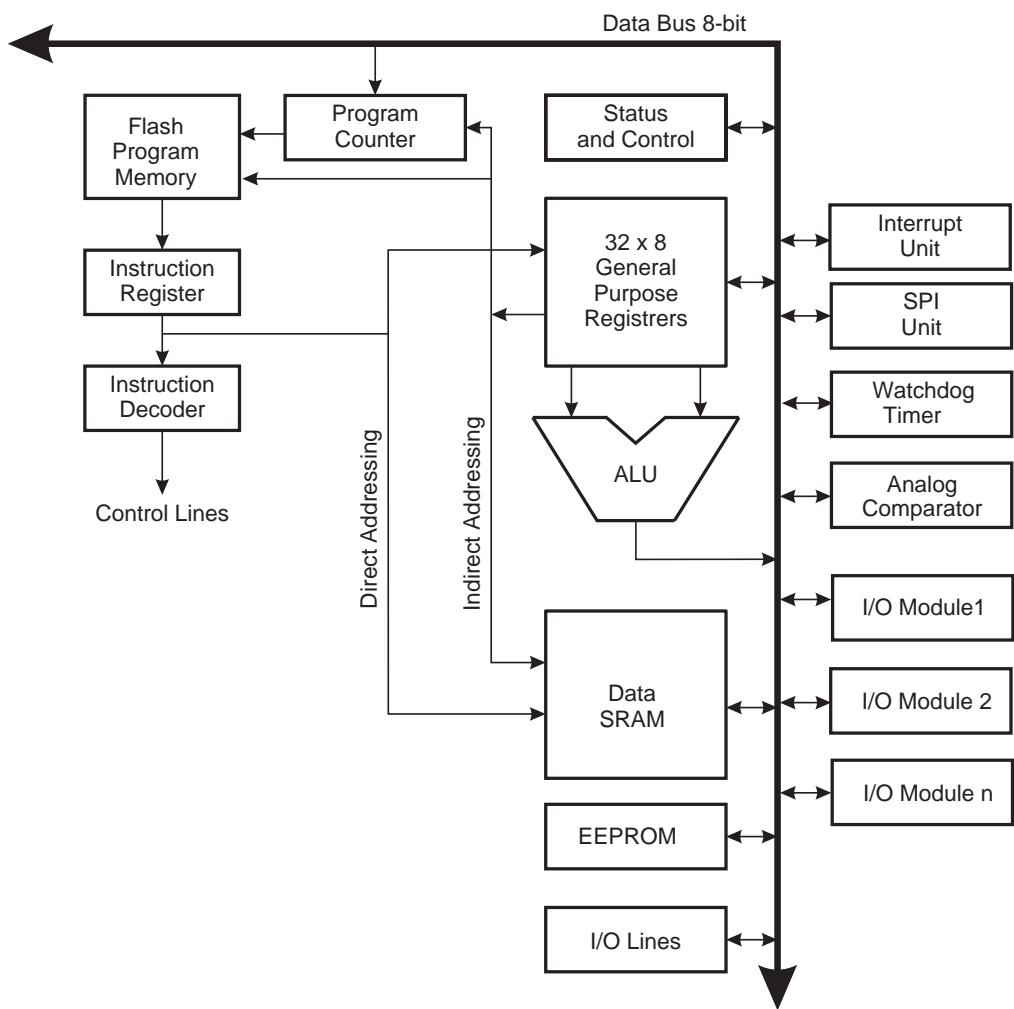
For I/O Registers located in extended I/O map, "IN", "OUT", "SBIS", "SBIC", "CBI", and "SBI" instructions must be replaced with instructions that allow access to extended I/O. Typically "LDS" and "STS" combined with "SBRS", "SBRC", "SBR", and "CBR".

## 6. AVR CPU Core

### 6.1 Overview

This section discusses the AVR core architecture in general. The main function of the CPU core is to ensure correct program execution. The CPU must therefore be able to access memories, perform calculations, control peripherals, and handle interrupts.

**Figure 6-1.** Block Diagram of the AVR Architecture



In order to maximize performance and parallelism, the AVR uses a Harvard architecture – with separate memories and buses for program and data. Instructions in the program memory are executed with a single level pipelining. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is In-System Reprogrammable Flash memory.

The fast-access Register File contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This allows single-cycle Arithmetic Logic Unit (ALU) operation. In a typ-

ical ALU operation, two operands are output from the Register File, the operation is executed, and the result is stored back in the Register File – in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for Data Space addressing – enabling efficient address calculations. One of these address pointers can also be used as an address pointer for look up tables in Flash program memory. These added function registers are the 16-bit X-, Y-, and Z-register, described later in this section.

The ALU supports arithmetic and logic operations between registers or between a constant and a register. Single register operations can also be executed in the ALU. After an arithmetic operation, the Status Register is updated to reflect information about the result of the operation.

Program flow is provided by conditional and unconditional jump and call instructions, able to directly address the whole address space. Most AVR instructions have a single 16-bit word format. Every program memory address contains a 16- or 32-bit instruction.

Program Flash memory space is divided in two sections, the Boot Program section and the Application Program section. Both sections have dedicated Lock bits for write and read/write protection. The SPM instruction that writes into the Application Flash memory section must reside in the Boot Program section.

During interrupts and subroutine calls, the return address Program Counter (PC) is stored on the Stack. The Stack is effectively allocated in the general data SRAM, and consequently the Stack size is only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the SP in the Reset routine (before subroutines or interrupts are executed). The Stack Pointer (SP) is read/write accessible in the I/O space. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps.

A flexible interrupt module has its control registers in the I/O space with an additional Global Interrupt Enable bit in the Status Register. All interrupts have a separate Interrupt Vector in the Interrupt Vector table. The interrupts have priority in accordance with their Interrupt Vector position. The lower the Interrupt Vector address, the higher the priority.

The I/O memory space contains 64 addresses for CPU peripheral functions as Control Registers, SPI, and other I/O functions. The I/O Memory can be accessed directly, or as the Data Space locations following those of the Register File, 0x20 - 0x5F. In addition, the ATmega48PA/88PA/168PA/328P has Extended I/O space from 0x60 - 0xFF in SRAM where only the ST/STS/STD and LD/LDS/LDD instructions can be used.

## 6.2 ALU – Arithmetic Logic Unit

The high-performance AVR ALU operates in direct connection with all the 32 general purpose working registers. Within a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate are executed. The ALU operations are divided into three main categories – arithmetic, logical, and bit-functions. Some implementations of the architecture also provide a powerful multiplier supporting both signed/unsigned multiplication and fractional format. See the “Instruction Set” section for a detailed description.

## 6.3 Status Register

The Status Register contains information about the result of the most recently executed arithmetic instruction. This information can be used for altering program flow in order to perform conditional operations. Note that the Status Register is updated after all ALU operations, as



specified in the Instruction Set Reference. This will in many cases remove the need for using the dedicated compare instructions, resulting in faster and more compact code.

The Status Register is not automatically stored when entering an interrupt routine and restored when returning from an interrupt. This must be handled by software.

### 6.3.1 SREG – AVR Status Register

The AVR Status Register – SREG – is defined as:

Bit	7	6	5	4	3	2	1	0	
0x3F (0x5F)	I	T	H	S	V	N	Z	C	SREG
Read/Write	R/W								
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – I: Global Interrupt Enable**

The Global Interrupt Enable bit must be set for the interrupts to be enabled. The individual interrupt enable control is then performed in separate control registers. If the Global Interrupt Enable Register is cleared, none of the interrupts are enabled independent of the individual interrupt enable settings. The I-bit is cleared by hardware after an interrupt has occurred, and is set by the RETI instruction to enable subsequent interrupts. The I-bit can also be set and cleared by the application with the SEI and CLI instructions, as described in the instruction set reference.

- **Bit 6 – T: Bit Copy Storage**

The Bit Copy instructions BLD (Bit LoaD) and BST (Bit STore) use the T-bit as source or destination for the operated bit. A bit from a register in the Register File can be copied into T by the BST instruction, and a bit in T can be copied into a bit in a register in the Register File by the BLD instruction.

- **Bit 5 – H: Half Carry Flag**

The Half Carry Flag H indicates a Half Carry in some arithmetic operations. Half Carry Is useful in BCD arithmetic. See the “Instruction Set Description” for detailed information.

- **Bit 4 – S: Sign Bit,  $S = N \oplus V$**

The S-bit is always an exclusive or between the Negative Flag N and the Two's Complement Overflow Flag V. See the “Instruction Set Description” for detailed information.

- **Bit 3 – V: Two's Complement Overflow Flag**

The Two's Complement Overflow Flag V supports two's complement arithmetics. See the “Instruction Set Description” for detailed information.

- **Bit 2 – N: Negative Flag**

The Negative Flag N indicates a negative result in an arithmetic or logic operation. See the “Instruction Set Description” for detailed information.

- **Bit 1 – Z: Zero Flag**

The Zero Flag Z indicates a zero result in an arithmetic or logic operation. See the “Instruction Set Description” for detailed information.

- **Bit 0 – C: Carry Flag**

The Carry Flag C indicates a carry in an arithmetic or logic operation. See the “Instruction Set Description” for detailed information.



## 6.4 General Purpose Register File

The Register File is optimized for the AVR Enhanced RISC instruction set. In order to achieve the required performance and flexibility, the following input/output schemes are supported by the Register File:

- One 8-bit output operand and one 8-bit result input
- Two 8-bit output operands and one 8-bit result input
- Two 8-bit output operands and one 16-bit result input
- One 16-bit output operand and one 16-bit result input

[Figure 6-2](#) shows the structure of the 32 general purpose working registers in the CPU.

**Figure 6-2.** AVR CPU General Purpose Working Registers

General Purpose Working Registers	7	0	Addr.
	R0		0x00
	R1		0x01
	R2		0x02
	...		
	R13		0x0D
	R14		0x0E
	R15		0x0F
	R16		0x10
	R17		0x11
	...		
	R26		0x1A
	R27		0x1B
	R28		0x1C
	R29		0x1D
	R30		0x1E
	R31		0x1F
			X-register Low Byte
			X-register High Byte
			Y-register Low Byte
			Y-register High Byte
			Z-register Low Byte
			Z-register High Byte

Most of the instructions operating on the Register File have direct access to all registers, and most of them are single cycle instructions.

As shown in [Figure 6-2](#), each register is also assigned a data memory address, mapping them directly into the first 32 locations of the user Data Space. Although not being physically implemented as SRAM locations, this memory organization provides great flexibility in access of the registers, as the X-, Y- and Z-pointer registers can be set to index any register in the file.

## 6.4.1 The X-register, Y-register, and Z-register

The registers R26..R31 have some added functions to their general purpose usage. These registers are 16-bit address pointers for indirect addressing of the data space. The three indirect address registers X, Y, and Z are defined as described in [Figure 6-3](#).

**Figure 6-3.** The X-, Y-, and Z-registers



In the different addressing modes these address registers have functions as fixed displacement, automatic increment, and automatic decrement (see the instruction set reference for details).

## 6.5 Stack Pointer

The Stack is mainly used for storing temporary data, for storing local variables and for storing return addresses after interrupts and subroutine calls. Note that the Stack is implemented as growing from higher to lower memory locations. The Stack Pointer Register always points to the top of the Stack. The Stack Pointer points to the data SRAM Stack area where the Subroutine and Interrupt Stacks are located. A Stack PUSH command will decrease the Stack Pointer.

The Stack in the data SRAM must be defined by the program before any subroutine calls are executed or interrupts are enabled. Initial Stack Pointer value equals the last address of the internal SRAM and the Stack Pointer must be set to point above start of the SRAM, see [Table 7-3 on page 18](#).

See [Table 6-1](#) for Stack Pointer details.

**Table 6-1.** Stack Pointer instructions

Instruction	Stack pointer	Description
PUSH	Decrement by 1	Data is pushed onto the stack
CALL ICALL RCALL	Decrement by 2	Return address is pushed onto the stack with a subroutine call or interrupt
POP	Incremented by 1	Data is popped from the stack
RET RETI	Incremented by 2	Return address is popped from the stack with return from subroutine or return from interrupt

The AVR Stack Pointer is implemented as two 8-bit registers in the I/O space. The number of bits actually used is implementation dependent. Note that the data space in some implementations of the AVR architecture is so small that only SPL is needed. In this case, the SPH Register will not be present.

## 6.5.1 SPH and SPL – Stack Pointer High and Stack Pointer Low Register

Bit	15	14	13	12	11	10	9	8	SPH
0x3E (0x5E)	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	
0x3D (0x5D)	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SPL
	7	6	5	4	3	2	1	0	
ReadWrite	R/W								
	R/W								
Initial Value	RAMEND								
	RAMEND								

## 6.6 Instruction Execution Timing

This section describes the general access timing concepts for instruction execution. The AVR CPU is driven by the CPU clock  $\text{clk}_{\text{CPU}}$ , directly generated from the selected clock source for the chip. No internal clock division is used.

Figure 6-4 shows the parallel instruction fetches and instruction executions enabled by the Harvard architecture and the fast-access Register File concept. This is the basic pipelining concept to obtain up to 1 MIPS per MHz with the corresponding unique results for functions per cost, functions per clocks, and functions per power-unit.

**Figure 6-4.** The Parallel Instruction Fetches and Instruction Executions

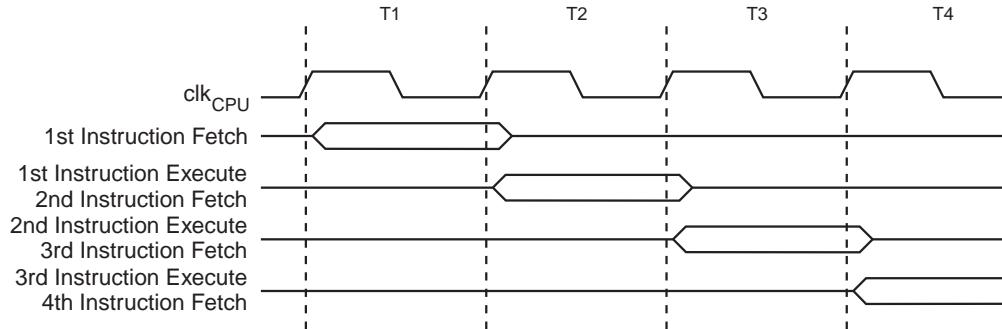
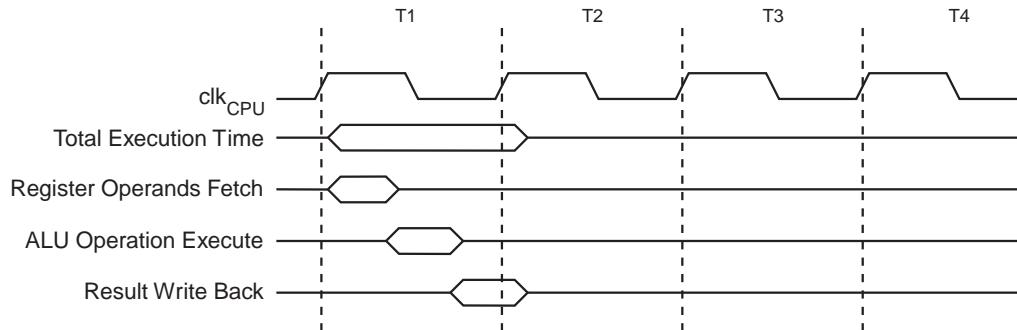


Figure 6-5 shows the internal timing concept for the Register File. In a single clock cycle an ALU operation using two register operands is executed, and the result is stored back to the destination register.

**Figure 6-5.** Single Cycle ALU Operation



## 6.7 Reset and Interrupt Handling

The AVR provides several different interrupt sources. These interrupts and the separate Reset Vector each have a separate program vector in the program memory space. All interrupts are assigned individual enable bits which must be written logic one together with the Global Interrupt Enable bit in the Status Register in order to enable the interrupt. Depending on the Program Counter value, interrupts may be automatically disabled when Boot Lock bits BLB02 or BLB12 are programmed. This feature improves software security. See the section "[Memory Programming](#)" on page 294 for details.

The lowest addresses in the program memory space are by default defined as the Reset and Interrupt Vectors. The complete list of vectors is shown in "[Interrupts](#)" on page 57. The list also determines the priority levels of the different interrupts. The lower the address the higher is the priority level. RESET has the highest priority, and next is INT0 – the External Interrupt Request 0. The Interrupt Vectors can be moved to the start of the Boot Flash section by setting the IVSEL bit in the MCU Control Register (MCUCR). Refer to "[Interrupts](#)" on page 57 for more information. The Reset Vector can also be moved to the start of the Boot Flash section by programming the BOOTRST Fuse, see "[Boot Loader Support – Read-While-Write Self-Programming, ATmega88PA, ATmega168PA and ATmega328P](#)" on page 277.

When an interrupt occurs, the Global Interrupt Enable I-bit is cleared and all interrupts are disabled. The user software can write logic one to the I-bit to enable nested interrupts. All enabled interrupts can then interrupt the current interrupt routine. The I-bit is automatically set when a Return from Interrupt instruction – RETI – is executed.

There are basically two types of interrupts. The first type is triggered by an event that sets the Interrupt Flag. For these interrupts, the Program Counter is vectored to the actual Interrupt Vector in order to execute the interrupt handling routine, and hardware clears the corresponding Interrupt Flag. Interrupt Flags can also be cleared by writing a logic one to the flag bit position(s) to be cleared. If an interrupt condition occurs while the corresponding interrupt enable bit is cleared, the Interrupt Flag will be set and remembered until the interrupt is enabled, or the flag is cleared by software. Similarly, if one or more interrupt conditions occur while the Global Interrupt Enable bit is cleared, the corresponding Interrupt Flag(s) will be set and remembered until the Global Interrupt Enable bit is set, and will then be executed by order of priority.

The second type of interrupts will trigger as long as the interrupt condition is present. These interrupts do not necessarily have Interrupt Flags. If the interrupt condition disappears before the interrupt is enabled, the interrupt will not be triggered.

When the AVR exits from an interrupt, it will always return to the main program and execute one more instruction before any pending interrupt is served.

Note that the Status Register is not automatically stored when entering an interrupt routine, nor restored when returning from an interrupt routine. This must be handled by software.

When using the CLI instruction to disable interrupts, the interrupts will be immediately disabled. No interrupt will be executed after the CLI instruction, even if it occurs simultaneously with the CLI instruction. The following example shows how this can be used to avoid interrupts during the timed EEPROM write sequence.

## Assembly Code Example

```
in r16, SREG      ; store SREG value
cli    ; disable interrupts during timed sequence
sbi EECR, EEMPE  ; start EEPROM write
sbi EECR, EEEPE
out SREG, r16     ; restore SREG value (I-bit)
```

## C Code Example

```
char cSREG;
cSREG = SREG; /* store SREG value */
/* disable interrupts during timed sequence */
_CLI();
EECR |= (1<<EEMPE); /* start EEPROM write */
EECR |= (1<<EEPE);
SREG = cSREG; /* restore SREG value (I-bit) */
```

When using the SEI instruction to enable interrupts, the instruction following SEI will be executed before any pending interrupts, as shown in this example.

## Assembly Code Example

```
sei  ; set Global Interrupt Enable
sleep; enter sleep, waiting for interrupt
; note: will enter sleep before any pending interrupt(s)
```

## C Code Example

```
__enable_interrupt(); /* set Global Interrupt Enable */
__sleep(); /* enter sleep, waiting for interrupt */
/* note: will enter sleep before any pending interrupt(s) */
```

### 6.7.1 Interrupt Response Time

The interrupt execution response for all the enabled AVR interrupts is four clock cycles minimum. After four clock cycles the program vector address for the actual interrupt handling routine is executed. During this four clock cycle period, the Program Counter is pushed onto the Stack. The vector is normally a jump to the interrupt routine, and this jump takes three clock cycles. If an interrupt occurs during execution of a multi-cycle instruction, this instruction is completed before the interrupt is served. If an interrupt occurs when the MCU is in sleep mode, the interrupt execution response time is increased by four clock cycles. This increase comes in addition to the start-up time from the selected sleep mode.

A return from an interrupt handling routine takes four clock cycles. During these four clock cycles, the Program Counter (two bytes) is popped back from the Stack, the Stack Pointer is incremented by two, and the I-bit in SREG is set.

# Adjustable 1.1A Single Resistor Low Dropout Regulator

## FEATURES

- Outputs May be Paralleled for Higher Current and Heat Spreading
- Output Current: 1.1A
- Single Resistor Programs Output Voltage
- 1% Initial Accuracy of SET Pin Current
- Output Adjustable to 0V
- Low Output Noise: 40 $\mu$ V<sub>RMS</sub> (10Hz to 100kHz)
- Wide Input Voltage Range: 1.2V to 36V
- Low Dropout Voltage: 350mV (Except SOT-223 Package)
- <1mV Load Regulation
- <0.001%/V Line Regulation
- Minimum Load Current: 0.5mA
- Stable with 2.2 $\mu$ F Minimum Ceramic Output Capacitor
- Current Limit with Foldback and Overtemperature Protected
- Available in 8-Lead MSOP, 3mm × 3mm DFN, 5-Lead DD-Pak, TO-220 and 3-Lead SOT-223

## APPLICATIONS

- High Current All Surface Mount Supply
- High Efficiency Linear Regulator
- Post Regulator for Switching Supplies
- Low Parts Count Variable Voltage Supply
- Low Output Voltage Power Supplies

## DESCRIPTION

The LT®3080 is a 1.1A low dropout linear regulator that can be paralleled to increase output current or spread heat in surface mounted boards. Architected as a precision current source and voltage follower allows this new regulator to be used in many applications requiring high current, adjustability to zero, and no heat sink. Also the device brings out the collector of the pass transistor to allow low dropout operation—down to 350 millivolts—when used with multiple supplies.

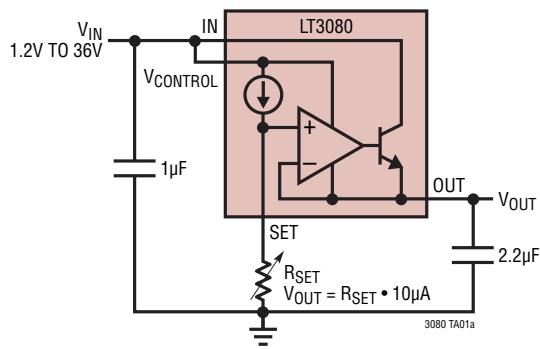
A key feature of the LT3080 is the capability to supply a wide output voltage range. By using a reference current through a single resistor, the output voltage is programmed to any level between zero and 36V. The LT3080 is stable with 2.2 $\mu$ F of capacitance on the output, and the IC uses small ceramic capacitors that do not require additional ESR as is common with other regulators.

Internal protection circuitry includes current limiting and thermal limiting. The LT3080 regulator is offered in the 8-lead MSOP (with an exposed pad for better thermal characteristics), a 3mm × 3mm DFN, 5-lead DD-Pak, TO-220 and a simple-to-use 3-lead SOT-223 version.

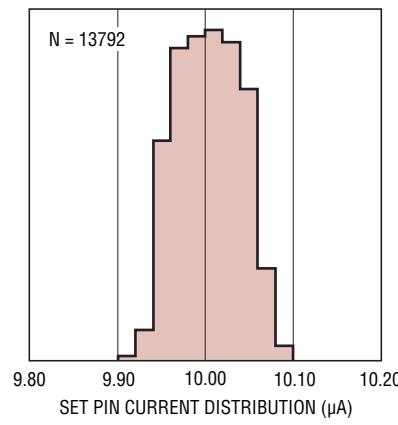
**LT**, LT, LTC, LTM, Linear Technology and the Linear logo are registered trademarks and VLDO and ThinSOT are trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners.

## TYPICAL APPLICATION

Variable Output Voltage 1.1A Supply



Set Pin Current Distribution



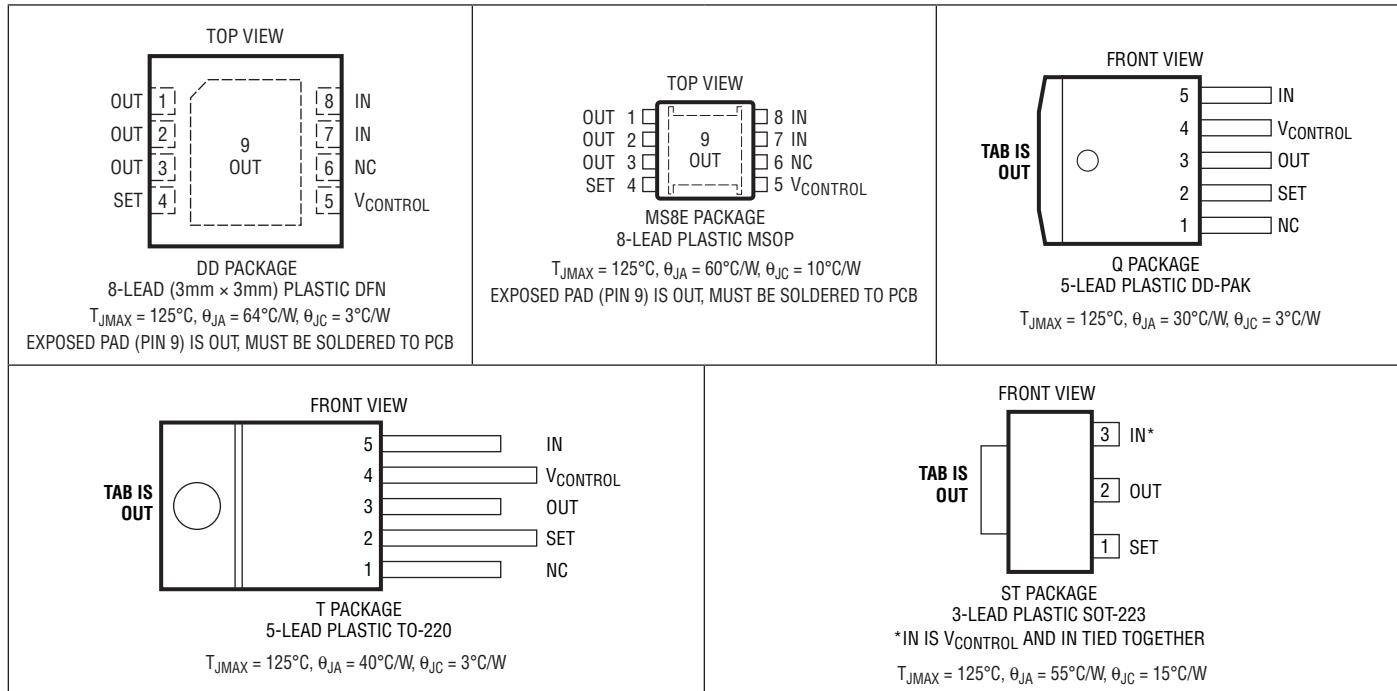
3080 G02

3080fc

## ABSOLUTE MAXIMUM RATINGS (Note 1)(All Voltages Relative to V<sub>OUT</sub>)

V <sub>CONTROL</sub> Pin Voltage.....	40V, -0.3V	Operating Junction Temperature Range (Notes 2, 10)
IN Pin Voltage .....	40V, -0.3V	E-, I-Grades..... -40°C to 125°C
SET Pin Current (Note 7) .....	±10mA	Storage Temperature Range:..... -65°C to 150°C
SET Pin Voltage (Relative to OUT) .....	±0.3V	Lead Temperature (Soldering, 10 sec)
Output Short-Circuit Duration .....	Indefinite	MS8E, Q, T and ST Packages Only..... 300°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3080EDD#PBF	LT3080EDD#TRPBF	LCBN	8-Lead (3mm x 3mm) Plastic DFN	-40°C to 125°C
LT3080IDD#PBF	LT3080IDD#TRPBF	LCBN	8-Lead (3mm x 3mm) Plastic DFN	-40°C to 125°C
LT3080EMS8E#PBF	LT3080EMS8E#TRPBF	LTCBM	8-Lead Plastic MSOP	-40°C to 125°C
LT3080IMS8E#PBF	LT3080IMS8E#TRPBF	LTCBM	8-Lead Plastic MSOP	-40°C to 125°C
LT3080EQ#PBF	LT3080EQ#TRPBF	LT3080Q	5-Lead Plastic DD-Pak	-40°C to 125°C
LT3080IQ#PBF	LT3080IQ#TRPBF	LT3080Q	5-Lead Plastic DD-Pak	-40°C to 125°C
LT3080ET#PBF	LT3080ET#TRPBF	LT3080ET	5-Lead Plastic TO-220	-40°C to 125°C
LT3080IT#PBF	LT3080IT#TRPBF	LT3080ET	5-Lead Plastic TO-220	-40°C to 125°C
LT3080EST#PBF	LT3080EST#TRPBF	3080	3-Lead Plastic SOT-223	-40°C to 125°C
LT3080IST#PBF	LT3080IST#TRPBF	3080	3-Lead Plastic SOT-223	-40°C to 125°C
LEAD BASED FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3080EDD	LT3080EDD#TR	LCBN	8-Lead (3mm x 3mm) Plastic DFN	-40°C to 125°C
LT3080IDD	LT3080IDD#TR	LCBN	8-Lead (3mm x 3mm) Plastic DFN	-40°C to 125°C
LT3080EMS8E	LT3080EMS8E#TR	LTCBM	8-Lead Plastic MSOP	-40°C to 125°C
LT3080IMS8E	LT3080IMS8E#TR	LTCBM	8-Lead Plastic MSOP	-40°C to 125°C
LT3080EQ	LT3080EQ#TR	LT3080Q	5-Lead Plastic DD-Pak	-40°C to 125°C
LT3080IQ	LT3080IQ#TR	LT3080Q	5-Lead Plastic DD-Pak	-40°C to 125°C
LT3080ET	LT3080ET#TR	LT3080ET	5-Lead Plastic TO-220	-40°C to 125°C
LT3080IT	LT3080IT#TR	LT3080ET	5-Lead Plastic TO-220	-40°C to 125°C
LT3080EST	LT3080EST#TR	3080	3-Lead Plastic SOT-223	-40°C to 125°C
LT3080IST	LT3080IST#TR	3080	3-Lead Plastic SOT-223	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

**ELECTRICAL CHARACTERISTICS**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 11)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SET Pin Current	$I_{\text{SET}}$ $V_{\text{IN}} = 1\text{V}$ , $V_{\text{CONTROL}} = 2.0\text{V}$ , $I_{\text{LOAD}} = 1\text{mA}$ , $T_J = 25^\circ\text{C}$ $V_{\text{IN}} \geq 1\text{V}$ , $V_{\text{CONTROL}} \geq 2.0\text{V}$ , $1\text{mA} \leq I_{\text{LOAD}} \leq 1.1\text{A}$ (Note 9)	● 9.90 9.80	10	10.10 10.20	$\mu\text{A}$ $\mu\text{A}$
Output Offset Voltage ( $V_{\text{OUT}} - V_{\text{SET}}$ ) $V_{\text{IN}} = 1\text{V}$ , $V_{\text{CONTROL}} = 2\text{V}$ , $I_{\text{OUT}} = 1\text{mA}$	DFN and MSOP Package	● -2 -3.5	2	3.5	$\text{mV}$ $\text{mV}$
	SOT-223, DD-Pak and T0-220 Package	● -5 -6	5	6	$\text{mV}$ $\text{mV}$
Load Regulation	$\Delta I_{\text{SET}}$ $\Delta V_{\text{OS}}$ $\Delta I_{\text{LOAD}} = 1\text{mA}$ to $1.1\text{A}$ $\Delta I_{\text{LOAD}} = 1\text{mA}$ to $1.1\text{A}$ (Note 8)	● -0.1 0.6	0.6	1.3	$\text{nA}$ $\text{mV}$
Line Regulation (Note 9) DFN and MSOP Package	$\Delta I_{\text{SET}}$ $\Delta V_{\text{OS}}$ $V_{\text{IN}} = 1\text{V}$ to $25\text{V}$ , $V_{\text{CONTROL}} = 2\text{V}$ to $25\text{V}$ , $I_{\text{LOAD}} = 1\text{mA}$ $V_{\text{IN}} = 1\text{V}$ to $25\text{V}$ , $V_{\text{CONTROL}} = 2\text{V}$ to $25\text{V}$ , $I_{\text{LOAD}} = 1\text{mA}$	● 0.1 0.003	0.1	0.5	$\text{nA/V}$ $\text{mV/V}$
Line Regulation (Note 9) SOT-223, DD-Pak and T0-220 Package	$\Delta I_{\text{SET}}$ $\Delta V_{\text{OS}}$ $V_{\text{IN}} = 1\text{V}$ to $26\text{V}$ , $V_{\text{CONTROL}} = 2\text{V}$ to $26\text{V}$ , $I_{\text{LOAD}} = 1\text{mA}$ $V_{\text{IN}} = 1\text{V}$ to $26\text{V}$ , $V_{\text{CONTROL}} = 2\text{V}$ to $26\text{V}$ , $I_{\text{LOAD}} = 1\text{mA}$	● 0.1 0.003	0.1	0.5	$\text{nA/V}$ $\text{mV/V}$
Minimum Load Current (Notes 3, 9)	$V_{\text{IN}} = V_{\text{CONTROL}} = 10\text{V}$ $V_{\text{IN}} = V_{\text{CONTROL}} = 25\text{V}$ (DFN and MSOP Package) $V_{\text{IN}} = V_{\text{CONTROL}} = 26\text{V}$ (SOT-223, DD-Pak and T0-220 Package)	● 300 ● 1 ● 1	500 1 1	$\mu\text{A}$ $\text{mA}$ $\text{mA}$	
$V_{\text{CONTROL}}$ Dropout Voltage (Note 4)	$I_{\text{LOAD}} = 100\text{mA}$ $I_{\text{LOAD}} = 1.1\text{A}$	● 1.2 ● 1.35	1.2 1.6	V V	
$V_{\text{IN}}$ Dropout Voltage (Note 4)	$I_{\text{LOAD}} = 100\text{mA}$ $I_{\text{LOAD}} = 1.1\text{A}$	● 100 ● 350	200 500	$\text{mV}$ $\text{mV}$	
$V_{\text{CONTROL}}$ Pin Current	$I_{\text{LOAD}} = 100\text{mA}$ $I_{\text{LOAD}} = 1.1\text{A}$	● 4 ● 17	6 30	$\text{mA}$ $\text{mA}$	
Current Limit	$V_{\text{IN}} = 5\text{V}$ , $V_{\text{CONTROL}} = 5\text{V}$ , $V_{\text{SET}} = 0\text{V}$ , $V_{\text{OUT}} = -0.1\text{V}$	● 1.1	1.4	A	
Error Amplifier RMS Output Noise (Note 6)	$I_{\text{LOAD}} = 1.1\text{A}$ , $10\text{Hz} \leq f \leq 100\text{kHz}$ , $C_{\text{OUT}} = 10\mu\text{F}$ , $C_{\text{SET}} = 0.1\mu\text{F}$		40	$\mu\text{VRMS}$	
Reference Current RMS Output Noise (Note 6)	$10\text{Hz} \leq f \leq 100\text{kHz}$		1	$\text{nARMS}$	
Ripple Rejection	$f = 120\text{Hz}$ , $V_{\text{RIPPLE}} = 0.5\text{V}_{\text{P-P}}$ , $I_{\text{LOAD}} = 0.2\text{A}$ , $C_{\text{SET}} = 0.1\mu\text{F}$ , $C_{\text{OUT}} = 2.2\mu\text{F}$ $f = 10\text{kHz}$ $f = 1\text{MHz}$		75 55 20	$\text{dB}$ $\text{dB}$ $\text{dB}$	
Thermal Regulation, $I_{\text{SET}}$	10ms Pulse		0.003	%/W	

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Unless otherwise specified, all voltages are with respect to  $V_{\text{OUT}}$ . The LT3080 is tested and specified under pulse load conditions such that  $T_J \equiv T_A$ . The LT3080E is tested at  $T_A = 25^\circ\text{C}$ . Performance of the LT3080E over the full  $-40^\circ\text{C}$  and  $125^\circ\text{C}$  operating temperature range is assured by design, characterization, and correlation with statistical process controls. The LT3080I is guaranteed over the full  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  operating junction temperature range.

**Note 3:** Minimum load current is equivalent to the quiescent current of the part. Since all quiescent and drive current is delivered to the output of the part, the minimum load current is the minimum current required to maintain regulation.

**Note 4:** For the LT3080, dropout is caused by either minimum control voltage ( $V_{\text{CONTROL}}$ ) or minimum input voltage ( $V_{\text{IN}}$ ). Both parameters are specified with respect to the output voltage. The specifications represent the minimum input-to-output differential voltage required to maintain regulation.

**Note 5:** The  $V_{\text{CONTROL}}$  pin current is the drive current required for the output transistor. This current will track output current with roughly a 1:6 ratio. The minimum value is equal to the quiescent current of the device.

**Note 6:** Output noise is lowered by adding a small capacitor across the voltage setting resistor. Adding this capacitor bypasses the voltage setting resistor shot noise and reference current noise; output noise is then equal to error amplifier noise (see Applications Information section).

**Note 7:** SET pin is clamped to the output with diodes. These diodes only carry current under transient overloads.

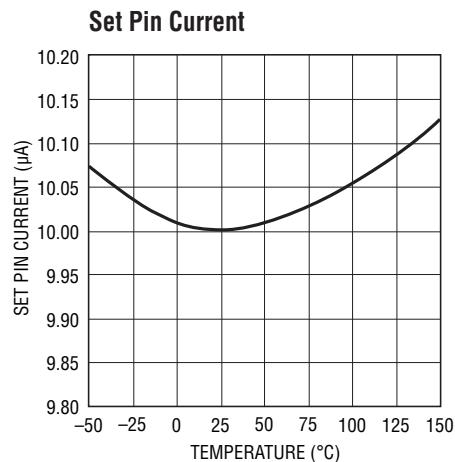
**Note 8:** Load regulation is Kelvin sensed at the package.

**Note 9:** Current limit may decrease to zero at input-to-output differential voltages ( $V_{\text{IN}} - V_{\text{OUT}}$ ) greater than  $25\text{V}$  (DFN and MSOP package) or  $26\text{V}$  (SOT-223, DD-Pak and T0-220 Package). Operation at voltages for both IN and  $V_{\text{CONTROL}}$  is allowed up to a maximum of  $36\text{V}$  as long as the difference between input and output voltage is below the specified differential ( $V_{\text{IN}} - V_{\text{OUT}}$ ) voltage. Line and load regulation specifications are not applicable when the device is in current limit.

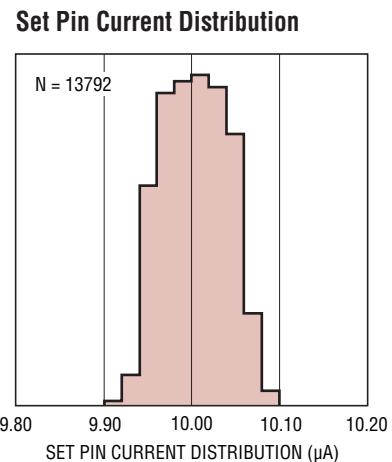
**Note 10:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

**Note 11:** The SOT-223 package connects the IN and  $V_{\text{CONTROL}}$  pins together internally. Therefore, test conditions for this pin follow the  $V_{\text{CONTROL}}$  conditions listed in the Electrical Characteristics Table.

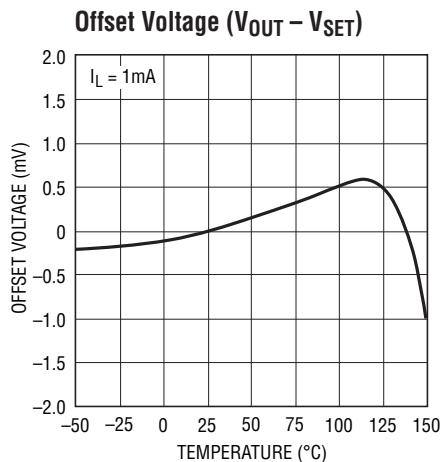
## TYPICAL PERFORMANCE CHARACTERISTICS



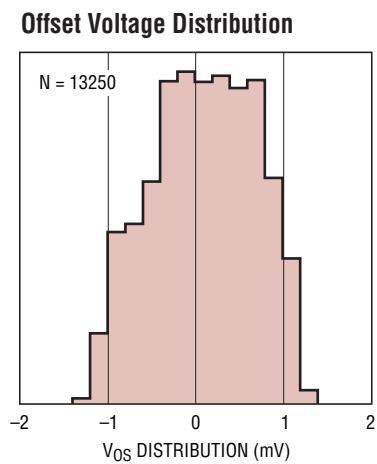
3080 G01



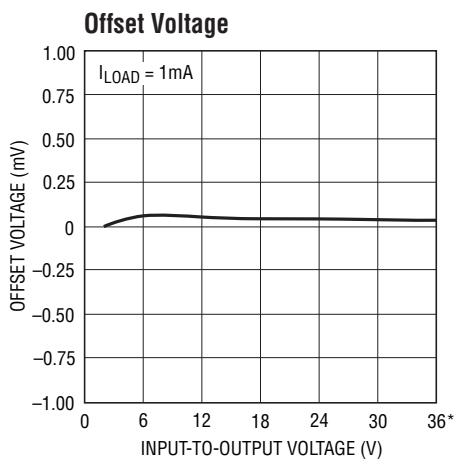
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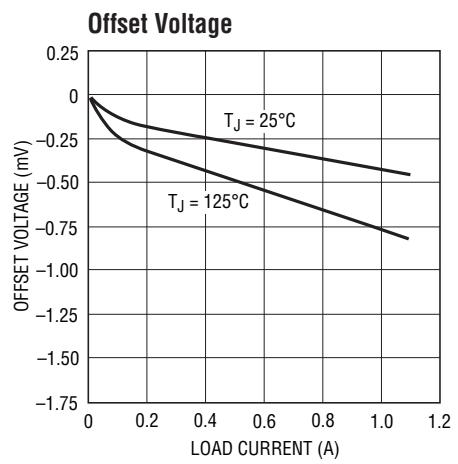
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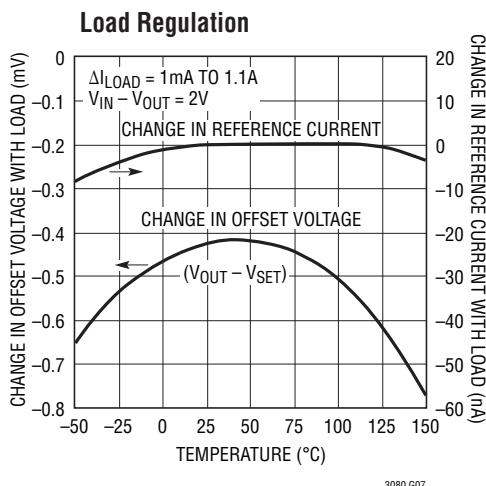
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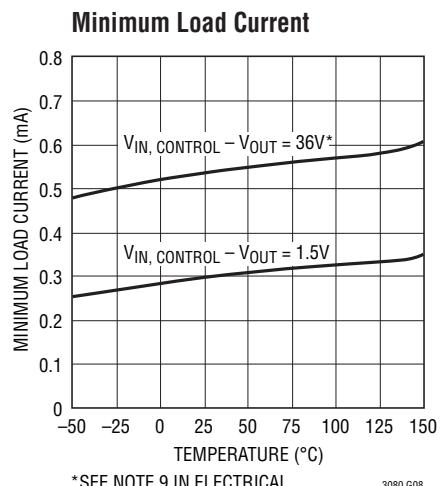
\* SEE NOTE 9 IN ELECTRICAL CHARACTERISTICS TABLE



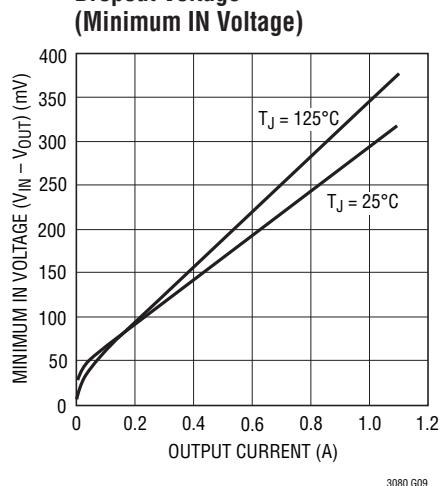
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3080 G07

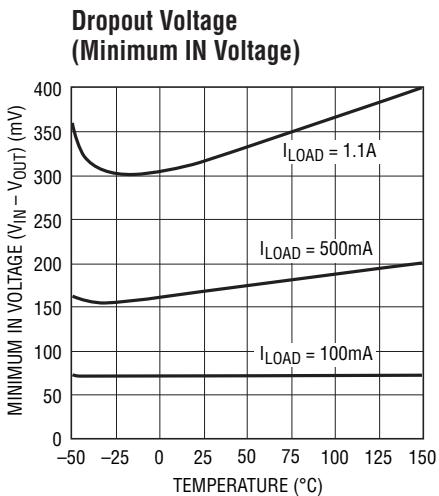


\* SEE NOTE 9 IN ELECTRICAL CHARACTERISTICS TABLE

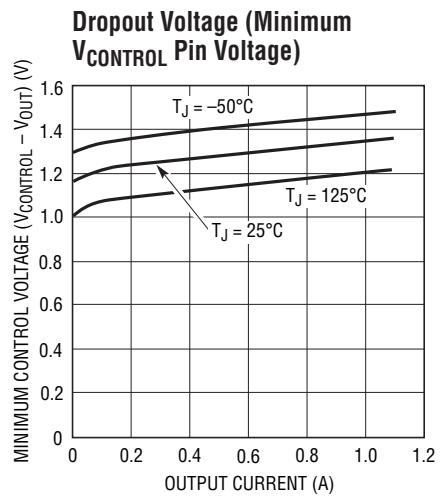


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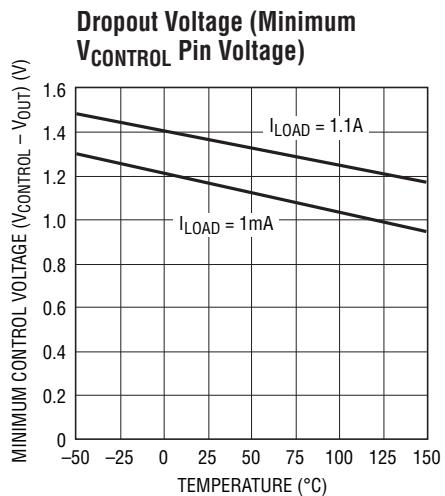
## TYPICAL PERFORMANCE CHARACTERISTICS



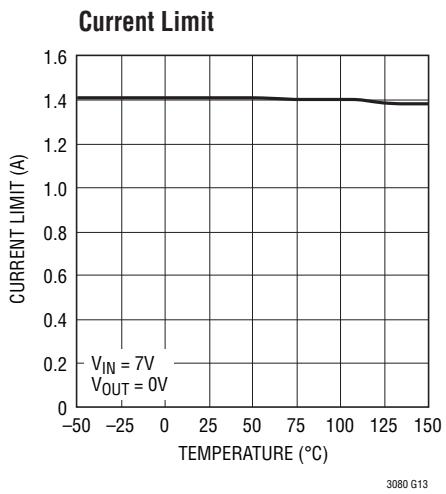
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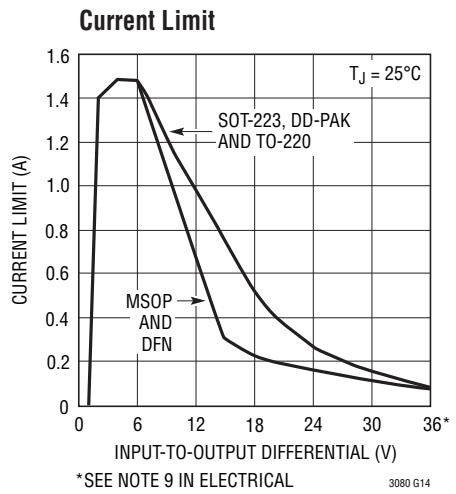
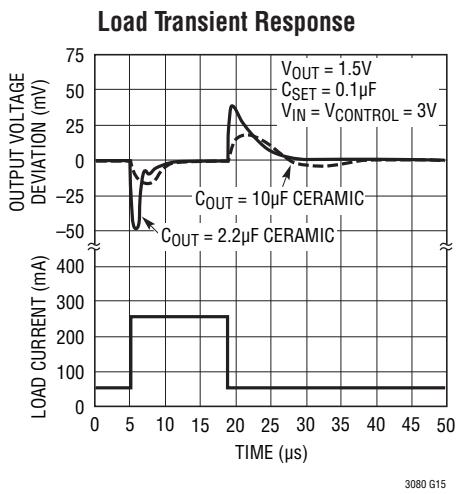
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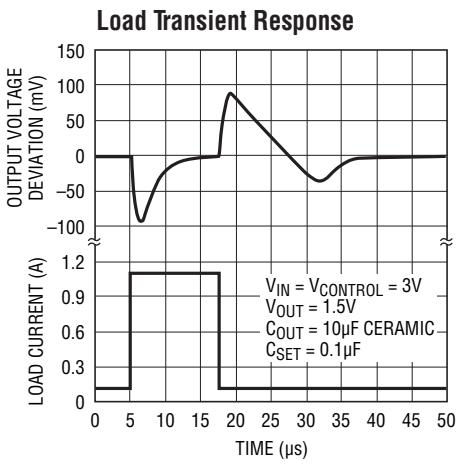
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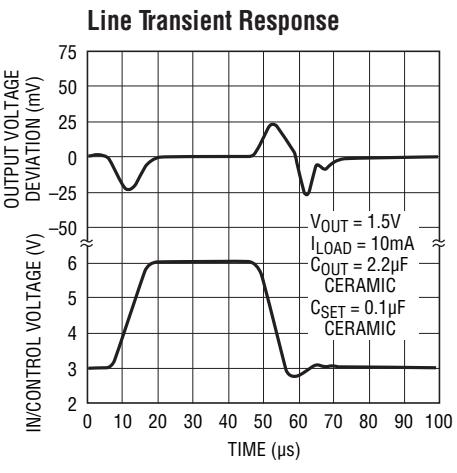
3080 G13

\* SEE NOTE 9 IN ELECTRICAL CHARACTERISTICS TABLE  
3080 G14

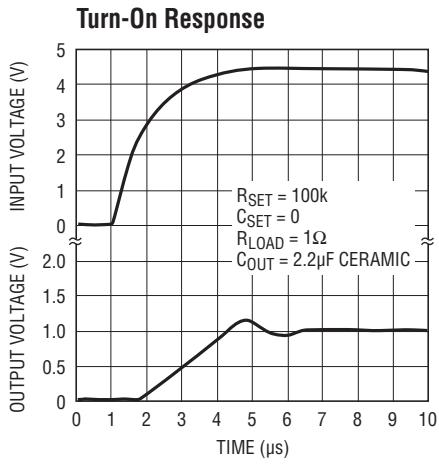
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3080 G16

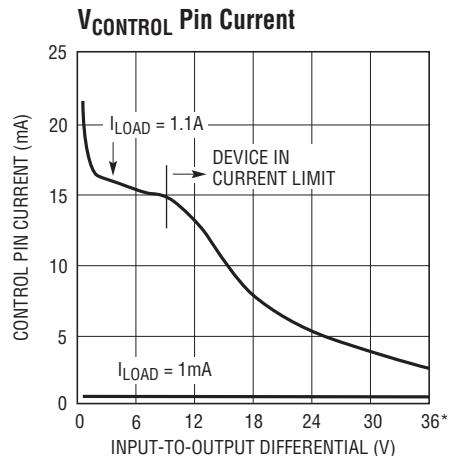


3080 G17



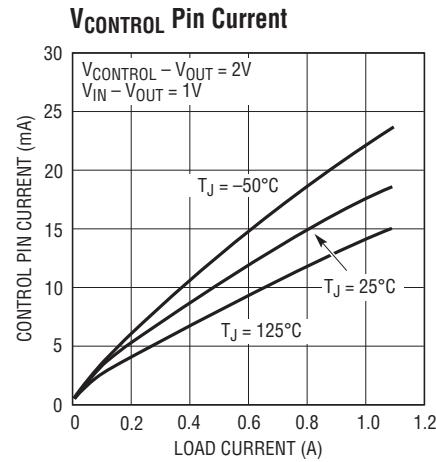
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## TYPICAL PERFORMANCE CHARACTERISTICS



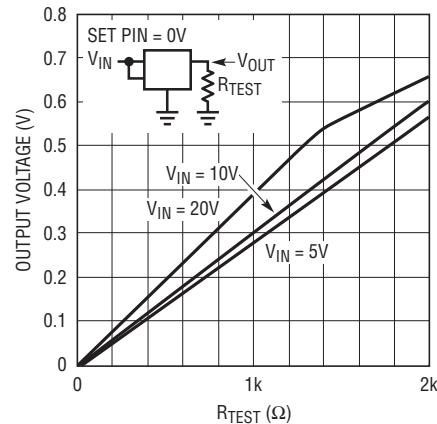
\*SEE NOTE 9 IN ELECTRICAL CHARACTERISTICS TABLE

3080 G19

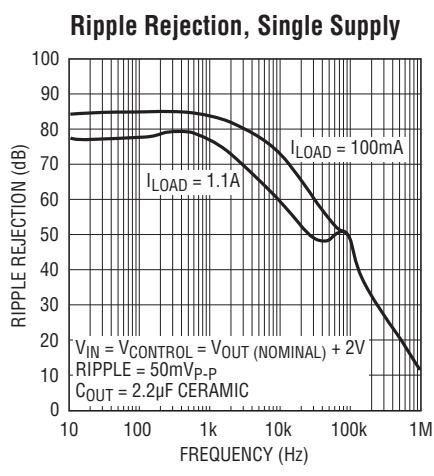


3080 G20

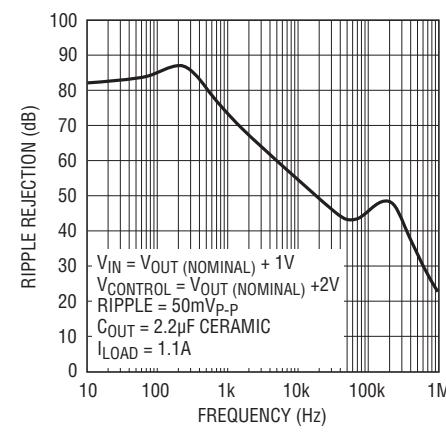
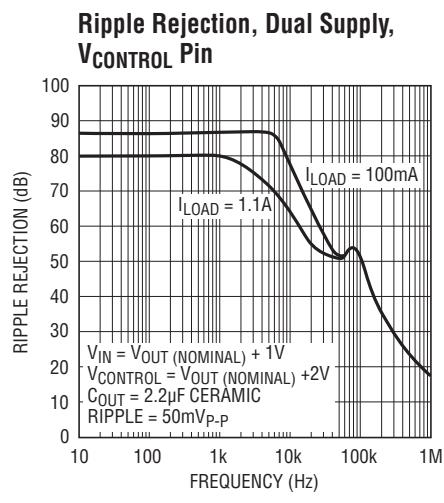
### Residual Output Voltage with Less Than Minimum Load



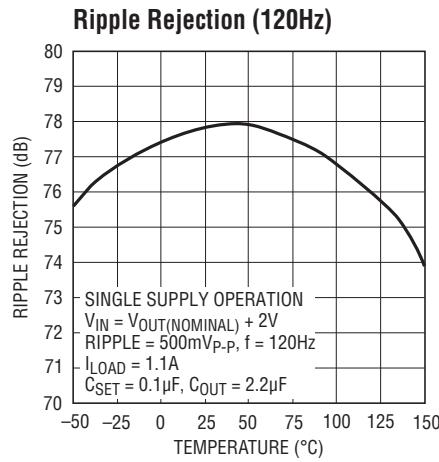
3080 G21



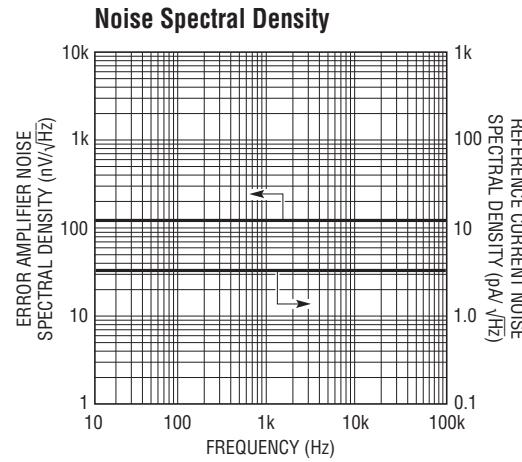
3080 G22



3080 G24

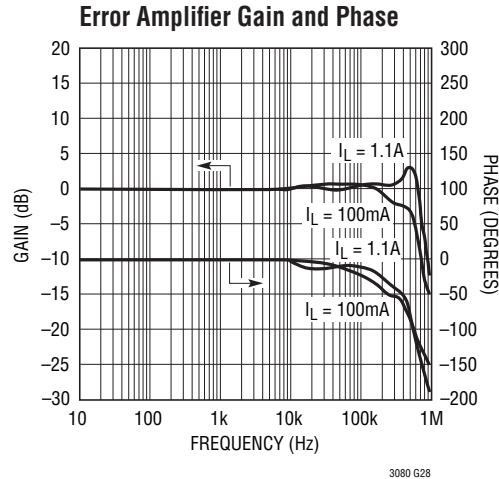
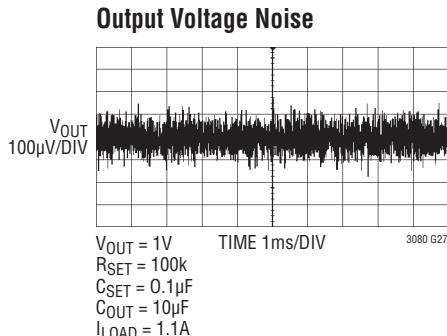


3080 G25



3080 G26

## TYPICAL PERFORMANCE CHARACTERISTICS



## PIN FUNCTIONS (DD/MS8E/Q/T/ST)

**V<sub>CONTROL</sub> (Pin 5/Pin 5/Pin 4/Pin 4/NA):** This pin is the supply pin for the control circuitry of the device. The current flow into this pin is about 1.7% of the output current. For the device to regulate, this voltage must be more than 1.2V to 1.35V greater than the output voltage (see dropout specifications).

**IN (Pins 7, 8/Pins 7, 8/Pin 5/Pin 3):** This is the collector to the power device of the LT3080. The output load current is supplied through this pin. For the device to regulate, the voltage at this pin must be more than 0.1V to 0.5V greater than the output voltage (see dropout specifications).

**NC (Pin 6/Pin 6/Pin 1/Pin 1/NA):** No Connection. No connect pins have no connection to internal circuitry and may be tied to V<sub>IN</sub>, V<sub>CONTROL</sub>, V<sub>OUT</sub>, GND or floated.

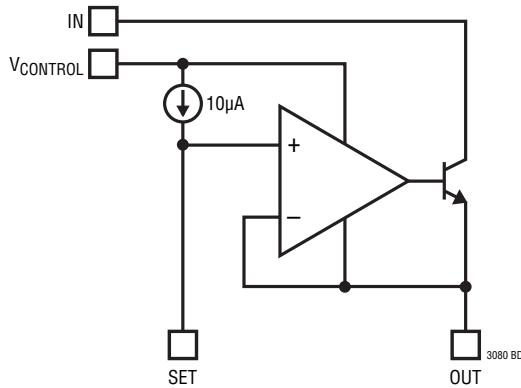
**OUT (Pins 1-3/Pins 1-3/Pin 3/Pin 2):** This is the power output of the device. There must be a minimum load current of 1mA or the output may not regulate.

**SET (Pin 4/Pin 4/Pin 2/Pin 1):** This pin is the input to the error amplifier and the regulation set point for the device. A fixed current of 10µA flows out of this pin through a single external resistor, which programs the output voltage of the device. Output voltage range is zero to the absolute maximum rated output voltage. Transient performance can be improved by adding a small capacitor from the SET pin to ground.

**Exposed Pad (Pin 9/Pin 9/NA/NA/NA):** OUT on MS8E and DFN packages.

**TAB:** OUT on DD-Pak, TO-220 and SOT-223 packages.

## BLOCK DIAGRAM



## APPLICATIONS INFORMATION

The LT3080 regulator is easy to use and has all the protection features expected in high performance regulators. Included are short-circuit protection and safe operating area protection, as well as thermal shutdown.

The LT3080 is especially well suited to applications needing multiple rails. The new architecture adjusts down to zero with a single resistor handling modern low voltage digital IC's as well as allowing easy parallel operation and thermal management without heat sinks. Adjusting to "zero" output allows shutting off the powered circuitry and when the input is pre-regulated—such as a 5V or 3.3V input supply—external resistors can help spread the heat.

A precision "0" TC  $10\mu\text{A}$  internal current source is connected to the noninverting input of a power operational amplifier. The power operational amplifier provides a low impedance buffered output to the voltage on the noninverting input. A single resistor from the noninverting input to ground sets the output voltage and if this resistor is set to zero, zero output results. As can be seen, any output voltage can be obtained from zero up to the maximum defined by the input power supply.

What is not so obvious from this architecture are the benefits of using a true internal current source as the reference as opposed to a bootstrapped reference in older regulators. A true current source allows the regulator to have gain and frequency response independent of the impedance on the positive input. Older adjustable regulators, such as the

LT1086 have a change in loop gain with output voltage as well as bandwidth changes when the adjustment pin is bypassed to ground. For the LT3080, the loop gain is unchanged by changing the output voltage or bypassing. Output regulation is not fixed at a percentage of the output voltage but is a fixed fraction of millivolts. Use of a true current source allows all the gain in the buffer amplifier to provide regulation and none of that gain is needed to amplify up the reference to a higher output voltage.

The LT3080 has the collector of the output transistor connected to a separate pin from the control input. Since the dropout on the collector (IN pin) is only 350mV, two supplies can be used to power the LT3080 to reduce dissipation: a higher voltage supply for the control circuitry and a lower voltage supply for the collector. This increases efficiency and reduces dissipation. To further spread the heat, a resistor can be inserted in series with the collector to move some of the heat out of the IC and spread it on the PC board.

The LT3080 can be operated in two modes. Three-terminal mode has the control pin connected to the power input pin which gives a limitation of 1.35V dropout. Alternatively, the "control" pin can be tied to a higher voltage and the power IN pin to a lower voltage giving 350mV dropout on the IN pin and minimizing the power dissipation. This allows for a 1.1A supply regulating from  $2.5V_{IN}$  to  $1.8V_{OUT}$  or  $1.8V_{IN}$  to  $1.2V_{OUT}$  with low dissipation.

## APPLICATIONS INFORMATION

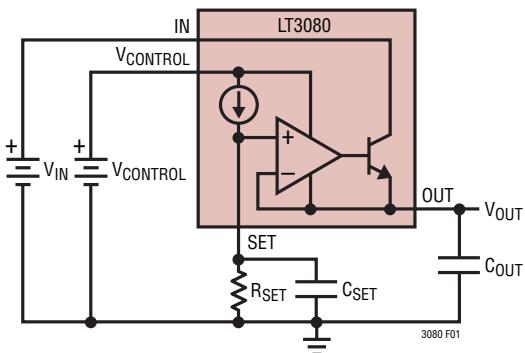


Figure 1. Basic Adjustable Regulator

## Output Voltage

The LT3080 generates a  $10\mu\text{A}$  reference current that flows out of the SET pin. Connecting a resistor from SET to ground generates a voltage that becomes the reference point for the error amplifier (see Figure 1). The reference voltage is a straight multiplication of the SET pin current and the value of the resistor. Any voltage can be generated and there is no minimum output voltage for the regulator. A minimum load current of  $1\text{mA}$  is required to maintain regulation regardless of output voltage. For true zero voltage output operation, this  $1\text{mA}$  load current must be returned to a negative supply voltage.

With the low level current used to generate the reference voltage, leakage paths to or from the SET pin can create errors in the reference and output voltages. High quality insulation should be used (e.g., Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the SET pin and circuitry with a guard ring operated at a potential close to itself; the guard ring should be tied to the OUT pin. Guarding both sides of the circuit board is required. Bulk leakage reduction depends on the guard ring width. Ten nanoamperes of leakage into or out of the SET pin and associated circuitry creates a 0.1% error in the reference voltage. Leakages of this magnitude, coupled with other sources of leakage, can cause significant offset voltage and reference drift, especially over the possible operating temperature range.

If guarding techniques are used, this bootstraps any stray capacitance at the SET pin. Since the SET pin is a high impedance node, unwanted signals may couple into the SET pin and cause erratic behavior. This will be most noticeable when operating with minimum output capacitors at full load current. The easiest way to remedy this is to bypass the SET pin with a small amount of capacitance from SET to ground,  $10\text{pF}$  to  $20\text{pF}$  is sufficient.

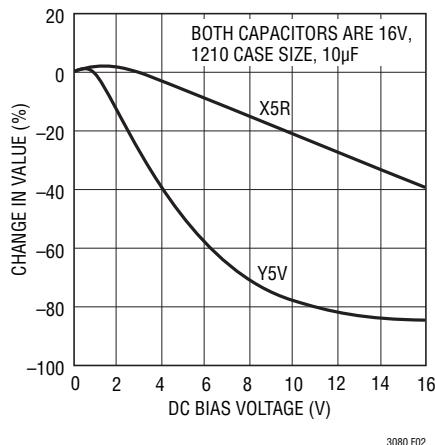
## Stability and Output Capacitance

The LT3080 requires an output capacitor for stability. It is designed to be stable with most low ESR capacitors (typically ceramic, tantalum or low ESR electrolytic). A minimum output capacitor of  $2.2\mu\text{F}$  with an ESR of  $0.5\Omega$  or less is recommended to prevent oscillations. Larger values of output capacitance decrease peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the LT3080, increase the effective output capacitor value.

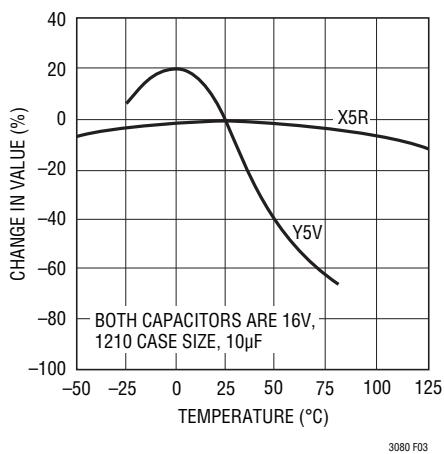
For improvement in transient performance, place a capacitor across the voltage setting resistor. Capacitors up to  $1\mu\text{F}$  can be used. This bypass capacitor reduces system noise as well, but start-up time is proportional to the time constant of the voltage setting resistor ( $R_{SET}$  in Figure 1) and SET pin bypass capacitor.

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but they tend to have strong voltage and temperature coefficients as shown in Figures 2 and 3. When used with a  $5\text{V}$  regulator, a  $16\text{V}$   $10\mu\text{F}$  Y5V capacitor can exhibit an effective value as low as  $1\mu\text{F}$  to  $2\mu\text{F}$  for the DC bias voltage applied and over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is

## APPLICATIONS INFORMATION



**Figure 2. Ceramic Capacitor DC Bias Characteristics**



**Figure 3. Ceramic Capacitor Temperature Characteristics**

available in higher values. Care still must be exercised when using X5R and X7R capacitors; the X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases, but expected capacitance at operating voltage should be verified.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric microphone works. For a

ceramic capacitor the stress can be induced by vibrations in the system or thermal transients.

### Paralleling Devices

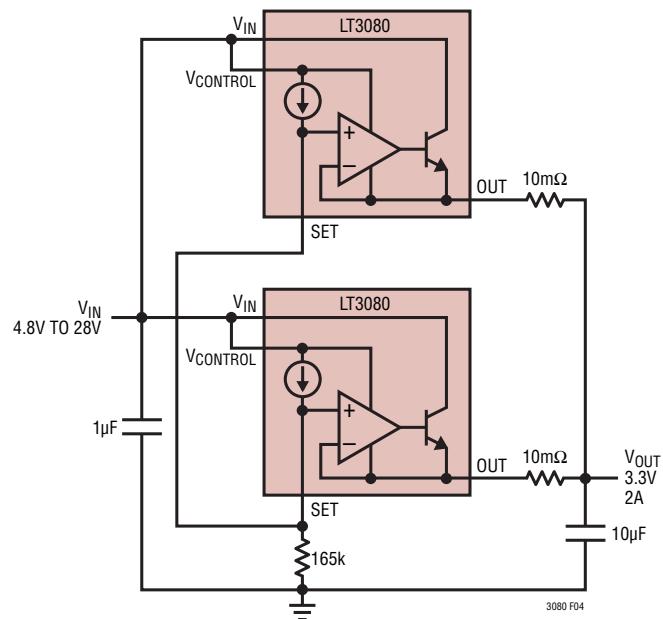
LT3080's may be paralleled to obtain higher output current. The SET pins are tied together and the IN pins are tied together. This is the same whether it's in three terminal mode or has separate input supplies. The outputs are connected in common using a small piece of PC trace as a ballast resistor to equalize the currents. PC trace resistance in milliohms/inch is shown in Table 1. Only a tiny area is needed for ballasting.

**Table 1. PC Board Trace Resistance**

WEIGHT (oz)	10 mil WIDTH	20 mil WIDTH
1	54.3	27.1
2	27.1	13.6

Trace resistance is measured in mOhms/in

The worse case offset between the set pin and the output of only  $\pm 2$  millivolts allows very small ballast resistors to be used. As shown in Figure 4, the two devices have a small 10 milliohm ballast resistor, which at full output current gives better than 80 percent equalized sharing of the current. The external resistance of 10 milliohms



**Figure 4. Parallel Devices**

## APPLICATIONS INFORMATION

(5 milliohms for the two devices in parallel) only adds about 10 millivolts of output regulation drop at an output of 2A. Even with an output voltage as low as 1V, this only adds 1% to the regulation. Of course, more than two LT3080's can be paralleled for even higher output current. They are spread out on the PC board, spreading the heat. Input resistors can further spread the heat if the input-to-output difference is high.

### Thermal Performance

In this example, two LT3080 3mm × 3mm DFN devices are mounted on a 1oz copper 4-layer PC board. They are placed approximately 1.5 inches apart and the board is mounted vertically for convection cooling. Two tests were set up to measure the cooling performance and current sharing of these devices.

The first test was done with approximately 0.7V input-to-output and 1A per device. This gave a 700 milliwatt dissipation in each device and a 2A output current. The temperature rise above ambient is approximately 28°C and both devices were within plus or minus 1°C. Both the thermal and electrical sharing of these devices is excellent. The thermograph in Figure 5 shows the temperature distribution between these devices and the PC board reaches ambient temperature within about a half an inch from the devices.

The power is then increased with 1.7V across each device. This gives 1.7 watts dissipation in each device and a device

temperature of about 90°C, about 65°C above ambient as shown in Figure 6. Again, the temperature matching between the devices is within 2°C, showing excellent tracking between the devices. The board temperature has reached approximately 40°C within about 0.75 inches of each device.

While 90°C is an acceptable operating temperature for these devices, this is in 25°C ambient. For higher ambients, the temperature must be controlled to prevent device temperature from exceeding 125°C. A 3-meter-per-second airflow across the devices will decrease the device temperature about 20°C providing a margin for higher operating ambient temperatures.

Both at low power and relatively high power levels devices can be paralleled for higher output current. Current sharing and thermal sharing is excellent, showing that acceptable operation can be had while keeping the peak temperatures below excessive operating temperatures on a board. This technique allows higher operating current linear regulation to be used in systems where it could never be used before.

### Quieting the Noise

The LT3080 offers numerous advantages when it comes to dealing with noise. There are several sources of noise in a linear regulator. The most critical noise source for any LDO is the reference; from there, the noise contribution

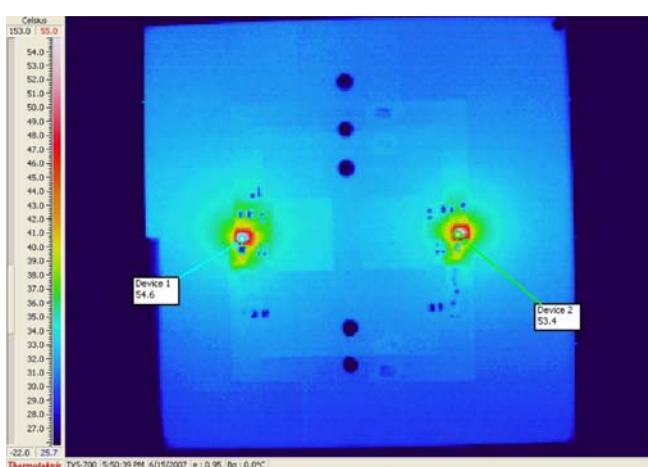


Figure 5. Temperature Rise at 700mW Dissipation

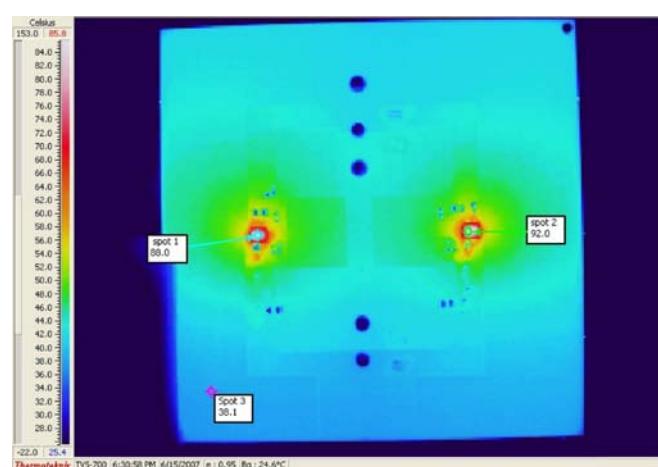


Figure 6. Temperature Rise at 1.7W Dissipation

## APPLICATIONS INFORMATION

from the error amplifier must be considered, and the gain created by using a resistor divider cannot be forgotten.

Traditional low noise regulators bring the voltage reference out to an external pin (usually through a large value resistor) to allow for bypassing and noise reduction of reference noise. The LT3080 does not use a traditional voltage reference like other linear regulators, but instead uses a reference current. That current operates with typical noise current levels of  $3.2\text{pA}/\sqrt{\text{Hz}}$  ( $1\text{nA}_{\text{RMS}}$  over the 10Hz to 100kHz bandwidth). The voltage noise of this is equal to the noise current multiplied by the resistor value. The resistor generates spot noise equal to  $\sqrt{4kT}$  ( $k = \text{Boltzmann's constant, } 1.38 \cdot 10^{-23} \text{ J/K}$ , and  $T$  is absolute temperature) which is RMS summed with the reference current noise. To lower reference noise, the voltage setting resistor may be bypassed with a capacitor, though this causes start-up time to increase as a factor of the RC time constant.

The LT3080 uses a unity-gain follower from the SET pin to drive the output, and there is no requirement to use a resistor to set the output voltage. Use a high accuracy voltage reference placed at the SET pin to remove the errors in output voltage due to reference current tolerance and resistor tolerance. Active driving of the SET pin is acceptable; the limitations are the creativity and ingenuity of the circuit designer.

One problem that a normal linear regulator sees with reference voltage noise is that noise is gained up along with the output when using a resistor divider to operate at levels higher than the normal reference voltage. With the LT3080, the unity-gain follower presents no gain whatsoever from the SET pin to the output, so noise figures do not increase accordingly. Error amplifier noise is typically  $125\text{nV}/\sqrt{\text{Hz}}$  ( $40\mu\text{V}_{\text{RMS}}$  over the 10Hz to 100kHz bandwidth); this is another factor that is RMS summed in to give a final noise figure for the regulator.

Curves in the Typical Performance Characteristics show noise spectral density and peak-to-peak noise characteristics for both the reference current and error amplifier over the 10Hz to 100kHz bandwidth.

### Overload Recovery

Like many IC power regulators, the LT3080 has safe operating area (SOA) protection. The SOA protection decreases

current limit as the input-to-output voltage increases and keeps the power dissipation at safe levels for all values of input-to-output voltage. The LT3080 provides some output current at all values of input-to-output voltage up to the device breakdown. See the Current Limit curve in the Typical Performance Characteristics.

When power is first turned on, the input voltage rises and the output follows the input, allowing the regulator to start into very heavy loads. During start-up, as the input voltage is rising, the input-to-output voltage differential is small, allowing the regulator to supply large output currents. With a high input voltage, a problem can occur wherein removal of an output short will not allow the output voltage to recover. Other regulators, such as the LT1085 and LT1764A, also exhibit this phenomenon so it is not unique to the LT3080.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations are immediately after the removal of a short circuit. The load line for such a load may intersect the output current curve at two points. If this happens, there are two stable operating points for the regulator. With this double intersection, the input power supply may need to be cycled down to zero and brought up again to make the output recover.

### Load Regulation

Because the LT3080 is a floating device (there is no ground pin on the part, all quiescent and drive current is delivered to the load), it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance

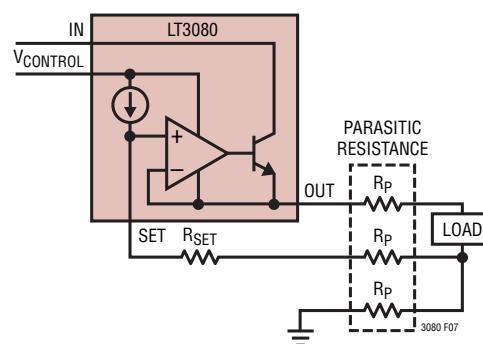


Figure 7. Connections for Best Load Regulation

## APPLICATIONS INFORMATION

of the connections between the regulator and the load. The data sheet specification for load regulation is Kelvin sensed at the pins of the package. Negative side sensing is a true Kelvin connection, with the bottom of the voltage setting resistor returned to the negative side of the load (see Figure 7). Connected as shown, system load regulation will be the sum of the LT3080 load regulation and the parasitic line resistance multiplied by the output current. It is important to keep the positive connection between the regulator and load as short as possible and use large wire or PC board traces.

### Thermal Considerations

The LT3080 has internal power and thermal limiting circuitry designed to protect it under overload conditions. For continuous normal load conditions, maximum junction temperature must not be exceeded. It is important to give consideration to all sources of thermal resistance from junction to ambient. This includes junction-to-case, case-to-heat sink interface, heat sink resistance or circuit board-to-ambient as the application dictates. Additional heat sources nearby must also be considered.

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Surface mount heat sinks and plated through-holes can also be used to spread the heat generated by power devices.

Junction-to-case thermal resistance is specified from the IC junction to the bottom of the case directly below the die. This is the lowest resistance path for heat flow. Proper mounting is required to ensure the best possible thermal flow from this area of the package to the heat sinking material. For the TO-220 package, thermal compound is strongly recommended for mechanical connections to a heat sink. A thermally conductive spacer can be used for electrical isolation as long as the added contribution to thermal resistance is considered. **Note that the Tab or Exposed Pad (depending on package) is electrically connected to the output.**

The following tables list thermal resistance for several different copper areas given a fixed board size. All measurements were taken in still air on two-sided 1/16" FR-4 board with one ounce copper.

**Table 2. MSE Package, 8-Lead MSOP**

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE*	BACKSIDE		
2500mm <sup>2</sup>	2500mm <sup>2</sup>	2500mm <sup>2</sup>	55°C/W
1000mm <sup>2</sup>	2500mm <sup>2</sup>	2500mm <sup>2</sup>	57°C/W
225mm <sup>2</sup>	2500mm <sup>2</sup>	2500mm <sup>2</sup>	60°C/W
100mm <sup>2</sup>	2500mm <sup>2</sup>	2500mm <sup>2</sup>	65°C/W

\*Device is mounted on topside

**Table 3. DD Package, 8-Lead DFN**

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE*	BACKSIDE		
2500mm <sup>2</sup>	2500mm <sup>2</sup>	2500mm <sup>2</sup>	60°C/W
1000mm <sup>2</sup>	2500mm <sup>2</sup>	2500mm <sup>2</sup>	62°C/W
225mm <sup>2</sup>	2500mm <sup>2</sup>	2500mm <sup>2</sup>	65°C/W
100mm <sup>2</sup>	2500mm <sup>2</sup>	2500mm <sup>2</sup>	68°C/W

\*Device is mounted on topside

**Table 4. ST Package, 3-Lead SOT-223**

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE*	BACKSIDE		
2500mm <sup>2</sup>	2500mm <sup>2</sup>	2500mm <sup>2</sup>	48°C/W
1000mm <sup>2</sup>	2500mm <sup>2</sup>	2500mm <sup>2</sup>	48°C/W
225mm <sup>2</sup>	2500mm <sup>2</sup>	2500mm <sup>2</sup>	56°C/W
100mm <sup>2</sup>	2500mm <sup>2</sup>	2500mm <sup>2</sup>	62°C/W

\*Device is mounted on topside

**Table 5. Q Package, 5-Lead DD-Pak**

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE*	BACKSIDE		
2500mm <sup>2</sup>	2500mm <sup>2</sup>	2500mm <sup>2</sup>	25°C/W
1000mm <sup>2</sup>	2500mm <sup>2</sup>	2500mm <sup>2</sup>	30°C/W
125mm <sup>2</sup>	2500mm <sup>2</sup>	2500mm <sup>2</sup>	35°C/W

\*Device is mounted on topside

### T Package, 5-Lead TO-220

Thermal Resistance (Junction-to-Case) = 3°C/W

### Calculating Junction Temperature

Example: Given an output voltage of 0.9V, a  $V_{CONTROL}$  voltage of  $3.3V \pm 10\%$ , an IN voltage of  $1.5V \pm 5\%$ , output current range from 1mA to 1A and a maximum ambient temperature of 50°C, what will the maximum junction temperature be for the DFN package on a 2500mm<sup>2</sup> board with topside copper area of 500mm<sup>2</sup>?

## APPLICATIONS INFORMATION

The power in the drive circuit equals:

$$P_{\text{DRIVE}} = (V_{\text{CONTROL}} - V_{\text{OUT}})(I_{\text{CONTROL}})$$

where  $I_{\text{CONTROL}}$  is equal to  $I_{\text{OUT}}/60$ .  $I_{\text{CONTROL}}$  is a function of output current. A curve of  $I_{\text{CONTROL}}$  vs  $I_{\text{OUT}}$  can be found in the Typical Performance Characteristics curves.

The power in the output transistor equals:

$$P_{\text{OUTPUT}} = (V_{\text{IN}} - V_{\text{OUT}})(I_{\text{OUT}})$$

The total power equals:

$$P_{\text{TOTAL}} = P_{\text{DRIVE}} + P_{\text{OUTPUT}}$$

The current delivered to the SET pin is negligible and can be ignored.

$$V_{\text{CONTROL}(\text{MAX CONTINUOUS})} = 3.630\text{V} (3.3\text{V} + 10\%)$$

$$V_{\text{IN}(\text{MAX CONTINUOUS})} = 1.575\text{V} (1.5\text{V} + 5\%)$$

$$V_{\text{OUT}} = 0.9\text{V}, I_{\text{OUT}} = 1\text{A}, T_A = 50^\circ\text{C}$$

Power dissipation under these conditions is equal to:

$$P_{\text{DRIVE}} = (V_{\text{CONTROL}} - V_{\text{OUT}})(I_{\text{CONTROL}})$$

$$I_{\text{CONTROL}} = \frac{I_{\text{OUT}}}{60} = \frac{1\text{A}}{60} = 17\text{mA}$$

$$P_{\text{DRIVE}} = (3.630\text{V} - 0.9\text{V})(17\text{mA}) = 46\text{mW}$$

$$P_{\text{OUTPUT}} = (V_{\text{IN}} - V_{\text{OUT}})(I_{\text{OUT}})$$

$$P_{\text{OUTPUT}} = (1.575\text{V} - 0.9\text{V})(1\text{A}) = 675\text{mW}$$

$$\text{Total Power Dissipation} = 721\text{mW}$$

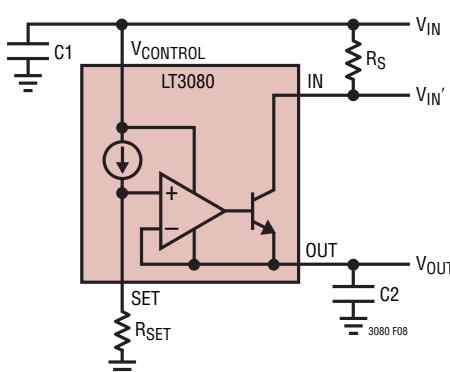


Figure 8. Reducing Power Dissipation Using a Series Resistor

Junction Temperature will be equal to:

$$T_J = T_A + P_{\text{TOTAL}} \cdot \theta_{JA} \text{ (approximated using tables)}$$

$$T_J = 50^\circ\text{C} + 721\text{mW} \cdot 64^\circ\text{C/W} = 96^\circ\text{C}$$

In this case, the junction temperature is below the maximum rating, ensuring reliable operation.

### Reducing Power Dissipation

In some applications it may be necessary to reduce the power dissipation in the LT3080 package without sacrificing output current capability. Two techniques are available. The first technique, illustrated in Figure 8, employs a resistor in series with the regulator's input. The voltage drop across  $R_S$  decreases the LT3080's IN-to-OUT differential voltage and correspondingly decreases the LT3080's power dissipation.

As an example, assume:  $V_{\text{IN}} = V_{\text{CONTROL}} = 5\text{V}$ ,  $V_{\text{OUT}} = 3.3\text{V}$  and  $I_{\text{OUT}(\text{MAX})} = 1\text{A}$ . Use the formulas from the Calculating Junction Temperature section previously discussed.

Without series resistor  $R_S$ , power dissipation in the LT3080 equals:

$$P_{\text{TOTAL}} = (5\text{V} - 3.3\text{V}) \cdot \left( \frac{1\text{A}}{60} \right) + (5\text{V} - 3.3\text{V}) \cdot 1\text{A}$$

$$= 1.73\text{W}$$

If the voltage differential ( $V_{\text{DIFF}}$ ) across the NPN pass transistor is chosen as  $0.5\text{V}$ , then  $R_S$  equals:

$$R_S = \frac{5\text{V} - 3.3\text{V} - 0.5\text{V}}{1\text{A}} = 1.2\Omega$$

Power dissipation in the LT3080 now equals:

$$P_{\text{TOTAL}} = (5\text{V} - 3.3\text{V}) \cdot \left( \frac{1\text{A}}{60} \right) + (0.5\text{V}) \cdot 1\text{A} = 0.53\text{W}$$

The LT3080's power dissipation is now only 30% compared to no series resistor.  $R_S$  dissipates  $1.2\text{W}$  of power. Choose appropriate wattage resistors to handle and dissipate the power properly.

# Micropower Low Dropout Regulators with Shutdown

## FEATURES

- 400mV Dropout Voltage
- 700mA Output Current
- 50 $\mu$ A Quiescent Current
- No Protection Diodes Needed
- Adjustable Output from 3.8V to 30V
- 3.3V and 5V Fixed Output Voltages
- Controlled Quiescent Current in Dropout
- Shutdown
- 16 $\mu$ A Quiescent Current in Shutdown
- Stable with 3.3 $\mu$ F Output Capacitor
- Reverse Battery Protection
- No Reverse Output Current
- Thermal Limiting
- Surface Mount SOT-223 and DD-Pak Packages

## APPLICATIONS

- Low Current Regulator
- Regulator for Battery-Powered Systems
- Post Regulator for Switching Supplies
- 5V to 3.3V Logic Regulator

## DESCRIPTION

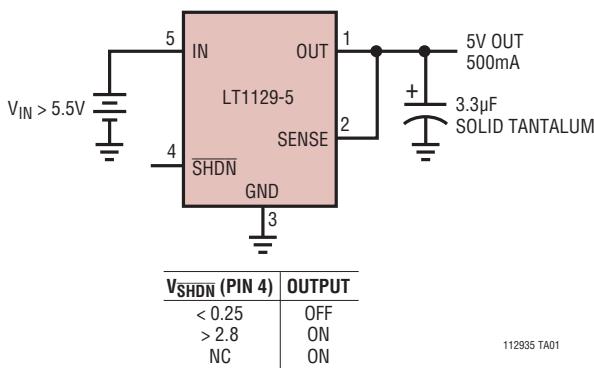
The LT®1129/LT1129-3.3/LT1129-5 are micropower low dropout regulators with shutdown. The devices are capable of supplying 700mA of output current with a dropout voltage of 400mV at maximum output. Designed for use in battery-powered systems, the low quiescent current, 50 $\mu$ A operating and 16 $\mu$ A in shutdown, make them an ideal choice. The quiescent current does not rise in dropout as it does with many other low dropout PNP regulators.

Other features of the LT1129/LT1129-3.3/LT1129-5 include the ability to operate with small output capacitors. They are stable with only 3.3 $\mu$ F on the output while most older devices require between 10 $\mu$ F and 100 $\mu$ F for stability. Also the input may be connected to ground or a reverse voltage without reverse current flow from output to input. This makes the LT1129/LT1129-3.3/LT1129-5 ideal for backup power situations where the output is held high and the input is at ground or reversed. Under these conditions, only 16 $\mu$ A will flow from the output pin to ground. The devices are available in 5-lead TO-220, 5-lead DD-Pak and 3-lead SOT-223 packages.

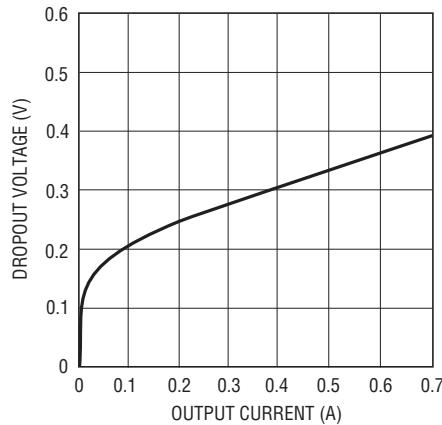
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## TYPICAL APPLICATION

**5V Supply with Shutdown**



**Dropout Voltage**



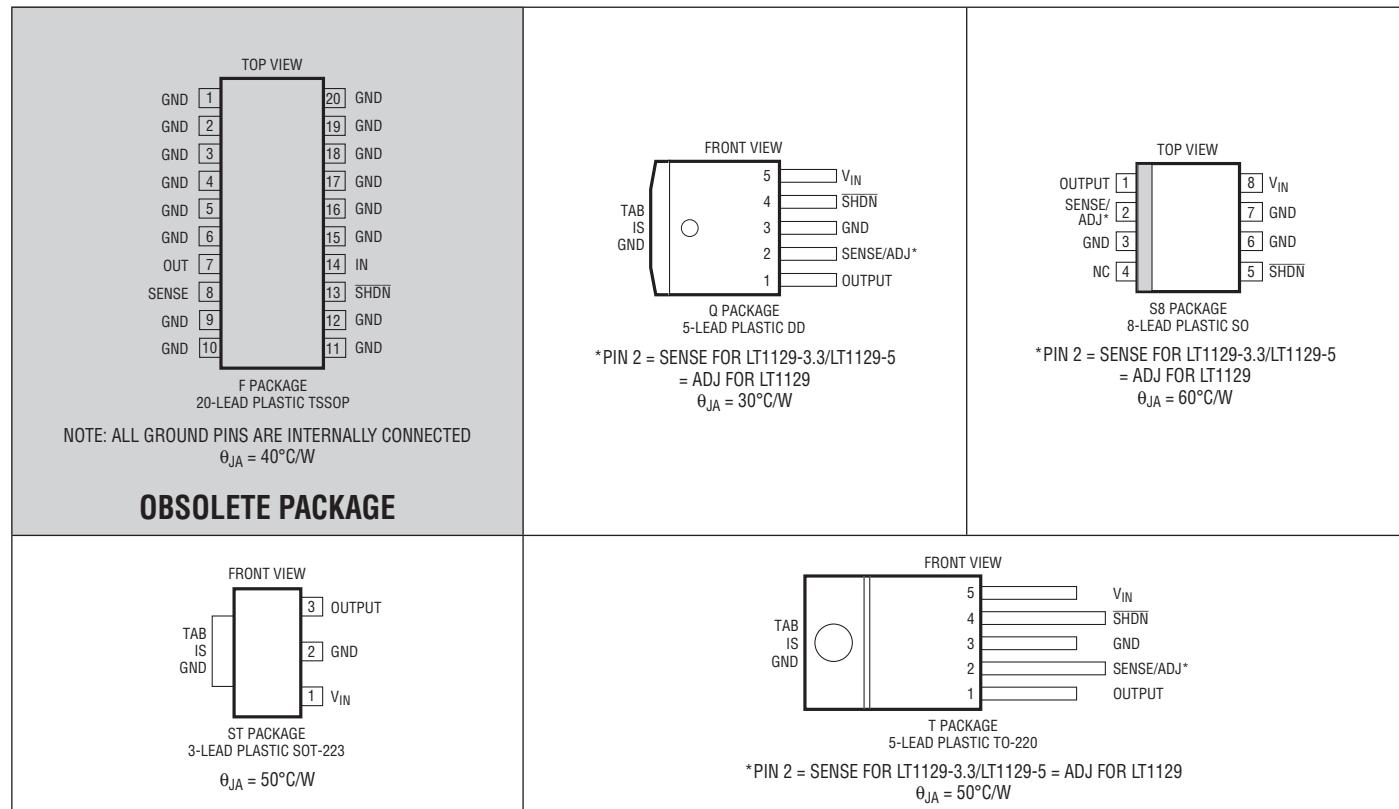
# LT1129/LT1129-3.3/LT1129-5

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage .....	$\pm 30V^*$	Storage Temperature Range.....	-65°C to 150°C
Output Pin Reverse Current .....	10mA	Operating Junction Temperature Range (Note 3)	
Sense Pin Current .....	10mA	LT1129C-X.....	0°C to 125°C
Adjust Pin Current .....	10mA	LT1129C-X Extended Temperature Range	
Sense Pin, Adjust Pin Reverse Voltage .....	-0.6V	(Note 12) .....	-40°C to 125°C
Shutdown Pin Input Voltage (Note 2) .....	6.5V, -0.6V	LT1129I-X(Note 12) .....	-40°C to 125°C
Shutdown Pin Input Current (Note 2) .....	20mA	LT1129MP-X(Note 12) .....	-55°C to 125°C
Output Short-Circuit Duration .....	Indefinite	Lead Temperature (Soldering, 10 sec) .....	300°C

\* For applications requiring input voltage ratings greater than 30V, contact the factory.

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1129CS8#PBF	LT1129CS8#TRPBF	1129	8-Lead Plastic SO	0°C to 125°C
LT1129IS8#PBF	LT1129IS8#TRPBF	1129I	8-Lead Plastic SO	-40°C to 125°C
LT1129CS8-3.3#PBF	LT1129CS8-3.3#TRPBF	11293	8-Lead Plastic SO	0°C to 125°C
LT1129IS8-3.3#PBF	LT1129IS8-3.3#TRPBF	1129I3	8-Lead Plastic SO	-40°C to 125°C
LT1129CS8-5#PBF	LT1129CS8-5#TRPBF	11295	8-Lead Plastic SO	0°C to 125°C

112935ff

**ORDER INFORMATION**

<b>LEAD FREE FINISH</b>	<b>TAPE AND REEL</b>	<b>PART MARKING*</b>	<b>PACKAGE DESCRIPTION</b>	<b>TEMPERATURE RANGE</b>
LT1129IS8-5#PBF	LT1129IS8-5#TRPBF	1129I5	8-Lead Plastic SO	-40°C to 125°C
LT1129CST-3.3#PBF	LT1129CST-3.3#TRPBF	11293	3-Lead Plastic SOT-223	0°C to 125°C
LT1129IST-3.3#PBF	LT1129IST-3.3#TRPBF	129I3	3-Lead Plastic SOT-223	-40°C to 125°C
LT1129MPST-3.3#PBF	LT1129MPST-3.3#TRPBF	129MP3	3-Lead Plastic SOT-223	-55°C to 125°C
LT1129CST-5#PBF	LT1129CST-5#TRPBF	11295	3-Lead Plastic SOT-223	0°C to 125°C
LT1129IST-5#PBF	LT1129IST-5#TRPBF	129I5	3-Lead Plastic SOT-223	-40°C to 125°C
LT1129CQ#PBF	LT1129CQ#TRPBF	LT1129CQ	5-Lead Plastic DD-PAK	0°C to 125°C
LT1129IQ#PBF	LT1129IQ#TRPBF	LT1129IQ	5-Lead Plastic DD-PAK	-40°C to 125°C
LT1129CQ-3.3#PBF	LT1129CQ-3.3#TRPBF	LT1129CQ-3.3	5-Lead Plastic DD-PAK	0°C to 125°C
LT1129IQ-3.3#PBF	LT1129IQ-3.3#TRPBF	LT1129IQ-3.3	5-Lead Plastic DD-PAK	-40°C to 125°C
LT1129CQ-5#PBF	LT1129CQ-5#TRPBF	LT1129CQ-5	5-Lead Plastic DD-PAK	0°C to 125°C
LT1129IQ-5#PBF	LT1129IQ-5#TRPBF	LT1129IQ-5	5-Lead Plastic DD-PAK	-40°C to 125°C
LT1129CT#PBF	LT1129CT#TRPBF	LT1129CT	5-Lead Plastic TO-220	0°C to 125°C
LT1129IT#PBF	LT1129IT#TRPBF	LT1129IT	5-Lead Plastic TO-220	-40°C to 125°C
LT1129CT-3.3#PBF	LT1129CT-3.3#TRPBF	LT1129CT-3.3	5-Lead Plastic TO-220	0°C to 125°C
LT1129IT-3.3#PBF	LT1129IT-3.3#TRPBF	LT1129IT-3.3	5-Lead Plastic TO-220	-40°C to 125°C
LT1129CT-5#PBF	LT1129CT-5#TRPBF	LT1129CT-5	5-Lead Plastic TO-220	0°C to 125°C
LT1129IT-5#PBF	LT1129IT-5#TRPBF	LT1129IT-5	5-Lead Plastic TO-220	-40°C to 125°C
<b>LEAD BASED FINISH</b>	<b>TAPE AND REEL</b>	<b>PART MARKING*</b>	<b>PACKAGE DESCRIPTION</b>	<b>TEMPERATURE RANGE</b>
LT1129CS8	LT1129CS8#TR	1129	8-Lead Plastic SO	0°C to 125°C
LT1129IS8	LT1129IS8#TR	1129I	8-Lead Plastic SO	-40°C to 125°C
LT1129CS8-3.3	LT1129CS8-3.3#TR	11293	8-Lead Plastic SO	0°C to 125°C
LT1129IS8-3.3	LT1129IS8-3.3#TR	1129I3	8-Lead Plastic SO	-40°C to 125°C
LT1129CS8-5	LT1129CS8-5#TR	11295	8-Lead Plastic SO	0°C to 125°C
LT1129IS8-5	LT1129IS8-5#TR	1129I5	8-Lead Plastic SO	-40°C to 125°C
LT1129CST-3.3	LT1129CST-3.3#TR	11293	3-Lead Plastic SOT-223	0°C to 125°C
LT1129IST-3.3	LT1129IST-3.3#TR	129I3	3-Lead Plastic SOT-223	-40°C to 125°C
LT1129MPST-3.3	LT1129MPST-3.3#TR	129MP3	3-Lead Plastic SOT-223	-55°C to 125°C
LT1129CST-5	LT1129CST-5#TR	11295	3-Lead Plastic SOT-223	0°C to 125°C
LT1129IST-5	LT1129IST-5#TR	129I5	3-Lead Plastic SOT-223	-40°C to 125°C
LT1129CQ	LT1129CQ#TR	LT1129CQ	5-Lead Plastic DD-PAK	0°C to 125°C
LT1129IQ	LT1129IQ#TR	LT1129IQ	5-Lead Plastic DD-PAK	-40°C to 125°C
LT1129CQ-3.3	LT1129CQ-3.3#TR	LT1129CQ-3.3	5-Lead Plastic DD-PAK	0°C to 125°C
LT1129IQ-3.3	LT1129IQ-3.3#TR	LT1129IQ-3.3	5-Lead Plastic DD-PAK	-40°C to 125°C
LT1129CQ-5	LT1129CQ-5#TR	LT1129CQ-5	5-Lead Plastic DD-PAK	0°C to 125°C
LT1129IQ-5	LT1129IQ-5#TR	LT1129IQ-5	5-Lead Plastic DD-PAK	-40°C to 125°C
LT1129CT	LT1129CT#TR	LT1129CT	5-Lead Plastic TO-220	0°C to 125°C
LT1129IT	LT1129IT#TR	LT1129IT	5-Lead Plastic TO-220	-40°C to 125°C
LT1129CT-3.3	LT1129CT-3.3#TR	LT1129CT-3.3	5-Lead Plastic TO-220	0°C to 125°C
LT1129IT-3.3	LT1129IT-3.3#TR	LT1129IT-3.3	5-Lead Plastic TO-220	-40°C to 125°C

## ORDER INFORMATION

LEAD BASED FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1129CT-5	LT1129CT-5#TR	LT1129CT-5	5-Lead Plastic TO-220	0°C to 125°C
LT1129IT-5	LT1129IT-5#TR	LT1129IT-5	5-Lead Plastic TO-220	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .

SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Regulated Output Voltage (Notes 4, 12)	LT1129-3.3 $V_{IN} = 3.8\text{V}$ , $I_{OUT} = 1\text{mA}$ , $T_J = 25^\circ\text{C}$ $4.3\text{V} < V_{IN} < 20\text{V}$ , $1\text{mA} < I_{OUT} < 700\text{mA}$	●	3.250	3.300	3.350	V
		●	3.200	3.300	3.400	V
	LT1129-5 $V_{IN} = 5.5\text{V}$ , $I_{OUT} = 1\text{mA}$ , $T_J = 25^\circ\text{C}$ $6\text{V} < V_{IN} < 20\text{V}$ , $1\text{mA} < I_{OUT} < 700\text{mA}$	●	4.925	5.000	5.075	V
Line Regulation (Note 12)	LT1129-3.3 $\Delta V_{IN} = 4.8\text{V}$ to $20\text{V}$ , $I_{OUT} = 1\text{mA}$	●	4.850	5.000	5.150	V
	LT1129-5 $\Delta V_{IN} = 5.5\text{V}$ to $20\text{V}$ , $I_{OUT} = 1\text{mA}$	●	3.695	3.750	3.805	V
	LT1129 (Note 5) $\Delta V_{IN} = 4.3\text{V}$ to $20\text{V}$ , $I_{OUT} = 1\text{mA}$ $4.8\text{V} < V_{IN} < 20\text{V}$ , $1\text{mA} < I_{OUT} < 700\text{mA}$	●	3.640	3.750	3.860	V
Load Regulation (Note 12)	LT1129-3.3 $\Delta I_{LOAD} = 1\text{mA}$ to $700\text{mA}$ , $T_J = 25^\circ\text{C}$ $\Delta I_{LOAD} = 1\text{mA}$ to $700\text{mA}$	●	6	20	20	mV
		●	15	30	30	mV
	LT1129-5 $\Delta I_{LOAD} = 1\text{mA}$ to $700\text{mA}$ , $T_J = 25^\circ\text{C}$ $\Delta I_{LOAD} = 1\text{mA}$ to $700\text{mA}$	●	6	20	20	mV
Dropout Voltage (Note 6)	LT1129 (Note 5) $\Delta I_{LOAD} = 1\text{mA}$ to $700\text{mA}$ , $T_J = 25^\circ\text{C}$ $\Delta I_{LOAD} = 1\text{mA}$ to $700\text{mA}$	●	20	30	30	mV
	$I_{LOAD} = 10\text{mA}$ , $T_J = 25^\circ\text{C}$	●	0.13	0.20	0.20	V
	$I_{LOAD} = 10\text{mA}$	●		0.25	0.25	V
	$I_{LOAD} = 100\text{mA}$ , $T_J = 25^\circ\text{C}$	●	0.25	0.35	0.35	V
	$I_{LOAD} = 100\text{mA}$	●		0.45	0.45	V
	$I_{LOAD} = 500\text{mA}$ , $T_J = 25^\circ\text{C}$	●	0.37	0.45	0.60	V
	$I_{LOAD} = 500\text{mA}$	●		0.45	0.60	V
	$I_{LOAD} = 700\text{mA}$ , $T_J = 25^\circ\text{C}$	●	0.45	0.55	0.70	V
	$I_{LOAD} = 700\text{mA}$	●		0.55	0.70	V
Ground Pin Current (Note 7)	$I_{LOAD} = 0\text{mA}$	●	50	70	70	$\mu\text{A}$
	$I_{LOAD} = 10\text{mA}$	●	310	450	450	$\mu\text{A}$
	$I_{LOAD} = 100\text{mA}$	●	2.0	3.5	3.5	mA
	$I_{LOAD} = 300\text{mA}$	●	10	20	20	mA
	$I_{LOAD} = 500\text{mA}$	●	25	45	45	mA
	$I_{LOAD} = 700\text{mA}$	●	50	90	90	mA
Adjust Pin Bias Current (Notes 5, 8)	$T_J = 25^\circ\text{C}$			150	300	nA
Shutdown Threshold	$V_{OUT} = \text{Off to On}$ $V_{OUT} = \text{On to Off}$	●	0.25	1.2	2.8	V
Shutdown Pin Current (Note 9)	$V_{SHDN} = 0\text{V}$	●	0.75	6	10	$\mu\text{A}$
Quiescent Current in Shutdown (Note 10)	$V_{IN} = 6\text{V}$ , $V_{SHDN} = 0\text{V}$	●	15	25	25	$\mu\text{A}$

112935ff

**ELECTRICAL CHARACTERISTICS**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .

SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Ripple Rejection	$V_{IN} - V_{OUT} = 1\text{V}$ (Avg), $V_{RIPPLE} = 0.5\text{V}_{P-P}$ , $f_{RIPPLE} = 120\text{Hz}$ , $I_{LOAD} = 0.7\text{A}$ , $T_J = 25^\circ\text{C}$	52	64		dB
Current Limit	$V_{IN} - V_{OUT} = 7\text{V}$ , $T_J = 25^\circ\text{C}$		1.2	1.6	A
Input Reverse Leakage Current	$V_{IN} = -20\text{V}$ , $V_{OUT} = 0\text{V}$	●		1.0	mA
Reverse Output Current (Note 11)	LT1129-3.3 $V_{OUT} = 3.3\text{V}$ , $V_{IN} = 0\text{V}$ LT1129-5 $V_{OUT} = 5\text{V}$ , $V_{IN} = 0\text{V}$ LT1129 (Note 5) $V_{OUT} = 3.8\text{V}$ , $V_{IN} = 0\text{V}$		16	25	$\mu\text{A}$
			16	25	$\mu\text{A}$
			16	25	$\mu\text{A}$

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The shutdown pin input voltage rating is required for a low impedance source. Internal protection devices connected to the shutdown pin will turn on and clamp the pin to approximately 7V or -0.6V. This range allows the use of 5V logic devices to drive the pin directly. For high impedance sources or logic running on supply voltages greater than 5.5V, the maximum current driven into the shutdown pin must be limited to less than 20mA.

**Note 3:** For junction temperatures greater than  $110^\circ\text{C}$ , a minimum load of 1mA is recommended. For  $T_J > 110^\circ\text{C}$  and  $I_{OUT} < 1\text{mA}$ , output voltage may increase by 1%.

**Note 4:** Operating conditions are limited by maximum junction temperature. The regulated output voltage specification will not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.

**Note 5:** The LT1129 is tested and specified with the adjust pin connected to the output pin.

**Note 6:** Dropout voltage is the minimum input/output voltage required to maintain regulation at the specified output current. In dropout the output

voltage will be equal to  $(V_{IN} - V_{DROPOUT})$ . Dropout voltage is measured between the input pin and the output pin. External voltage drops between the output pin and the sense pin will add to the dropout voltage.

**Note 7:** Ground pin current is tested with  $V_{IN} = V_{OUT}$  (nominal) and a current source load. This means that the device is tested while operating in its dropout region. This is the worst case ground pin current. The ground pin current will decrease slightly at higher input voltages.

**Note 8:** Adjust pin bias current flows into the adjust pin.

**Note 9:** Shutdown pin current at  $V_{SHDN} = 0\text{V}$  flows out of the shutdown pin.

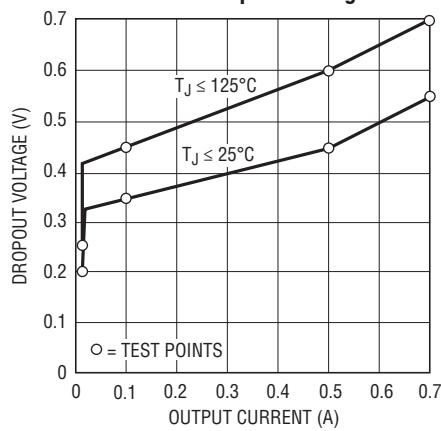
**Note 10:** Quiescent current in shutdown is equal to the sum total of the shutdown pin current ( $6\mu\text{A}$ ) and the ground pin current ( $9\mu\text{A}$ ).

**Note 11:** Reverse output current is tested with the input pin grounded. The output pin and the sense pin are forced to the rated output voltage. This current flows into the sense pin and out of the ground pin. For the LT1129 (adjustable version) the sense pin is internally tied to the output pin.

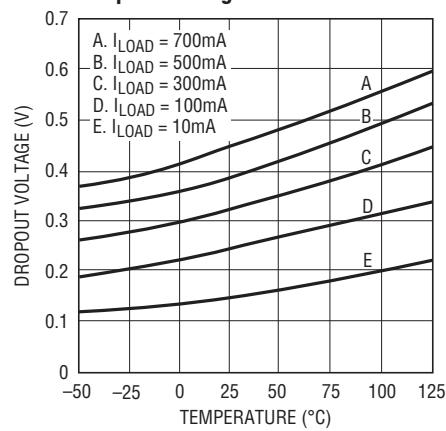
**Note 12:** The LT1129 regulators are tested and specified under pulse load conditions such that  $T_J \leq T_A$ . The LT1129C regulators are 100% tested at  $T_A = 25^\circ\text{C}$ . For C-grade devices, Regulated Output Voltage, Line Regulation and Load Regulation performance at  $-40^\circ\text{C}$  and  $125^\circ\text{C}$  is assured by design, characterization and correlation with statistical process controls. The LT1129I regulators are guaranteed over the full  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  operating junction temperature range. The LT1129MP regulators are 100% tested and guaranteed over the  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  temperature range.

**TYPICAL PERFORMANCE CHARACTERISTICS**

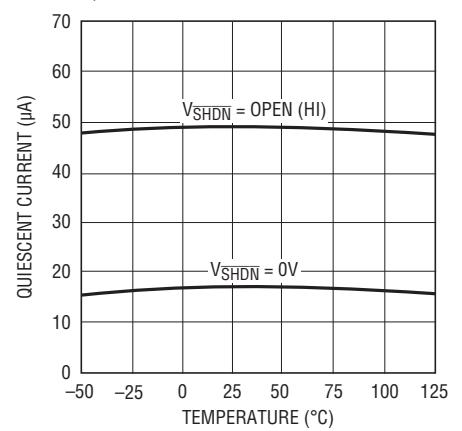
Guaranteed Dropout Voltage



Dropout Voltage



Quiescent Current

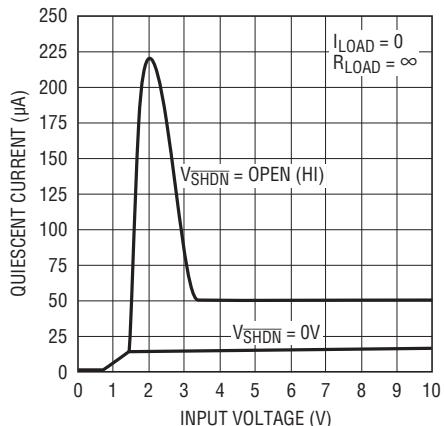


# LT1129/LT1129-3.3/LT1129-5

## TYPICAL PERFORMANCE CHARACTERISTICS

**LT1129-3.3**

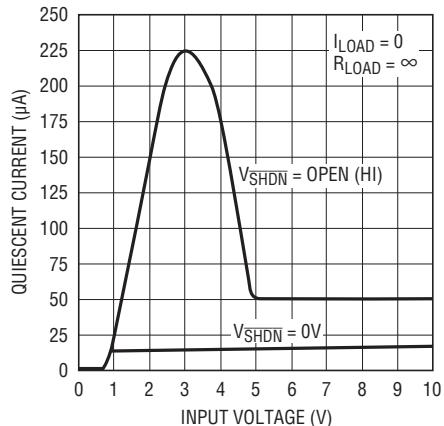
Quiescent Current



112935 G04

**LT1129-5**

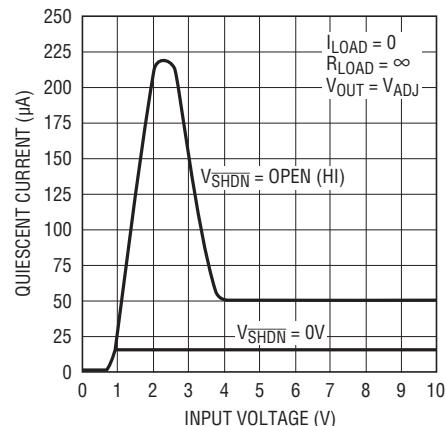
Quiescent Current



112935 G05

**LT1129**

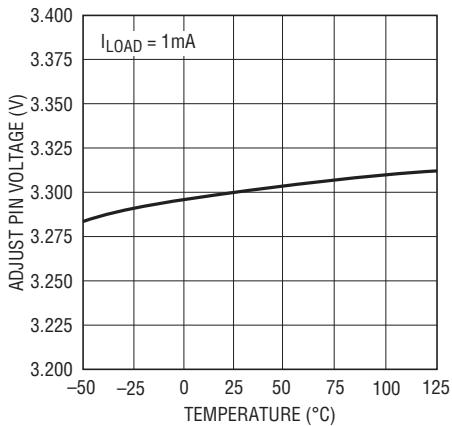
Quiescent Current



112935 G06

**LT1129-3.3**

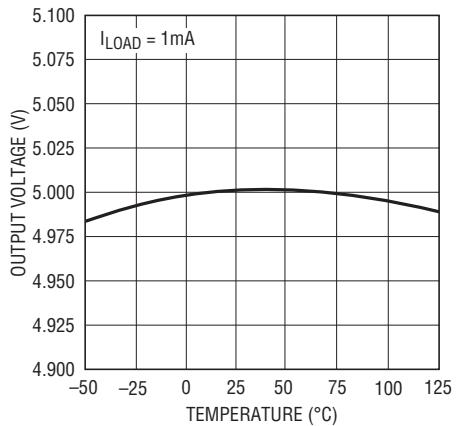
Output Voltage



112935 G07

**LT1129-5**

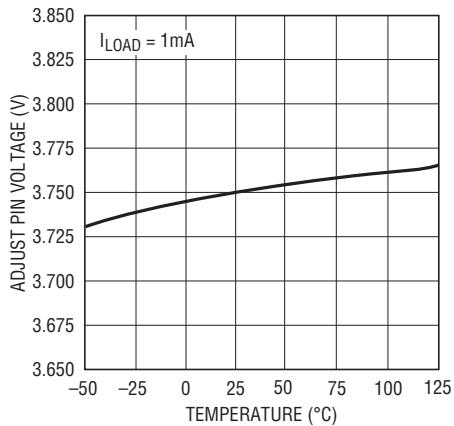
Output Voltage



112935 G08

**LT1129**

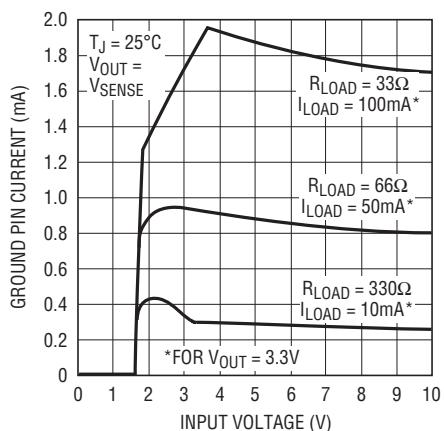
Adjust Pin Voltage



112935 G09

**LT1129-3.3**

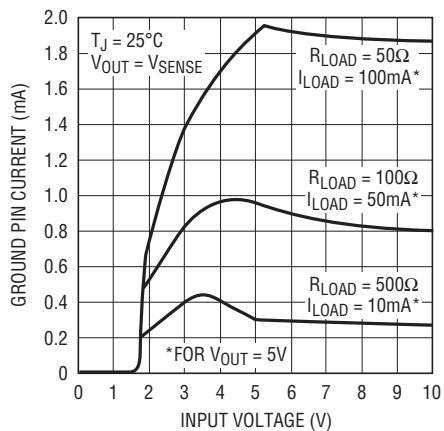
Ground Pin Current



112935 G10

**LT1129-5**

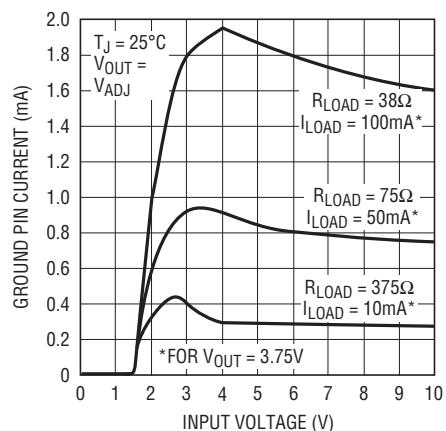
Ground Pin Current



112935 G11

**LT1129**

Ground Pin Current



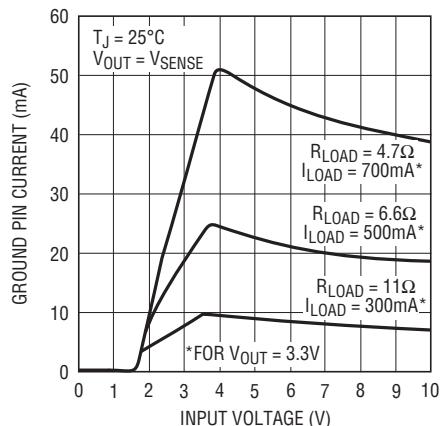
112935 G12

112935ff

## TYPICAL PERFORMANCE CHARACTERISTICS

**LT1129-3.3**

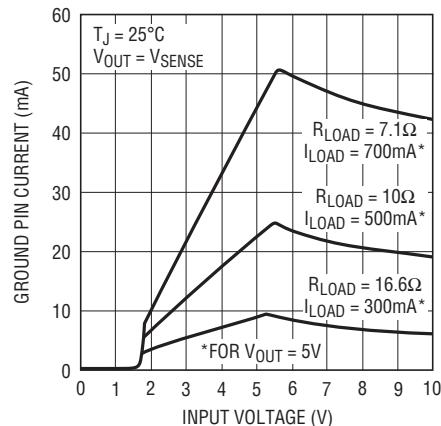
Ground Pin Current



112935 G13

**LT1129-5**

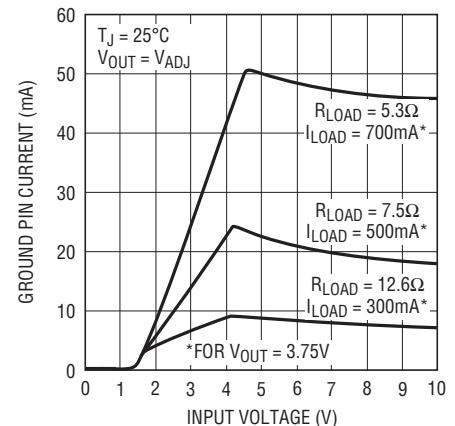
Ground Pin Current



112935 G14

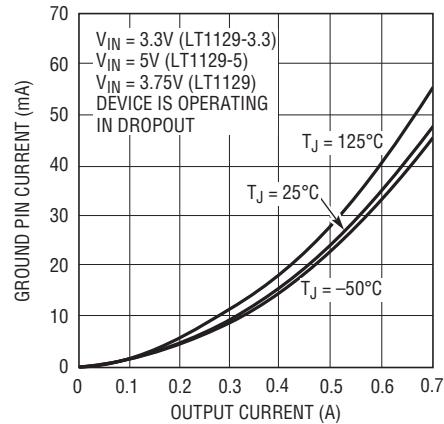
**LT1129**

Ground Pin Current



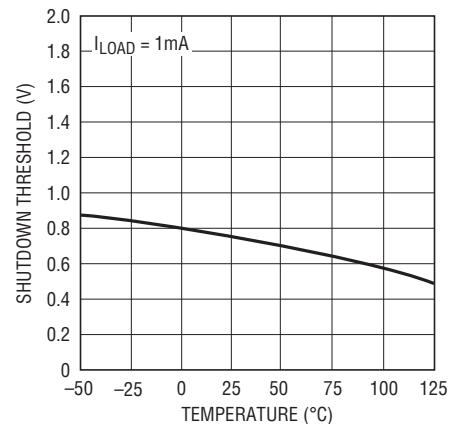
112935 G15

Ground Pin Current



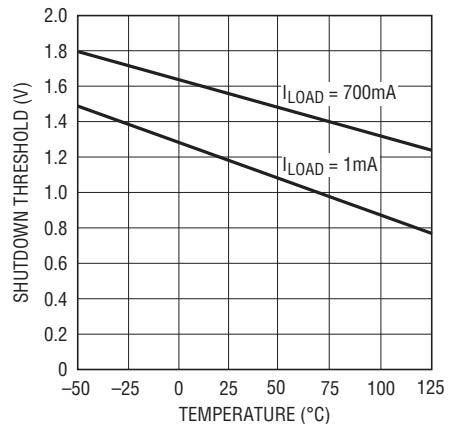
112935 G16

Shutdown Pin Threshold  
(On-to-Off)



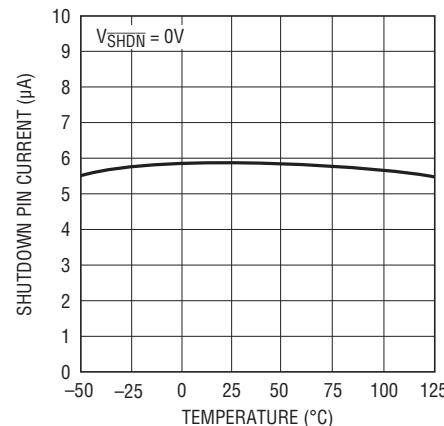
112935 G17

Shutdown Pin Threshold  
(Off-to-On)



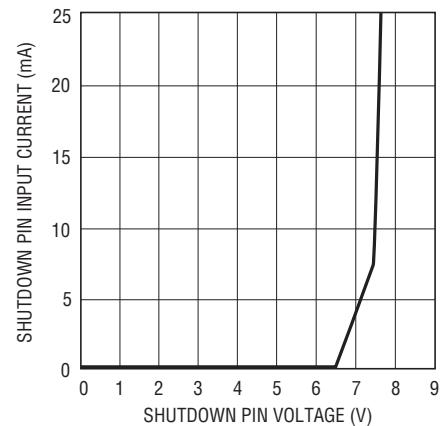
112935 G18

Shutdown Pin Current



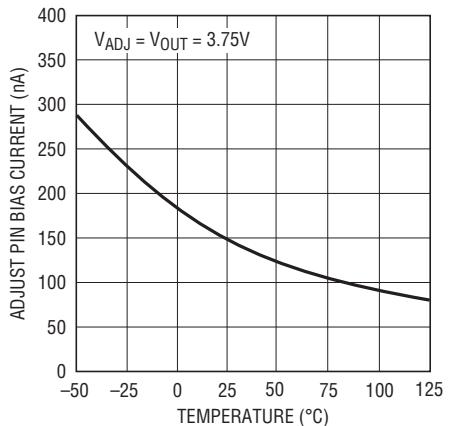
112935 G19

Shutdown Pin Input Current



112935 G20

Adjust Pin Bias Current



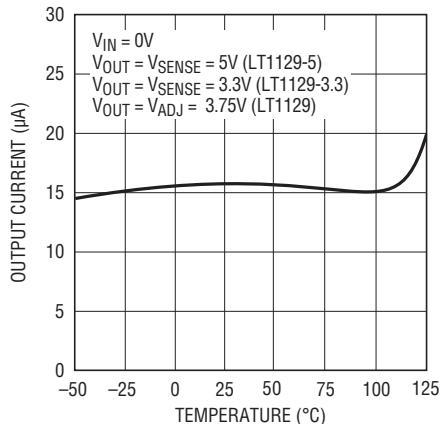
112935 G21

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# LT1129/LT1129-3.3/LT1129-5

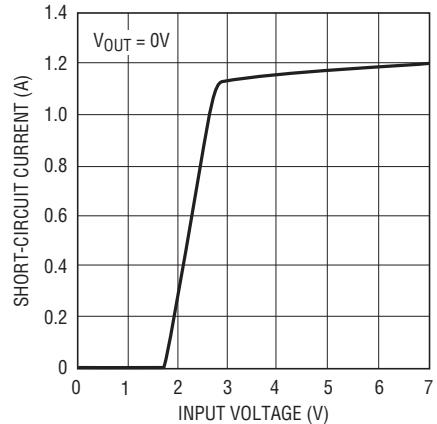
## TYPICAL PERFORMANCE CHARACTERISTICS

**Reverse Output Current**



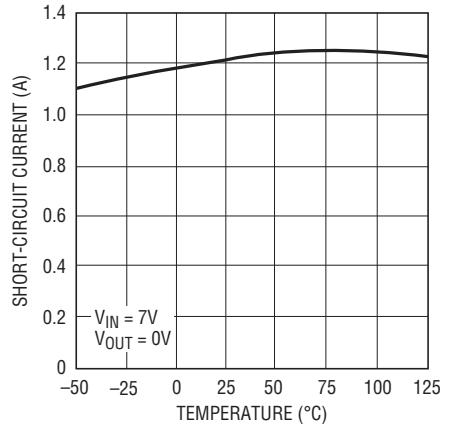
112935 G22

**Current Limit**



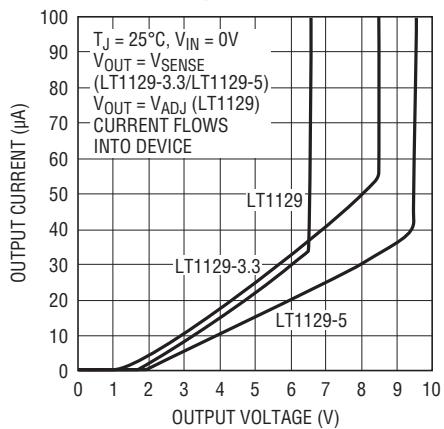
112935 G23

**Current Limit**



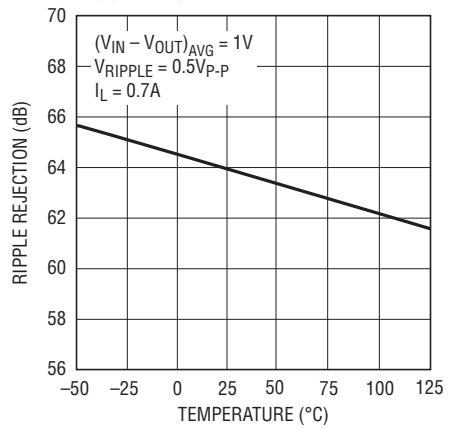
112935 G24

**Reverse Output Current**



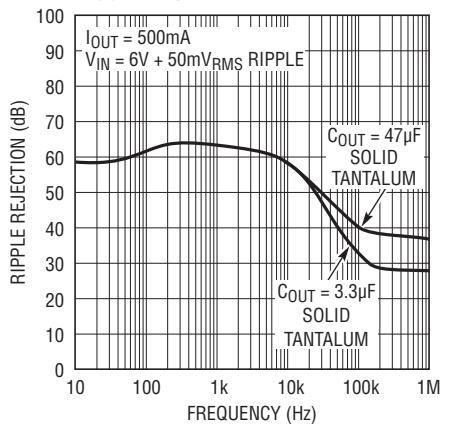
112935 G25

**Ripple Rejection**



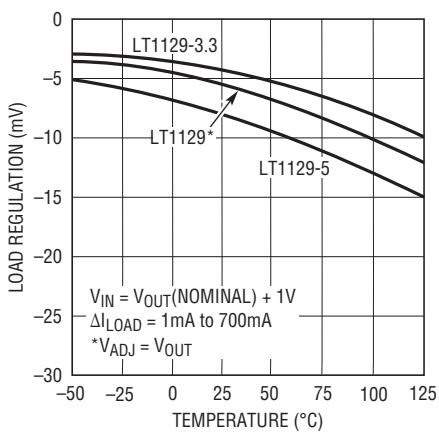
112935 G26

**Ripple Rejection**



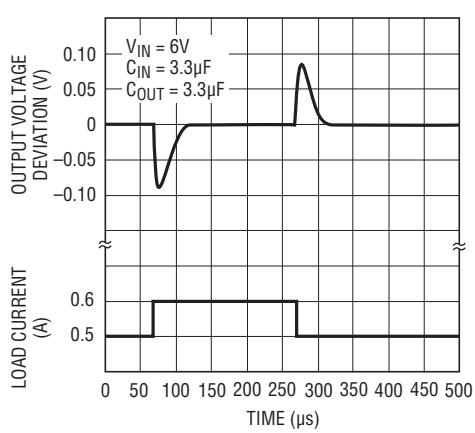
112935 G27

**Load Regulation**



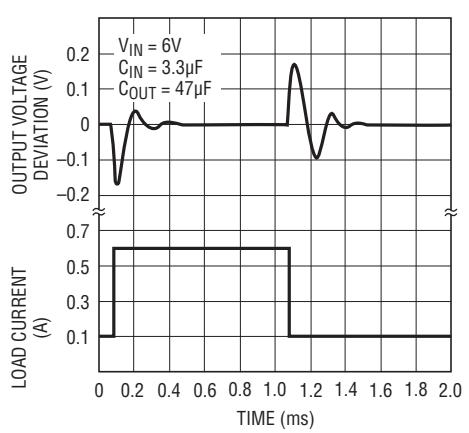
112935 G28

**LT1129-5  
Transient Response**



112935 G29

**LT1129-5  
Transient Response**



112935 G30

112935ff

## PIN FUNCTIONS

**Input Pin:** Power is supplied to the device through the input pin. The input pin should be bypassed to ground if the device is more than 6 inches away from the main input filter capacitor. In general, the output impedance of a battery rises with frequency so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor in the range of  $1\mu\text{F}$  to  $10\mu\text{F}$  is sufficient. The LT1129 is designed to withstand reverse voltages on the input pin with respect to both ground and the output pin. In the case of a reversed input, which can happen if a battery is plugged in backwards, the LT1129 will act as if there is a diode in series with its input. There will be no reverse current flow into the LT1129 and no reverse voltage will appear at the load. The device will protect both itself and the load.

**Output Pin:** The output pin supplies power to the load. An output capacitor is required to prevent oscillations. See the Applications Information section for recommended value of output capacitance and information on reverse output characteristics.

**Shutdown Pin ( $\overline{\text{SHDN}}$ ):** This pin is used to put the device into shutdown. In shutdown the output of the device is turned off. This pin is active low. The device will be shut down if the shutdown pin is actively pulled low. The shutdown pin current with the pin pulled to ground will be  $6\mu\text{A}$ . The shutdown pin is internally clamped to  $7\text{V}$  and  $-0.6\text{V}$  (one  $V_{\text{BE}}$ ). This allows the shutdown pin to be driven directly by  $5\text{V}$  logic or by open collector logic with a pull-up resistor. The pull-up resistor is only required to supply the leakage current of the open collector gate, normally several microamperes. Pull-up current must be limited to a maximum of  $20\text{mA}$ . A curve of shutdown pin input current as a function of voltage appears in the Typical Performance Characteristics. If the shutdown pin is not

used it can be left open circuit. The device will be active, output on, if the shutdown pin is not connected.

**Sense Pin:** For fixed voltage versions of the LT1129 (LT1129-3.3, LT1129-5) the sense pin is the input to the error amplifier. Optimum regulation will be obtained at the point where the sense pin is connected to the output pin. For most applications the sense pin is connected directly to the output pin at the regulator. In critical applications small voltage drops caused by the resistance ( $R_P$ ) of PC traces between the regulator and the load, which would normally degrade regulation, may be eliminated by connecting the sense pin to the output pin at the load as shown in Figure 1 (Kelvin Sense Connection). Note that the voltage drop across the external PC traces will add to the dropout voltage of the regulator. The sense pin bias current is  $15\mu\text{A}$  at the nominal regulated output voltage. This pin is internally clamped to  $-0.6\text{V}$  (one  $V_{\text{BE}}$ ).

**Adjust Pin:** For the LT1129 (adjustable version) the adjust pin is the input to the error amplifier. This pin is internally clamped to  $6\text{V}$  and  $-0.6\text{V}$  (one  $V_{\text{BE}}$ ). This pin has a bias current of  $150\text{nA}$  which flows into the pin. See Bias Current curve in the Typical Performance Characteristics. The adjust pin reference voltage is equal to  $3.75\text{V}$  referenced to ground.

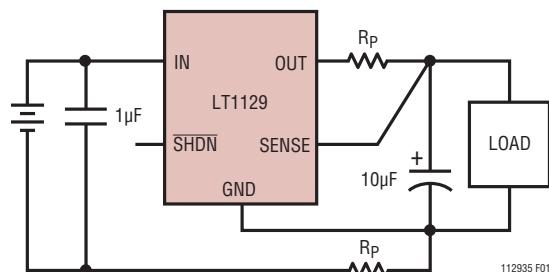


Figure 1. Kelvin Sense Connection

## APPLICATIONS INFORMATION

The LT1129 is a micropower low dropout regulator with shutdown, capable of supplying  $700\text{mA}$  of output current at a dropout voltage of  $0.4\text{V}$ . The device operates with very low quiescent current ( $50\mu\text{A}$ ). In shutdown the quiescent current drops to only  $16\mu\text{A}$ . In addition to the low quiescent current the LT1129 incorporates several protection

features which make it ideal for use in battery-powered systems. The device is protected against reverse input voltages. In battery backup applications where the output can be held up by a backup battery when the input is pulled to ground, the LT1129 acts like it has a diode in series with its output and prevents reverse current flow.

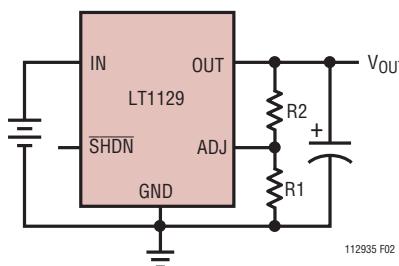
## APPLICATIONS INFORMATION

### Adjustable Operation

The adjustable version of the LT1129 has an output voltage range of 3.75V to 30V. The output voltage is set by the ratio of two external resistors as shown in Figure 2. The device servos the output voltage to maintain the voltage at the adjust pin at 3.75V. The current in R1 is then equal to  $3.75V/R1$ . The current in R2 is equal to the sum of the current in R1 and the adjust pin bias current. The adjust pin bias current, 150nA at 25°C, flows through R2 into the adjust pin. The output voltage can be calculated according to the formula in Figure 2. The value of R1 should be less than 400k to minimize errors in the output voltage caused by the adjust pin bias current. Note that in shutdown the output is turned off and the divider current will be zero. Curves of Adjust Pin Voltage vs Temperature and Adjust Pin Bias Current vs Temperature appear in the Typical Performance Characteristics. The reference voltage at the adjust pin has a positive temperature coefficient of approximately 15ppm/°C. The adjust pin bias current has a negative temperature coefficient. These effects are small and will tend to cancel each other.

The adjustable device is specified with the adjust pin tied to the output pin. This sets the output voltage to 3.75V. Specifications for output voltages greater than 3.75V will be proportional to the ratio of the desired output voltage to 3.75V ( $V_{OUT}/3.75V$ ). For example: load regulation for an output current change of 1mA to 700mA is -6mV typical at  $V_{OUT} = 3.75V$ . At  $V_{OUT} = 12V$ , load regulation would be:

$$\left(\frac{12V}{3.75V}\right) \bullet (-6mV) = (-19mV)$$



$$V_{OUT} = 3.75V \left(1 + \frac{R_2}{R_1}\right) + (I_{ADJ} \bullet R_2)$$

$$V_{ADJ} = 3.75V$$

$$I_{ADJ} = 150nA \text{ at } 25^\circ C$$

OUTPUT RANGE = 3.75V to 30V

Figure 2. Adjustable Operation

### Thermal Considerations

The power handling capability of the device will be limited by the maximum rated junction temperature (125°C). The power dissipated by the device will be made up of two components:

1. Output current multiplied by the input/output voltage differential:  $I_{OUT} \bullet (V_{IN} - V_{OUT})$ , and
2. Ground pin current multiplied by the input voltage:  $I_{GND} \bullet V_{IN}$ .

The ground pin current can be found by examining the Ground Pin Current curves in the Typical Performance Characteristics. Power dissipation will be equal to the sum of the two components listed above.

The LT1129 series regulators have internal thermal limiting designed to protect the device during overload conditions. For continuous normal load conditions the maximum junction temperature rating of 125°C must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

For surface mount devices heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Experiments have shown that the heat spreading copper layer does not need to be electrically connected to the tab of the device. The PC material can be very effective at transmitting heat between the pad area, attached to the tab of the device, and a ground or power plane layer either inside or on the opposite side of the board. Although the actual thermal resistance of the PC material is high, the length/area ratio of the thermal resistor between layers is small. Copper board stiffeners and plated through holes can also be used to spread the heat generated by power devices.

The following tables list thermal resistances for each package. For the TO-220 package, thermal resistance is given for junction-to-case only since this package is usually mounted to a heat sink. Measured values of thermal resistance for several different board sizes and copper areas are listed for each package. All measurements were taken in still air on 3/32" FR-4 board with 1-oz

## OPERATION

copper. This data can be used as a rough guideline in estimating thermal resistance. The thermal resistance for each application will be affected by thermal interactions with other components as well as board size and shape. Some experimentation will be necessary to determine the actual value.

**Table 1. Q Package, 5-Lead DD**

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE*	BACKSIDE		
2500 sq. mm	2500 sq. mm	2500 sq. mm	25°C/W
1000 sq. mm	2500 sq. mm	2500 sq. mm	27°C/W
125 sq. mm	2500 sq. mm	2500 sq. mm	35°C/W

\* Tab of device attached to topside copper

**Table 2. ST Package, 3-Lead SOT-223**

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE*	BACKSIDE		
2500 sq. mm	2500 sq. mm	2500 sq. mm	45°C/W
1000 sq. mm	2500 sq. mm	2500 sq. mm	45°C/W
225 sq. mm	2500 sq. mm	2500 sq. mm	53°C/W
100 sq. mm	2500 sq. mm	2500 sq. mm	59°C/W

\* Tab of device attached to topside copper

**Table 3. S8 Package, 8-Lead Plastic SOIC**

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE*	BACKSIDE		
2500 sq. mm	2500 sq. mm	2500 sq. mm	55°C/W
1000 sq. mm	2500 sq. mm	2500 sq. mm	55°C/W
225 sq. mm	2500 sq. mm	2500 sq. mm	63°C/W
100 sq. mm	2500 sq. mm	2500 sq. mm	69°C/W

\* Device attached to topside copper

### T Package, 5-Lead TO-220

Thermal Resistance (Junction-to-Case) = 5°C/W

### Calculating Junction Temperature

Example: Given an output voltage of 3.3V, an input voltage range of 4.5V to 5.5V, an output current range of 0mA to 500mA, and a maximum ambient temperature of 50°C, what will the maximum junction temperature be?

The power dissipated by the device will be equal to:

$$I_{OUT\ MAX} \cdot (V_{IN\ MAX} - V_{OUT}) + (I_{GND} \cdot V_{IN\ MAX})$$

where,  $I_{OUT\ MAX} = 500\text{mA}$

$$V_{IN\ MAX} = 5.5\text{V}$$

$$I_{GND} \text{ at } (I_{OUT} = 500\text{mA}, V_{IN} = 5.5\text{V}) = 25\text{mA}$$

$$\begin{aligned} \text{so, } P &= 500\text{mA} \cdot (5.5\text{V} - 3.3\text{V}) + (25\text{mA} \cdot 5.5\text{V}) \\ &= 1.24\text{W} \end{aligned}$$

If we use a DD package, then the thermal resistance will be in the range of 25°C/W to 35°C/W depending on copper area. So the junction temperature rise above ambient will be approximately equal to:

$$1.24\text{W} \cdot 30\text{°C/W} = 37.2\text{°C}$$

The maximum junction temperature will then be equal to the maximum junction temperature rise above ambient plus the maximum ambient temperature or:

$$T_{JMAX} = 50\text{°C} + 37.2\text{°C} = 87.2\text{°C}$$

### Output Capacitance and Transient Performance

The LT1129 is designed to be stable with a wide range of output capacitors. The minimum recommended value is 3.3μF with an ESR of 2Ω or less. The LT1129 is a micropower device and output transient response will be a function of output capacitance. See the Transient Response curves in the Typical Performance Characteristics. Larger values of output capacitance will decrease the peak deviations and provide improved output transient response. Bypass capacitors, used to decouple individual components powered by the LT1129, will increase the effective value of the output capacitor.

### Protection Features

The LT1129 incorporates several protection features which make it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device is protected against reverse input voltages, and reverse voltages from output to input. For fixed voltage devices the output and sense pins are tied together at the output.

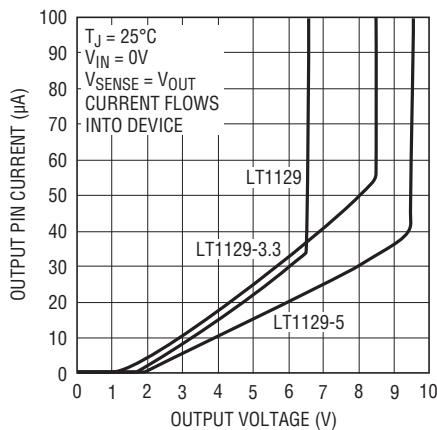
## APPLICATIONS INFORMATION

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 125°C.

The input of the device will withstand reverse voltages of 30V. Current flow into the device will be limited to less than 1mA (typically less than 100µA) and no negative voltage will appear at the output. The device will protect both itself and the load. This provides protection against batteries that can be plugged in backwards.

For fixed voltage versions of the device, the sense pin is internally clamped to one diode drop below ground. For the adjustable version of the device, the output pin is internally clamped at one diode drop below ground. If the output pin of an adjustable device, or the sense pin of a fixed voltage device, is pulled below ground, with the input open or grounded, current must be limited to less than 5mA.

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open circuit. Current flow back into the output will vary depending on the conditions. Many battery-powered circuits incorporate some form of power management. The following information will help optimize battery life. Table 4 summarizes the following information.



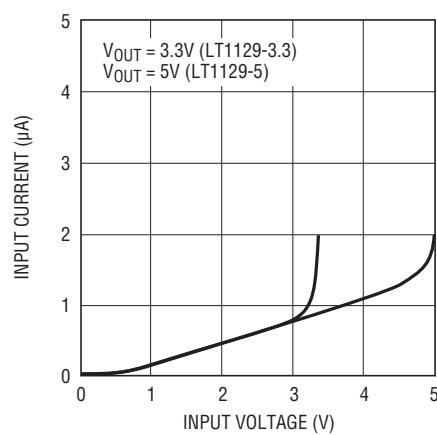
**Figure 3. Reverse Output Current**

The reverse output current will follow the curve in Figure 3 when the input pin is pulled to ground. This current flows through the output pin to ground. The state of the shutdown pin will have no effect on output current when the input pin is pulled to ground.

In some applications it may be necessary to leave the input to the LT1129 unconnected when the output is held high. This can happen when the LT1129 is powered from a rectified AC source. If the AC source is removed, then the input of the LT1129 is effectively left floating. The reverse output current also follows the curve in Figure 3 if the input pin is left open. The state of the shutdown pin will have no effect on the reverse output current when the input pin is floating.

When the input of the LT1129 is forced to a voltage below its nominal output voltage and its output is held high, the reverse output current will still follow the curve shown in Figure 3. This can happen if the input of the LT1129 is connected to a discharged (low voltage) battery and the output is held up by either a backup battery or by a second regulator circuit.

When the input pin is forced below the output pin or the output pin is pulled above the input pin, the input current will typically drop to less than 2µA (see Figure 4). The state of the shutdown pin will have no effect on the reverse output current when the output is pulled above the input.



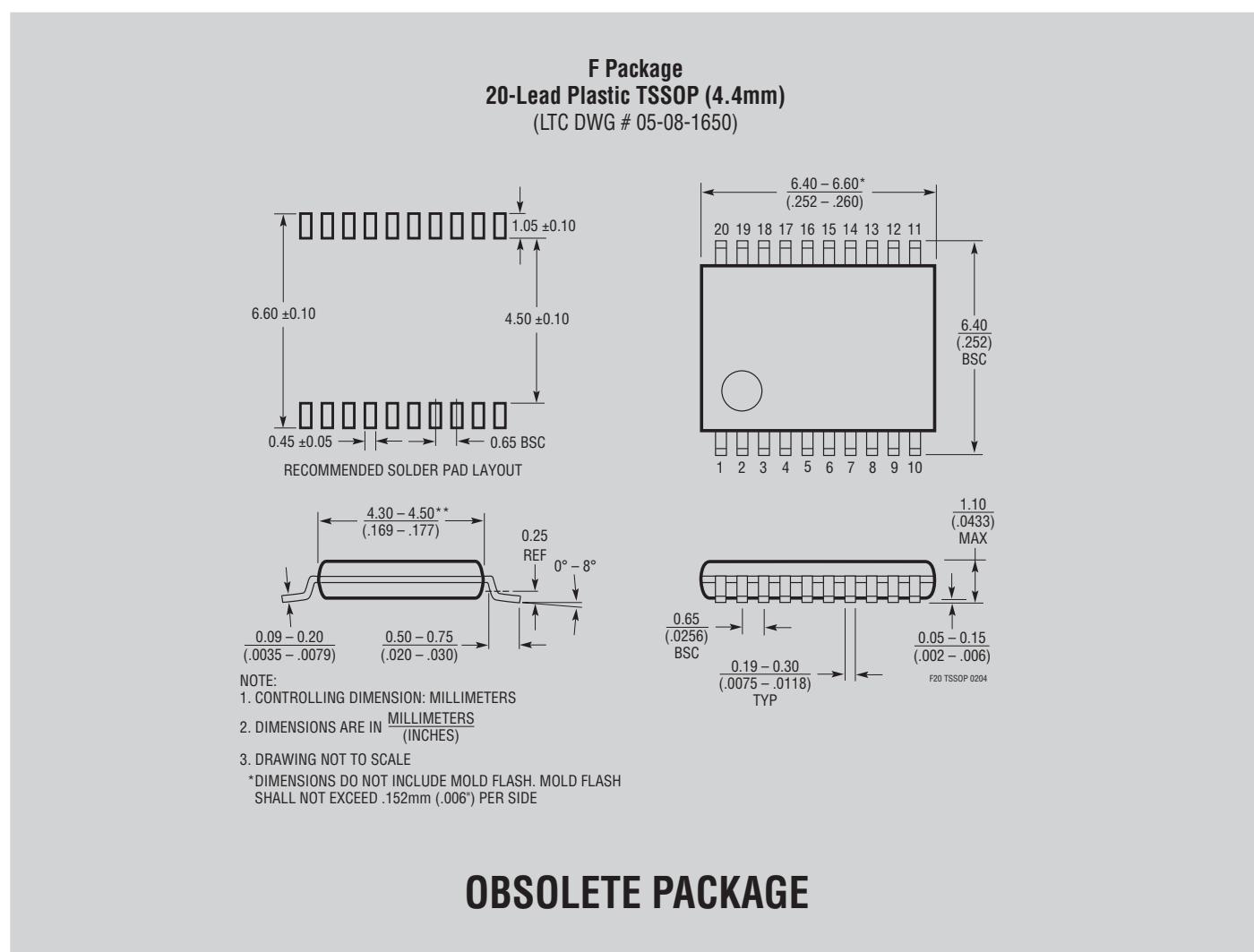
**Figure 4. Input Current**

## APPLICATIONS INFORMATION

**Table 4. Fault Conditions**

INPUT PIN	SHDN PIN	OUTPUT PIN	
< V <sub>OUT</sub> (Nominal)	Open (Hi)	Forced to V <sub>OUT</sub> (Nominal)	Reverse Output Current ≈ 15µA (See Figure 3) Input Current ≈ 1µA (See Figure 4)
< V <sub>OUT</sub> (Nominal)	Grounded	Forced to V <sub>OUT</sub> (Nominal)	Reverse Output Current ≈ 15µA (See Figure 3) Input Current ≈ 1µA (See Figure 4)
Open	Open (Hi)	Forced to V <sub>OUT</sub> (Nominal)	Reverse Output Current ≈ 15µA (See Figure 3)
Open	Grounded	Forced to V <sub>OUT</sub> (Nominal)	Reverse Output Current ≈ 15µA (See Figure 3)

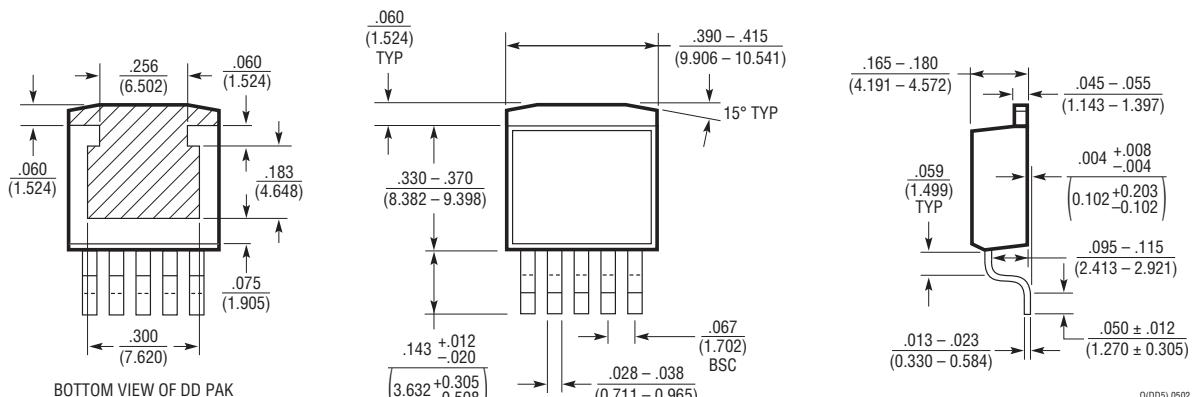
## PACKAGE DESCRIPTION



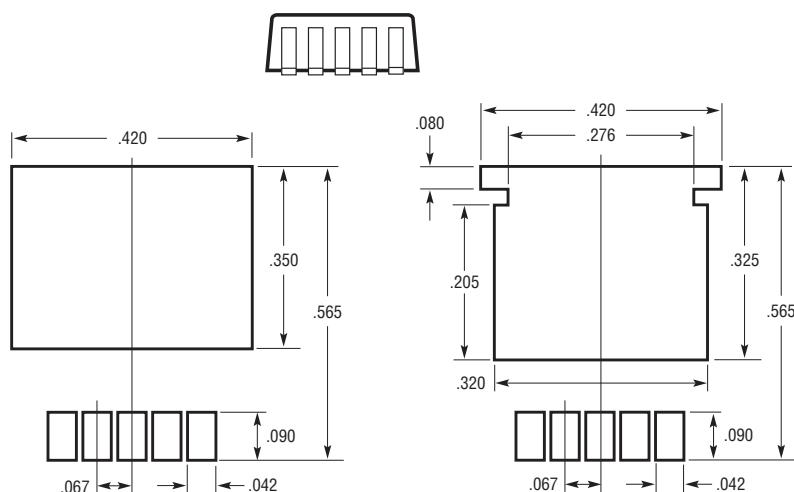
## OBSOLETE PACKAGE

## PACKAGE DESCRIPTION

**Q Package  
5-Lead Plastic DD Pak  
(LTC DWG # 05-08-1461)**



Q(DDS) 0502



RECOMMENDED SOLDER PAD LAYOUT

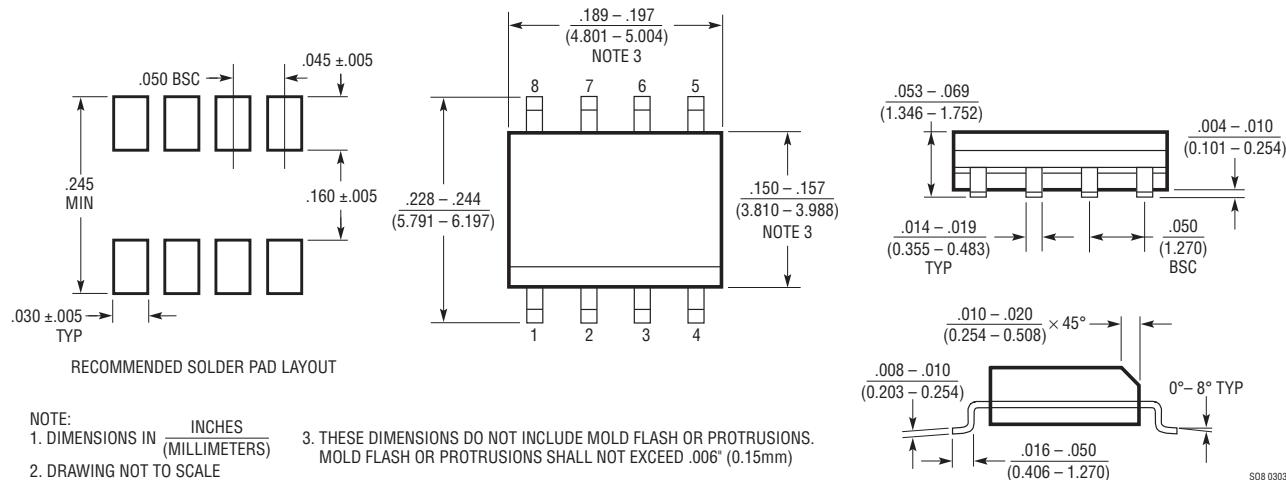
NOTE:

1. DIMENSIONS IN INCH/(MILLIMETER)
2. DRAWING NOT TO SCALE

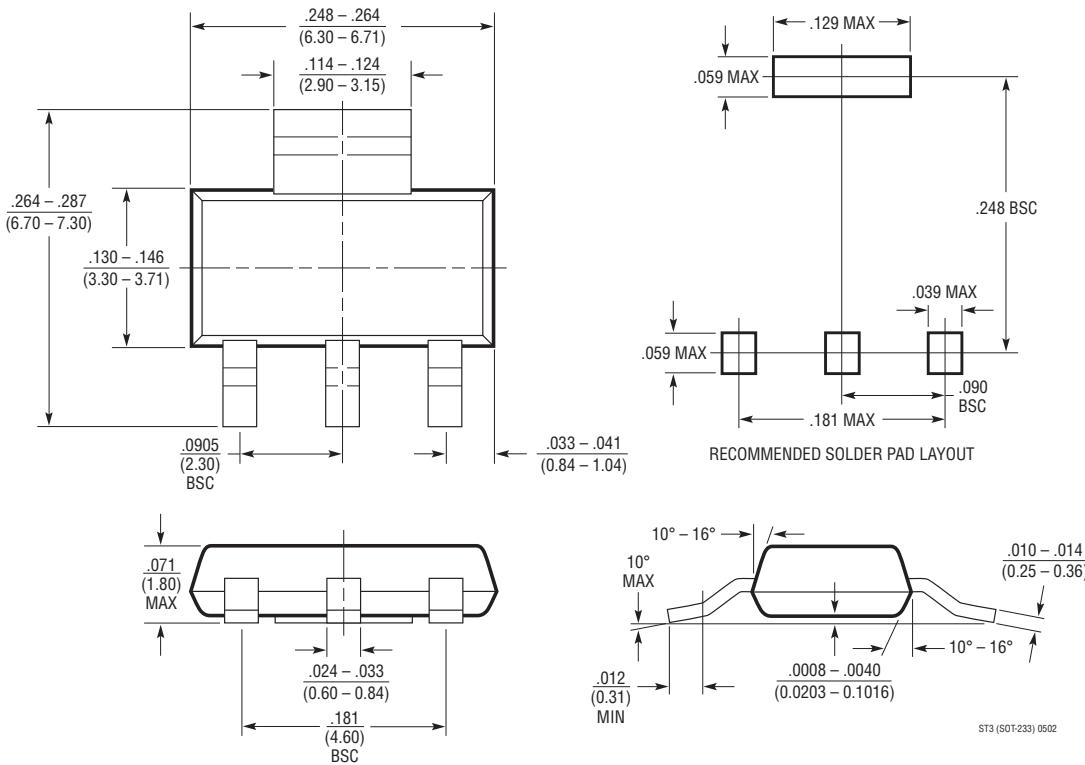
RECOMMENDED SOLDER PAD LAYOUT  
FOR THICKER SOLDER PASTE APPLICATIONS

## PACKAGE DESCRIPTION

**S8 Package**  
**8-Lead Plastic Small Outline (Narrow 0.150)**  
(LTC DWG # 05-08-1610)



**ST Package**  
**3-Lead Plastic SOT-223**  
(LTC DWG # 05-08-1630)



**MAXIM**

# Preset/Adjustable Output CMOS Inverting Switching Regulators

**MAX635/636/637**

## General Description

The MAX635/MAX636/MAX637 inverting switching regulators are designed for minimum component DC-DC conversion in the 5mW to 500mW range.

Low power applications require only a diode, output filter capacitor, and a low-cost inductor. An additional MOSFET and driver are needed for higher power applications. Low battery detection circuitry is included on chip.

The MAX635/636/637 are preset for -5V, -12V, and -15V outputs, respectively. However, the regulators can be set to other levels by adding 2 resistors.

Maxim manufactures a broad line of step-up, step-down, and inverting DC-DC converters, with features such as logic-level shutdown, adjustable oscillator frequency, and external MOSFET drive.

## Applications

Minimum Component, High-Efficiency DC-DC Converters

Portable Instruments

Battery Power Conversion

Board Level DC-DC Conversion

## Features

- ◆ Preset -5V, -12V, -15V Output Voltages
- ◆ Adjustable Output with 2 Resistors
- ◆ 85% Typ Efficiency
- ◆ Only 3 External Components
- ◆ 80 $\mu$ A Typ Operating Current
- ◆ Low Battery Detector

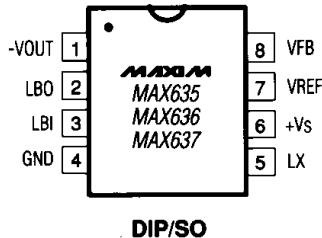
## Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE
MAX635XCPA	0°C to +70°C	8 Plastic DIP
MAX635XCSA	0°C to +70°C	8 Narrow SO
MAX635XC/D	0°C to +70°C	Dice
MAX635XEPA	-40°C to +85°C	8 Plastic DIP
MAX635XESA	-40°C to +85°C	8 Narrow SO
MAX635XEJA	-40°C to +85°C	8 CERDIP
MAX635XMJA	-55°C to +125°C	8 CERDIP
MAX636XCPA	0°C to +70°C	8 Plastic DIP
MAX636XCSA	0°C to +70°C	8 Narrow SO
MAX636XC/D	0°C to +70°C	Dice
MAX636XEPA	-40°C to +85°C	8 Plastic DIP
MAX636XESA	-40°C to +85°C	8 Narrow SO
MAX636XEJA	-40°C to +85°C	8 CERDIP
MAX636XMJA	-55°C to +125°C	8 CERDIP

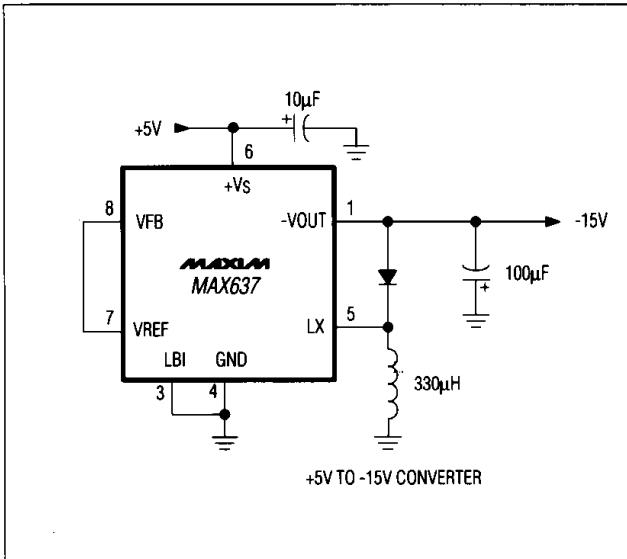
\*X = A for 5% Output Accuracy, X = B for 10% Output Accuracy.  
Ordering Information continued on last page.

## Pin Configuration

Top View



## Typical Operating Circuit

**MAXIM**

Maxim Integrated Products 1

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# Preset/Adjustable Output CMOS Inverting Switching Regulators

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage, +Vs (Note 1)	+18V
Input Voltage, LBO, LBI, VFB	-0.3V to (+Vs + 0.3V)
LX Output Current	525mA Peak
LBO Output Current	50mA
Power Dissipation	

- Plastic DIP (derate 8.33mW/°C above +50°C) 625mW
- Small Outline (derate 6mW/°C above +50°C) 450mW
- CERDIP (derate 8mW/°C above +50°C) 800mW

Operating Temperature Range	
MAX63_C	0°C to +70°C
MAX63_E	-40°C to +85°C
MAX63_M	-55°C to +125°C
Storage Temperature	-65°C to +160°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(TA = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Note 1)	+Vs	TA = +25°C Over Temperature	2.3 2.6		16.5 16.5	V
Supply Current	Is	No Load, LX Off, Over Temperature +Vs = +5V +Vs = +15V		80 260	150 500	µA
Reference Voltage	VREF	TA = +25°C Over Temperature	1.24 1.20	1.31	1.38 1.42	V
VOUT Voltage (Note 2)		No Load, VFB = VREF, +Vs = +5V Over Temperature  MAX635A } 5% Output Accuracy MAX636A } MAX637A }  MAX635B } 10% Output Accuracy MAX636B } MAX637B }	-4.75 -11.4 -14.25  -4.5 -10.8 -13.5	-5.0 -12.0 -15.0  -5.0 -12.0 -15.0	-5.25 -12.6 -15.75  -5.5 -13.2 -16.5	V
Efficiency				85		%
Line Regulation (Note 2)		+5V < +Vs < +15V		0.5		%VOUT
Load Regulation (Note 2)		POUT = 0mW to 150mW		0.2		%VOUT
Oscillator Frequency	f <sub>0</sub>	+Vs = +5V    MAX63_A MAX63_B	45 40	50 50	56 65	kHz
Oscillator Duty Cycle		+Vs = +5V	40	50	60	%
LX On Resistance	R <sub>ON</sub>	I <sub>X</sub> = 100mA, +Vs = +5V = +15V		9 4	16 8	Ω
LX Leakage Current	I <sub>XL</sub>	+Vs = +16.5V TA = +25°C Over Temperature		0.01	1.0 30	µA
VFB Input Bias Current	I <sub>FB</sub>			0.01	10	nA
Low Battery Threshold	V <sub>LBI</sub>			1.31		V
Low Battery Input Bias Current	I <sub>LBI</sub>			0.01	10	nA
Low Battery Output Current	I <sub>LBO</sub>	V <sub>2</sub> = +0.4V, V <sub>3</sub> = +1.1V TA = 25°C Over Temperature		0.5	1.0	mA
Low Battery Output Leakage Current	I <sub>LBOL</sub>	V <sub>2</sub> = +16.5V, V <sub>3</sub> = +1.4V		0.01	3.0	µA

Note 1: In addition to the Absolute Maximum Rating of +18V, the input voltage also must not exceed 24V - | -VOUT | .

Note 2: Guaranteed by correlation with DC pulse measurements.

# Preset/Adjustable Output CMOS Inverting Switching Regulators

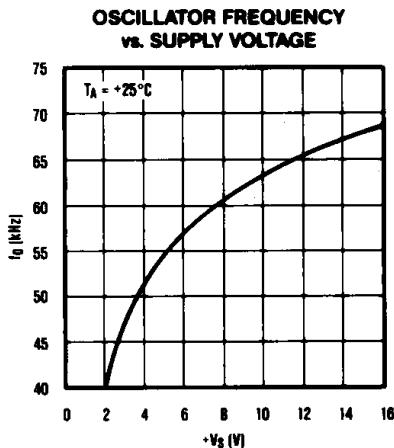
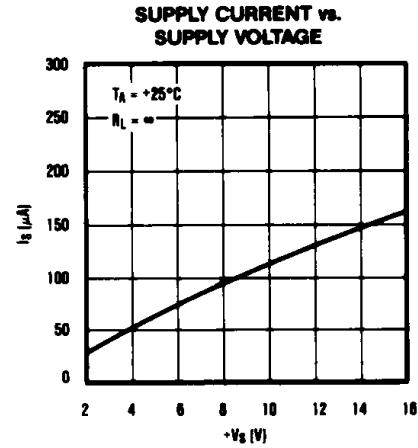
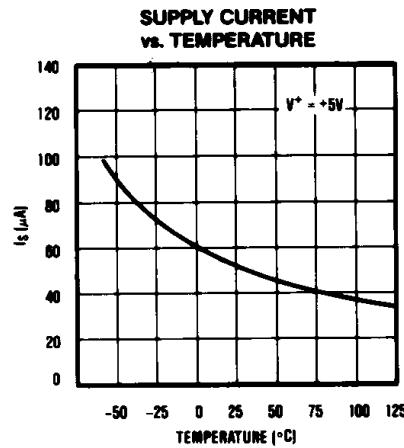
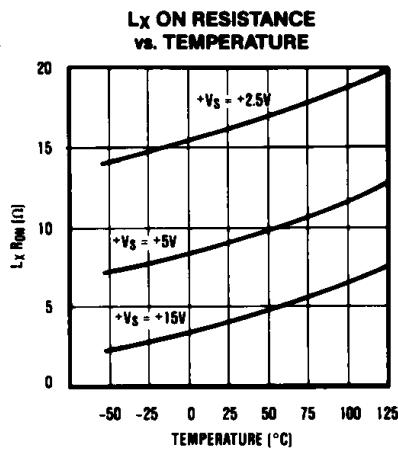
## Pin Description

PIN	NAME	FUNCTION
1	-VOUT	The sense INPUT for fixed output operation, -VOUT, is internally connected to the on-chip voltage divider. Although it is connected to the output of the DC-DC converter (Figure 2), VOUT does not supply current, LX does.
2	LBO	Low Battery Detector Output. An open drain N-channel MOSFET which sinks current when the voltage at LBI is below 1.31V.
3	LBI	Low Battery Detector Input. When the voltage at LBI is lower than the low Battery Detector threshold (+1.31V), LBO sinks current.
4	GND	Ground

PIN	NAME	FUNCTION
5	LX	This pin drives the external inductor with an internal P-channel power MOSFET. LX has an output resistance of typically 6Ω and a peak current rating of 525mA.
6	+Vs	The positive Supply Voltage, from +2V to +16.5V. The total difference between the negative output voltage and the positive input must be less than 24V.
7	VREF	The Voltage Reference output is +1.31V, generated by an on-chip bandgap reference.
8	VFB	When VFB is tied to VREF, the DC-DC converter output will be the factory preset value. When an external voltage divider is connected to VFB and VREF, this pin becomes the feedback input for adjustable output operation.

MAX635/636/637

## Typical Operating Characteristics



# Preset/Adjustable Output CMOS Inverting Switching Regulators

## Detailed Description

### Principle of Operation

Figure 1 shows a simplified inverting converter. When the switch is closed, a charging current flows through the inductor, creating a magnetic field. When the switch opens, the current continues to flow through the inductor in the same direction as the charging current. Since the switch is now open, the current must flow through the diode, thereby charging the capacitor with a negative voltage. As the energy stored in the inductor is transferred to the output filter capacitor, the current linearly decays to zero, and the magnetic field collapses.

The MAX635/636/637 controls the magnitude of the negative output voltage by turning the switch on and off only when the output voltage has become more positive than the desired value.

### Basic Circuit Operation

Figure 2 shows the standard circuit for converting a positive voltage into a negative one. When the output becomes more positive than the preset level, the Error Comparator switches low, and the MOSFET at LX is toggled on and off at the clock frequency. During the low-going period of the oscillator, P1 is on, and current is delivered to the external inductor through the LX pin.

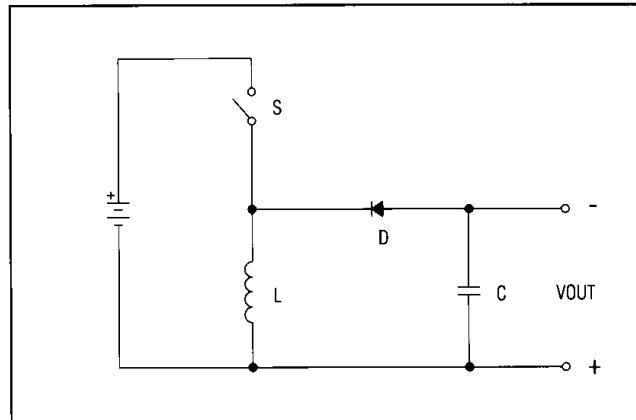


Figure 1. Simplified Inverting Converter

When the oscillator output goes high, the MOSFET turns off, but current continues to flow through the inductor. Diode D1 thus conducts, and the output filter capacitor, C1, is charged negatively.

### Basic Step-Down Circuit

Table 1 lists some coil manufacturers and typical part numbers. Table 2 shows nominal inductor parameters for a variety of input and output voltages. The data refers to the circuit of Figure 2. When noise is not critical, a

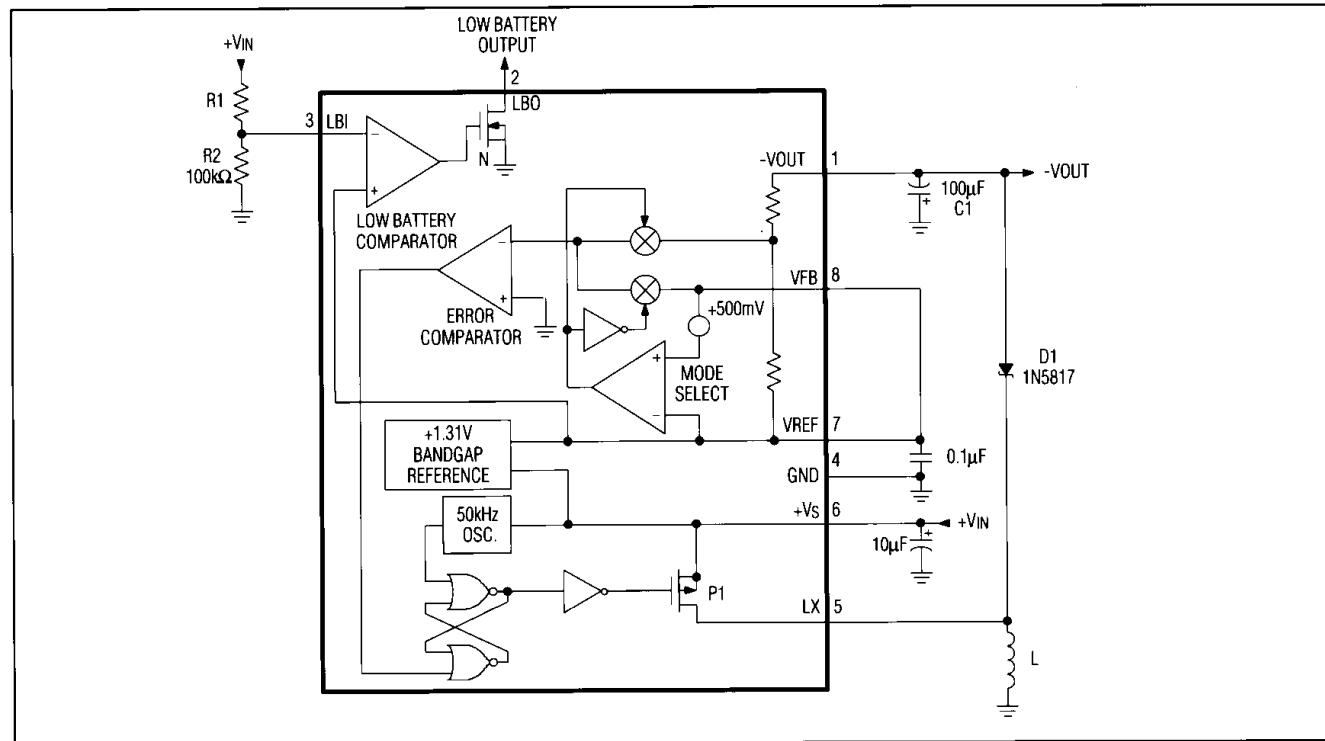


Figure 2. MAX635/636/637 Block Diagram and Typical Circuit (Table 2)

# Preset/Adjustable Output CMOS Inverting Switching Regulators

low-cost bobbin inductor will suffice. For higher power circuits, or when low noise and EMI are required, pot cores or toroids should be used. If more output power is desired, see the Medium Power Inverters section.

**Table 1. Coil and Core Manufacturers (Note 3)**

MANUFACTURER	TYPICAL PART #	DESCRIPTION
<b>ASIA</b>		
TDK Corporation 13-1, Nihonbashi 1-chome Chuo-ku Tokyo 103 Japan		
<b>EUROPE</b>		
Richard Jahre GmbH Luetzowstrasse 90 1000 Berlin 30 Germany		
<b>BOBBIN INDUCTORS</b>		
Dale	IHA-104	500 $\mu$ H, 0.5 $\Omega$
Caddell-Burns	7070-29	220 $\mu$ H, 0.55 $\Omega$
Gowanda	1B253	250 $\mu$ H, 0.44 $\Omega$
TRW	LL-500	500 $\mu$ H, 0.75 $\Omega$
<b>POTTED TOROIDAL INDUCTORS</b>		
Dale	TE-3Q4TA	1mH, 0.82 $\Omega$
TRW	MH-1	600 $\mu$ H, 1.9 $\Omega$
Gowanda	050AT1003	100 $\mu$ H, 0.05 $\Omega$
<b>FERRITE CORES AND TOROIDS (Note 4)</b>		
Allen Bradley	T0451S100A	Tor. Core, 500nH/T <sup>2</sup>
Siemens	B64290-K38-X38	Tor. Core, 4 $\mu$ H/T <sup>2</sup>
Magnetics	555.130	Tor. Core, 53nH/T <sup>2</sup>
Stackpole	57-3215	Pot Core, 14mm x 8mm
Magnetics	G-41408-25	Pot Core, 14 x 8, 250nH/T <sup>2</sup>

**Note 3:** This list does not constitute an endorsement by Maxim Integrated Products and is not intended to be a comprehensive list of all manufacturers of these components.

**Note 4:** Permag Corp. is a distributor for many of the listed core and toroid manufacturers (516) 822-3311.

**Table 2. Inductor Selection for Common Designs (Figure 2)**

V <sub>IN</sub> (V)	V <sub>OUT</sub> (V)	I <sub>OUT</sub> (mA)	INDUCTOR	
			Part No.	$\mu$ H $\Omega$
+3	-5	5	7070-27	150 $\mu$ H 0.43
+5	-5	25	7070-27	150 $\mu$ H 0.43
+9	-5	40	7070-31	330 $\mu$ H 0.72
+12	-5	45	7070-33	470 $\mu$ H 0.88
+15	-5	50	7070-35	680 $\mu$ H 1.5
+5	-12	12	7070-26	120 $\mu$ H 0.32
+9	-12	30	7070-31	330 $\mu$ H 0.72
+12	-12	40	7070-33	470 $\mu$ H 0.88
+3	-15	2	7070-27	150 $\mu$ H 0.43
+5	-15	8	7070-27	150 $\mu$ H 0.43
+9	-15	25	7070-31	330 $\mu$ H 0.72

**Note 5:** Caddell-Burns N.Y. (516) 746-2310.

## Low Battery Detector

The Low Battery Output, LBO, sinks current whenever the input voltage at Low Battery Input, LBI, is less than +1.31V. LBI is a high impedance CMOS input, with less than 10nA leakage current. LBO is an open drain N-channel MOSFET with about 500 $\Omega$  of output resistance. The trip voltage of the Low Battery Detector can be adjusted using an external voltage divider as shown in Figure 2. If hysteresis is desired, add a resistor between LBO and LBI.

Let R<sub>2</sub> be any resistance in the 10k $\Omega$  to 10M $\Omega$  range, typically 100k $\Omega$ , then:

$$R_1 = R_2 \left( \frac{V_{LB}}{1.31V} - 1 \right)$$

(V<sub>LB</sub> is the desired Low Battery detection voltage.)

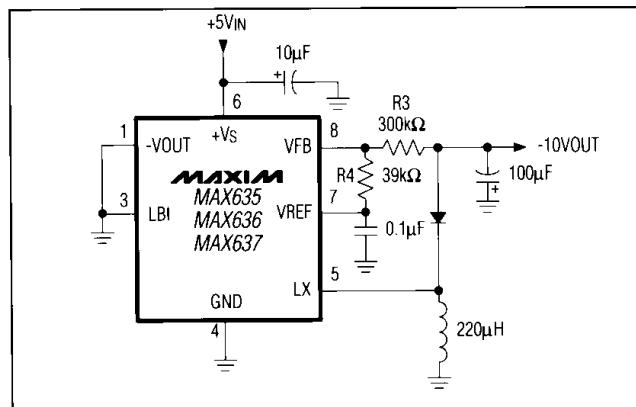


Figure 3. Adjustable Output Operation

# Preset/Adjustable Output CMOS Inverting Switching Regulators

## Fixed or Adjustable Output

For operation at one of the preset output voltages (-5V for the MAX635, -12V for the MAX636, and -15V for the MAX637), VFB is connected to VREF, and no external resistors are required.

Other output voltages are selected by connecting an external voltage divider to VFB as shown in Figure 3. The output is set by R3 and R4 as follows:

Let R4 be any resistance in the  $10\text{k}\Omega$  to  $10\text{M}\Omega$  range, typically  $100\text{k}\Omega$ , then:

$$V_{OUT} = -1.31V \times \frac{R_3}{R_4}$$

## External Components

### What Value of Inductor?

#### A General Discussion

The converters in this data sheet operate by charging an inductor from a DC input and then discharging the inductor to generate a DC output that is opposite in polarity to the input.

Inductor selection for any DC-DC converter depends on three things: the desired output power, the input voltage (or input voltage range), and the converter's oscillator frequency and duty cycle. The oscillator timing is important because it determines how long the coil will be charged during each cycle. This, along with the input voltage, determines how much energy will be stored in the coil.

The maximum amount of energy ( $E_L$ ) in the coil each cycle is a function of the peak current ( $I_{pk}$ ) and the inductance of the coil ( $L$ ):

The inductor must meet four electrical criteria:

[ ] **Value** – low enough inductance so it stores adequate energy at the worst-case, low input voltage.

High enough so excessive and potentially destructive currents are avoided under worst-case high conditions for power-switch transistor on time and high input voltage.

[ ] **Saturation** – The coil must deliver the correct inductance value at the worst-case, high peak operating current.

[ ] **EMI** – Electromagnetic interference must not upset nearby circuitry or the regulator IC. Ferrite bobbin types work well for digital circuits; toroid or pot core types work well for EMI-sensitive analog circuits.

[ ] **DC resistance** – Winding resistance must be adequately low so efficiency is not affected and self-heating

does not occur. Values less than  $0.5\Omega$  are usually more than adequate.

Other inductor parameters, such as core loss or self-resonant frequency, are not a factor at the relatively low MAX635/636/637 operating frequency.

### Inductor Value – Low Enough?

The problem that bites designs most often, especially in the production or pre-production phase, happens when the inductor value is too high. These units fail to deliver enough load current and exhibit poor load regulation. The worst case is:

- [ ] Maximum load current
- [ ] Minimum supply voltage
- [ ] Maximum inductor value, including tolerance
- [ ] Maximum on resistance of the switch because it reduces the excitation voltage across the inductor
- [ ] Worst-case low on time

### Inductor Value – High Enough?

The inductor value must also be high enough so peak currents do not stress the transistor or cause the inductor core to saturate. Odd symptoms can be traced to excessive inductor currents: low efficiency, rattling heat sinks, whining coils, and increased output ripple. Very low inductor values can result in damaged power transistors.

The slope of the inductor current, and therefore the peak value that it reaches in a given on time, is determined by the supply voltage and the inductor value. The worst case occurs at:

- [ ] Maximum supply voltage
- [ ] Minimum inductor value, including tolerance
- [ ] Minimum on resistance of the switch
- [ ] Low switching frequency (or maximum switch on time)

### Inductor Selection

The inductor equations below must be calculated for both worst-case sets of conditions. The final value chosen should be between the minimum value and maximum value calculated. Within these bounds, the value can be adjusted slightly lower for extra load capability or higher for lowest ripple.

$$[1] \quad I_{pk} = \frac{V_{OUT} + V_{DIODE}}{(0.25)(V_{IN} - V_{SW})} (I_{OUT})$$

$$[2] \quad L = \frac{V_{IN} - V_{SW}}{I_{pk}} (t_{ON})$$

where  $V_{SW}$  is the voltage drop across the switch in the on state. Conservatively, the worst case is about 0.75V

# Preset/Adjustable Output CMOS Inverting Switching Regulators

max, 0.25V min with VIN = +15V and 1.5V max, 0.5V min with VIN = +5V.

Example: A +5V 10% input must be converted to -12V at 12mA.

A Schottky diode (1N5817) and a MAX636A are used.

Calculate the maximum inductor value allowed:

$$I_{pk} = \frac{12V - 0.4V}{(0.25)(4.5V - 1.5V)} (12mA) = 198mA$$

$$L = \frac{4.5V - 1.5V}{198mA} (9\mu s) = 136\mu H$$

Calculate the minimum inductor value allowed:

$I_{pk}$  = 525mA (from table of max ratings; use the power MOSFET max ratings for external transistor circuits.)

$$L = \frac{5.5V - 0.5V}{525mA} (11\mu s) = 105\mu H$$

A value of 120 $\mu$ H would be a good choice for this application.

$I_{pk}$  must also be compared to the current rating of the LX switch. If  $I_{pk}$  exceeds the peak current rating of the switch (525mA), an external MOSFET or transistor with an adequate current rating must be used (see Medium Power Inverters).

The coil resistance has a significant effect on the output current; a coil with a low resistance will increase the output current and overall efficiency. The inductor

should have a powdered iron or ferrite core and should have a resistance less than 0.5 $\Omega$ .

## Medium Power Inverters

In the circuit of Figure 4, the MAX626 MOSFET driver is used to convert the open drain LX output to a signal suitable for driving the gate of an external P-Channel MOSFET. The IRF9541 has a gate threshold voltage of 2V to 4V so it will have a relatively high resistance if driven with only 5V of gate drive. To increase the gate drive voltage, and thereby increase efficiency, the negative supply pin of the CMOS inverter is connected to the negative output rather than to the ground. Once the circuit is started, the gate drive swings from +5V to -VOUT.

At start-up, the voltage at -VOUT is one Schottky diode drop above ground, and the gate drive to the power MOSFET is slightly less than 5V. The output should be only lightly loaded to ensure start-up, since the output power capability of the circuit is very low until -VOUT is a couple of volts negative. (See Table 3 for component values for L2 and IC1.)

**Table 3. Component Selector for Medium Power Inverters (Figure 4)**

V <sub>IN</sub>	-V <sub>OUT</sub>	I <sub>OUT</sub>	EFFICIENCY	IC1	L1
5V	-5V	400mA	70%	MAX635	27 $\mu$ H
5V	-5V	500mA	64%	MAX635	18 $\mu$ H
5V	-12V	150mA	75%	MAX636	27 $\mu$ H
5V	-12V	200mA	70%	MAX636	18 $\mu$ H

**Notes:** 18 $\mu$ H Coil = Caddell-Burn's (Mineola, NY) Model 6860-04.

27 $\mu$ H Coil = Caddell-Burn's Model 6860-06.

## External Diode

In most DC-DC converter circuits, the current in the "catch" diode (Figure 2, D1) abruptly goes from zero to its peak value each time the MOSFET at LX switches off. To avoid excessive losses, the diode must have a fast turn-on time. For low power circuits with peak currents less than 100mA, signal diodes such as 1N4148s perform well. For higher current circuits, or for maximum efficiency at low power, the 1N5817 series of Schottky diodes are recommended. Although 1N4001s and other general purpose rectifiers are rated for high currents, they are unacceptable because their slow turn-on time results in excessive losses.

## Output Filter Capacitor

The MAX635/636/637's output ripple has 2 components which are 90° out of phase. One component results from the change in the stored charge on the filter capacitor with each LX pulse. The other is the product of the capacitor's charge-discharge current and its Equivalent

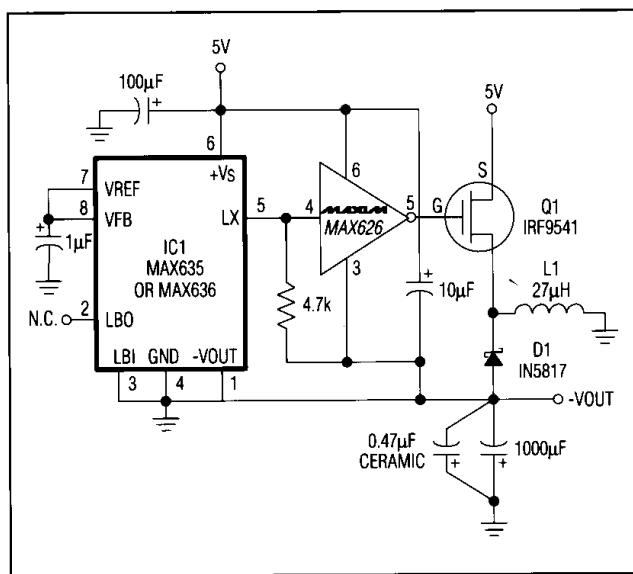


Figure 4. Medium Power Inverter

# Preset/Adjustable Output CMOS Inverting Switching Regulators

**Series Resistance (ESR).** With low-cost aluminum electrolytic capacitors, the ESR produced ripple is often larger than that caused by the change in charge. Consequently, high quality aluminum or tantalum filter capacitors will minimize output ripple, even if smaller capacitance values are used. Best results at reasonable cost are typically achieved with a high quality aluminum electrolytic, in the 100 $\mu$ F to 500 $\mu$ F range, in parallel with a 0.1 $\mu$ F ceramic capacitor.

## Application Hints

### Inductor Saturation

When using off-the-shelf inductors, make sure that their peak current rating is observed. When designing your own inductors, observe the core manufacturer's Ampere-turns on NI ratings. Failure to observe the peak current or NI ratings may lead to saturation of the inductor, especially in circuits with external boosting transistors. Inductor saturation leads to very high current levels through the power switching device causing excessive power dissipation, poor efficiency, and possible damage.

Test for saturation by applying the maximum load and the maximum input voltage while monitoring the inductor current with a current probe. The normal inductor current waveform is a sawtooth with a linear current ramp. Saturation creates a nonlinear current waveform with a very rapid increase in current once the inductor saturates.

## Ordering Information (continued)

PART*	TEMP. RANGE	PIN - PACKAGE
MAX637XCPA	0°C to +70°C	8 Plastic DIP
MAX637XCSA	0°C to +70°C	8 Narrow SO
MAX637XCJA	0°C to +70°C	8 CERDIP
MAX637XC/D	0°C to +70°C	Dice
MAX637XEPA	-40°C to +85°C	8 Plastic DIP
MAX637XESA	-40°C to +85°C	8 Narrow SO
MAX637XEJA	-40°C to +85°C	8 CERDIP
MAX637XMJA	-55°C to +125°C	8 CERDIP

\*X = A for 5% Output Accuracy, X = B for 10% Output Accuracy.

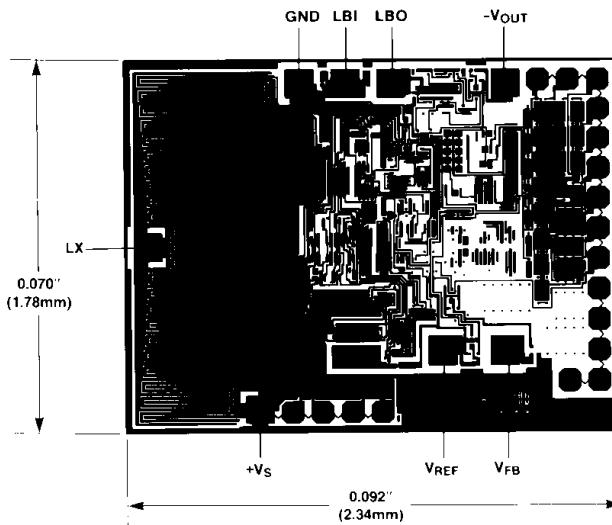
## Bypassing and Compensation

The high current pulses in the LX output and the external inductor can cause erratic operation unless the MAX635/636/637 is properly bypassed. Connect a 10mF bypass capacitor directly across the device between +VS and GND to minimize the inductance and high frequency impedance of the power source. Also make sure that the high current ground return path of the inductor does not cause a voltage drop in the regulator's ground line.

The reference voltage output, VREF, should be bypassed to ground with a 0.1 $\mu$ F capacitor. Avoid coupling to the high current path that includes the LX output and the inductor ground return.

When the value of the voltage setting resistors (R3 and R4, Figure 3) exceed 50k $\Omega$ , stray capacitance at the VFB input can add a "lag" to the feedback response causing output pulses to occur in bursts. This increases low-frequency ripple and lowers efficiency. This problem can often be avoided by minimizing lead lengths and circuit board trace size at the VFB node. Normal operation with evenly distributed output pulses can be restored by adding a "lead" compensation capacitor (100pF to 10nF) in parallel with R3.

## Chip Topography



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

## FEATURES

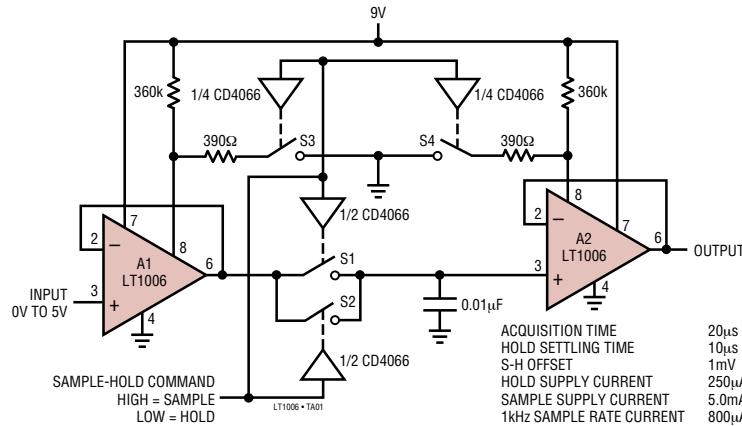
- Single Supply Operation
  - Input Voltage Range Extends to Ground
  - Output Swings to Ground while Sinking Current
- *Guaranteed* Offset Voltage: 50 $\mu$ V Max
- *Guaranteed* Low Drift: 1.3 $\mu$ V/ $^{\circ}$ C Max
- *Guaranteed* Offset Current: 0.5nA Max
- *Guaranteed* High Gain
  - 5mA Load Current: 1.5 Million Min
  - 17mA Load Current: 0.8 Million Min
- *Guaranteed* Low Supply Current: 520 $\mu$ A Max
- Supply Current can be Reduced by a Factor of 4
- Low Voltage Noise, 0.1Hz to 10Hz: 0.55 $\mu$ V<sub>P-P</sub>
- Low Current Noise—
  - Better than OP-07: 0.07pA/ $\sqrt$ Hz at 10Hz
- High Input Impedance: 250M $\Omega$  Min
- Minimum Supply Voltage: 2.7V Min

## APPLICATIONS

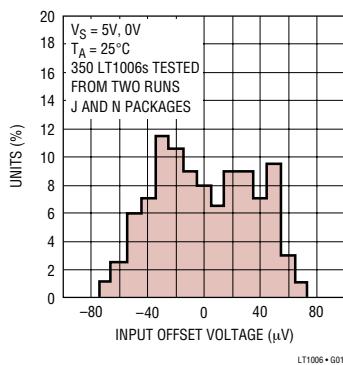
- Low Power Sample-and-Hold Circuits
- Battery-Powered Precision Instrumentation
  - Strain Gauge Signal Conditioners
  - Thermocouple Amplifiers
- 4mA to 20mA Current Loop Transmitters
- Active Filters

## TYPICAL APPLICATION

**LT1006 Single Supply, Micropower Sample and Hold**



**Distribution of Input Offset Voltage**

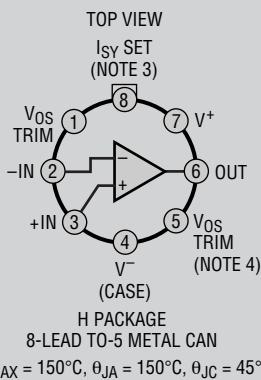
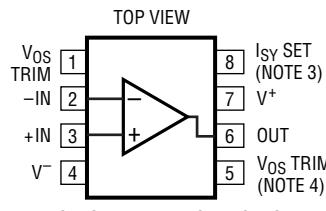


**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Supply Voltage ..... ±22V  
 Input Voltage ..... Equal to Positive Supply Voltage  
 Input Voltage ..... 5V Below Negative Supply Voltage  
 Differential Input Voltage ..... 30V  
 Output Short-Circuit Duration ..... Indefinite

Operating Temperature Range  
**LT1006AM/LT1006M (OBSOLETE)** ..... −55°C to 125°C  
**LT1006AC/LT1006C/LT1006S8** ..... 0°C to 70°C  
 Storage Temperature Range ..... −65°C to 150°C  
 Lead Temperature (Soldering, 10 sec) ..... 300°C

**PACKAGE/ORDER INFORMATION**

	ORDER PART NUMBER	 N8 PACKAGE 8-LEAD PDIP      S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 100^\circ\text{C}$ , $\theta_{JA} = 130^\circ\text{C}/\text{W}$ (N8) $T_{JMAX} = 150^\circ\text{C}$ , $\theta_{JA} = 200^\circ\text{C}/\text{W}$ (S8)	ORDER PART NUMBER
	LT1006AMH		LT1006CN8
	LT1006MH		LT1006S8
	LT1006ACH		S8 PART MARKING
	LT1006CH		1006
<b>OBSOLETE PACKAGES</b>		Consider the N8 or S8 Package for Alternate Source	LT1006AMJ8
			LT1006MJ8
		J8 PACKAGE 8-LEAD CERDIP	LT1006ACJ8
			LT1006CJ8

Consult LTC Marketing for parts specified with wider operating temperature ranges.

**ELECTRICAL CHARACTERISTICS**

$V_S = 5\text{V}$ ,  $V_{CM} = 0\text{V}$ ,  $V_{OUT} = 1.4\text{V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1006AM/AC			LT1006M/C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage	LT1006S8		20	50		30	80	$\mu\text{V}$
							80	400	$\mu\text{V}$
$\Delta V_{OS}$ $\Delta \text{Time}$	Long-Term Input Offset Voltage Stability	LT1006S8		0.4			0.5		$\mu\text{V}/\text{Mo}$
							0.7		$\mu\text{V}/\text{Mo}$
$I_{OS}$	Input Offset Current			0.12	0.5		0.15	0.9	nA
$I_B$	Input Bias Current			9	15		10	25	nA
$e_n$	Input Noise Voltage	0.1Hz to 10Hz		0.55			0.55		$\mu\text{V}_{\text{P-P}}$
	Input Noise Voltage Density	$f_0 = 10\text{Hz}$ $f_0 = 1000\text{Hz}$		23	32		23	32	$\text{nV}/\sqrt{\text{Hz}}$
				22	25		22	25	$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input Noise Current Density	$f_0 = 10\text{Hz}$		0.07			0.08		$\text{pA}/\sqrt{\text{Hz}}$
	Input Resistance Differential Mode	(Note 2)	180	400	5	100	300	4	$\text{M}\Omega$
	Common Mode								$\text{G}\Omega$

**ELECTRICAL CHARACTERISTICS** $V_S = 5V$ ,  $V_{CM} = 0V$ ,  $V_{OUT} = 1.4V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1006AM/AC			LT1006M/C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
	Input Voltage Range		3.5 0	3.8 -0.3		3.5 0	3.8 -0.3		V V
CMRR	Common Mode Rejection Ratio	$V_{CM} = 0V$ to $3.5V$	100	114		97	112		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$ , $V_0 = 0V$	106	126		103	124		dB
$A_{VOL}$	Large-Signal Voltage Gain	$V_0 = 0.03V$ to $4V$ , $R_L = 10k$ $V_0 = 0.03V$ to $3.5V$ , $R_L = 2k$	1.0 0.5	2.5 2.0		0.7 0.3	2.0 1.8		$V/\mu V$ $V/\mu V$
	Maximum Output Voltage Swing	Output Low, No Load Output Low, $600\Omega$ to GND Output Low, $I_{SINK} = 1mA$ Output High, No Load Output High, $600\Omega$ to GND		15 5 220 4.0 3.4	25 10 350 4.4 4.0		15 5 220 4.0 3.4	25 10 350 4.4 4.0	mV mV mV V V
SR	Slew Rate		0.25	0.4		0.25	0.4		$V/\mu s$
$I_S$	Supply Current	$R_{SET} = \infty$ $R_{SET} = 180k$ Pin 8 to Pin 7 (Note 3)		340 90	520		350 90	570	$\mu A$ $\mu A$
	Minimum Supply Voltage		2.7			2.7			V

The ● denotes the specifications which apply over the full operating temperature range.  $V_S = 5V$ ,  $0V$ ;  $V_{CM} = 0.1V$ ;  $V_0 = 1.4V$ ;  $-55^\circ C \leq T_A \leq 125^\circ C$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1006AM			LT1006M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage		●	40	180		60	250	$\mu V$
$\frac{\Delta V_{OS}}{\Delta Temp}$	Input Offset Voltage Drift		●	0.2	1.3		0.3	1.8	$\mu V/\circ C$
$I_{OS}$	Input Offset Current		●	0.4	2.0		0.5	4.0	nA
$I_B$	Input Bias Current		●	13	25		16	40	nA
$A_{VOL}$	Large-Signal Voltage Gain	$V_0 = 0.05V$ to $3.5V$ , $R_L = 2k$	●	0.25	0.8		0.15	0.7	$V/\mu V$
CMRR	Common Mode Rejection Ratio	$V_{CM} = 0.1V$ to $3.2V$	●	90	103		87	102	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$ , $V_0 = 0V$	●	100	117		97	116	dB
	Maximum Output Voltage Swing	Output Low, $600\Omega$ to GND Output High, $600\Omega$ to GND	● ●	6 3.2	15 3.8		6 3.1	18 3.8	mV V
$I_S$	Supply Current		●	380	630		400	680	$\mu A$

# LT1006

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range.  $V_S = 5V, 0V; V_{CM} = 0V; V_0 = 1.4V; 0^\circ C \leq T_A \leq 70^\circ C$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1006AC			LT1006C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage	J8/H Package N8 Package S8 Package	● ● ●	30	110	45 50 110	160 190 560	$\mu V$ $\mu V$ $\mu V$	
$\frac{\Delta V_{OS}}{\Delta T_{Temp}}$	Input Offset Voltage Drift	J8/H Package N8 Package S8 Package	● ● ●	0.2	1.3	0.3 0.5 0.7	1.8 2.5 3.5	$\mu V/^\circ C$ $\mu V/^\circ C$ $\mu V/^\circ C$	
$I_{OS}$	Input Offset Current		●	0.25	1.2	0.3	2.5	nA	
$I_B$	Input Bias Current		●	11	20	12	30	nA	
$A_{VOL}$	Large-Signal Voltage Gain	$V_0 = 0.04V$ to $3.5V$ , $R_L = 2k$	●	0.35	1.3	0.25	1.2	$V/\mu V$	
CMRR	Common Mode Rejection Ratio	$V_{CM} = 0V$ to $3.4V$	●	96	109	92	108	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$ , $V_0 = 0V$	●	101	120	97	118	dB	
	Maximum Output Voltage Swing	Output Low, $600\Omega$ to GND Output High, $600\Omega$ to GND	● ●	6 3.3	13 3.9	3.2	3.9	mV V	
$I_S$	Supply Current		●	350	570	360	620	$\mu A$	

$V_S = \pm 15V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1006AM/AC			LT1006M/C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage	LT1006S8		30	100	50 100	180 525	$\mu V$ $\mu V$	
$I_{OS}$	Input Offset Current			0.1	0.5	0.15	0.9	nA	
$I_B$	Input Bias Current			7.5	12.0	8	20	nA	
	Input Voltage Range		13.5 -15.0	13.8 -15.3		13.5 -15.0	13.8 -15.3		V V
CMRR	Common Mode Rejection Ratio	$V_{CM} = +13.5V, -15V$	100	117		97	116		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$ , $V_0 = 0V$	106	126		103	124		dB
$A_{VOL}$	Large Signal Voltage Gain	$V_0 = \pm 10V, R_L = 2k$ $V_0 = \pm 10V, R_L = 600\Omega$	1.5 0.8	5.0 1.5		1.2 0.5	4.0 1.0	$V/\mu V$ $V/\mu V$	
$V_{OUT}$	Maximum Output Voltage Swing	$R_L = 2k$	$\pm 13$	$\pm 14$		$\pm 12.5$	$\pm 14$		V
SR	Slew Rate	$R_{SET} = \infty$ $R_{SET} = 390\Omega$ Pin 8 to Pin 4	0.25 1.0	0.4 1.2		0.25 1.0	0.4 1.2		$V/\mu s$ $V/\mu s$
$I_S$	Supply Current			360	540	360	600	$\mu A$	

**ELECTRICAL CHARACTERISTICS**

The ● denotes the specifications which apply over the full operating temperature range.  $V_S = \pm 15V$ ,  $-55^\circ C \leq T_A \leq 125^\circ C$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1006AM			LT1006M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage		●	80	320	110	460	μV	
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Input Offset Voltage Drift		●	0.5	2.2	0.6	2.8	μV/°C	
$I_{OS}$	Input Offset Current		●	0.2	2.0	0.3	3.0	nA	
$I_B$	Input Bias Current		●	9	18	11	27	nA	
$A_{VOL}$	Large-Signal Voltage Gain	$V_0 = \pm 10V$ , $R_L = 2k$	●	0.5	1.5	0.25	1.0	V/μV	
CMRR	Common Mode Rejection Ratio	$V_{CM} = +13V$ , $-14.9V$	●	97	114	94	113	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$ , $V_0 = 0V$	●	100	117	97	116	dB	
	Maximum Output Voltage Swing	$R_L = 2k$	●	±12	±13.8	±11.5	±13.8	V	
$I_S$	Supply Current		●	400	650	400	750	μA	

The ● denotes the specifications which apply over the full operating temperature range.  $V_S = \pm 15V$ ,  $0^\circ C \leq T_A \leq 70^\circ C$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1006AC			LT1006C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage	J8/H Package N8 Package S8 Package	● ● ●	50	200	75	300	μV	
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Input Offset Voltage Drift	J8/H Package N8 Package S8 Package	● ● ●	0.5	2.2	0.6	2.8	μV/°C	
$I_{OS}$	Input Offset Current		●	0.15	1	0.25	2	nA	
$I_B$	Input Bias Current		●	8	15	10	23	nA	
$A_{VOL}$	Large-Signal Voltage Gain	$V_0 = \pm 10V$ , $R_L = 2k$	●	1	3	0.7	2.5	V/μV	
CMRR	Common Mode Rejection Ratio	$V_{CM} = 13V$ , $-15V$	●	98	116	94	114	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$ , $V_0 = 0V$	●	101	120	97	118	dB	
	Maximum Output Voltage Swing	$R_L = 2k$	●	±12.5	±13.9	±11.5	±13.8	V	
$I_S$	Supply Current		●	370	600	380	660	μA	

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

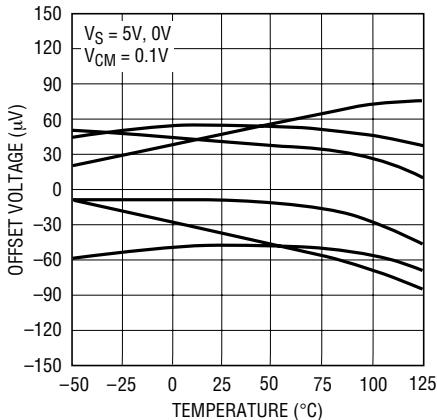
**Note 2:** This parameter is guaranteed by design and is not tested.

**Note 3:** Regular operation does not require an external resistor. In order to program the supply current for low power or high speed operation, connect an external resistor from Pin 8 to Pin 7 or from Pin 8 to Pin 4, respectively. Supply current specifications (for  $R_{SET} = 180k$ ) do not include current in  $R_{SET}$ .

**Note 4:** Optional offset nulling is accomplished with a potentiometer connected between the trim terminals and the wiper to  $V^-$ . A 10k pot (providing a null range of ±6mV) is recommended for minimum drift of nulled offset voltage with temperature. For increased trim resolution and accuracy, two fixed resistors can be used in conjunction with a smaller potentiometer. For example, two 4.7k resistors tied to Pins 1 and 5, with a 500Ω pot in the middle, will have a null range of ±150μV.

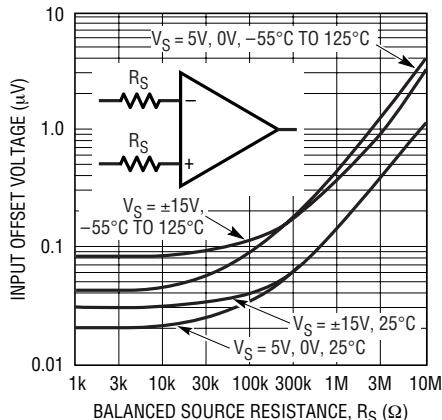
## TYPICAL PERFORMANCE CHARACTERISTICS

Offset Voltage Drift with Temperature of Representative Units

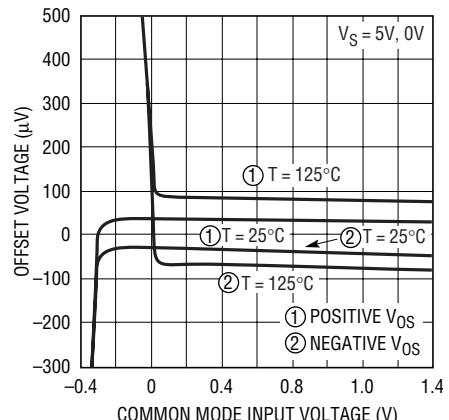


LT1006 • G02

Offset Voltage vs Balanced Source Resistor

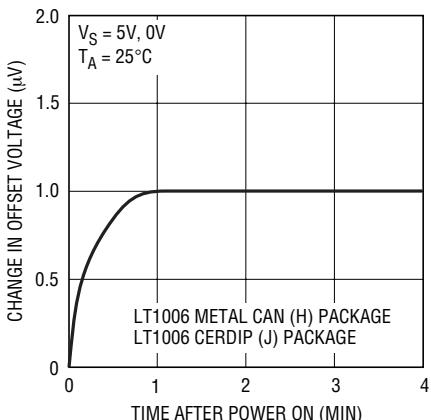


LT1006 • G03

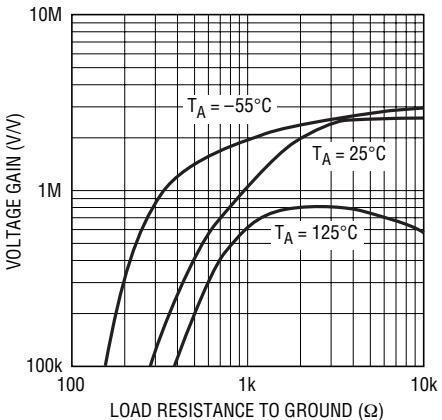
 $V_{OS}$  vs Common Mode Voltage vs Temperature

LT1006 • G04

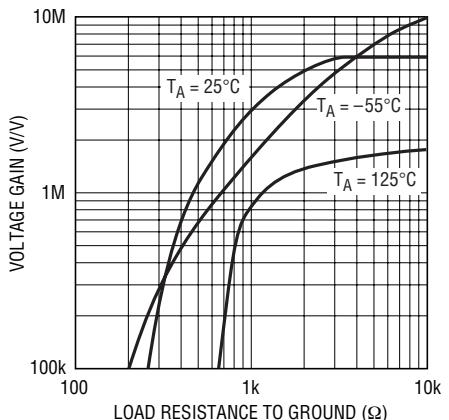
Warm-Up Drift



LT1006 • G05

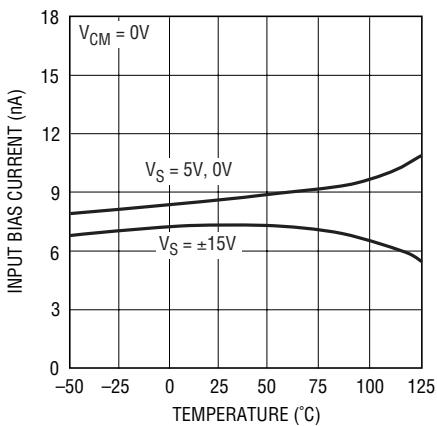
Voltage Gain vs Load Resistance,  $V_S = 5V, 0V$ 

LT1006 • G06

Voltage Gain vs Load Resistance with  $V_S = \pm 15V$ 

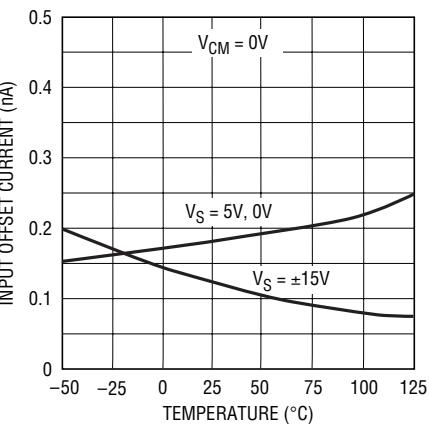
LT1006 • G07

Input Bias Current vs Temperature



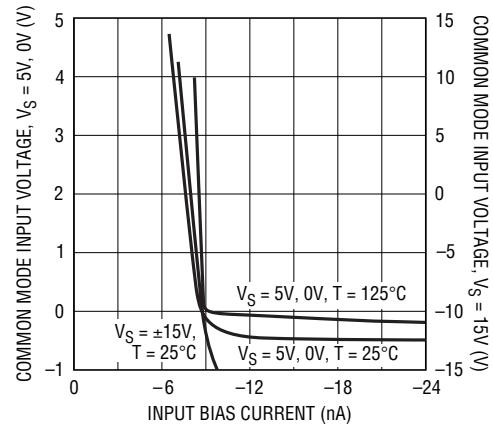
LT1006 • G08

Input Offset Current vs Temperature



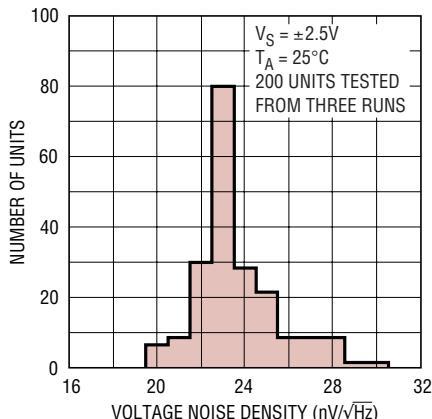
LT1006 • G09

Input Bias Current vs Common Mode Voltage

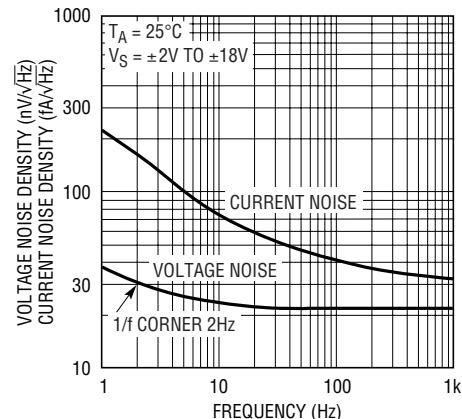


LT1006 • G10

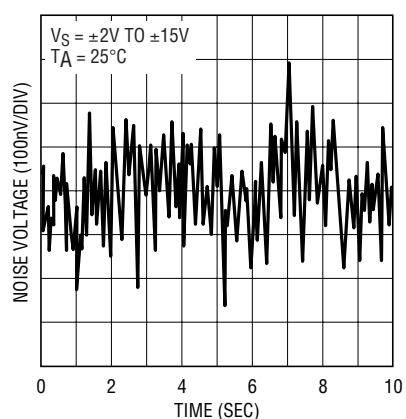
## TYPICAL PERFORMANCE CHARACTERISTICS

**10Hz Voltage Noise Distribution**


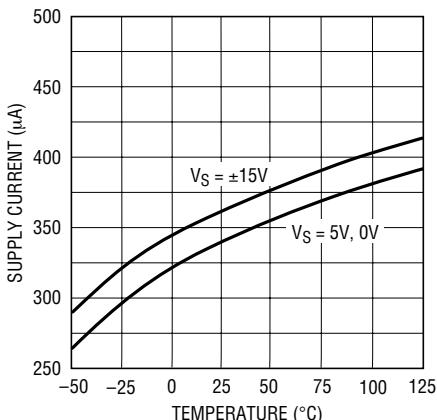
LT1006 • G11

**Noise Spectrum**


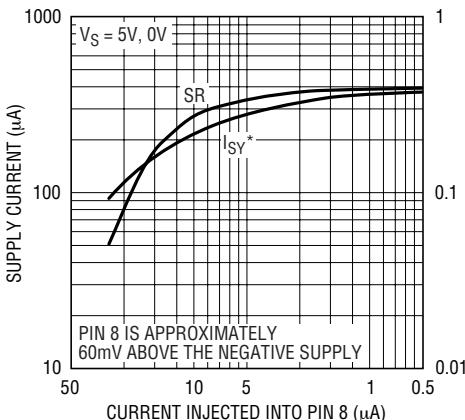
LT1006 • G12

**0.1Hz to 10Hz Noise**


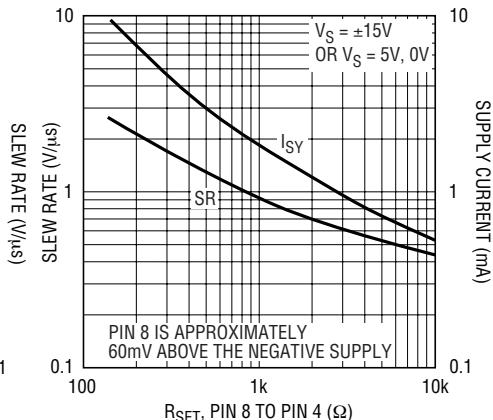
LT1006 • G13

**Supply Current vs Temperature**


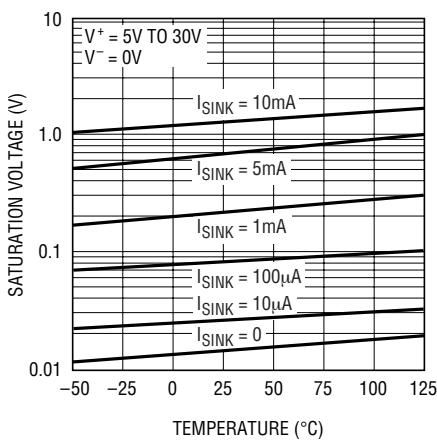
LT1006 • G14

**Reducing Power Dissipation**
\*ISY DOES NOT INCLUDE CURRENT THROUGH R<sub>SET</sub>

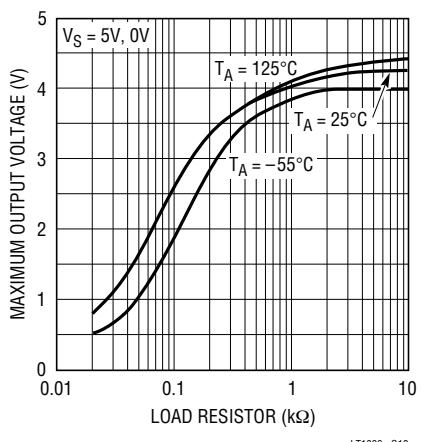
LT1006 • G15

**Increasing Slew Rate (R<sub>SET</sub> to V<sup>-</sup>)**


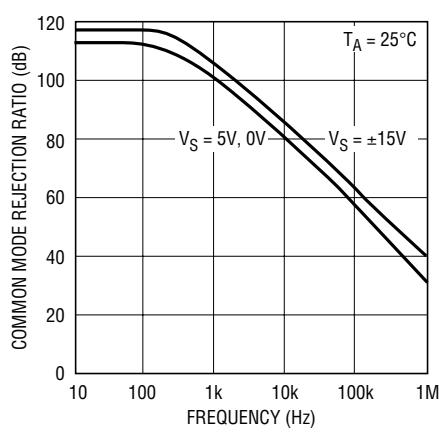
LT1006 • G16

**Output Saturation vs Sink Current vs Temperature**


LT1006 • G17

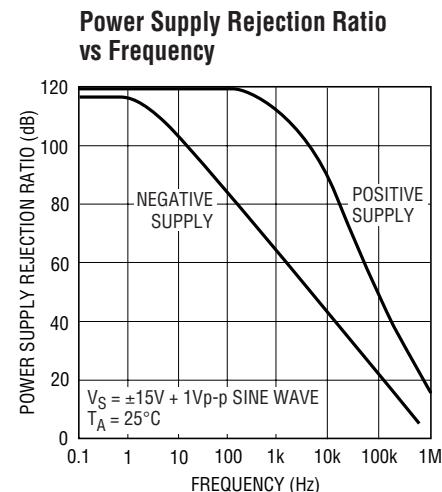
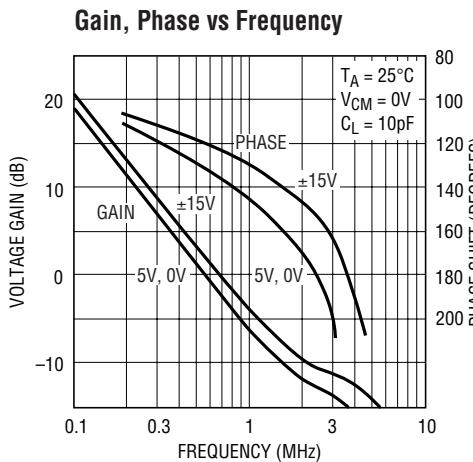
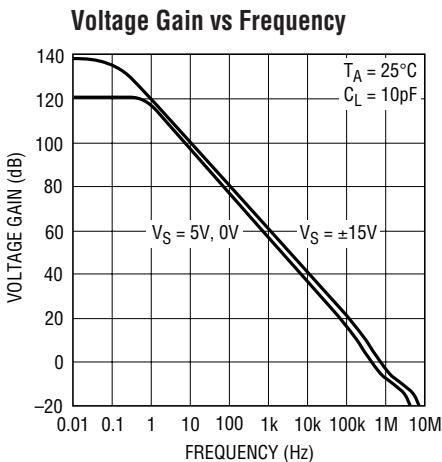
**Maximum Output Swing vs Load Resistor**


LT1006 • G18

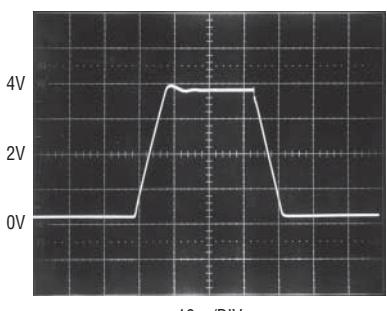
**Common Mode Rejection Ratio vs Frequency**


LT1006 • G19

## TYPICAL PERFORMANCE CHARACTERISTICS

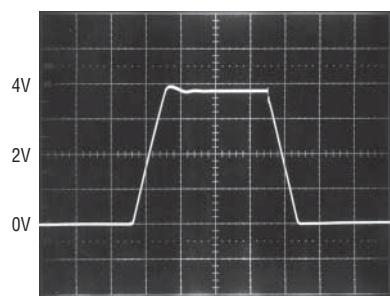


**Large Transient Response,  
 $V_S = 5V, 0V$**



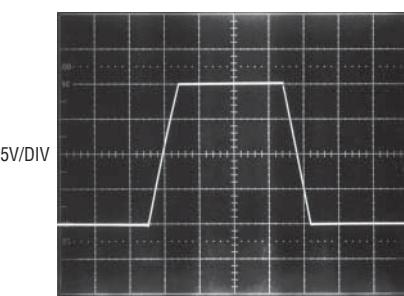
$A_V = 1$   
 $R_L = 4.7k$  TO  $5V$   
INPUT =  $0V$  TO  $3.8V$

**Large-Signal Transient Response,  
 $V_S = 5V, 0V$**



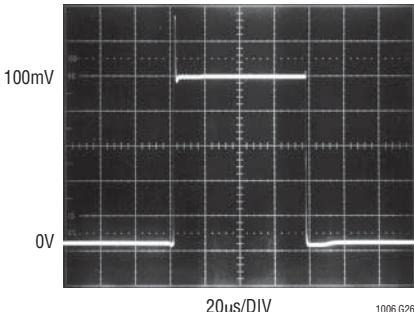
$A_V = 1$   
 $R_L = 4.7k$  TO GROUND  
INPUT =  $0V$  TO  $3.8V$

**Large-Signal Transient Response,  
 $V_S = \pm 15V$**



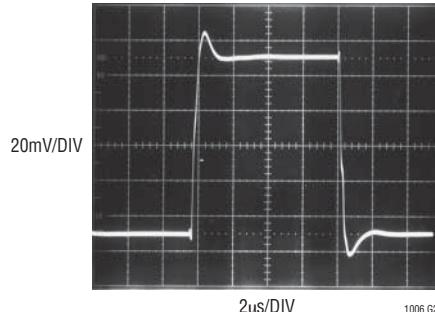
$A_V = 1$

**Small-Signal Transient Response,  
 $V_S = 5V, 0V$**



$A_V = 1$   
 $C_L = 10\text{pF}$   
 $R_L = 600\Omega$  TO GND  
INPUT =  $0V$  TO  $100\text{mV}$  PULSE

**Small-Signal Transient Response,  
 $V_{CC} = \pm 2.5V$  to  $\pm 15V$**



$A_V = 1$   
 $C_L = 10\text{pF}$

## APPLICATIONS INFORMATION

The LT1006 is fully specified for single supply operation, (i.e., when the negative supply is 0V). Input common mode range includes ground; the output swings within a few millivolts of ground. Single supply operation, however, can create special difficulties, both at the input and at the output. The LT1006 has specific circuitry which addresses these problems.

At the input, the driving signal can fall below 0V— inadvertently or on a transient basis. If the input is more than a few hundred millivolts below ground, two distinct problems can occur on previous single supply designs, such as the LM124, LM158, OP-20, OP-21, OP-220, OP-221, OP-420:

- a) When the input is more than a diode drop below ground, unlimited current will flow from the substrate ( $V^-$  terminal) to the input. This can destroy the unit. On the LT1006, the  $400\Omega$  resistors, in series with the input (see Schematic Diagram), protect the devices even when the input is 5V below ground.
- b) When the input is more than 400mV below ground (at  $25^\circ\text{C}$ ), the input stage saturates (transistors Q3 and

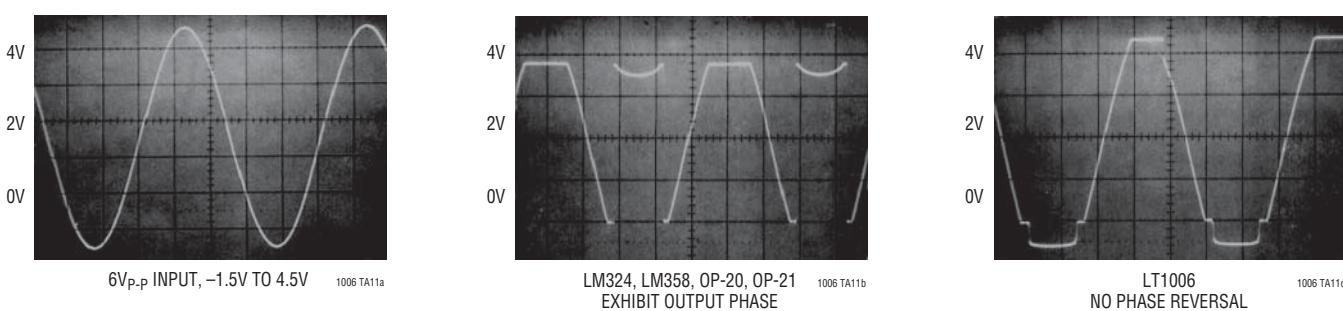
Q4) and phase reversal occurs at the output. This can cause lock-up in servo systems. Due to a unique phase reversal protection circuitry (Q21, Q22, Q27, Q28), the LT1006's output does not reverse, as illustrated below, even when the inputs are at  $-1.5\text{V}$ .

At the output, the aforementioned single supply designs either cannot swing to within 600mV of ground (OP-20) or cannot sink more than a few microamperes while swinging to ground (LM124, LM158). The LT1006's all-NPN output stage maintains its low output resistance and high gain characteristics until the output is saturated.

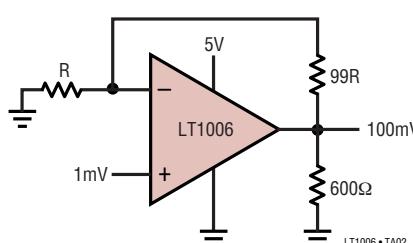
In dual supply operations, the output stage is crossover distortion free.

Since the output cannot go exactly to ground, but can only approach ground to within a few millivolts, care should be exercised to ensure that the output is not saturated. For example, a 1mV input signal will cause the amplifier to set up in its linear region in the gain 100 configuration shown below, but is not enough to make the amplifier function properly in the voltage follower mode.

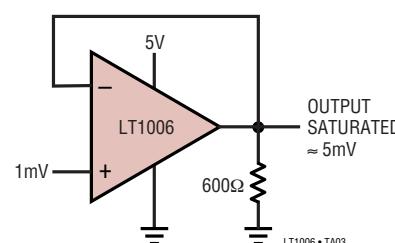
**Voltage Follower with Input Exceeding the Negative Common Mode Range ( $V_S = 5\text{V}$ , 0V)**



**Gain 100 Amplifier**



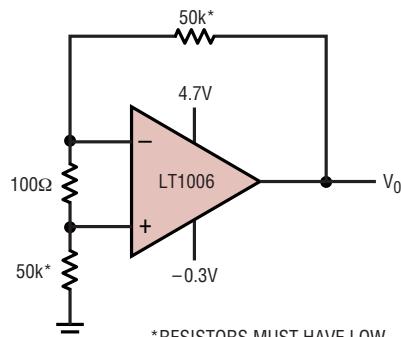
**Voltage Follower**



## APPLICATIONS INFORMATION

In automated production testing the output is forced to 1.4V by the test loop; offset voltage is measured with a common mode voltage of zero and the negative supply at zero (Pin 4). Without the test loop, these exact conditions cannot be achieved. The test circuit shown ensures that the output will never saturate even with worst-case offset voltages ( $-250\mu\text{V}$  over the  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  range). The effective common mode input is 0.3V with respect to the negative supply. As indicated by the common mode rejection specifications the difference is only a few microvolts between the two methods of offset voltage measurement.

**Test Circuit for Offset Voltage and Offset Drift with Temperature**



\*RESISTORS MUST HAVE LOW THERMOELECTRIC POTENTIAL.

\*\*THIS CIRCUIT IS ALSO USED AS THE BURN-IN CONFIGURATION, WITH SUPPLY VOLTAGES INCREASED TO  $\pm 20\text{V}$

$V_0 = 1000V_{OS}$

LT1006 • TA04

### Low Supply Operation

The minimum guaranteed supply voltage for proper operation of the LT1006 is 2.7V. Typical supply current at this voltage is  $320\mu\text{A}$ ; therefore, power dissipation is only  $860\mu\text{W}$ .

### Noise Testing

For application information on noise testing and calculations, please see the LT1007 or LT1028 data sheet.

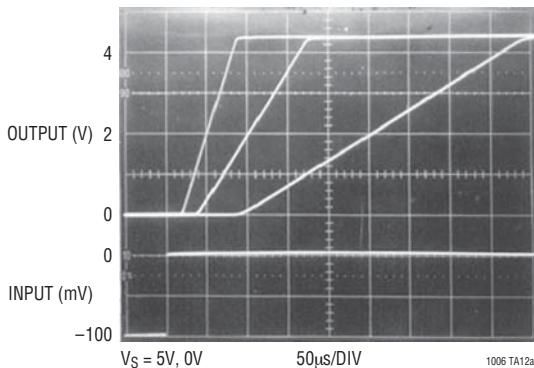
### Supply Current Programming

Connecting an optional external resistor to Pin 8 changes the biasing of the LT1006 in order to increase its speed or to decrease its power consumption. If a higher slew rate is required, connect the external resistor for Pin 8 to Pin 4 [see performance curves for Increasing Slew Rate ( $R_{SET}$  to  $V^-$ )]. For lower power consumption, inject a current into Pin 8 (which is approximately 60mV above  $V^-$ ) as shown on the Reducing Power Dissipation plot. This can be accomplished by connecting  $R_{SET}$  to the positive supply, or to save additional power, by obtaining the injected current from a low voltage battery.

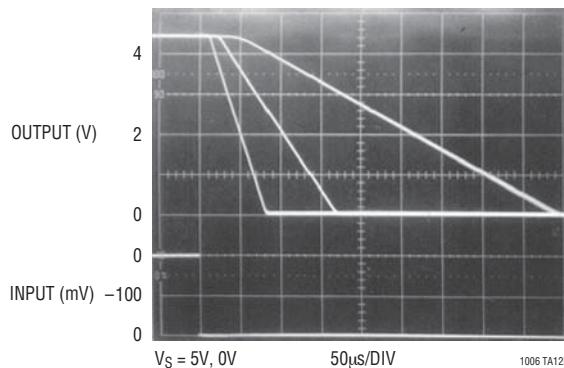
### Comparator Applications

The single supply operation of the LT1006 and its ability to swing close to ground while sinking current lends itself to use as a precision comparator with TTL compatible output.

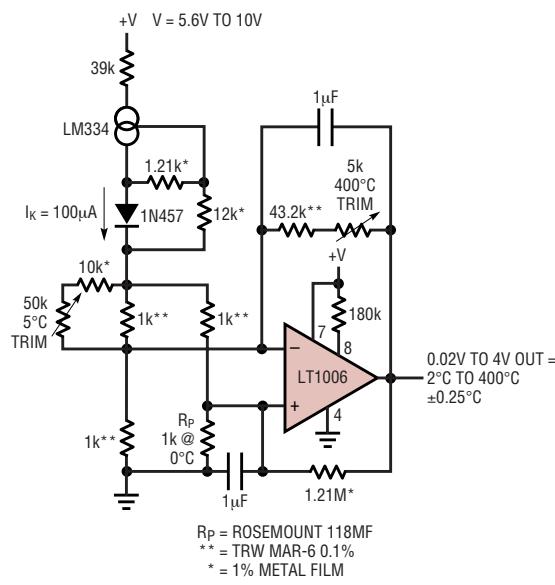
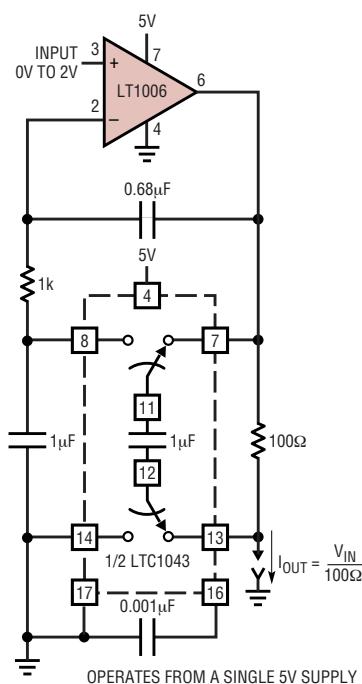
**Comparator Rise Response Time to 10mV, 5mV, 2mV Overdrives**



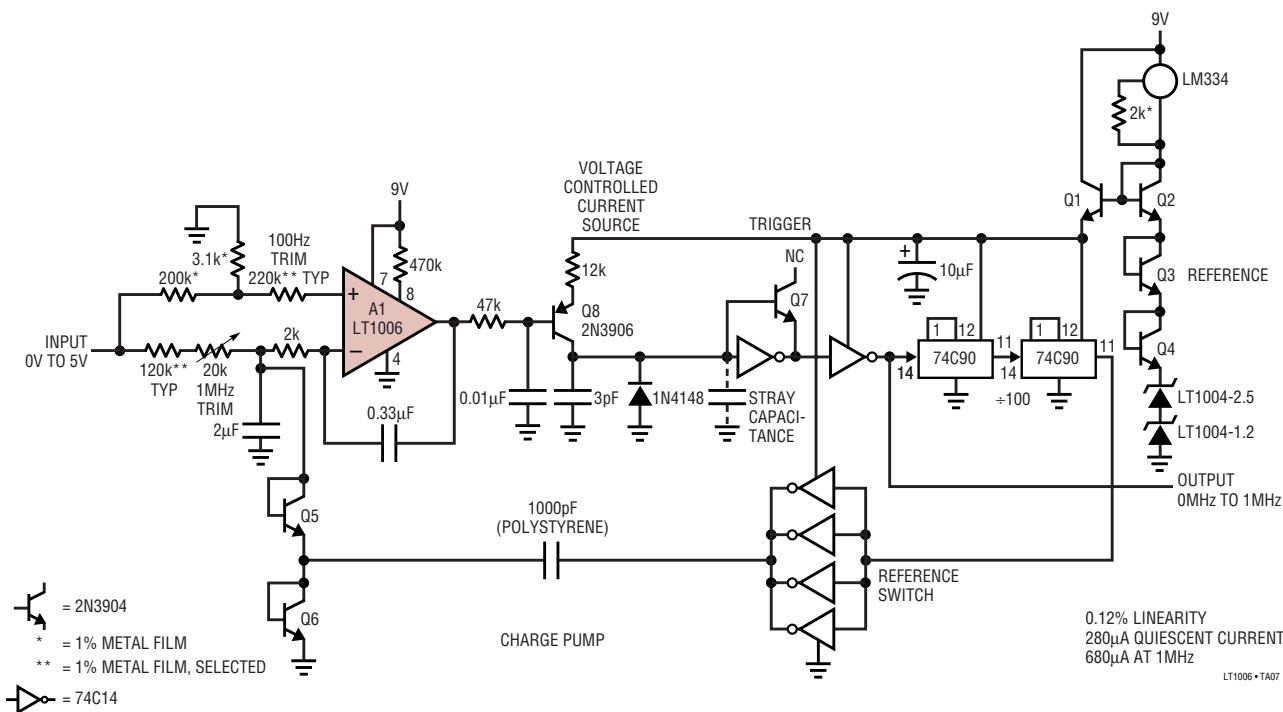
**Comparator Fall Response Time to 10mV, 5mV, 2mV Overdrives**



## TYPICAL APPLICATIONS

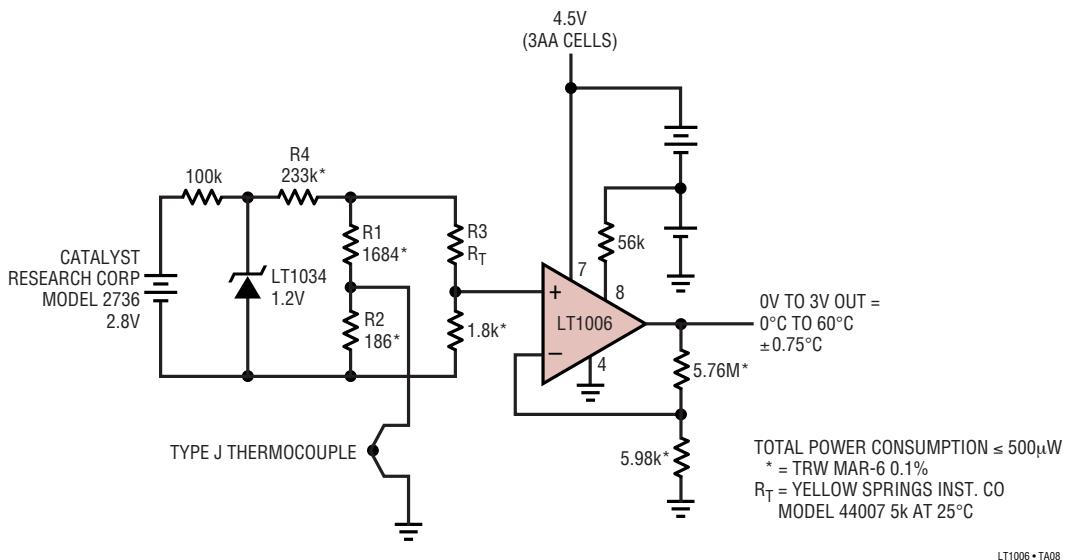
Platinum RTD Signal Conditioner  
with Curvature CorrectionVoltage Controlled Current Source  
with Ground Referred Input and Output

Micropower 1MHz V/F Converter



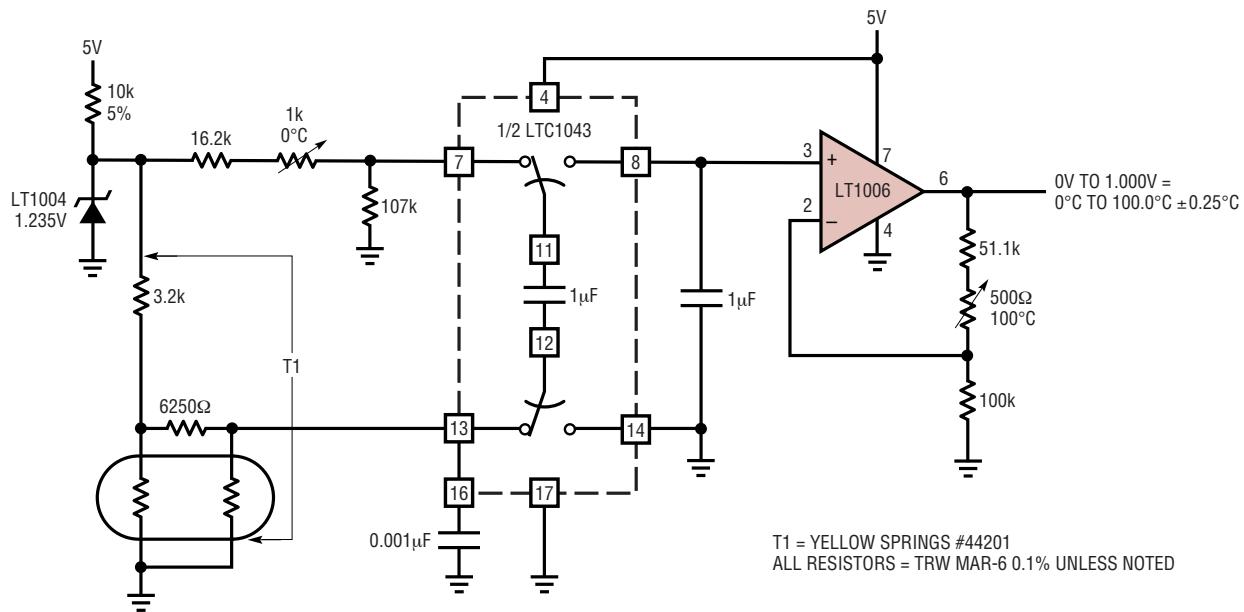
## TYPICAL APPLICATIONS

### Micropower Thermocouple Signal Conditioner with Cold Junction Compensation



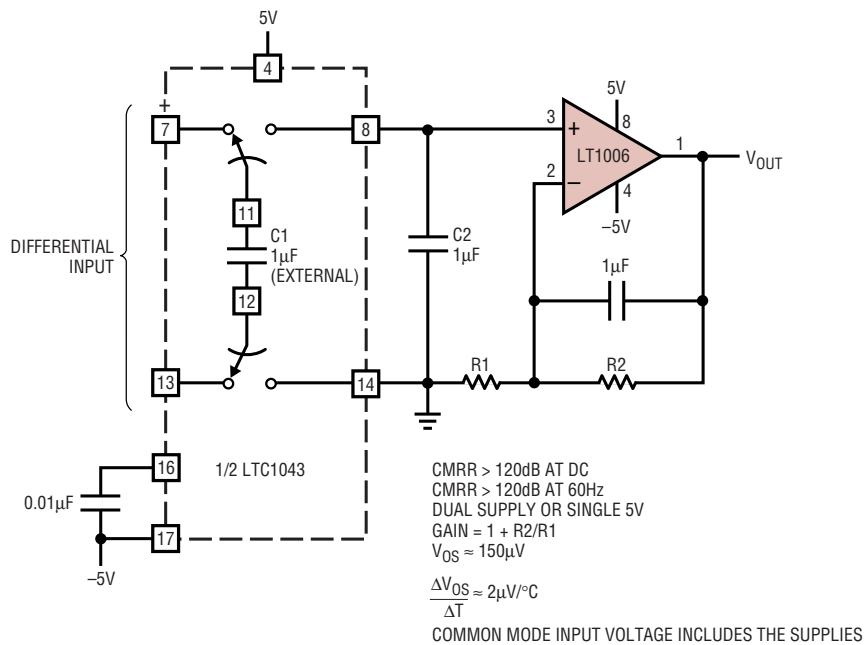
LT1006 • TA08

### Linear Thermometer

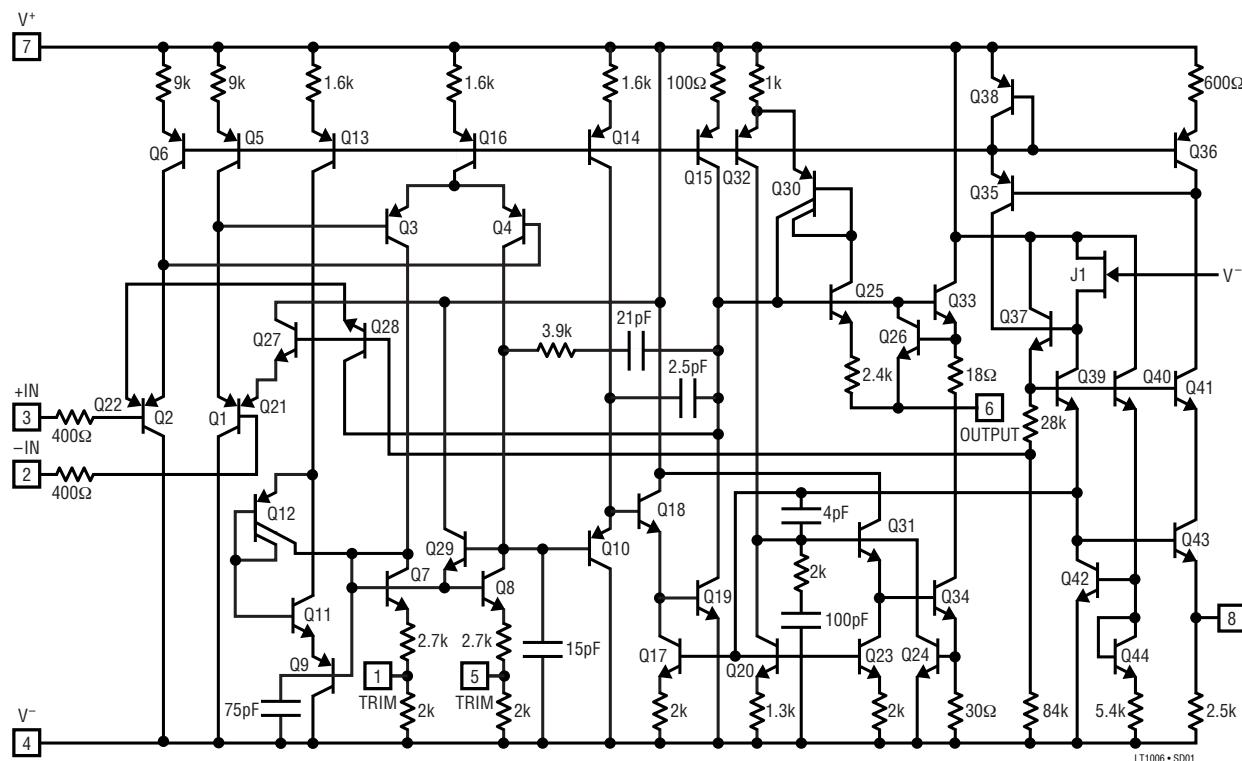


LT1006 • TA09

## TYPICAL APPLICATIONS

**±5V Precision Instrumentation Amplifier**

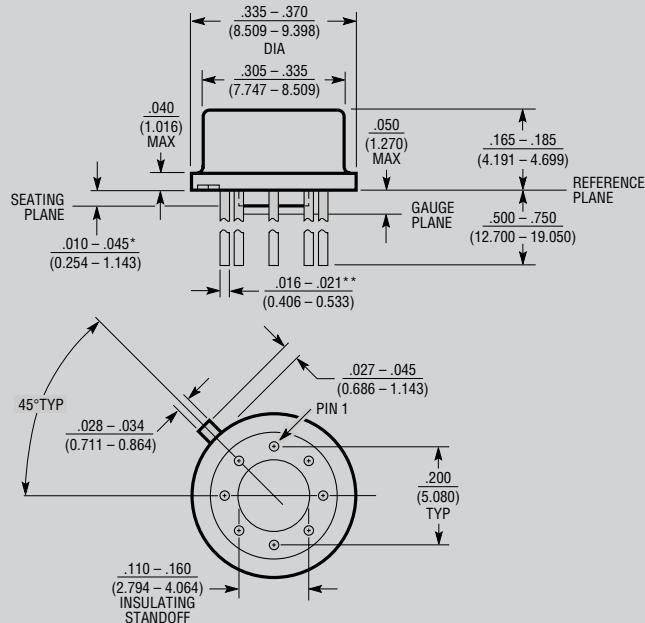
## SCHEMATIC DIAGRAM



1006fa

## PACKAGE DESCRIPTION

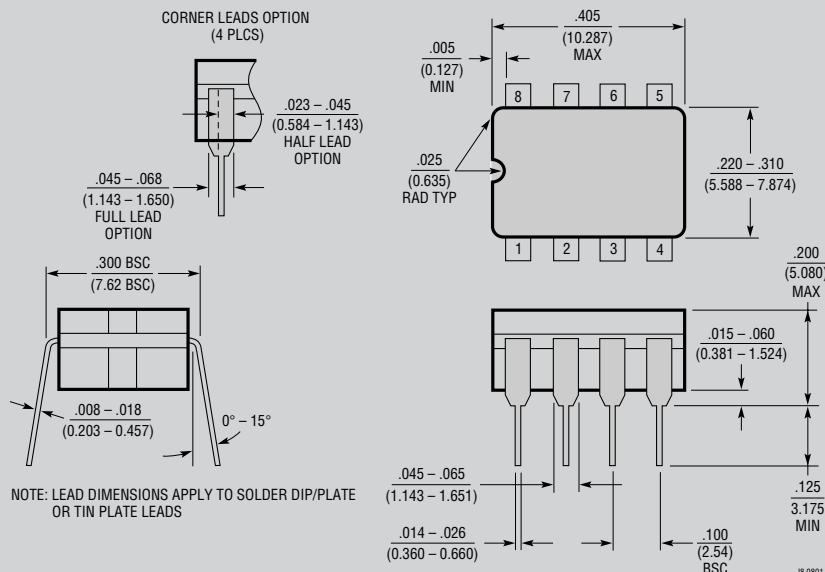
**H Package**  
**8-Lead TO-5 Metal Can (.200 Inch PCD)**  
(Reference LTC DWG # 05-08-1320)



\*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND THE SEATING PLANE

\*\*FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS  $\frac{.016 - .024}{(.406 - 0.610)}$  H8(TO-5) 0.200 PCD 0801

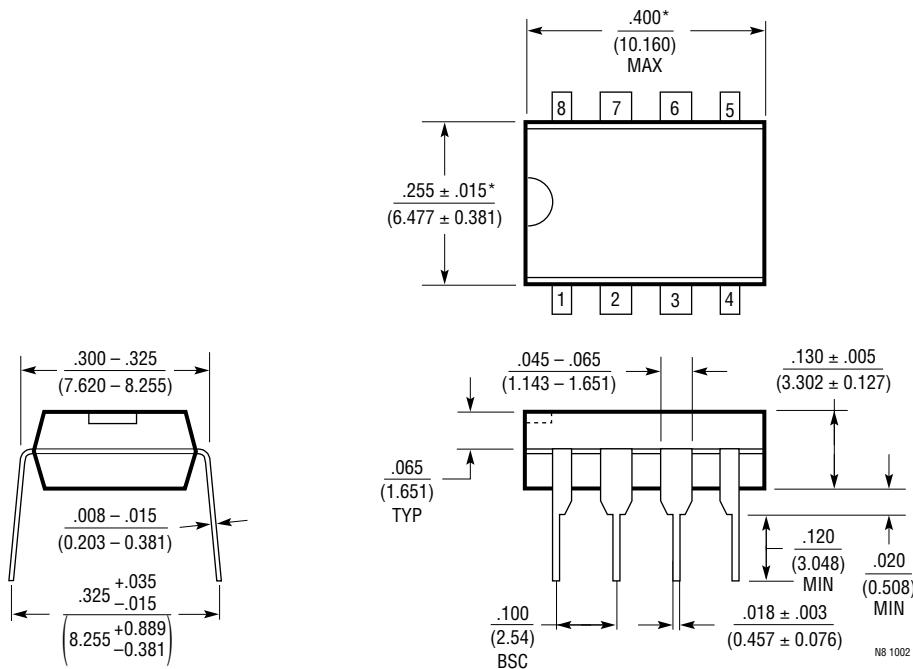
**J8 Package**  
**8-Lead CERDIP (Narrow .300 Inch, Hermetic)**  
(Reference LTC DWG # 05-08-1110)



## OBSOLETE PACKAGES

## PACKAGE DESCRIPTION

**N8 Package**  
**8-Lead PDIP (Narrow .300 Inch)**  
(Reference LTC DWG # 05-08-1510)

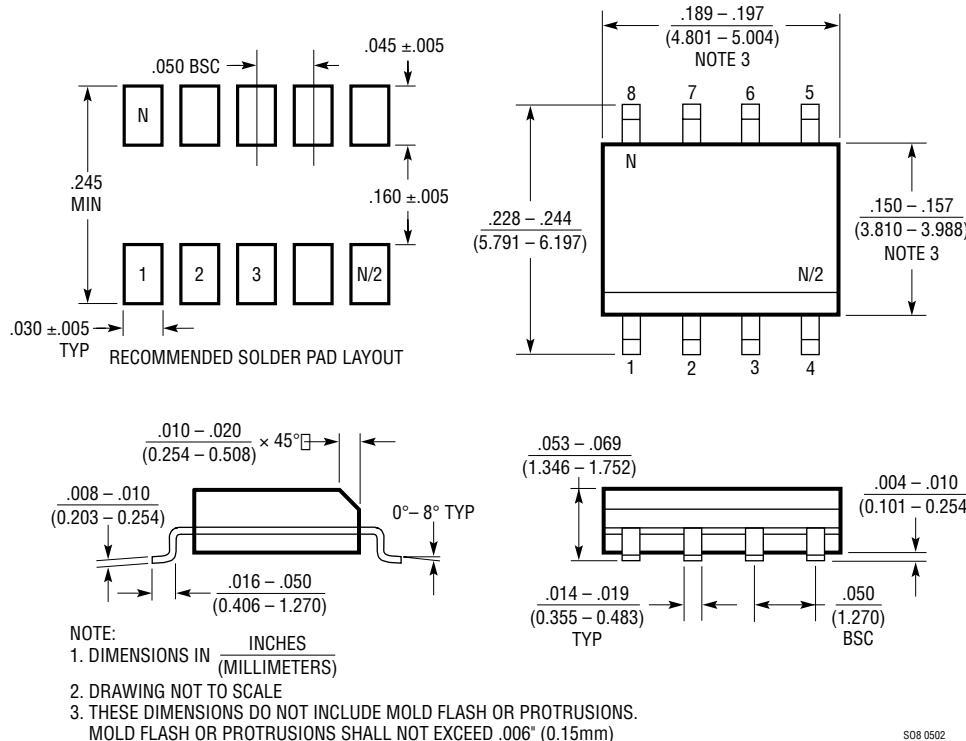


NOTE:

1. DIMENSIONS ARE INCHES  
MILLIMETERS\*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

## PACKAGE DESCRIPTION

**S8 Package**  
**8-Lead Plastic Small Outline (Narrow .150 Inch)**  
(Reference LTC DWG # 05-08-1610)





44 FARRAND STREET  
BLOOMFIELD, NJ 07003  
(973) 748-5089

## NTE957

### Integrated Circuit

### 3-Terminal Adjustable Negative

### Voltage Regulator

#### **Description:**

The NTE957 is an adjustable 3-terminal negative voltage regulator in a TO220 type package capable of supplying in excess of  $-1.5\text{A}$  over a  $-1.2\text{V}$  to  $-37\text{V}$  output range. The circuit design has been optimized for excellent regulation and low thermal transients. Further, the NTE957 features internal current limiting, thermal shutdown, and safe-area compensation, making this device virtually blowout-proof against overloads.

The NTE957 serves a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The NTE957 is the ideal complement to the NTE956 adjustable positive regulator.

#### **Features:**

- Output Voltage Adjustable from  $-1.2\text{V}$  to  $-37\text{V}$
- Guaranteed  $1.5\text{A}$  Output Current
- Line Regulation Typically  $0.01\%/\text{V}$
- Load Regulation Typically  $0.3\%$
- Excellent Thermal Regulation:  $0.002\%/\text{W}$
- $77\text{dB}$  Ripple Rejection
- Temperature-Independent Current Limit
- Internal Thermal Overload Protection
- $100\%$  Electrical Burn-In
- Eliminates the Need to Stock Many Voltages

#### **Absolute Maximum Ratings:**

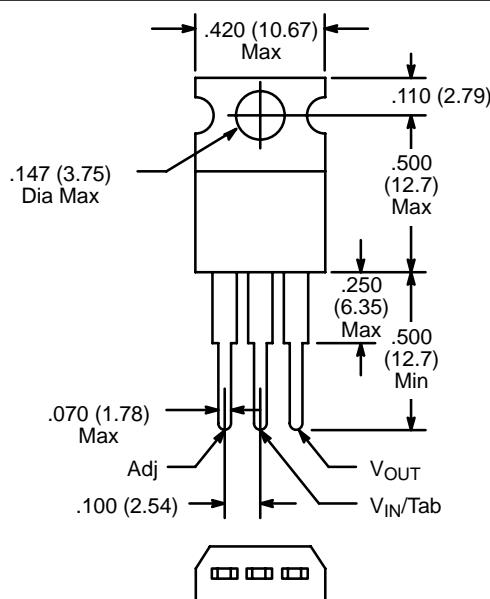
Power Dissipation, $P_D$ .....	Internally Limited
Input-Output Voltage Differential, $V_I - V_O$ .....	$40\text{V}$
Operating Junction Temperature Range, $T_J$ .....	$0^\circ \text{ to } +125^\circ\text{C}$
Storage Temperature Range, $T_{stg}$ .....	$-65^\circ \text{ to } +150^\circ\text{C}$
Typical Thermal Resistance, Junction-to-Case, $R_{thJC}$ .....	$4^\circ\text{C}/\text{W}$
Lead Temperature (During Soldering, 10sec), $T_L$ .....	$+300^\circ\text{C}$

**Electrical Characteristics:** ( $0^\circ \leq T_J \leq +125^\circ\text{C}$ ,  $V_{IN} - V_{OUT} = 5\text{V}$ ,  $I_O = 500\text{mA}$ ,  $I_{MAX} = 1.5\text{A}$ , Note 1 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Line Regulation	Reg <sub>line</sub>	$T_A = +25^\circ\text{C}$ , $3\text{V} \leq (V_{IN} - V_{OUT}) \leq 40\text{V}$ , Note 2	—	0.01	0.04	%/V	
		$3\text{V} \leq (V_{IN} - V_{OUT}) \leq 40\text{V}$	—	0.02	0.07	%/V	
Load Regulation	Reg <sub>load</sub>	$T_A = +25^\circ\text{C}$ , $10\text{mA} \leq I_O \leq I_{MAX}$ , Note 2	$V_{OUT} \leq 5\text{V}$	—	15	50	mV
			$V_{OUT} \geq 5\text{V}$	—	0.3	1.0	%
		$10\text{mA} \leq I_O \leq 1_{MAX}$ , Note 2	$V_{OUT} \leq 5\text{V}$	—	20	70	mV
			$V_{OUT} \geq 5\text{V}$	—	0.3	1.5	%
Thermal Regulation		$T_A = +25^\circ\text{C}$ , 20ms Pulse	—	0.003	0.04	%/W	
Adjustment Pin Current	$I_{Adj}$		—	65	100	$\mu\text{A}$	
Adjustment Pin Current Change	$\Delta I_{Adj}$	$10\text{mA} \leq I_L \leq I_{MAX}$ , $2.5\text{V} \leq (V_{IN} - V_{OUT}) \leq 40\text{V}$ , $T_A = +25^\circ\text{C}$	—	2	5	$\mu\text{A}$	
Reference Voltage	$V_{ref}$	$T_A = +25^\circ\text{C}$	—1.213	—1.250	—1.287	V	
		$3\text{V} \leq (V_{IN} - V_{OUT}) \leq 40\text{V}$ , $10\text{mA} \leq I_O \leq 1_{MAX}$ , $P \leq P_{MAX}$	—1.200	—1.250	—1.300	V	
Temperature Stability	$T_S$	$0^\circ \leq T_J \leq +125^\circ\text{C}$	—	0.6	—	%	
Minimum Load Current	$I_{Lmin}$	$(V_{IN} - V_{OUT}) \leq 40\text{V}$	—	2.5	10	mA	
		$(V_{IN} - V_{OUT}) \leq 10\text{V}$	—	1.5	6.0	mA	
Maximum Output Current Limit	$I_{max}$	$V_{IN} - V_{OUT} \leq 15\text{V}$	1.5	2.2	—	A	
		$V_{IN} - V_{OUT} = 40\text{V}$	—	0.4	—	A	
RMS Output Noise, % of $V_{OUT}$	N	$T_A = +25^\circ\text{C}$ , $10\text{Hz} \leq f \leq 10\text{kHz}$	—	0.003	—	%	
Ripple Rejection Ratio	RR	$V_{OUT} = 10\text{V}$ , $f = 120\text{Hz}$	—	60	—	dB	
			$C_{ADJ} = 10\mu\text{F}$	66	77	—	dB
Long Term Stability	S	$T_A = +125^\circ\text{C}$ , 1000 Hours	—	0.3	1.0	%	

Note 1. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 20W.

Note 2. Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.



**MICROCHIP****MCP4725**

## 12-Bit Digital-to-Analog Converter with EEPROM Memory in SOT-23-6

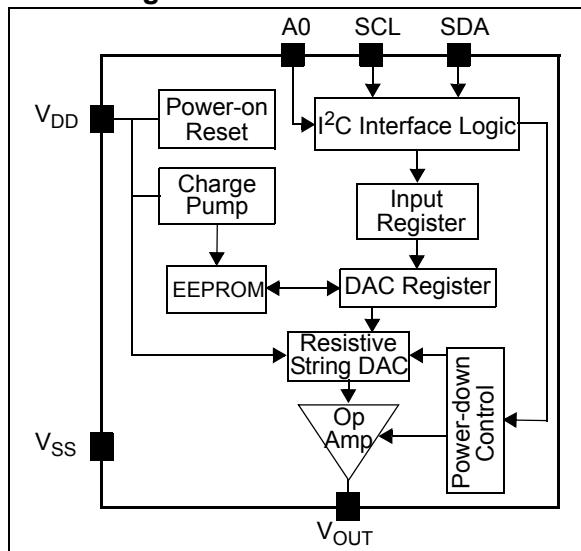
### Features

- 12-Bit Resolution
- On-Board Non-Volatile Memory (EEPROM)
- $\pm 0.2$  LSB DNL (typical)
- External A0 Address Pin
- Normal or Power-Down Mode
- Fast Settling Time: 6  $\mu$ s (typical)
- External Voltage Reference ( $V_{DD}$ )
- Rail-to-Rail Output
- Low Power Consumption
- Single-Supply Operation: 2.7V to 5.5V
- I<sup>2</sup>C™ Interface:
  - Eight Available Addresses
  - Standard (100 kbps), Fast (400 kbps), and High-Speed (3.4 Mbps) Modes
- Small 6-lead SOT-23 Package
- Extended Temperature Range: -40°C to +125°C

### Applications

- Set Point or Offset Trimming
- Sensor Calibration
- Closed-Loop Servo Control
- Low Power Portable Instrumentation
- PC Peripherals
- Data Acquisition Systems

### Block Diagram



### DESCRIPTION

The MCP4725 is a low-power, high accuracy, single channel, 12-bit buffered voltage output Digital-to-Analog Convertor (DAC) with non-volatile memory (EEPROM). Its on-board precision output amplifier allows it to achieve rail-to-rail analog output swing.

The DAC input and configuration data can be programmed to the non-volatile memory (EEPROM) by the user using I<sup>2</sup>C interface command. The non-volatile memory feature enables the DAC device to hold the DAC input code during power-off time, and the DAC output is available immediately after power-up. This feature is very useful when the DAC device is used as a supporting device for other devices in the network.

The device includes a Power-On-Reset (POR) circuit to ensure reliable power-up and an on-board charge pump for the EEPROM programming voltage. The DAC reference is driven from  $V_{DD}$  directly. In power-down mode, the output amplifier can be configured to present a known low, medium, or high resistance output load.

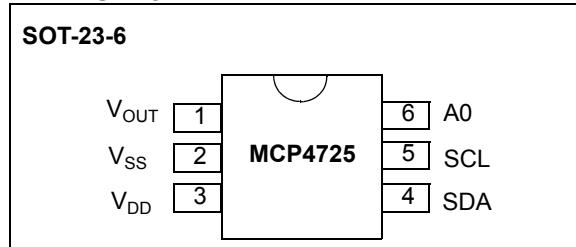
The MCP4725 has an external A0 address bit selection pin. This A0 pin can be tied to  $V_{DD}$  or  $V_{SS}$  of the user's application board.

The MCP4725 has a two-wire I<sup>2</sup>C™ compatible serial interface for standard (100 kHz), fast (400 kHz), or high speed (3.4 MHz) mode.

The MCP4725 is an ideal DAC device where design simplicity and small footprint is desired, and for applications requiring the DAC device settings to be saved during power-off time.

The device is available in a small 6-pin SOT-23 package.

### Package Type



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

$V_{DD}$	.....	6.5V
All inputs and outputs w.r.t $V_{SS}$	.....	-0.3V to $V_{DD}+0.3V$
Current at Input Pins	.....	$\pm 2$ mA
Current at Supply Pins	.....	$\pm 50$ mA
Current at Output Pins	.....	$\pm 25$ mA
Storage Temperature	.....	-65°C to +150°C
Ambient Temp. with Power Applied	.....	-55°C to +125°C
ESD protection on all pins	.....	$\geq 6$ kV HBM, $\geq 400$ V MM
Maximum Junction Temperature ( $T_J$ )	.....	+150°C

† Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability

### ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated, all parameters apply at  $V_{DD} = + 2.7V$  to 5.5V,  $V_{SS} = 0V$ ,  $R_L = 5$  kΩ from  $V_{OUT}$  to  $V_{SS}$ ,  $C_L = 100$  pF,  $T_A = -40^\circ C$  to  $+125^\circ C$ . Typical values are at  $+25^\circ C$ .

Parameter	Sym	Min	Typ	Max	Units	Conditions
<b>Power Requirements</b>						
Operating Voltage	$V_{DD}$	2.7		5.5	V	
Supply Current	$I_{DD}$	—	210	400	µA	Digital input pins are grounded, Output pin ( $V_{OUT}$ ) is not connected (unloaded), Code = 000h
Power-Down Current	$I_{DDP}$	—	0.06	2.0	µA	$V_{DD} = 5.5V$
Power-On-Reset Threshold Voltage	$V_{POR}$	—	2	—	V	
<b>DC Accuracy</b>						
Resolution	n	12	—	—	Bits	Code Range = 000h to FFFh
INL Error	INL	—	$\pm 2$	$\pm 14.5$	LSB	<b>Note 1</b>
DNL	DNL	-0.75	$\pm 0.2$	$\pm 0.75$	LSB	<b>Note 1</b>
Offset Error	$V_{OS}$		0.02	0.75	% of FSR	Code = 000h
Offset Error Drift	$\Delta V_{OS}/^\circ C$	—	$\pm 1$	—	ppm/°C	-45°C to +25°C
		—	$\pm 2$	—	ppm/°C	+25°C to +85°C
Gain Error	$G_E$	-2	-0.1	2	% of FSR	Code = FFFh, Offset error is not included.
Gain Error Drift	$\Delta G_E/^\circ C$	—	-3	—	ppm/°C	
<b>Output Amplifier</b>						
Phase Margin	$p_M$	—	66	—	Degree(°)	$C_L = 400$ pF, $R_L = \infty$
Capacitive Load Stability	$C_L$	—	—	1000	pF	$R_L = 5$ kΩ, <b>Note 2</b>
Slew Rate	SR	—	0.55	—	V/µs	
Short Circuit Current	$I_{SC}$	—	15	24	mA	$V_{DD} = 5V$ , $V_{OUT}$ = Grounded
Output Voltage Settling Time	$T_S$	—	6	—	µs	<b>Note 3</b>

**Note 1:** Test Code Range: 100 to 4000.

**2:** This parameter is ensure by design and not 100% tested.

**3:** Within 1/2 LSB of the final value when code changes from 1/4 to 3/4 (400h to C00h) of full scale range.

**4:** Logic state of external address selection pin (A0 pin).

# MCP4725

## ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical Specifications:** Unless otherwise indicated, all parameters apply at  $V_{DD} = +2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $R_L = 5\text{ k}\Omega$  from  $V_{OUT}$  to  $V_{SS}$ ,  $C_L = 100\text{ pF}$ ,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ . Typical values are at  $+25^\circ\text{C}$ .

Parameter	Sym	Min	Typ	Max	Units	Conditions
Power Up Time	$T_{PU}$	—	2.5	—	$\mu\text{s}$	$V_{DD} = 5V$
		—	5	—	$\mu\text{s}$	$V_{DD} = 3V$ Exit Power-down Mode, (Started from falling edge of ACK pulse)
DC Output Impedance	$R_{OUT}$	—	1	—	$\Omega$	Normal mode ( $V_{OUT}$ to $V_{SS}$ )
		—	1	—	$\text{k}\Omega$	Power-Down Mode 1 ( $V_{OUT}$ to $V_{SS}$ )
		—	100	—	$\text{k}\Omega$	Power-Down Mode 2 ( $V_{OUT}$ to $V_{SS}$ )
		—	500	—	$\text{k}\Omega$	Power-Down Mode 3 ( $V_{OUT}$ to $V_{SS}$ )
Supply Voltage Power-up Ramp Rate for EEPROM loading	$V_{DD\_RAMP}$	1	—	—	$\text{V/ms}$	Validation only.
<b>Dynamic Performance</b>						
Major Code Transition Glitch		—	45	—	$\text{nV-s}$	1 LSB change around major carry (from 800h to 7FFh) <b>(Note 2)</b>
Digital Feedthrough		—	<10	—	$\text{nV-s}$	<b>Note 2</b>
<b>Digital Interface</b>						
Output Low Voltage	$V_{OL}$	—	—	0.4	$\text{V}$	$I_{OL} = 3\text{ mA}$
Input High Voltage (SDA and SCL Pins)	$V_{IH}$	$0.7V_{DD}$	—	—	$\text{V}$	
Input Low Voltage (SDA and SCL Pins)	$V_{IL}$	—	—	$0.3V_{DD}$	$\text{V}$	
Input High Voltage (A0 Pin)	$V_{A0-HI}$	$0.8V_{DD}$	—	—		<b>Note 4</b>
Input Low Voltage (A0 Pin)	$V_{A0-IL}$	—	—	$0.2V_{DD}$		<b>Note 4</b>
Input Leakage	$I_{LI}$	—	—	$\pm 1$	$\mu\text{A}$	$SCL = SDA = A0 = V_{SS}$ or $SCL = SDA = A0 = V_{DD}$
Pin Capacitance	$C_{PIN}$	—	—	3	$\text{pF}$	<b>Note 2</b>
<b>EEPROM</b>						
EEPROM Write Time	$T_{WRITE}$	—	25	50	ms	
Data Retention		—	200	—	Years	At $+25^\circ\text{C}$ , <b>(Note 2)</b>
Endurance		1	—	—	Million Cycles	At $+25^\circ\text{C}$ , <b>(Note 2)</b>

**Note 1:** Test Code Range: 100 to 4000.

**2:** This parameter is ensure by design and not 100% tested.

**3:** Within 1/2 LSB of the final value when code changes from 1/4 to 3/4 (400h to C00h) of full scale range.

**4:** Logic state of external address selection pin (A0 pin).

## TEMPERATURE CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated,  $V_{DD} = +2.7V$  to  $+5.5V$ ,  $V_{SS} = GND$ .

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Temperature Ranges</b>						
Specified Temperature Range	$T_A$	-40	—	+125	°C	
Operating Temperature Range	$T_A$	-40	—	+125	°C	
Storage Temperature Range	$T_A$	-65	—	+150	°C	
<b>Thermal Package Resistances</b>						
Thermal Resistance, 6L-SOT-23	$\theta_{JA}$	—	190.5	—	°C/W	

### 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

**TABLE 3-1: PIN FUNCTION TABLE**

MCP4725	Name	Description
SOT-23		
1	V <sub>OUT</sub>	Analog Output Voltage
2	V <sub>SS</sub>	Ground Reference
3	V <sub>DD</sub>	Supply Voltage
4	SDA	I <sup>2</sup> C Serial Data
5	SCL	I <sup>2</sup> C Serial Clock Input
6	A0	I <sup>2</sup> C Address Bit Selection pin (A0 bit). This pin can be tied to V <sub>SS</sub> or V <sub>DD</sub> , or can be actively driven by the digital logic levels. The logic state of this pin determines what the A0 bit of the I <sup>2</sup> C address bits should be.

#### 3.1 Analog Output Voltage (V<sub>OUT</sub>)

V<sub>OUT</sub> is an analog output voltage from the DAC device. DAC output amplifier drives this pin with a range of V<sub>SS</sub> to V<sub>DD</sub>.

#### 3.2 Supply Voltage (V<sub>DD</sub> or V<sub>SS</sub>)

V<sub>DD</sub> is the power supply pin for the device. The voltage at the V<sub>DD</sub> pin is used as the supply input as well as the DAC reference input. The power supply at the V<sub>DD</sub> pin should be clean as possible for a good DAC performance.

This pin requires an appropriate bypass capacitor of about 0.1 µF (ceramic) to ground. An additional 10 µF capacitor (tantalum) in parallel is also recommended to further attenuate high frequency noise present in application boards. The supply voltage (V<sub>DD</sub>) must be maintained in the 2.7V to 5.5V range for specified operation.

V<sub>SS</sub> is the ground pin and the current return path of the device. The user must connect the V<sub>SS</sub> pin to a ground plane through a low impedance connection. If an analog ground path is available in the application PCB (printed circuit board), it is highly recommended that the V<sub>SS</sub> pin be tied to the analog ground path or isolated within an analog ground plane of the circuit board.

#### 3.3 Serial Data Pin (SDA)

SDA is the serial data pin of the I<sup>2</sup>C interface. The SDA pin is used to write or read the DAC register and EEPROM data. The SDA pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor from the V<sub>DD</sub> line to the SDA pin. Except for START and STOP conditions, the data on the SDA pin must be stable during the high period of the clock. The high or low state of the SDA pin can only change when the clock signal on the SCL pin is low. Refer to [Section 7.0 “I<sup>2</sup>C Serial Interface Communication”](#) for more details of I<sup>2</sup>C Serial Interface communication.

#### 3.4 Serial Clock Pin (SCL)

SCL is the serial clock pin of the I<sup>2</sup>C interface. The MCP4725 acts only as a slave and the SCL pin accepts only external serial clocks. The input data from the Master device is shifted into the SDA pin on the rising edges of the SCL clock and output from the MCP4725 occurs at the falling edges of the SCL clock. The SCL pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor from the V<sub>DD</sub> line to the SCL pin. Refer to [Section 7.0 “I<sup>2</sup>C Serial Interface Communication”](#) for more details of I<sup>2</sup>C Serial Interface communication.

#### 3.5 Device Address Selection Pin (A0)

This pin is used to select the A0 address bit by the user. The user can tie this pin to V<sub>SS</sub> (logic ‘0’), or V<sub>DD</sub> (logic ‘1’), or can be actively driven by the digital logic levels, such as the I<sup>2</sup>C Master Output. See [Section 7.2 “Device Addressing”](#) for more details of the address bits.

## 4.0 TERMINOLOGY

### 4.1 Resolution

The resolution is the number of DAC output states that divide the full scale range. For the 12-bit DAC, the resolution is  $2^{12}$  or the DAC code ranges from 0 to 4095.

### 4.2 LSB

The least significant bit or the ideal voltage difference between two successive codes.

#### EQUATION 4-1:

$$LSB_{Ideal} = \frac{V_{REF}}{2^n} = \frac{(V_{Full\ Scale} - V_{Zero\ Scale})}{2^n - 1}$$

Where:

- $V_{REF}$  = The reference voltage =  $V_{DD}$  in the MCP4725. This  $V_{REF}$  is the ideal full scale voltage range  
 $n$  = The number of digital input bits.  
 $(n = 12$  for MCP4725)

### 4.3 Integral Nonlinearity (INL) or Relative Accuracy

INL error is the maximum deviation between an actual code transition point and its corresponding ideal transition point (straight line). [Figure 2-5](#) shows the INL curve of the MCP4725. The end-point method is used for the calculation. The INL error at a given input DAC code is calculated as:

#### EQUATION 4-2:

$$INL = \frac{(V_{OUT} - V_{Ideal})}{LSB}$$

Where:

- $V_{Ideal}$  = Code\*LSB  
 $V_{OUT}$  = The output voltage measured at the given input code

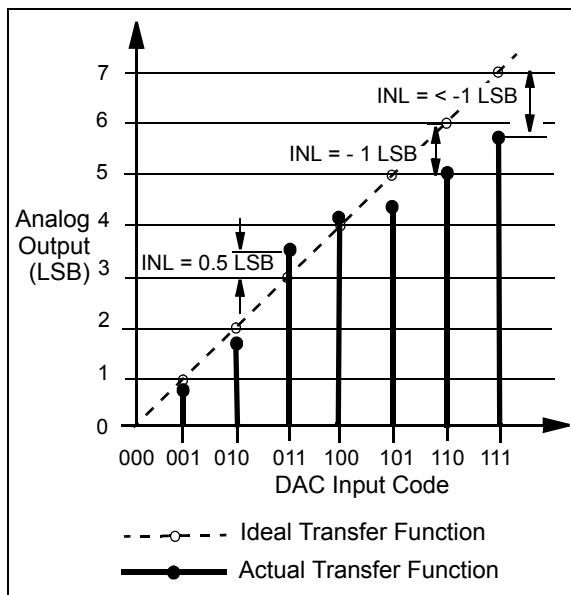


FIGURE 4-1: INL Accuracy.

### 4.4 Differential Nonlinearity (DNL)

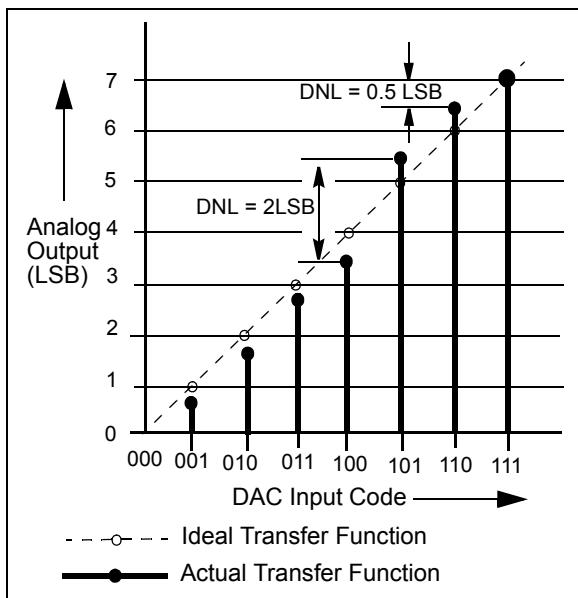
Differential nonlinearity error ([Figure 4-2](#)) is the measure of step size between codes in actual transfer function. The ideal step size between codes is 1 LSB. A DNL error of zero would imply that every code is exactly 1 LSB wide. If the DNL error is less than 1 LSB, the DAC guarantees monotonic output and no missing codes. The DNL error between any two adjacent codes is calculated as follows:

#### EQUATION 4-3:

$$DNL = \frac{\Delta V_{OUT} - LSB}{LSB}$$

Where:

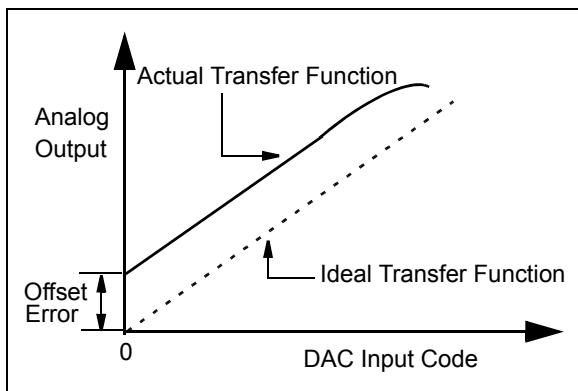
- $\Delta V_{OUT}$  = The measured DAC output voltage difference between two adjacent input codes.



**FIGURE 4-2:** DNL Accuracy.

## 4.5 Offset Error

Offset error (Figure 4-3) is the deviation from zero voltage output when the digital input code is zero. This error affects all codes by the same amount. In the MCP4725, the offset error is not trimmed at the factory. However, it can be calibrated by software in application circuits.



**FIGURE 4-3:** Offset Error.

## 4.6 Gain Error

Gain error (see Figure 4-4) is the difference between the actual full scale output voltage from the ideal output voltage on the transfer curve. The gain error is calculated after nullifying the offset error, or full scale error minus the offset error.

The gain error indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. The gain error is usually expressed as percent of full scale range (% of FSR) or in LSB.

In the MCP4725, the gain error is not calibrated at the factory and most of the gain error is contributed by the output op amp saturation near the code range beyond 4000. For the applications which need the gain error specification less than 1% maximum, the user may consider using the DAC code range between 100 and 4000 instead of using full code range (code 0 to 4095). The DAC output of the code range between 100 and 4000 is much linear than full scale range (0 to 4095). The gain error can be calibrated by software in applications.

## 4.7 Full Scale Error (FSE)

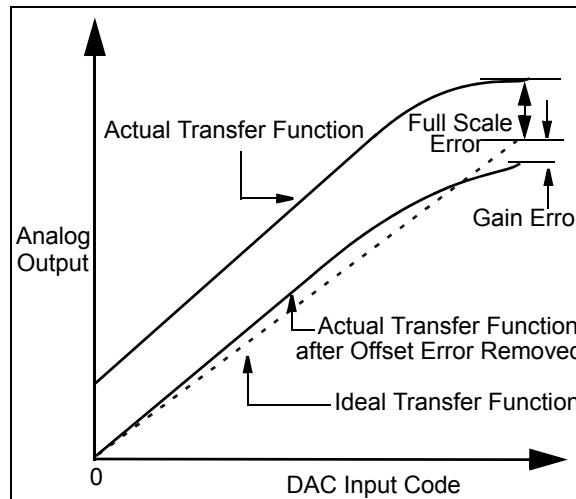
Full scale error (Figure 4-4) is the sum of offset error plus gain error. It is the difference between the ideal and measured DAC output voltage with all bits set to one (DAC input code = FFFh).

### EQUATION 4-4:

$$FSE = \frac{(V_{OUT} - V_{Ideal})}{LSB}$$

Where:

$$\begin{aligned} V_{Ideal} &= (V_{REF}) (1 - 2^{-n}) - V_{OFFSET} \\ V_{REF} &= \text{The reference voltage.} \\ V_{REF} &= V_{DD} \text{ in the MCP4725} \end{aligned}$$



**FIGURE 4-4:** Gain Error and Full Scale Error.

## 4.8 Gain Error Drift

Gain error drift is the variation in gain error due to a change in ambient temperature. The gain error drift is typically expressed in ppm/ $^{\circ}\text{C}$ .

## 4.9 Offset Error Drift

Offset error drift is the variation in offset error due to a change in ambient temperature. The offset error drift is typically expressed in ppm/ $^{\circ}$ C.

## 4.10 Settling Time

The Settling time is the time delay required for the DAC output to settle to its new output value from the start of code transition, within specified accuracy. In the MCP4725, the settling time is a measure of the time delay until the DAC output reaches its final value (within 0.5 LSB) when the DAC code changes from 400h to C00h.

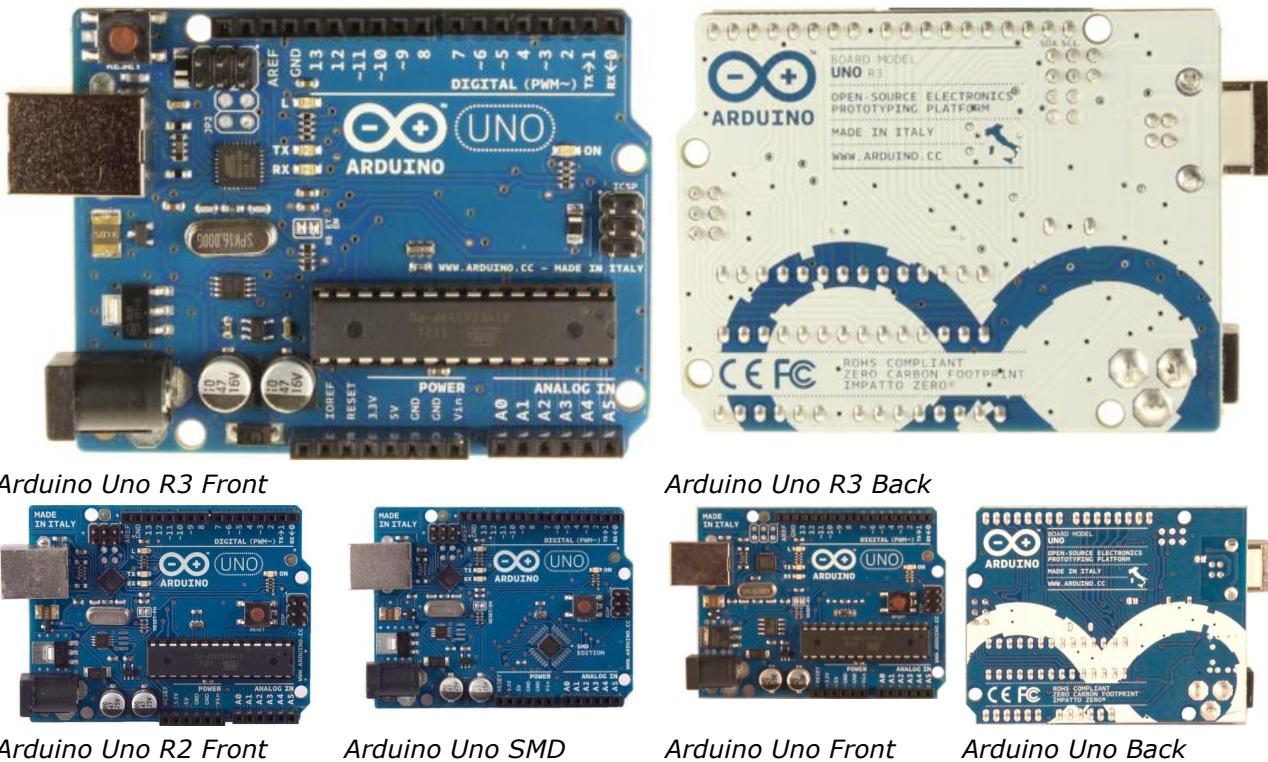
## 4.11 Major-Code Transition Glitch

Major-code transition glitch is the impulse energy injected into the DAC analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV-Sec. and is measured when the digital code is changed by 1 LSB at the major carry transition (Example: 011...111 to 100... 000, or 100... 000 to 011 ... 111).

## 4.12 Digital Feedthrough

Digital feedthrough is the glitch that appears at the analog output caused by coupling from the digital input pins of the device. It is specified in nV-Sec. and is measured with a full scale change on the digital input pins (Example: 000... 000 to 111... 111, or 111... 111 to 000... 000). The digital feedthrough is measured when the DAC is not being written to the register.

# Arduino Uno



## Overview

The Arduino Uno is a microcontroller board based on the ATmega328 ([datasheet](#)). It has 14 digital input/output pins (of which 6 can be used as PWM outputs), 6 analog inputs, a 16 MHz ceramic resonator, a USB connection, a power jack, an ICSP header, and a reset button. It contains everything needed to support the microcontroller; simply connect it to a computer with a USB cable or power it with a AC-to-DC adapter or battery to get started.

The Uno differs from all preceding boards in that it does not use the FTDI USB-to-serial driver chip. Instead, it features the Atmega16U2 (Atmega8U2 up to version R2) programmed as a USB-to-serial converter.

| [Revision 2](#) of the Uno board has a resistor pulling the 8U2 HWB line to ground, making it easier to put into [DFU mode](#).

| [Revision 3](#) of the board has the following new features:

- 1.0 pinout: added SDA and SCL pins that are near to the AREF pin and two other new pins placed near to the RESET pin, the IOREF that allow the shields to adapt to the voltage provided from the board. In future, shields will be compatible both with the board that use the AVR, which operate with 5V and with the Arduino Due that operate with 3.3V. The second one is a not connected pin, that is reserved for future purposes.
- Stronger RESET circuit.
- Atmega 16U2 replace the 8U2.

"Uno" means one in Italian and is named to mark the upcoming release of Arduino 1.0. The Uno and version 1.0 will be the reference versions of Arduino, moving forward. The Uno is the latest in a series of USB Arduino boards, and the reference model for the Arduino platform; for a comparison with previous versions, see the [index of Arduino boards](#).

## Summary

Microcontroller	ATmega328
Operating Voltage	5V
Input Voltage (recommended)	7-12V

Input Voltage (limits)	6-20V
Digital I/O Pins	14 (of which 6 provide PWM output)
Analog Input Pins	6
DC Current per I/O Pin	40 mA
DC Current for 3.3V Pin	50 mA
Flash Memory	32 KB (ATmega328) of which 0.5 KB used by bootloader
SRAM	2 KB (ATmega328)
EEPROM	1 KB (ATmega328)
Clock Speed	16 MHz

## Schematic & Reference Design

EAGLE files: [arduino-uno-Rev3-reference-design.zip](#) (NOTE: works with Eagle 6.0 and newer)

Schematic: [arduino-uno-Rev3-schematic.pdf](#)

**Note:** The Arduino reference design can use an Atmega8, 168, or 328, Current models use an ATmega328, but an Atmega8 is shown in the schematic for reference. The pin configuration is identical on all three processors.

## Power

The Arduino Uno can be powered via the USB connection or with an external power supply. The power source is selected automatically.

External (non-USB) power can come either from an AC-to-DC adapter (wall-wart) or battery. The adapter can be connected by plugging a 2.1mm center-positive plug into the board's power jack. Leads from a battery can be inserted in the Gnd and Vin pin headers of the POWER connector.

The board can operate on an external supply of 6 to 20 volts. If supplied with less than 7V, however, the 5V pin may supply less than five volts and the board may be unstable. If using more than 12V, the voltage regulator may overheat and damage the board. The recommended range is 7 to 12 volts.

The power pins are as follows:

- **VIN.** The input voltage to the Arduino board when it's using an external power source (as opposed to 5 volts from the USB connection or other regulated power source). You can supply voltage through this pin, or, if supplying voltage via the power jack, access it through this pin.
- **5V.** This pin outputs a regulated 5V from the regulator on the board. The board can be supplied with power either from the DC power jack (7 - 12V), the USB connector (5V), or the VIN pin of the board (7-12V). Supplying voltage via the 5V or 3.3V pins bypasses the regulator, and can damage your board. We don't advise it.
- **3V3.** A 3.3 volt supply generated by the on-board regulator. Maximum current draw is 50 mA.
- **GND.** Ground pins.

## Memory

The ATmega328 has 32 KB (with 0.5 KB used for the bootloader). It also has 2 KB of SRAM and 1 KB of EEPROM (which can be read and written with the [EEPROM library](#)).

## Input and Output

Each of the 14 digital pins on the Uno can be used as an input or output, using [pinMode\(\)](#), [digitalWrite\(\)](#), and [digitalRead\(\)](#) functions. They operate at 5 volts. Each pin can provide or receive a maximum of 40 mA and has an internal pull-up resistor (disconnected by default) of 20-50 kOhms. In addition, some pins have specialized functions:

- **Serial: 0 (RX) and 1 (TX).** Used to receive (RX) and transmit (TX) TTL serial data. These pins are connected to the corresponding pins of the ATmega8U2 USB-to-TTL Serial chip.
- **External Interrupts: 2 and 3.** These pins can be configured to trigger an interrupt on a low value, a rising or falling edge, or a change in value. See the [attachInterrupt\(\)](#) function for details.
- **PWM: 3, 5, 6, 9, 10, and 11.** Provide 8-bit PWM output with the [analogWrite\(\)](#) function.

- **SPI: 10 (SS), 11 (MOSI), 12 (MISO), 13 (SCK).** These pins support SPI communication using the [SPI library](#).
- **LED: 13.** There is a built-in LED connected to digital pin 13. When the pin is HIGH value, the LED is on, when the pin is LOW, it's off.

The Uno has 6 analog inputs, labeled A0 through A5, each of which provide 10 bits of resolution (i.e. 1024 different values). By default they measure from ground to 5 volts, though it is possible to change the upper end of their range using the AREF pin and the [analogReference\(\)](#) function. Additionally, some pins have specialized functionality:

- **TWI: A4 or SDA pin and A5 or SCL pin.** Support TWI communication using the [Wire library](#).

There are a couple of other pins on the board:

- **AREF.** Reference voltage for the analog inputs. Used with [analogReference\(\)](#).
- **Reset.** Bring this line LOW to reset the microcontroller. Typically used to add a reset button to shields which block the one on the board.

See also the [mapping between Arduino pins and ATmega328 ports](#). The mapping for the Atmega8, 168, and 328 is identical.

## Communication

The Arduino Uno has a number of facilities for communicating with a computer, another Arduino, or other microcontrollers. The ATmega328 provides UART TTL (5V) serial communication, which is available on digital pins 0 (RX) and 1 (TX). An ATmega16U2 on the board channels this serial communication over USB and appears as a virtual com port to software on the computer. The '16U2 firmware uses the standard USB COM drivers, and no external driver is needed. However, [on Windows, a .inf file is required](#). The Arduino software includes a serial monitor which allows simple textual data to be sent to and from the Arduino board. The RX and TX LEDs on the board will flash when data is being transmitted via the USB-to-serial chip and USB connection to the computer (but not for serial communication on pins 0 and 1).

A [SoftwareSerial library](#) allows for serial communication on any of the Uno's digital pins.

The ATmega328 also supports I2C (TWI) and SPI communication. The Arduino software includes a Wire library to simplify use of the I2C bus; see the [documentation](#) for details. For SPI communication, use the [SPI library](#).

## Programming

The Arduino Uno can be programmed with the Arduino software ([download](#)). Select "Arduino Uno" from the **Tools > Board** menu (according to the microcontroller on your board). For details, see the [reference](#) and [tutorials](#).

The ATmega328 on the Arduino Uno comes preburned with a [bootloader](#) that allows you to upload new code to it without the use of an external hardware programmer. It communicates using the original STK500 protocol ([reference](#), [C header files](#)).

You can also bypass the bootloader and program the microcontroller through the ICSP (In-Circuit Serial Programming) header; see [these instructions](#) for details.

The ATmega16U2 (or 8U2 in the rev1 and rev2 boards) firmware source code is available . The ATmega16U2/8U2 is loaded with a DFU bootloader, which can be activated by:

- On Rev1 boards: connecting the solder jumper on the back of the board (near the map of Italy) and then resetting the 8U2.
- On Rev2 or later boards: there is a resistor that pulling the 8U2/16U2 HWB line to ground, making it easier to put into DFU mode.

You can then use [Atmel's FLIP software](#) (Windows) or the [DFU programmer](#) (Mac OS X and Linux) to load a new firmware. Or you can use the ISP header with an external programmer (overwriting the DFU bootloader). See [this user-contributed tutorial](#) for more information.

## Automatic (Software) Reset

Rather than requiring a physical press of the reset button before an upload, the Arduino Uno is designed in a way that allows it to be reset by software running on a connected computer. One of the hardware flow control lines (DTR) of the ATmega8U2/16U2 is connected to the reset line of the ATmega328 via a 100 nanofarad capacitor. When this line is asserted (taken low), the reset line drops long enough to reset the chip. The Arduino software uses this capability to allow you to upload code by simply pressing the upload button in the Arduino environment. This means that the bootloader can have a shorter timeout, as the lowering of DTR can be well-coordinated with the start of the upload. This setup has other implications. When the Uno is connected to either a computer running Mac OS X or Linux, it resets each time a connection is made to it from software (via USB). For the following half-second or so, the bootloader is running on the Uno. While it is programmed to ignore malformed data (i.e. anything besides an upload of new code), it will intercept the first few bytes of data sent to the board after a connection is opened. If a sketch running on the board receives one-time configuration or other data when it first starts, make sure that the software with which it communicates waits a second after opening the connection and before sending this data.

The Uno contains a trace that can be cut to disable the auto-reset. The pads on either side of the trace can be soldered together to re-enable it. It's labeled "RESET-EN". You may also be able to disable the auto-reset by connecting a 110 ohm resistor from 5V to the reset line; see [this forum thread](#) for details.

## USB Overcurrent Protection

The Arduino Uno has a resettable polyfuse that protects your computer's USB ports from shorts and overcurrent. Although most computers provide their own internal protection, the fuse provides an extra layer of protection. If more than 500 mA is applied to the USB port, the fuse will automatically break the connection until the short or overload is removed.

## Physical Characteristics

The maximum length and width of the Uno PCB are 2.7 and 2.1 inches respectively, with the USB connector and power jack extending beyond the former dimension. Four screw holes allow the board to be attached to a surface or case. Note that the distance between digital pins 7 and 8 is 160 mil (0.16"), not an even multiple of the 100 mil spacing of the other pins.

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## Data Sheet

## AD8671/AD8672/AD8674

### FEATURES

- Very low noise:** 2.8 nV/ $\sqrt{\text{Hz}}$ , 77 nV p-p
- Wide bandwidth:** 10 MHz
- Low input bias current:** 12 nA max
- Low offset voltage:** 75  $\mu\text{V}$  max
- High open-loop gain:** 120 dB min
- Low supply current:** 3 mA typ per amplifier
- Dual-supply operation:**  $\pm 5 \text{ V}$  to  $\pm 15 \text{ V}$
- Unity-gain stable**
- No phase reversal**

### APPLICATIONS

- PLL filters**
- Filters for GPS**
- Instrumentation**
- Sensors and controls**
- Professional quality audio**

### GENERAL DESCRIPTION

The AD8671/AD8672/AD8674 are very high precision amplifiers featuring very low noise, very low offset voltage and drift, low input bias current, 10 MHz bandwidth, and low power consumption. Outputs are stable with capacitive loads of over 1000 pF. Supply current is less than 3 mA per amplifier at 30 V.

The AD8671/AD8672/AD8674's combination of ultralow noise, high precision, speed, and stability is unmatched. The MSOP version of the AD8671/AD8672 requires only half the board space of comparable amplifiers.

Applications for these amplifiers include high quality PLL filters, precision filters, medical and analytical instrumentation, precision power supply controls, ATE, data acquisition, and precision controls as well as professional quality audio.

The AD8671/AD8672 are specified over the extended industrial temperature range ( $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ ), and the AD8674 is specified over the industrial temperature range ( $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ ).

The AD8671/AD8672 are available in the 8-lead SOIC and 8-lead MSOP packages. The AD8674 is available in 14-lead SOIC and 14-lead TSSOP packages.

Surface-mount devices in MSOP packages are available in tape and reel only.

### PIN CONFIGURATIONS

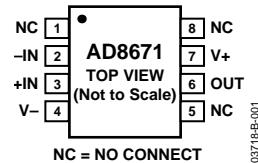


Figure 1. 8-Lead SOIC\_N (R-8) and 8-Lead MSOP (RM-8)

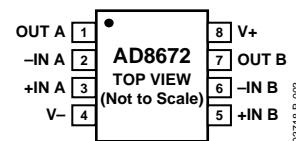


Figure 2. 8-Lead SOIC-N (R-8) and 8-Lead MSOP (RM-8)

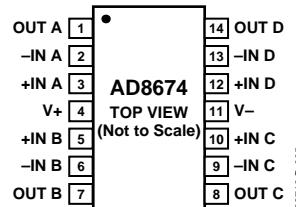


Figure 3. 14-Lead SOIC\_N (R-14) and 14-Lead TSSOP (RU-14)

The AD8671, AD8672, and AD8674 are members of a growing series of low noise op amps offered by Analog Devices, Inc.

**Table 1. Voltage Noise**

Package	0.9 nV	1.1 nV	1.8 nV	2.8 nV	3.8 nV
Single	<a href="#">AD797</a>	<a href="#">AD8597</a>	<a href="#">ADA4004-1</a>	<a href="#">AD8675</a>	<a href="#">AD8671</a>
Dual		<a href="#">AD8599</a>	<a href="#">ADA4004-2</a>	<a href="#">AD8676</a>	<a href="#">AD8672</a>
Quad			<a href="#">ADA4004-4</a>		<a href="#">AD8674</a>

Rev. F

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### 3/13—Rev. E to Rev. F

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Updated Outline Dimensions .....	15
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### 6/10—Rev. D to Rev. E

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### 12/09—Rev. C to Rev. D

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Added Power Dissipation Calculations Section .....	11
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### 1/04—Rev. 0 to Rev. A

Added AD8672 and AD8674 parts .....	Universal
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Deleted Figure 3.....	6
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Changes to Figure 37.....	12
Added new Figure 32 .....	10

**SPECIFICATIONS****ELECTRICAL CHARACTERISTICS,  $\pm 5.0\text{ V}$** 

$V_S = \pm 5.0\text{ V}$ ,  $V_{CM} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 2.**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	$V_{OS}$		20	75		$\mu\text{V}$
Offset Voltage Drift AD8671	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	30	125		$\mu\text{V}/^\circ\text{C}$
Offset Voltage Drift AD8672/AD8674		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.3	0.5	$\mu\text{V}/^\circ\text{C}$
Input Bias Current AD8671	$I_B$		-12	+3	+12	$\text{nA}$
Input Bias Current AD8672/AD8674		$+25^\circ\text{C} < T_A < +125^\circ\text{C}$	-20	+5	+20	$\text{nA}$
Input Offset Current AD8671	$I_{OS}$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-40	+8	+40	$\text{nA}$
Input Offset Current AD8672/AD8674		$+25^\circ\text{C} < T_A < +125^\circ\text{C}$	-12	+6	+12	$\text{nA}$
Input Offset Current AD8671		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-20	+6	+20	$\text{nA}$
Input Offset Current AD8672/AD8674			-40	+8	+40	$\text{nA}$
Input Voltage Range			-2.5		+2.5	$\text{V}$
Common-Mode Rejection Ratio	$CMRR$	$V_{CM} = -2.5\text{ V}$ to $+2.5\text{ V}$	100	120		$\text{dB}$
Large Signal Voltage Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ , $V_O = -3\text{ V}$ to $+3\text{ V}$	1000	6000		$\text{V/mV}$
Input Capacitance, Common Mode	$C_{INCM}$			6.25		$\text{pF}$
Input Capacitance, Differential Mode	$C_{INDM}$			7.5		$\text{pF}$
Input Resistance, Common Mode	$R_{IN}$			3.5		$\text{G}\Omega$
Input Resistance, Differential Mode	$R_{INDM}$			15		$\text{M}\Omega$
OUTPUT CHARACTERISTICS						
Output Voltage High	$V_{OH}$	$R_L = 2\text{ k}\Omega$ , $-40^\circ\text{C}$ to $+125^\circ\text{C}$	+3.8	+4.0		$\text{V}$
Output Voltage Low	$V_{OL}$	$R_L = 2\text{ k}\Omega$ , $-40^\circ\text{C}$ to $+125^\circ\text{C}$		-3.9	-3.8	$\text{V}$
Output Voltage High	$V_{OH}$	$R_L = 600\Omega$	+3.7	+3.9		$\text{V}$
Output Voltage Low	$V_{OL}$	$R_L = 600\Omega$		-3.8	-3.7	$\text{V}$
Output Current	$I_{OUT}$			$\pm 10$		$\text{mA}$
POWER SUPPLY						
Power Supply Rejection Ratio AD8671/AD8672	$PSRR$	$V_S = \pm 4\text{ V}$ to $\pm 18\text{ V}$	110	130		$\text{dB}$
AD8674			106	115		$\text{dB}$
Supply Current/Amplifier	$I_{SY}$	$V_O = 0\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		3	3.5	$\text{mA}$
					4.2	$\text{mA}$
DYNAMIC PERFORMANCE						
Slew Rate	$SR$	$R_L = 2\text{ k}\Omega$		4		$\text{V}/\mu\text{s}$
Settling Time	$t_s$	To 0.1% (4 V step, $G = 1$ )		1.4		$\mu\text{s}$
		To 0.01% (4 V step, $G = 1$ )		5.1		$\mu\text{s}$
Gain Bandwidth Product	$GBP$			10		$\text{MHz}$
NOISE PERFORMANCE						
Peak-to-Peak Noise	$e_{n,p-p}$	0.1 Hz to 10 Hz		77	100	$\text{nV p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		2.8	3.8	$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.3		$\text{pA}/\sqrt{\text{Hz}}$
Channel Separation AD8672/AD8674	$C_S$	$f = 1\text{ kHz}$		-130		$\text{dB}$
		$f = 10\text{ kHz}$		-105		$\text{dB}$

**ELECTRICAL CHARACTERISTICS,  $\pm 15\text{ V}$**  $V_S = \pm 15\text{ V}$ ,  $V_{CM} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$		20	75		$\mu\text{V}$
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	30	125		$\mu\text{V}$
Offset Voltage Drift AD8671	$\Delta V_{OS}/\Delta T$		0.3	0.5		$\mu\text{V}/^\circ\text{C}$
AD8672/AD8674			0.3	0.8		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$		-12	+3	+12	nA
		$+25^\circ\text{C} < T_A < +125^\circ\text{C}$	-20	+5	+20	nA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-40	+8	+40	nA
Input Offset Current	$I_{OS}$		-12	+6	+12	nA
		$+25^\circ\text{C} < T_A < +125^\circ\text{C}$	-20	+6	+20	nA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-40	+8	+40	nA
Input Voltage Range			-12		+12	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -12\text{ V}$ to $+12\text{ V}$	100	120		dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ , $V_O = -10\text{ V}$ to $+10\text{ V}$	1000	6000		V/mV
Input Capacitance, Common Mode	$C_{INCM}$			6.25		pF
Input Capacitance, Differential Mode	$C_{INDM}$			7.5		pF
Input Resistance, Common Mode	$R_{IN}$			3.5		G $\Omega$
Input Resistance, Differential Mode	$R_{INDM}$			15		M $\Omega$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$R_L = 2\text{ k}\Omega$ , $-40^\circ\text{C}$ to $+125^\circ\text{C}$	+13.2	+13.8		V
Output Voltage Low	$V_{OL}$	$R_L = 2\text{ k}\Omega$ , $-40^\circ\text{C}$ to $+125^\circ\text{C}$		-13.8	-13.2	V
Output Voltage High	$V_{OH}$	$R_L = 600\text{ }\Omega$	+11	+12.3		V
Output Voltage Low	$V_{OL}$	$R_L = 600\text{ }\Omega$		-12.4	-11	V
Output Current	$I_{OUT}$			$\pm 20$		mA
Short Circuit Current	$I_{SC}$			$\pm 30$		mA
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio AD8671/AD8672	PSRR	$V_S = \pm 4\text{ V}$ to $\pm 18\text{ V}$	110	130		dB
AD8674			106	115		dB
Supply Current/Amplifier	$I_{SY}$	$V_O = 0\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		3	3.5	mA
					4.2	mA
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		4		V/ $\mu\text{s}$
Settling Time	$t_s$	To 0.1% (10 V step, $G = 1$ )		2.2		$\mu\text{s}$
		To 0.01% (10 V step, $G = 1$ )		6.3		$\mu\text{s}$
Gain Bandwidth Product	GBP			10		MHz
<b>NOISE PERFORMANCE</b>						
Peak-to-Peak Noise	$e_{n,p-p}$	0.1 Hz to 10 Hz		77	100	nV p-p
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		2.8	3.8	nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.3		pA/ $\sqrt{\text{Hz}}$
Channel Separation AD8672/AD8674	$C_s$	$f = 1\text{ kHz}$		-130		dB
		$f = 10\text{ kHz}$		-105		dB

## ABSOLUTE MAXIMUM RATINGS

Table 4.<sup>1</sup>

Parameter	Rating
Supply Voltage	36 V
Input Voltage	$V_{S^-}$ to $V_{S^+}$
Differential Input Voltage	$\pm 0.7$ V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range All Packages	-65°C to +150°C
Operating Temperature Range 8-Lead Packages	-40°C to +125°C
14-Lead Packages	-40°C to +85°C
Junction Temperature Range All Packages	-65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

<sup>1</sup> Absolute maximum ratings apply at 25°C, unless otherwise noted.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

See the Applications section for a related discussion on power.

Table 5. Package Characteristics

Package Type	$\theta_{JA}^1$	$\theta_{JC}$	Unit
8-Lead MSOP (RM)	142	44	°C/W
8-Lead SOIC_N (R)	120	43	°C/W
14-Lead SOIC_N (R)	90	36	°C/W
14-Lead TSSOP (RU)	112	35	°C/W

<sup>1</sup>  $\theta_{JA}$  is specified for the worst-case conditions, that is,  $\theta_{JA}$  is specified for the device soldered on a 4-layer circuit board for surface-mount packages.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## TYPICAL PERFORMANCE CHARACTERISTICS

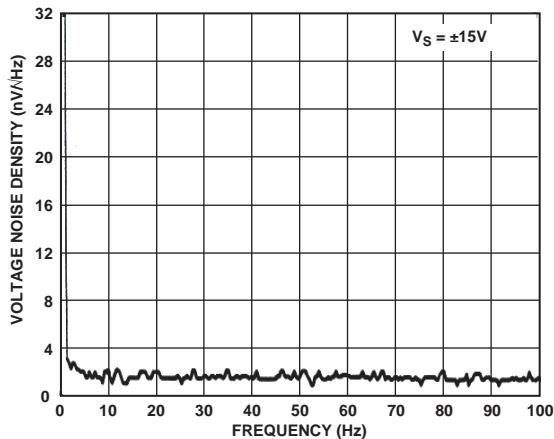


Figure 4. Voltage Noise Density vs. Frequency

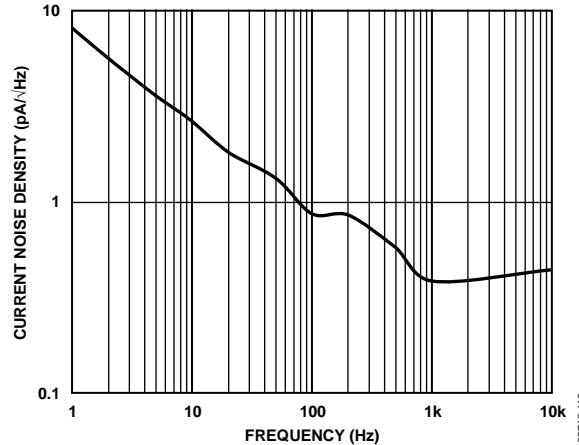
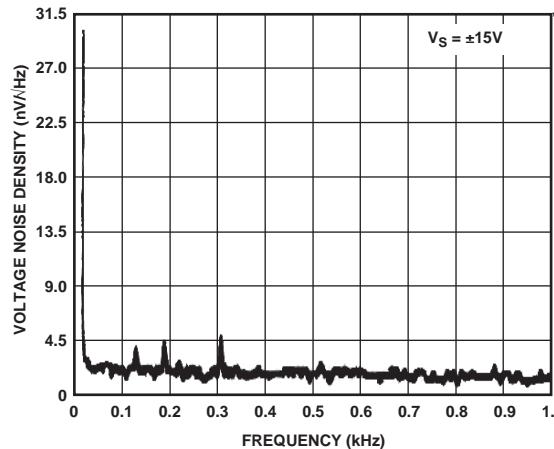
Figure 7. Current Noise Density  $V_S = \pm 15V$ 

Figure 5. Voltage Noise Density vs. Frequency

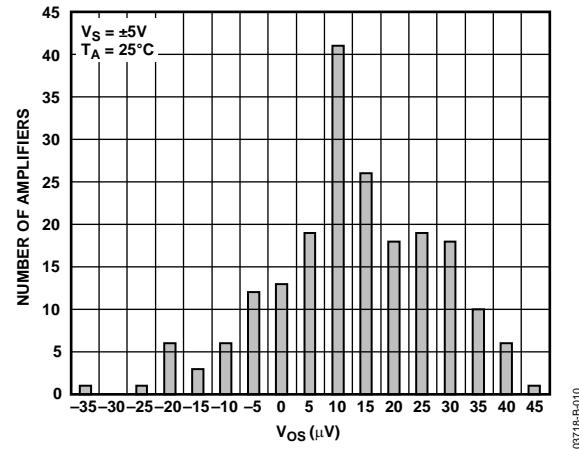


Figure 8. Input Offset Voltage Distribution

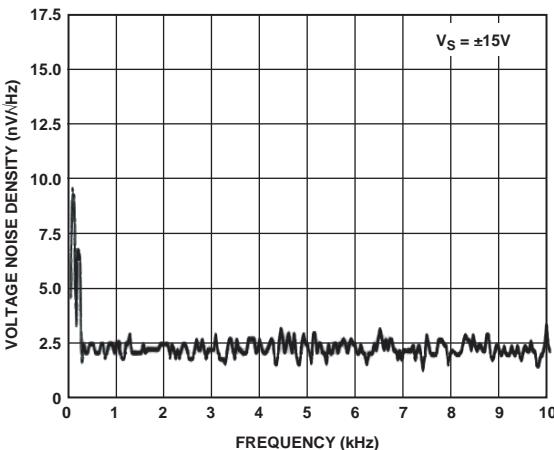


Figure 6. Voltage Noise Density vs. Frequency

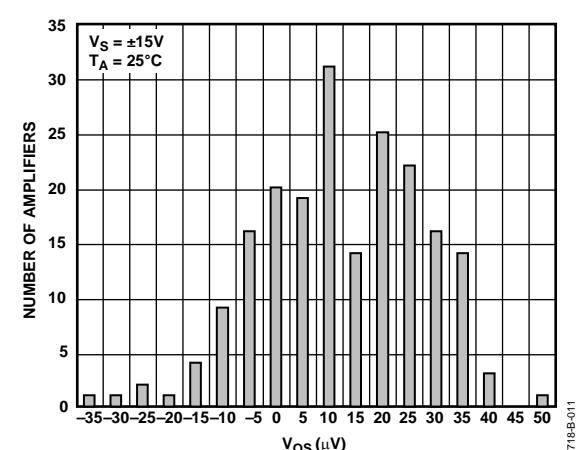


Figure 9. Input Offset Voltage Distribution

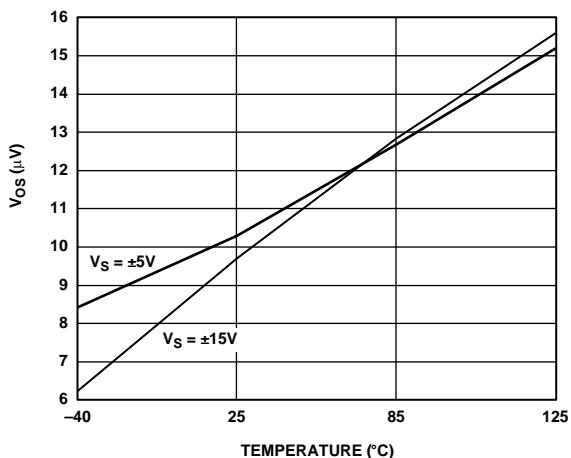


Figure 10. Input Offset Voltage vs. Temperature

03718-B-012

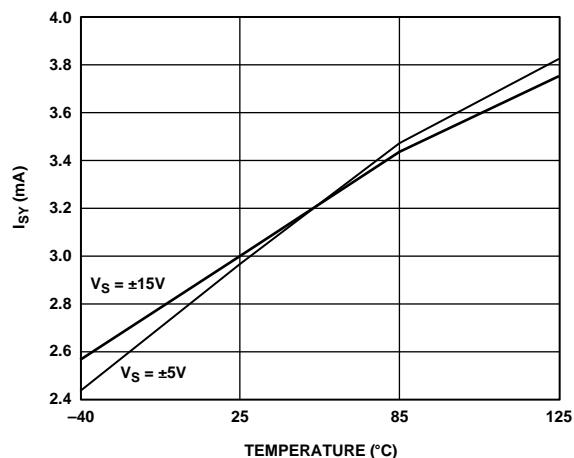


Figure 13. Supply Current vs. Temperature

03718-B-015

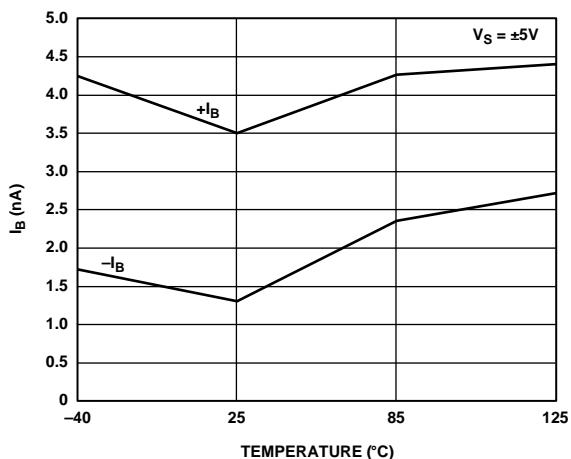


Figure 11. Input Bias Current vs. Temperature

03718-B-013

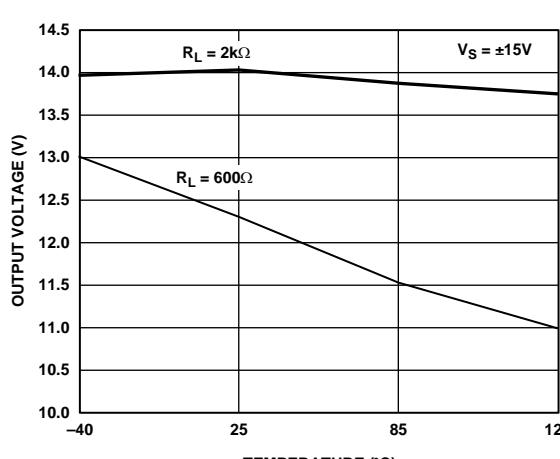


Figure 14. Output Voltage High vs. Temperature

03718-B-016

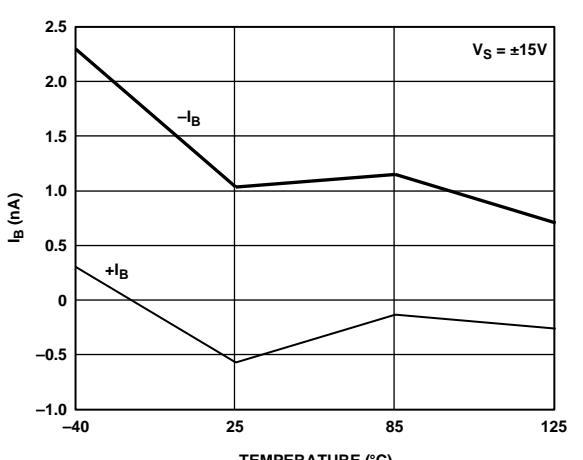


Figure 12. Input Bias Current vs. Temperature

03718-B-014

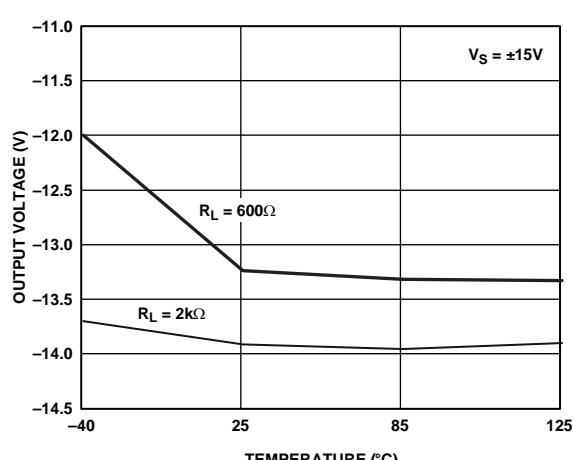
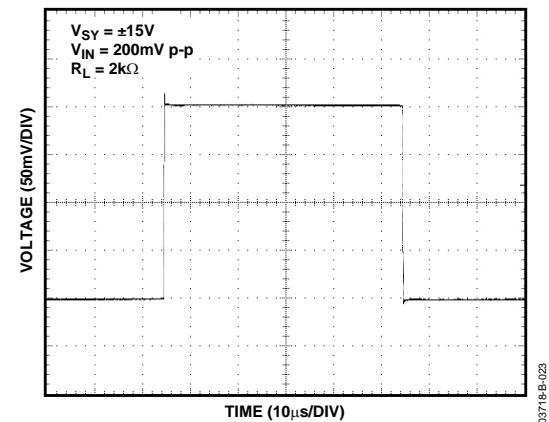
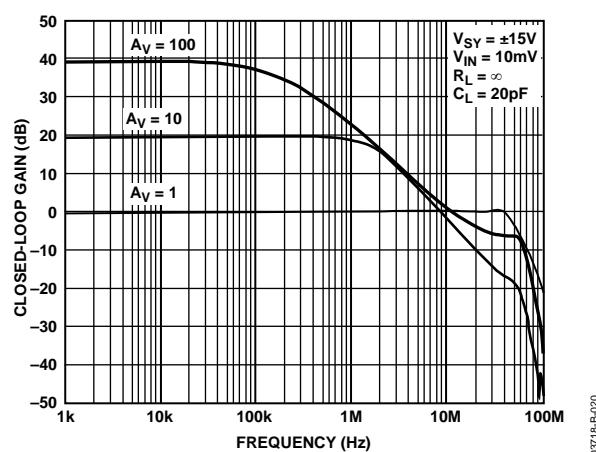
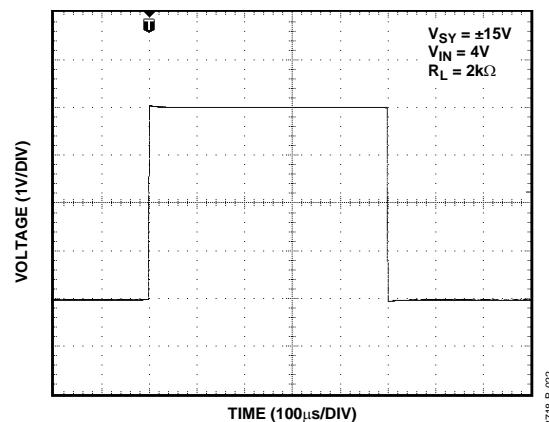
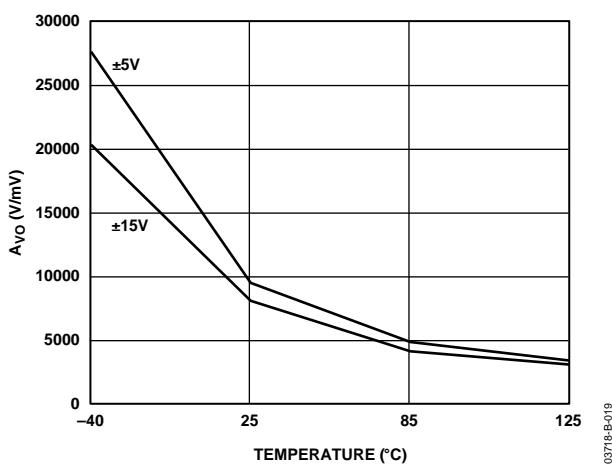
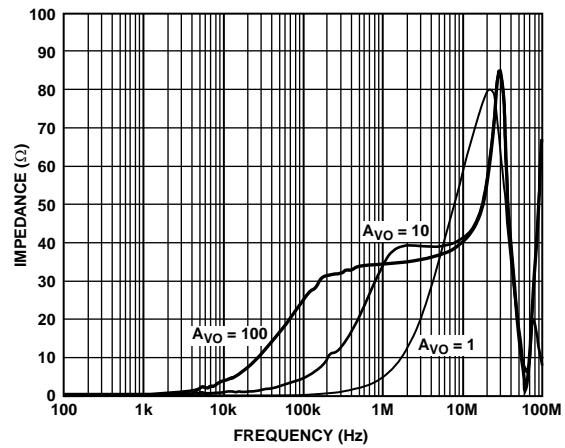
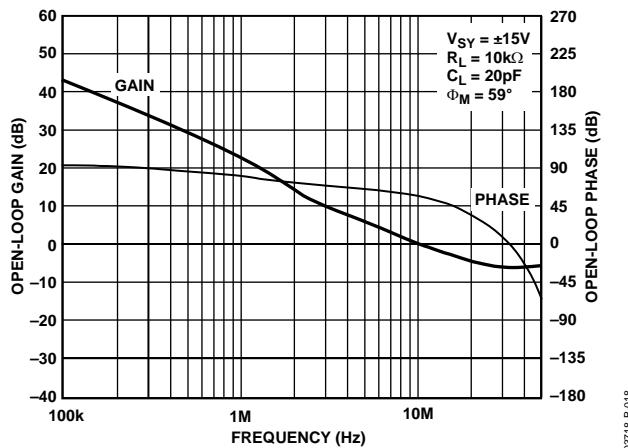


Figure 15. Output Voltage Low vs. Temperature

03718-B-017



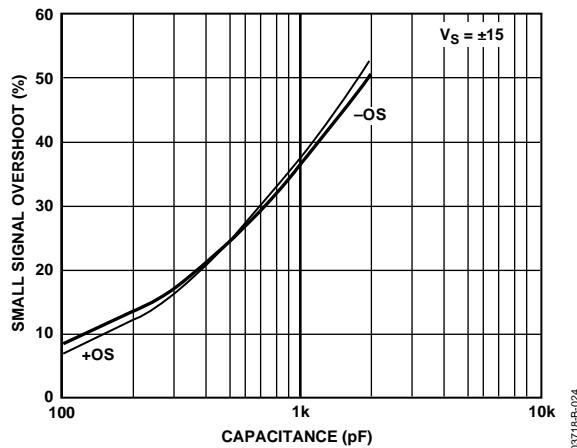


Figure 22. Small Signal Overshoot vs. Load Capacitance

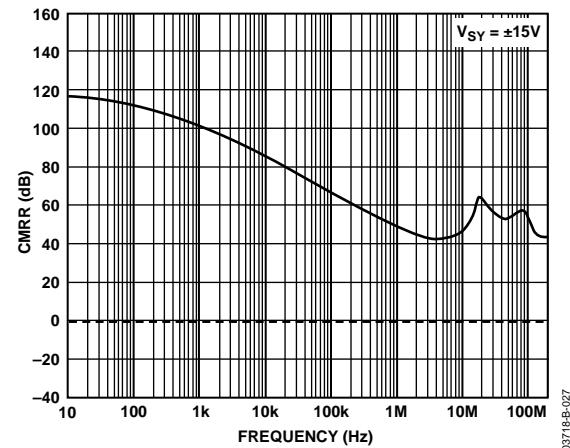


Figure 25. CMRR vs. Frequency

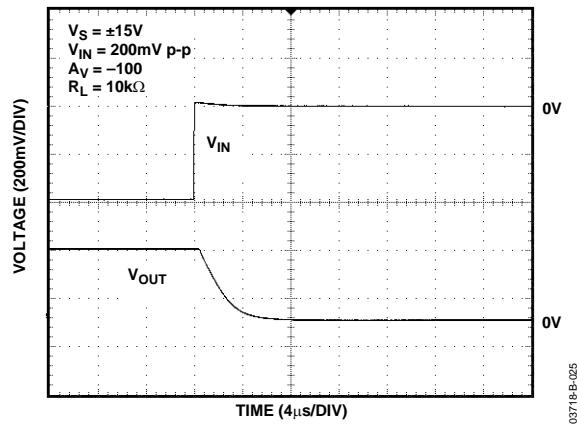


Figure 23. Positive Overdrive Recovery

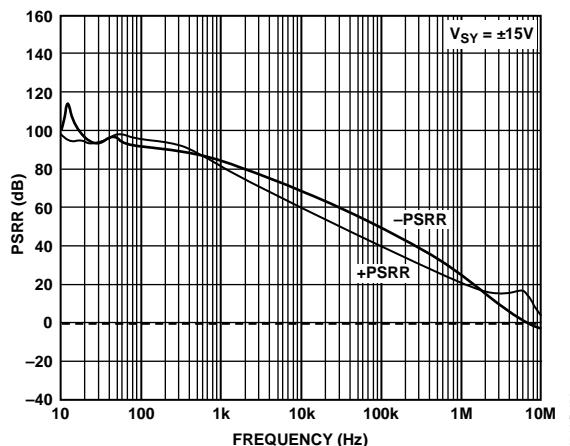


Figure 26. PSRR vs. Frequency

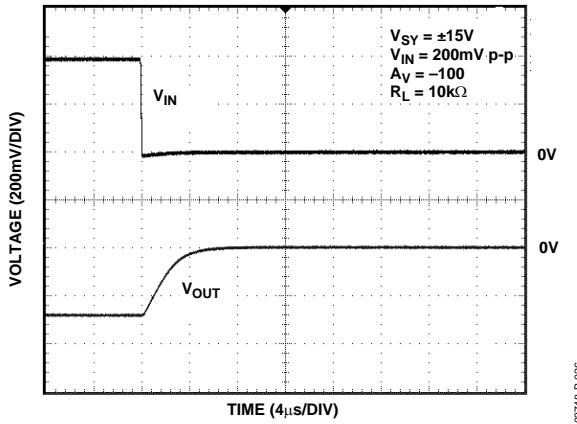


Figure 24. Negative Overdrive Recovery

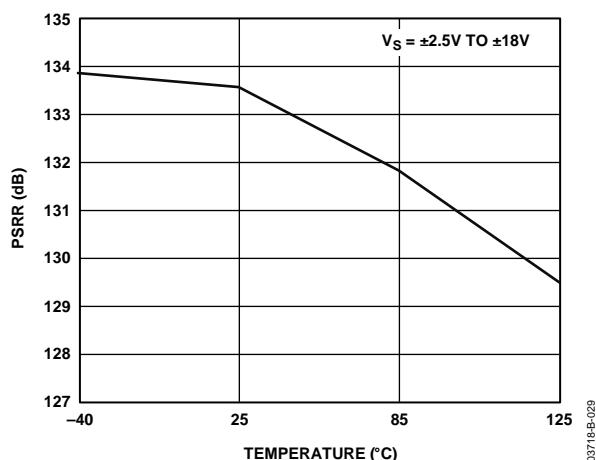


Figure 27. PSRR vs. Temperature

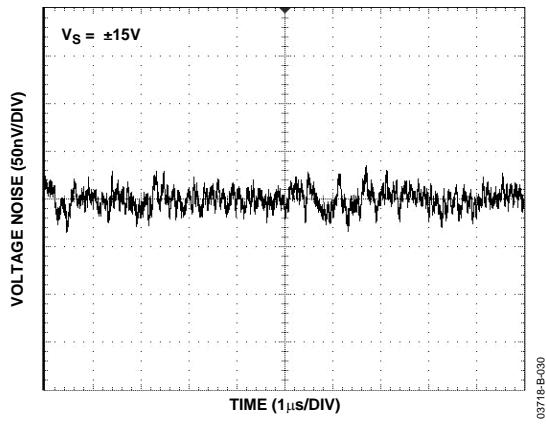


Figure 28. 0.1 Hz to 10 Hz Input Voltage Noise

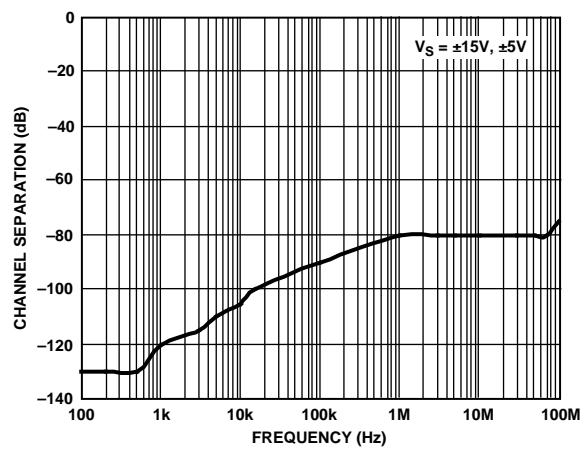


Figure 29. Channel Separation

03718-B-031

## APPLICATIONS

### POWER DISSIPATION CALCULATIONS

To achieve low voltage noise in a bipolar op amp, the current must be increased. The emitter-base theoretical voltage noise is approximately

$$e_n = 10^9 kT \sqrt{\frac{2}{qI_c}} \text{ nV}/\sqrt{\text{Hz}}$$

To achieve the low voltage noise of  $2.8 \text{ nV}/\sqrt{\text{Hz}}$ , the input stage current is higher than most op amps with an equivalent gain bandwidth product. The thermal noise of a  $1 \text{ k}\Omega$  resistor is  $4 \text{ nV}/\sqrt{\text{Hz}}$ , which is higher than the voltage noise of AD8671 family. Low voltage noise requires using low values of resistors, so low voltage noise op amps should have good drive capability, such as a  $600 \text{ }\Omega$  load. This means that the second stage and output stage are also biased at higher currents. As a result, the supply current of a single op amp is  $3.5 \text{ mA}$  maximum at room temperature.

Junction temperature has a direct affect on reliability. For more information, visit the following Analog Devices, Inc., website: <http://www.analog.com/en/quality-and-reliability/reliability-data/content/index.html>

MTTF and FIT calculations can be done based on the junction temperature and IC process. Use the following equation to determine the junction temperature:

$$T_J = T_A + P_D \times \theta_{JA}$$

For the AD8671 single in the 8-lead MSOP package, the thermal resistance,  $\theta_{JA}$ , is  $142^\circ\text{C}/\text{W}$ . If the ambient temperature is  $30^\circ\text{C}$  and the supply voltages are  $\pm 12 \text{ V}$ , the power dissipation is

$$24 \text{ V} \times 3.5 \text{ mA} = 84 \text{ mW}$$

Therefore, the rise above ambient temperature is

$$84 \text{ mW} \times 142^\circ\text{C}/\text{W} = 12^\circ\text{C}$$

If the ambient temperature is  $30^\circ\text{C}$ , the junction temperature is  $42^\circ\text{C}$ . The previously mentioned website that details the effect of the junction temperature on reliability has a calculator that requires only the part number and the junction temperature to determine the process technology.

For the AD8674 single in the 14-Lead TSSOP package, the thermal resistance,  $\theta_{JA}$ , is  $112^\circ\text{C}/\text{W}$ . Although  $\theta_{JA}$  is lower than it is for the 8-lead package, the four op amps are powered simultaneously. If the ambient temperature is  $50^\circ\text{C}$  and the supply voltages are  $\pm 15 \text{ V}$ , the power dissipation is

$$30 \text{ V} \times 4.2 \text{ mA} \times \text{four op amps} = 504 \text{ mW}$$

Therefore, the rise above ambient temperature is

$$504 \text{ mW} \times 112^\circ\text{C}/\text{W} = 56^\circ\text{C}$$

With an ambient temperature of  $50^\circ\text{C}$ , the junction temperature is  $106^\circ\text{C}$ . This is less than the specified absolute maximum junction temperature, but for systems with long product lifetimes (years), this should be considered carefully.

Note that these calculations do not include the additional dissipation caused by the load current on each op amp. Possible solutions to reduce junction temperature include system level considerations such as fans, Peltier thermoelectric coolers, and heat pipes. Board considerations include operation on lower voltages, such as  $\pm 12 \text{ V}$  or  $\pm 5 \text{ V}$ , and using two dual op amps instead of one quad op amp. If the extremely low voltage noise and high gain bandwidth is not required, using other quad op amps, such as [ADA4091-4](#), [OP4177](#), [ADA4004-4](#), [OP497](#), or [AD704](#) can be considered.

### UNITY-GAIN FOLLOWER APPLICATIONS

When large transient pulses ( $>1 \text{ V}$ ) are applied at the positive terminal of amplifiers (such as the OP27, LT1007, OPA227, and AD8671) with back-to-back diodes at the input stage, the use of a resistor in the feedback loop is recommended to avoid having the amplifier load the signal generator. The feedback resistor,  $R_F$ , should be at least  $500 \text{ }\Omega$ . However, if large values must be used for  $R_F$ , a small capacitor,  $C_F$ , should be inserted in parallel with  $R_F$  to compensate for the pole introduced by the input capacitance and  $R_F$ .

Figure 30 shows the uncompensated output response with a  $10 \text{ k}\Omega$  resistor in the feedback and the compensated response with  $C_F = 15 \text{ pF}$ .

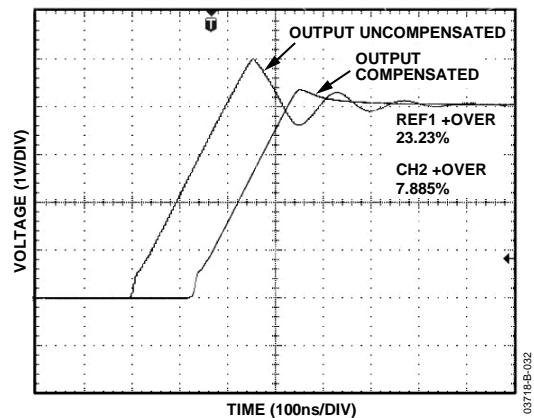


Figure 30. Transient Output Response

## OUTPUT PHASE REVERSAL

Phase reversal is a change of polarity in the amplifier transfer function that occurs when the input voltage exceeds the supply voltage. The AD8671/AD8672/AD8674 do not exhibit phase reversal even when the input voltage is 1 V beyond the supplies.

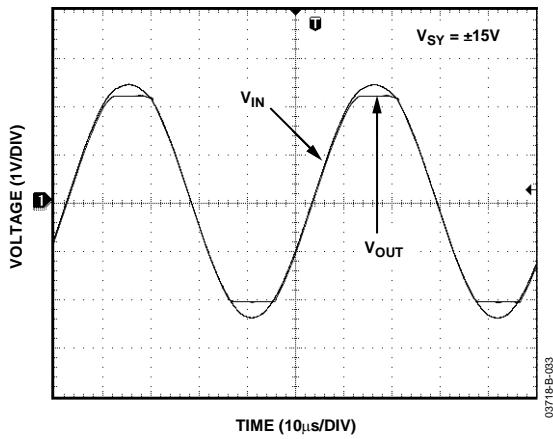


Figure 31. Output Phase Reversal

## TOTAL NOISE VS. SOURCE RESISTANCE

The low input voltage noise of the AD8671/AD8672/AD8674 makes them a great choice for applications with low source resistance. However, because they have low input current noise, they can also be used in circuits with substantial source resistance.

Figure 32 shows the voltage noise, current noise, thermal noise, and total rms noise of the AD8671 as a function of the source resistance.

For  $R_s < 475 \Omega$ , the input voltage noise,  $e_n$ , dominates.

For  $475 \Omega < R_s < 412 \text{ k}\Omega$ , thermal noise dominates.

For  $R_s > 412 \text{ k}\Omega$ , the input current noise dominates.

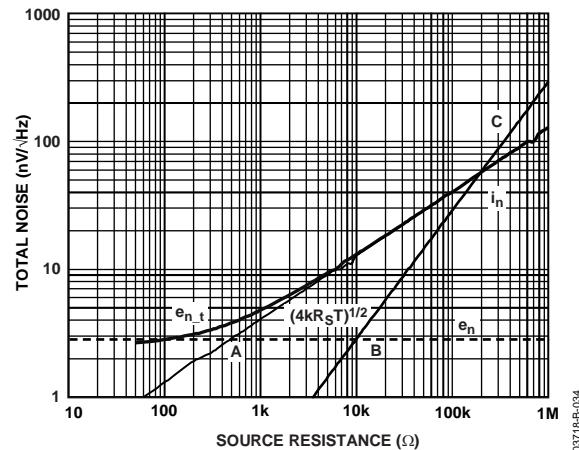


Figure 32. Noise vs. Source Resistance

## TOTAL HARMONIC DISTORTION (THD) AND NOISE

The AD8671/AD8672/AD8674 exhibit low total harmonic distortion (THD) over the entire audio frequency range. This makes them suitable for applications with high closed-loop gains, including audio applications. Figure 33 shows approximately 0.0006% of THD + N in a positive unity gain, the worst-case configuration for distortion.

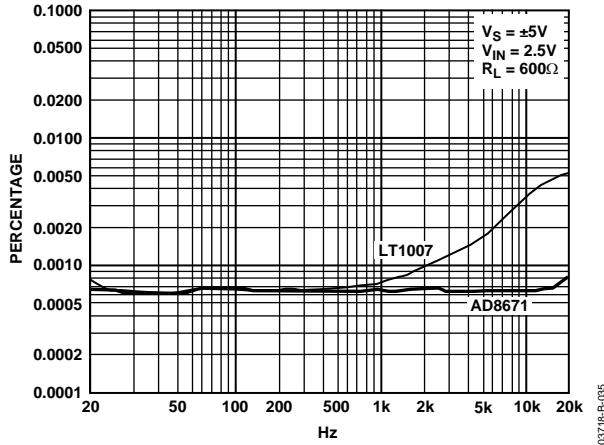


Figure 33. Total Harmonic Distortion and Noise

## DRIVING CAPACITIVE LOADS

The AD8671/AD8672/AD8674 can drive large capacitive loads without causing instability. However, when configured in unity gain, driving very large loads can cause unwanted ringing or instability.

Figure 34 shows the output of the AD8671 with a capacitive load of 1 nF. If heavier loads are used in low closed-loop gain or unity-gain configurations, it is recommended to use external compensation as shown in the circuit in Figure 35. This technique reduces the overshoot and prevents the op amp from oscillation. The trade-off of this circuit is a reduction in output swing. However, a great added benefit stems from the fact that the input signal and the op amp's noise are filtered, and thus the overall output noise is kept to a minimum.

The output response of the circuit is shown in Figure 36.

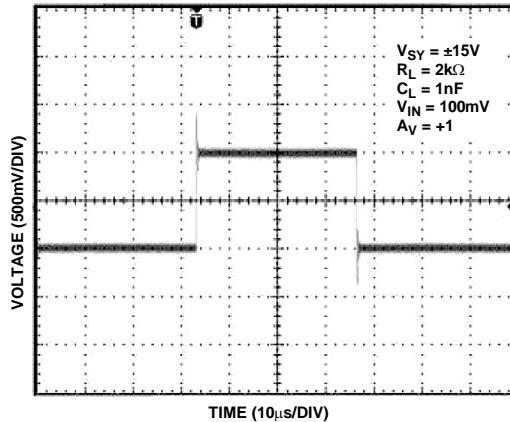


Figure 34. AD8671 Capacitive Load Drive

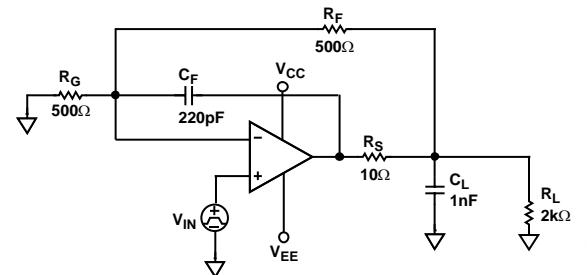


Figure 35. Recommended Capacitive Load Circuit

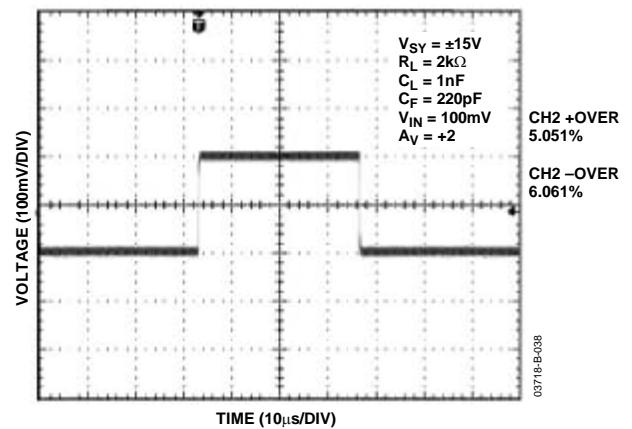


Figure 36. Compensated Load Drive

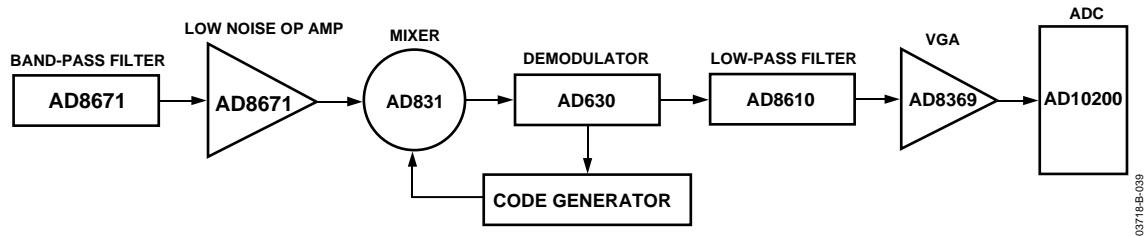


Figure 37. Simplified Block Diagram of a GPS Receiver

## GPS RECEIVER

GPS receivers require low noise to minimize RF effects. The precision of the AD8671 makes it an excellent choice for such applications. Its very low noise and wide bandwidth make it suitable for band-pass and low-pass filters without the penalty of high power consumption.

Figure 37 shows a simplified block diagram of a GPS receiver. The next section details the design equations.

## BAND-PASS FILTER

Filters are useful in many applications; for example, band-pass filters are used in GPS systems, as discussed in the previous section. Figure 38 shows a second-order band-pass KRC filter.

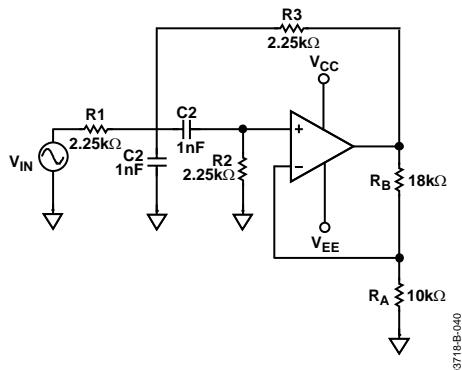


Figure 38. Band-Pass KRC Filter

The equal component topology yields a center frequency

$$f_0 = \frac{\sqrt{2}}{2\pi RC}$$

$$\text{and } Q = \frac{\sqrt{2}}{4 - K}$$

where:

$$K = 1 + \frac{R_B}{R_A}$$

The band-pass response is shown in Figure 39.

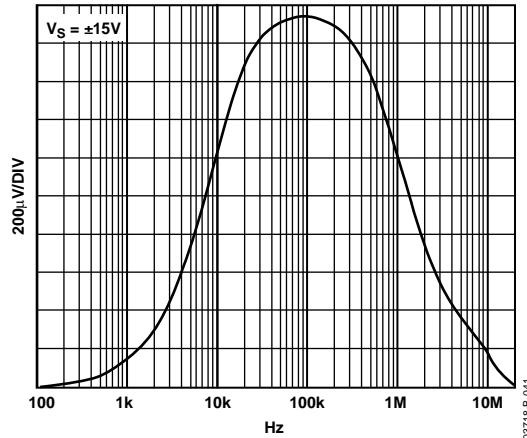


Figure 39. Band-Pass Response

## PLL SYNTHESIZERS AND LOOP FILTERS

Phase-lock loop filters are used in AM/FM modulation.

Loop filters in PLL design require accuracy and care in their implementation. The AD8671/AD8672/AD8674 are ideal candidates for such filter design; the low offset voltage and low input bias current minimize the output error. In addition to the excellent dc specifications, the AD8671/AD8672/AD8674 have a unique performance at high frequencies; the high open-loop gain and wide bandwidth allow the user to design a filter with a high closed-loop gain if desirable. To optimize the filter design, it is recommended to use small value resistors to minimize the thermal noise. A simple example is shown in Figure 40.

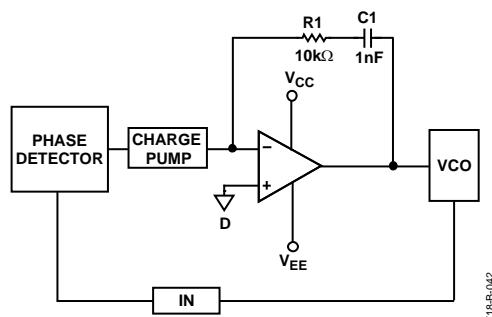
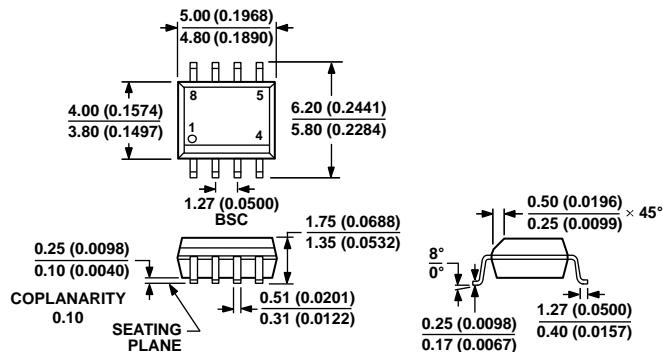


Figure 40. PLL Filter Simplified Block Diagram

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

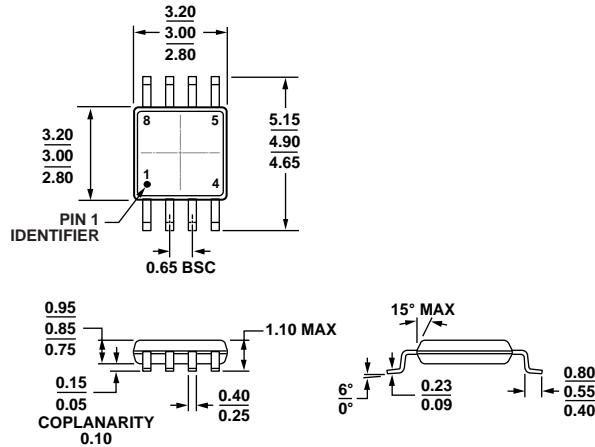
012407-A

Figure 41. 8-Lead Standard Small Outline Package [SOIC\_N]

Narrow Body

(R-8)

Dimensions shown in millimeters and (inches)



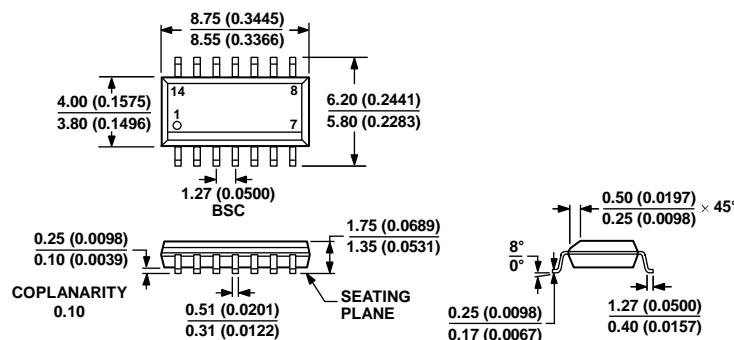
COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 42. 8-Lead Mini Small Outline Package [MSOP]

(RM-8)

Dimensions shown in millimeters

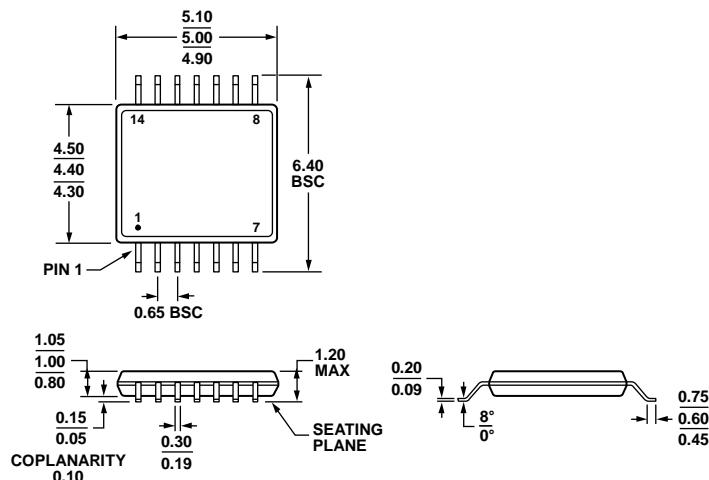
10-07-2009-B



COMPLIANT TO JEDEC STANDARDS MS-012-AB  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 43. 14-Lead Standard Small Outline Package [SOIC\_N]  
 Narrow Body  
 (R-14)  
 Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1  
 Figure 44. 14-Lead Thin Shrink Small Outline Package [TSSOP]  
 (RU-14)  
 Dimensions shown in millimeters

061908-A

**ORDERING GUIDE**

<b>Model<sup>1</sup></b>	<b>Temperature Range</b>	<b>Package Description</b>	<b>Package Option</b>	<b>Branding</b>
AD8671ARZ	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8671ARZ-REEL	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8671ARZ-REEL7	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8671ARMZ	-40°C to +125°C	8-Lead MSOP	RM-8	A0V
AD8671ARMZ-REEL	-40°C to +125°C	8-Lead MSOP	RM-8	A0V
AD8672AR	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8672AR-REEL	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8672AR-REEL7	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8672ARZ	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8672ARZ-REEL	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8672ARZ-REEL7	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8672ARMZ	-40°C to +125°C	8-Lead MSOP	RM-8	A0W
AD8672ARMZ-REEL	-40°C to +125°C	8-Lead MSOP	RM-8	A0W
AD8674ARZ	-40°C to +85°C	14-Lead SOIC_N	R-14	
AD8674ARZ-REEL	-40°C to +85°C	14-Lead SOIC_N	R-14	
AD8674ARZ-REEL7	-40°C to +85°C	14-Lead SOIC_N	R-14	
AD8674ARU	-40°C to +85°C	14-Lead TSSOP	RU-14	
AD8674ARUZ	-40°C to +85°C	14-Lead TSSOP	RU-14	
AD8674ARUZ-REEL	-40°C to +85°C	14-Lead TSSOP	RU-14	

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**

**NOTES**

**NOTES**