Sheffield Hallam University
Semester I of academic year 2021/22

"SoC architectures and FPGA prototyping"

Lab 1 -
Combinational digital design using structural and behavioural Verilog

Assignment 1:

Open the project from the folder Lab_1_1

Follow the Lab1cast in order to implement the same design as in the Lab0 using the project template in the following ways

- Behavioural like in Lab 0;
- Structural like in lecture 2;
- Structural with a single XOR gate;
- Behavioural with a single XOR operation.

Take a screenshot of your HDL code and the resource utilisation screenshot (as circled in the example Fig.1 below) for the lab report.

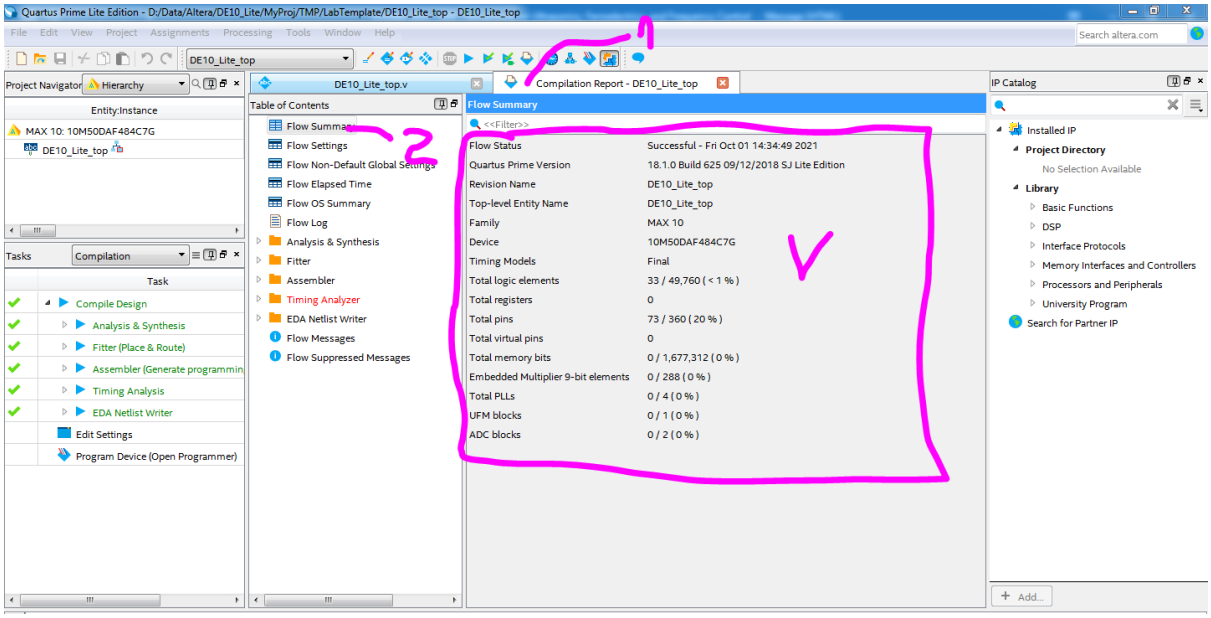

Figure 1. Example for a screenshot with resource utilisation

Introduction to the assignments 2 (structural Verilog) and 3 (behavioural Verilog):

For the a.m. assignments you are going to design in Verilog and implement using your DE10-Lite FPGA board the following combinational digital circuit (Fig.2) using the on-board hardware (Fig.3).

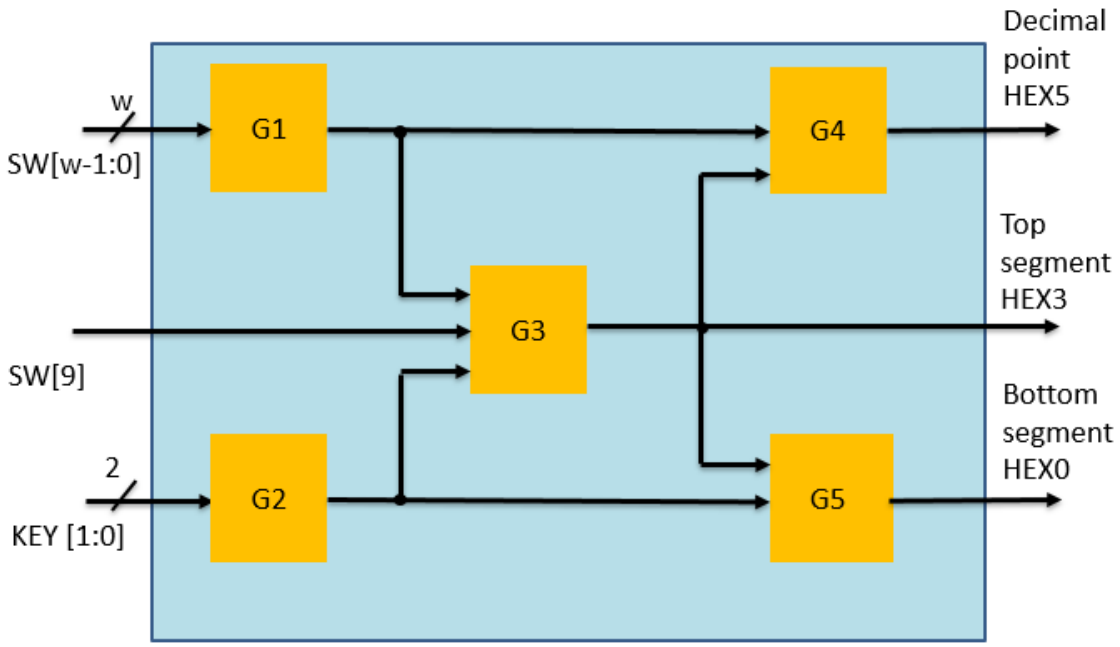

Figure 2. Digital design to implement
(value of w and types of the five gates depend on your student ID number)

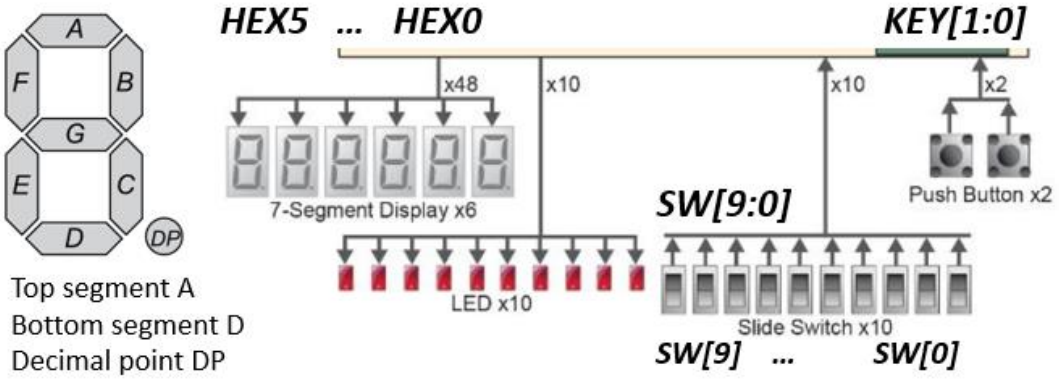

Figure 3. On board hardware used for the design

The input data to the circuit will be set by the on-board slide switches and push buttons; the output data will be displayed by the on board seven segment displays. Please use the template project to find out which bits of HEX drive the required segments.

Your particular design will depend on your seven-digit student ID number, here ABCDEFG, as follows:

- width of the input and output data w, bits:

G	0	1	2	3	4	5	6	7	8	9
w	2	3	4	5	2	3	4	5	2	3

- ***bitwise*** operations to implement

F	0	1	2	3	4	5	6	7	8	9
G1	AND	AND	NAND	NAND	OR	OR	NOR	NOR	XOR	XNOR
G2	NOR	XNOR	OR	XOR	NAND	XNOR	AND	XOR	NAND	OR

- ***bitwise*** operations to implement

E	0	1	2	3	4	5	6	7	8	9
G3	AND	AND	NAND	NAND	OR	OR	NOR	NOR	AND	NAND
G4	NOR	XNOR	OR	XOR	NAND	XNOR	AND	XOR	NAND	OR
G5	XNOR	AND	XOR	NAND	OR	NOR	XNOR	OR	XOR	NAND

For example, the students with ID number 1234567 will use

- width of the data ***w*** = 5 bits;
- operations NOR (for G1) and AND (for G2);
- operations OR (for G3), XNOR (for G4) and NOR (for G5).

The seven segment LEDs are controlled by 8 bits data as shown below for each segment DP_G_F_E_D_C_B_A

1 is to switch the segment OFF and 0 to get it ON.

Here are the expressions you need to use for the schematic diagram shown in Fig.2:

Decimal point HEX5: HEX5[7] // 7th bit of HEX5

Top segment HEX3: HEX3[0] // 0th bit of HEX3

Bottom segment HEX0: HEX0[3] // 3rd bit of HEX0

Assignment 2 (structural Verilog):

Using the PPT file provided, create your personalised circuit and take a screenshot.

First recall what is the truth table and complete your truth table assuming that all the inputs to the gate G1 are set high (logical 1). Complete the output column of the table 1.

Table 1. The truth table - fill in only one output column of your choice

INPUTS			***OUTPUTS***
SW[9]	***KEY[1]***	***KEY[0]***	***HEX3[0]***
0	***0***	***0***	
0	***0***	***1***	
…	***…***	***…***	

Hint: your table will need 8 rows of data

Open the project from the folder Lab_1_2

Develop and debug the structural Verilog code for the design. Take a screenshot of the developed code for the report.

Put all the slide switches in the top position and leave the push buttons depressed. Take a photograph of the board's LED and HEXes for the report.

Check operation of your design using the truth table.

Remember that, if logic 1 is supplied to a segment, it will be OFF because of the way the HEXes are wired on board; and when a KEY is depressed it reads 1.

Take a screenshot of the resource utilisation for the report.

Assignment 3 (behavioural Verilog):

Copy the folder Lab_1_2 to the same folder and rename new folder to Lab_1_3. Open the project from the renamed folder. Develop and debug the behavioural Verilog code for the design.

Make sure you use the reduction Verilog operator for the G1 and G2 – this is the requirement for this assignment.

Take a screenshot of the developed code for the report.

Take a screenshot of the resource utilisation for the report.

Report for the lab 1: answer questions at the end of the report template for the lab 1.