HighRISCHighReward

Roadmap for CP 2 (Submitted with CP1)

Feature	**Feature Description**	**Design Assigned To**
Hazard Detection & Forwarding	Data needs to be forwarded between stages in the pipeline: from the EX/MEM and MEM/WB registers to the EX stage in order to reduce stalls for data hazards. To address control hazards, we will need to add forwarding paths into our decode stage as well, since our branches are resolved there. Stalls will need to be implemented, for read-after-load hazards, as well as when the registers to be compared for a branch are not read (Branch after ALU op or Branch after load hazard)	Calvin
Static non-taken branch prediction	Static non-taken branch prediction: always predict that branch is not taken, i.e fetch original PC+4 instruction in ‘delay slot’. If the branch is found to have been taken in decode state, then make the next instruction a no-op and route the correct target address to PC.	Mandy
L1 split caches (single cycle hit)	Should implement single-cycle-hit split instruction cache and data cache. May need to stall future pipeline stages on a cache miss	Ayush
Arbiter	Determines order in which to pass requests to memory. When only one request is made, then the request is passed along. When the arbiter receives multiple	Ayush

	requests, then the order in which the requests are passed to memory are decided by the **arbitration rules.**	