HighRISCHighReward

Roadmap for CP 3 (Submitted with CP2)

Feature	**Feature Description**	**Design Assigned To**
Pipelined L1 caches[6]	This cache is implemented so that cache can be read/write to the I cache and D cache in parallel.	Mandy
L2+ cache system [2]	It is a unified cache at the lower level than I cache and D cache, and has an upper level hierarchy than physical memory.	Ayush
4-Way Set Associative Cache [2]	It is also an unified cache that uses pseudo-LRU algorithm to evict the cache line in corresponding way. We are implementing this cache on our L2 cache.	Mandy
4-way set associative or higher BTB [3]	The Branch target buffer is implemented using 4-way set associative which has 4 ways and 16 sets.	Ayush
Parameterized Cache (extra credit)	A x-way set-associative cache is implemented where we can change the number of ways, number of sets to achieve better performance.	Mandy
Local branch history table [2]	There is a Branch Target Buffer that uses PC as index and generates target address as output. There are also Branch History Table that is indexed by PC, which outputs history to index the Predict History Table that outputs the local Predict bit. After the decode stage, BTB, BHT and PHT are updated.	Calvin

Global 2-level branch history table [3]	There is a GHR that is a shift register which is used to index the global PHT. The output of PHT is used as global predict bit. The GHR and PHT is updated in decode stage after br_en bit is generated. Also, the BTB is updated.	Calvin
Branch target buffer, support for jumps [1]	It is a buffer that is indexed by PC bits and output target address and whether is is op_br, op_jal or op_jalr.	Ayush
Tournament branch predictor [5]	We combine our local branch history table and global 2-level branch history table and use selection buffer to select the MUX. This buffer is updated depending on decode stage br_en, local and global prediction.	Calvin