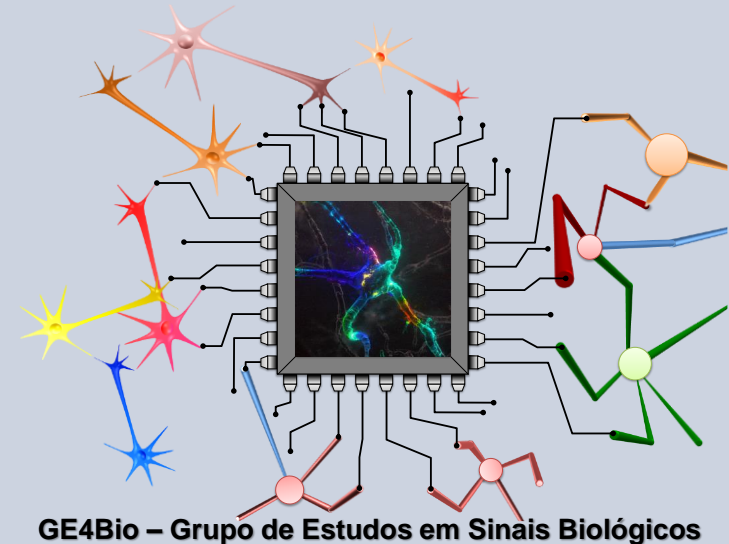


Universidade de São Paulo  
Instituto de Ciências Matemáticas e de Computação  
Departamento de Sistemas de Computação

**SSC512**  
**Elementos de Lógica Digital**

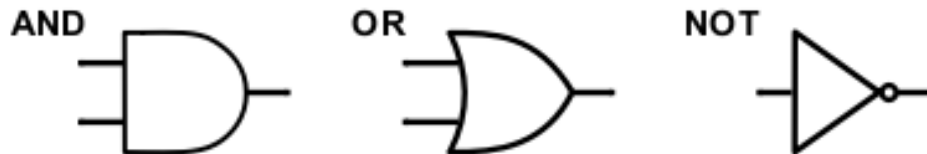
**Tutorial Configuração**  
**Quartus**



**Prof.Dr. Danilo Spatti**

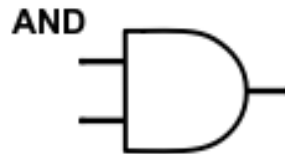
**São Carlos - 2018**

- A Álgebra de Boole pode ser **desenvolvida** a partir de **símbolos** pré-definidos, **tabela de funcionamento (verdade)** e **equações lógicas**.
- As ditas operações lógicas **primitivas** são formadas por **AND**, **OR** e **NOT**, sendo as demais derivadas a partir destas.



- Resulta em **verdadeira** se, e somente se, **todas** as proposições forem verdadeiras.
- A operação AND (E) é dita **conjunção** ou também **produto lógico** e é representada pela conectiva “.” (ponto).

$$S(a, b) = a \cdot b$$



<i>a</i>	<i>b</i>	<i>S</i>
0	0	0
0	1	0
1	0	0
1	1	1

Quartus II 64-Bit

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Compilation Hierarchy

Hierarchy Files Design UI

Tasks

Flow: Compilation Customize...

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate programming file)
  - TimeQuest Timing Analysis
  - EDA Netlist Writer
- Program Device (Open Programmer)

Tools

- Run Simulation Tool
- Launch Simulation Library Compiler
- Launch Design Space Explorer II
- TimeQuest Timing Analyzer
- Advisors
- Chip Planner
- Design Partition Planner
- Netlist Viewers
- SignalTap II Logic Analyzer
- In-System Memory Content Editor
- Logic Analyzer Interface Editor
- In-System Sources and Probes Editor
- SignalProbe Pins...
- Programmer
- JTAG Chain Debugger
- Fault Injection Debugger
- System Debugging Tools
- IP Catalog
- Nios II Software Build Tools for Eclipse
- Qsys
- Td Scripts...
- Customize...
- Options...
- License Setup...**
- Install Devices...

License Setup...

IP Catalog

Device Family: Cyclone IV GX

Installed IP

- Project Directory
  - No Selection Available
- Library
  - Basic Functions
  - DSP
  - Interface Protocols
  - Memory Interfaces and C
  - Processors and Periphera
- Search for Partner IP

Web vs Subscription Edition

Buy Software

Documentation

Training

Support

What's New

Notification Center

Close page after project load

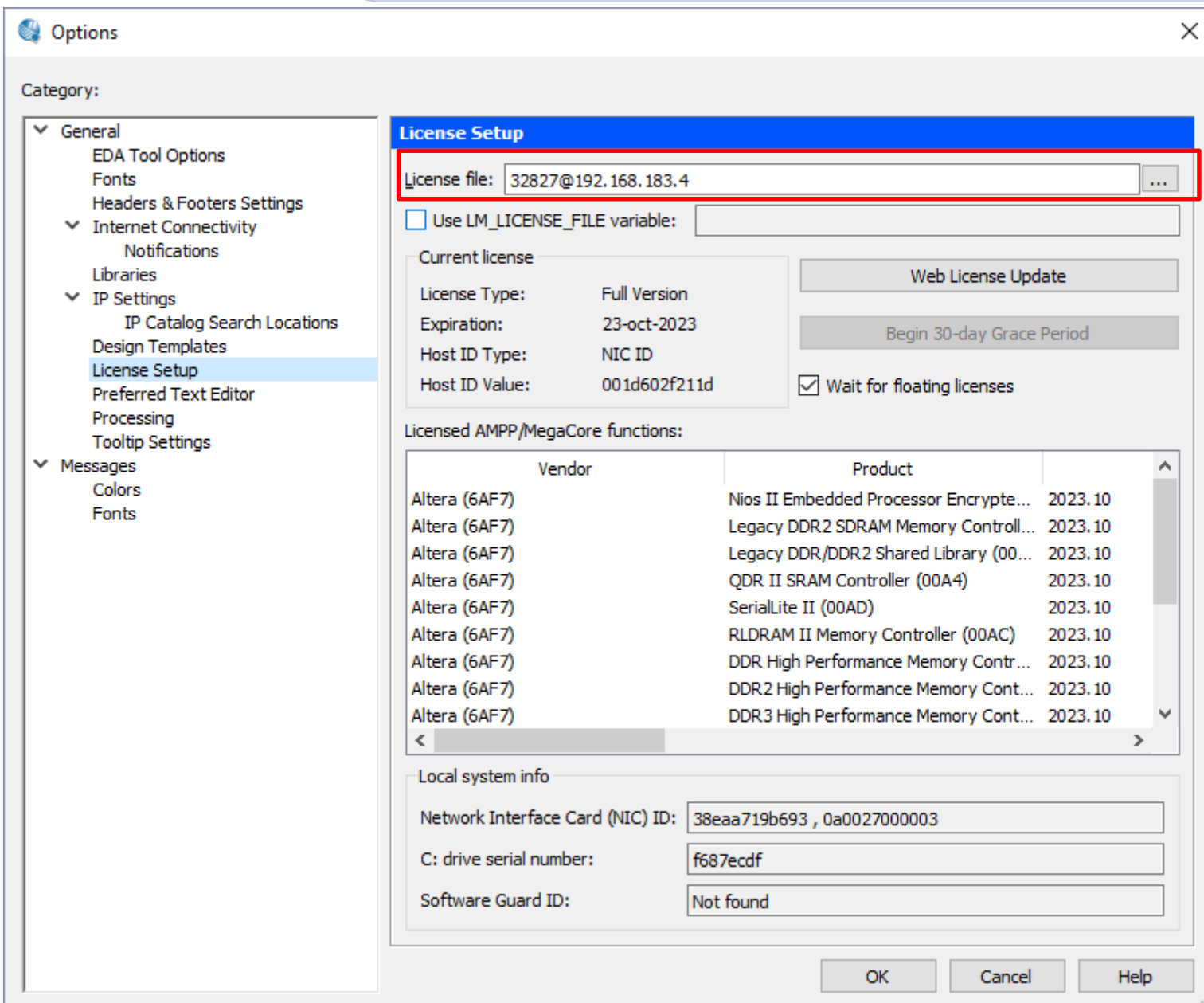
Messages

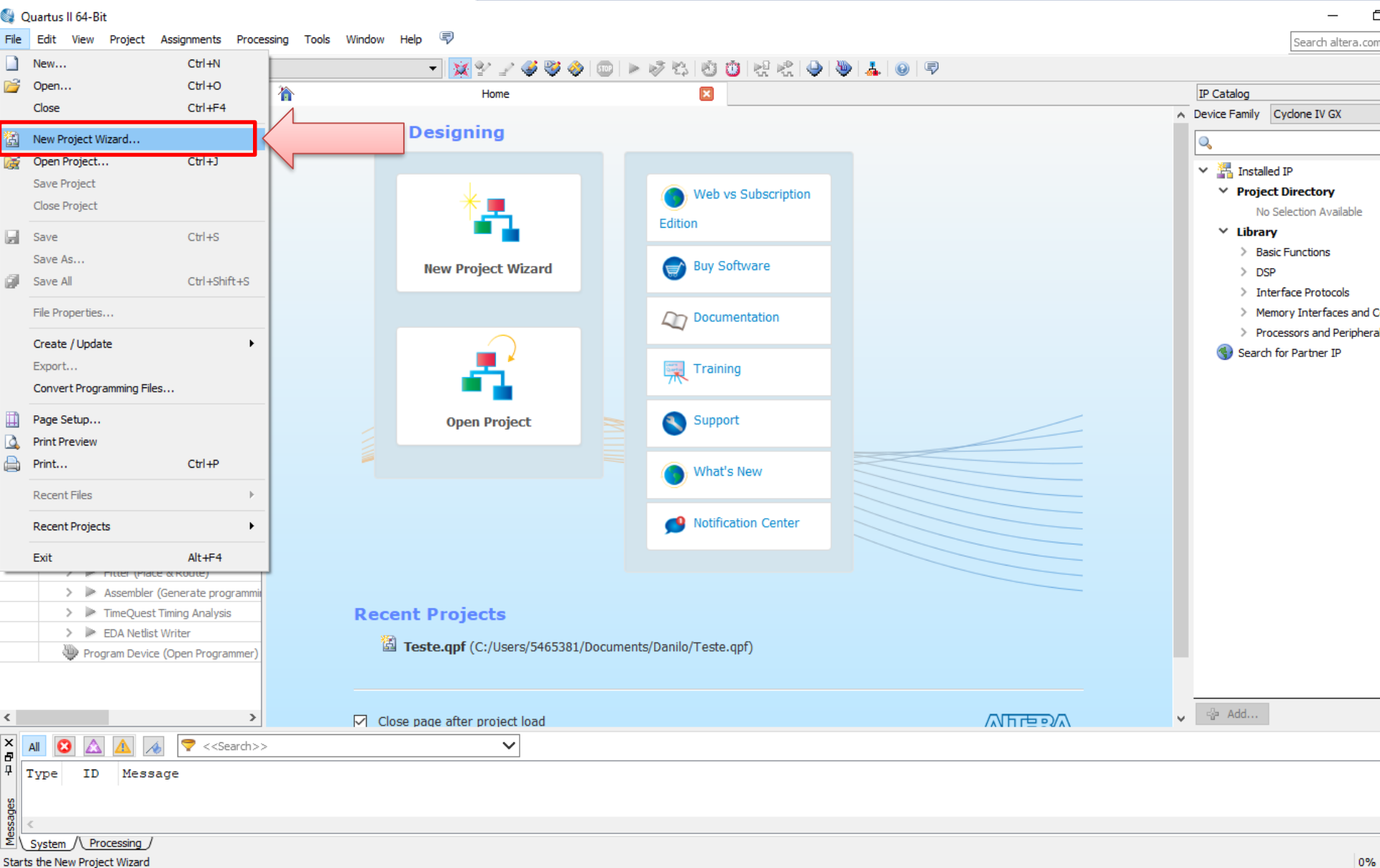
System Processing

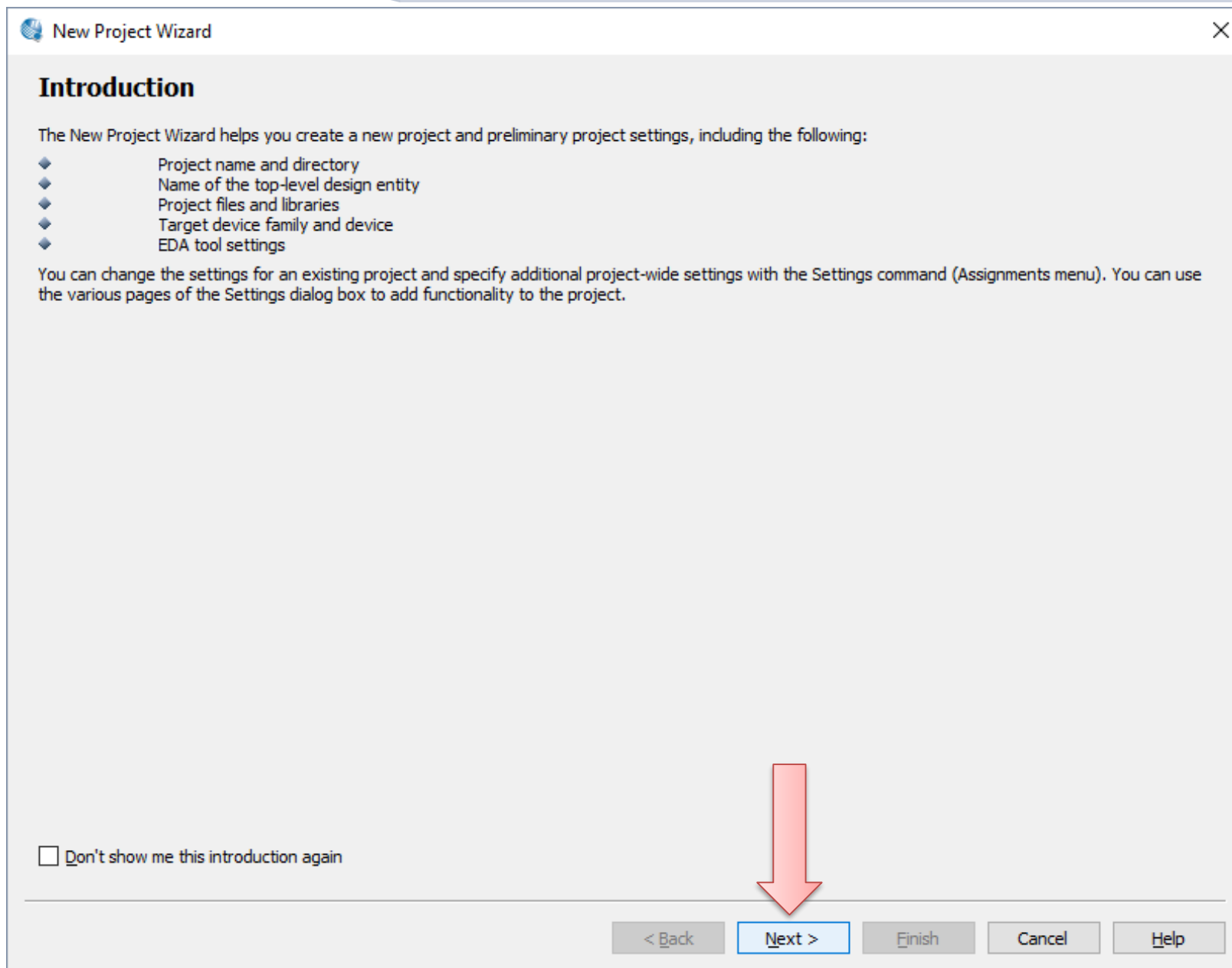
Sets up user licensing

Digite aqui para pesquisar

15:55 12/03/20







New Project Wizard

**Directory, Name, Top-Level Entity**

What is the working directory for this project?

C:/Users/5465381/Documents/Spatti

What is the name of this project?

PortaAND

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

PortaAND

Use Existing Project Settings...

Crie uma pasta com nomes curtos, sem espaços, fora da área de disco do Quartus

Crie um nome para o projeto também contendo nomes curtos e sem caracteres especiais

< Back Next > Finish Cancel Help



New Project Wizard

**Project Type**

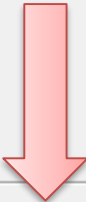
Select the type of project to create.

☒ Empty project

Create new project by specifying project files and libraries, target device family and device, and EDA tool settings.

☐ Project template

Create a project from an existing design template. You can choose from design templates installed with the Quartus II software, or download design templates from the [Design Store](#).



< Back   **Next >**   Finish   Cancel   Help

New Project Wizard

Add Files

Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project.  
Note: you can always add design files to the project later.

File name:

File Name	Type	Library	Design Entry/Synthesis Tool	HDL Version
-----------	------	---------	-----------------------------	-------------

Add

Add All

Remove

Up

Down

Properties

Specify the path names of any non-default libraries.

< Back

Next >

Finish

Cancel

Help


New Project Wizard


### Family & Device Settings

Select the family and device you want to target for compilation.  
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus II software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: Cyclone V (E/GX/GT/SX/SE/ST) 

Devices: All 


Target device


☐ Auto device selected by the Fitter


☒ Specific device selected in 'Available devices' list


☐ Other: n/a

Show in 'Available devices' list

Package: Any 

Pin count: Any 

Core Speed grade: Any 

Name filter: 5CEBA4F23C7 

☒ Show advanced devices

Available devices:

Name	Core Voltage	ALMs	User I/Os	GXB Channel PMA	GXB Channel PCS	PCIe Hard IP Blocks	M
5CEBA4F23C7	1.1V	18480	224	0	0	0	0

Em Name Filter digite 5CEBA4F23C7

< Back Next > Finish Cancel Help

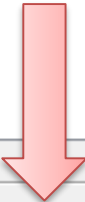
New Project Wizard

EDA Tool Settings

Specify the other EDA tools used with the Quartus II software to develop your project.

EDA tools:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synthesis	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	ModelSim-Altera	VHDL	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Formal Verification	<None>		
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	



< Back

Next >

Finish

Cancel

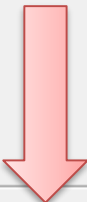
Help

New Project Wizard

**Summary**

When you click Finish, the project will be created with the following settings:

Project directory:	C:/Users/5465381/Documents/Spatti
Project name:	PortaAND
Top-level design entity:	PortaAND
Number of files added:	0
Number of user libraries added:	0
Device assignments:	
Design template:	n/a
Family name:	Cyclone V (E/GX/GT/SX/SE/ST)
Device:	5CEBA4F23C7
EDA tools:	
Design entry/synthesis:	<None> (<None>)
Simulation:	ModelSim-Altera (VHDL)
Timing analysis:	0
Operating conditions:	
Core voltage:	1.1V
Junction temperature range:	0-85 °C



< Back   Next >   **Finish**   Cancel   Help

Quartus II 64-Bit - C:/Users/5465381/Documents/Spatti/PortaAND - PortaAND

File Edit View Project Assignments Processing Tools Window Help

New... Ctrl+N

Open... Ctrl+O

Close Ctrl+F4

New Project Wizard...

Open Project... Ctrl+J

Save Project

Close Project

Save Ctrl+S

Save As...

Save All Ctrl+Shift+S

File Properties...

Create / Update

Export...

Convert Programming Files...

Page Setup...

Print Preview

Print... Ctrl+P

Recent Files

Recent Projects

Exit Alt+F4

Filter (Place & Route)

Assembler (Generate programming files)

TimeQuest Timing Analysis

EDA Netlist Writer

Program Device (Open Programmer)

ALTERA®

QUARTUS® II

Version 14.1

View Quartus II Information

Documentation

Notification Center

IP Catalog

Installed IP

Project Directory

No Selection Available

Library

Basic Functions

DSP

Interface Protocols

Memory Interfaces and C

Processors and Periphera

Search for Partner IP

Add...

Messages

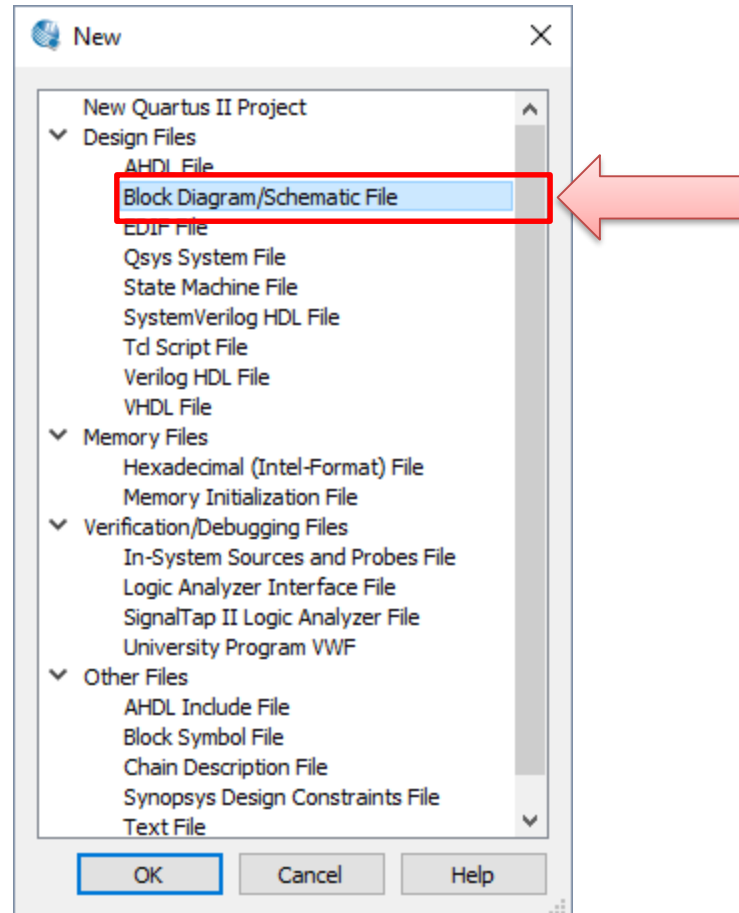
System Processing

Creates a new file

0%

16:00

12/03/20



Quartus II 64-Bit - C:/Users/5465381/Documents/Spatti/PortaAND - PortaAND

File Edit View Project Assignments Processing Tools Window Help

PortaAND

Block1.bdf

Project Navigator

Entity

Cyclone V: 5CEBA4F23C7

PortaAND

Hierarchy Files Design UI

Tasks

Flow: Compilation Customize...

Task

Compile Design

Analysis & Synthesis

Fitter (Place & Route)

Assembler (Generate programming file)

TimeQuest Timing Analysis

EDA Netlist Writer

Program Device (Open Programmer)

Symbol

Libraries:

primitives

buffer

logic

and12

and2

and3

and4

and6

and8

band12

Name:

and2

Repeat-insert mode

Insert symbol as block

OK Cancel

IP Catalog

Installed IP

Project Directory

No Selection Available

Library

Basic Functions

DSP

Interface Protocols

Memory Interfaces and Controllers

Processors and Peripherals

Search for Partner IP

Messages

Type ID Message

System Processing

136,0 0%

16:01 12/03/2020

Windows Taskbar



Quartus II 64-Bit - C:/Users/5465381/Documents/Spatti/PortaAND - PortaAND

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Entity

Cyclone V: 5CEBA4F23C7

PortaAND

Hierarchy Files Design UI

Tasks

Flow: Compilation Customize...

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate programming file)
  - TimeQuest Timing Analysis
  - EDA Netlist Writer
- Program Device (Open Programmer)

Block Library

Input

Output

Bidir

AND2

inst

IP Catalog

Installed IP

Project Directory

No Selection Available

Library

- Basic Functions
- DSP
- Interface Protocols
- Memory Interfaces and C
- Processors and Periphera

Search for Partner IP

Add...

Messages

All

Type ID Message

System Processing



Quartus II 64-Bit - C:/Users/5465381/Documents/Spatti/PortaAND - PortaAND

File Edit View Project Assignments Processing Tools Window Help

PortaAND

Project Navigator

Entity

Salvar como

Salvar em: Spatti

Nome	Data de modificaç...	Tipo	Tam
db	12/03/2018 15:59	Pasta de arquivos	

Nome: PortaAND

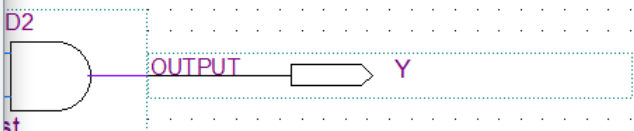
Tipo: Block Diagram/Schematic Files (\*.bdf)

☒ Add file to current project

Salvar

Cancelar

Block1.bdf\*



IP Catalog

Installed IP

Project Directory

No Selection Available

Library

Basic Functions

DSP

Interface Protocols

Memory Interfaces and C

Processors and Periphera

Search for Partner IP

Program Device (Open Programmer)

Messages

System Processing

185, 147 0%

16:03 12/03/20

Quartus II 64-Bit - C:/Users/5465381/Documents/Spatti/PortaAND - PortaAND

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Entity

Cyclone V: SCEBA4F23C7

PortaAND

Start Compilation Ctrl+L

Analyze Current File

Start

Update Memory Initialization File

Compilation Report Ctrl+R

Dynamic Synthesis Report

PowerPlay Power Analyzer Tool

SSN Analyzer Tool

Receive Compilation Status Notifications

IP Catalog

Installed IP

Project Directory

No Selection Available

Library

Basic Functions

DSP

Interface Protocols

Memory Interfaces and C

Processors and Periphera

Search for Partner IP

Hierarchy Files Design UI

Tasks

Flow: Compilation Customize...

Task

Compile Design

Analysis & Synthesis

Fitter (Place & Route)

Assembler (Generate programmi

TimeQuest Timing Analysis

EDA Netlist Writer

Program Device (Open Programmer)

AND2

inst

INPUT VCC

INPUT VCC

OUTPUT

Y

Messages

System Processing

Starts a new compilation

194, 152 0%

16:04

12/03/20

Quartus II 64-Bit - C:/Users/5465381/Documents/Spatti/PortaAND - PortaAND

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

PortaAND

Project Navigator

Entity

Cyclone V: 5CEBA4F23C7

PortaAND

Hierarchy Files Design UI

Tasks

Flow: Compilation Customize...

Task

20% Compile Design

Analysis & Synthesis

0% Fitter (Place & Route)

0% Assembler (Generate programming file)

0% TimeQuest Timing Analysis

0% EDA Netlist Writer

Program Device (Open Programmer)

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Flow Settings

Flow Non-Default Global Settings

Flow Elapsed Time

Flow OS Summary

Flow Log

Analysis & Synthesis

Flow Messages

Flow Suppressed Messages

Flow Summary

Flow Status

Quartus II 64-Bit Version

Revision Name

Top-level Entity Name

Family

Device

Timing Models

Logic utilization (in ALMs)

Total registers

Total pins

Total virtual pins

Total block memory bits

Total DSP Blocks

Total HSSI RX PCSs

Total HSSI PMA RX Deserializers

Total HSSI TX PCSs

Total HSSI PMA TX Serializers

Total PLLs

Total DLLs

Successful - Mon Mar 12 16:05:45 2018

14.1.0 Build 186 12/03/2014 SJ Web Edition

PortaAND

PortaAND

Cyclone V

5CEBA4F23C7

Final

N/A

0

3

0

0

0

0

0

0

0

0

0

0

0

0

0

0

0

0

IP Catalog

Installed IP

Project Directory

No Selection Available

Library

Basic Functions

DSP

Interface Protocols

Memory Interfaces and C

Processors and Periphera

Search for Partner IP

Add...

Messages

Type ID Message

Quartus II 64-Bit Analysis & Synthesis was successful. 0 errors, 0 warnings

System Processing (10)

Quartus II 64-Bit - C:/Users/5465381/Documents/Spatti/PortaAND - PortaAND

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Entity

Cyclone V: 5CEBA4F23C7

PortaAND

Assignments

- Device...
- Settings... Ctrl+Shift+E
- Assignment Editor Ctrl+Shift+A
- Pin Planner Ctrl+Shift+N**
- Remove Assignments...
- Back-Annotate Assignments...
- Import Assignments...
- Export Assignments...
- Assignment Groups...
- LogicLock Regions Window Alt+L
- Design Partitions Window Alt+D

TimeQuest Timing Analyzer

EDA Netlist Writer

Flow Messages

Flow Suppressed Messages

Tasks

Flow: Compilation Customize...

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate programming file)
- TimeQuest Timing Analysis
- EDA Netlist Writer
- Program Device (Open Programmer)

Messages

Type ID Message

293000 Quartus II Full Compilation was successful. 0 errors, 10 warnings

System Processing (126)

Edits pin assignments

Compilation Report - PortaAND

Flow Summary

Successful - Mon Mar 12 16:08:59 2018

14.1.0 Build 186 12/03/2014 SJ Web Edition

Revision Name	PortaAND
Top-level Entity Name	PortaAND
Family	Cyclone V
Device	5CEBA4F23C7
Timing Models	Final
Logic utilization (in ALMs)	1 / 18,480 (< 1 %)
Total registers	0
Total pins	3 / 224 (1 %)
Total virtual pins	0
Total block memory bits	0 / 3,153,920 (0 %)
Total DSP Blocks	0 / 66 (0 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 4 (0 %)
Total DLLs	0 / 4 (0 %)

IP Catalog

Installed IP

Project Directory

No Selection Available

Library

- Basic Functions
- DSP
- Interface Protocols
- Memory Interfaces and C
- Processors and Periphera

Search for Partner IP

Add...

184, 147 100%

16:09 12/03/20

Report

Report not available

Groups Report

Tasks

Early Pin Planning

Early Pin Planning...

Run I/O Assignment Analysis

Export Pin Assignments...

Pin Finder...

Highlight Pins

I/O Banks

VREF Groups

Edges

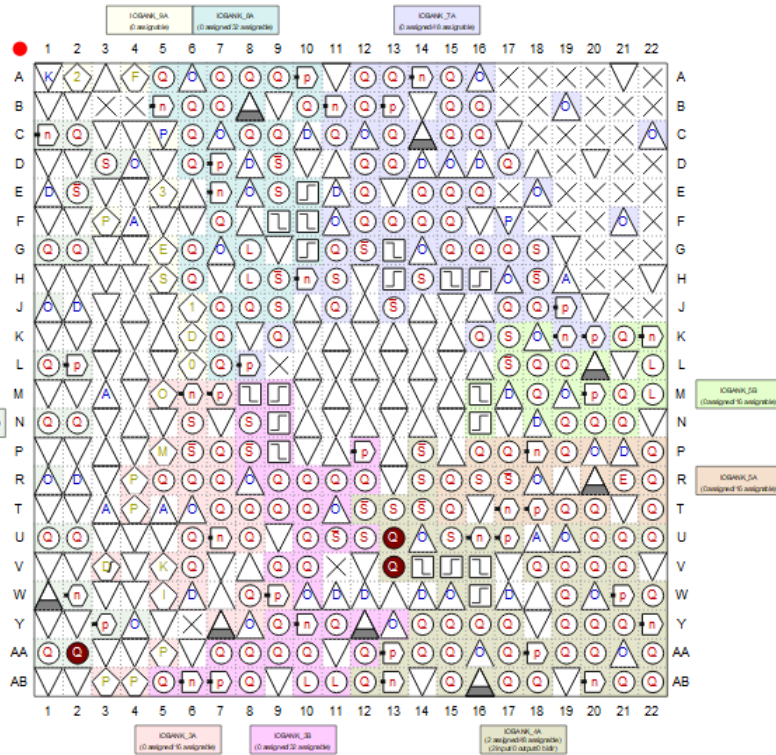
Clock Pins

Clock

PLL/DLL Input

Top View - Wire Bond

Cyclone V - 5CEBA4F23C7



Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	ver Analog Settings	_GXB/VCCT_G
A	Input	PIN_U13		N0	PIN_L17	2.5 V (default)		12mA (default)				
B	Input	PIN_V13		N0	PIN_K17	2.5 V (default)		12mA (default)				
Y	Output	PIN_AA2		B2A_N0	PIN_M21	2.5 V (default)		12mA (default)	1 (default)			
<<new node>>												



Table 3-3 Pin Assignment of Slide Switches

Signal Name	FPGA Pin No.	Description
SW0	PIN_U13	Slide Switch[0]
SW1	PIN_V13	Slide Switch[1]
SW2	PIN_T13	Slide Switch[2]
SW3	PIN_T12	Slide Switch[3]
SW4	PIN_AA15	Slide Switch[4]
SW5	PIN_AB15	Slide Switch[5]
SW6	PIN_AA14	Slide Switch[6]
SW7	PIN_AA13	Slide Switch[7]
SW8	PIN_AB13	Slide Switch[8]
SW9	PIN_AB12	Slide Switch[9]



Table 3-4 Pin Assignment of LEDs

<i>Signal Name</i>	<i>FPGA Pin No.</i>	<i>Description</i>
LEDR0	PIN_AA2	LED [0]
LEDR1	PIN_AA1	LED [1]
LEDR2	PIN_W2	LED [2]
LEDR3	PIN_Y3	LED [3]
LEDR4	PIN_N2	LED [4]
LEDR5	PIN_N1	LED [5]
LEDR6	PIN_U2	LED [6]
LEDR7	PIN_U1	LED [7]
LEDR8	PIN_L2	LED [8]
LEDR9	PIN_L1	LED [9]

Quartus II 64-Bit - C:/Users/5465381/Documents/Spatti/PortaAND - PortaAND

File Edit View Project Assignments Processing Tools Window Help

PortaAND

Project Navigator

PortaAND.bdf

Compilation Report - PortaAND

IP Catalog

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Quartus II 64-Bit Version

Revision Name

Top-level Entity Name

Family

Device

Timing Models

Logic utilization (in ALMs)

Total registers

Total pins

Total virtual pins

Total block memory bits

Total DSP Blocks

Total HSSI RX PCSs

Total HSSI PMA RX Deserializers

Total HSSI TX PCSs

Total HSSI PMA TX Serializers

Total PLLs

Total DLLs

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Flow: Compilation

Task

Compile Design

Analysis & Synthesis

Fitter (Place & Route)

Assembler (Generate programming file)

TimeQuest Timing Analysis

EDA Netlist Writer

Program Device (Open Programmer)

Messages

293000 Quartus II Full Compilation was successful. 0 errors, 10 warnings

System Processing (126)

Opens up Device dialog to modify current device assignment

184, 147 100%

16:10 12/03/2020

Device (Não está respondendo) ✕

Select the family and device you want to target for compilation.  
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus II software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: Cyclone V (E/GX/GT/SX/SE/ST) ▾

Devices: All ▾

Show in 'Available devices' list

Package: Any ▾

Pin count: Any ▾

Core Speed grade: Any ▾

Name filter:

☒ Show advanced devices

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

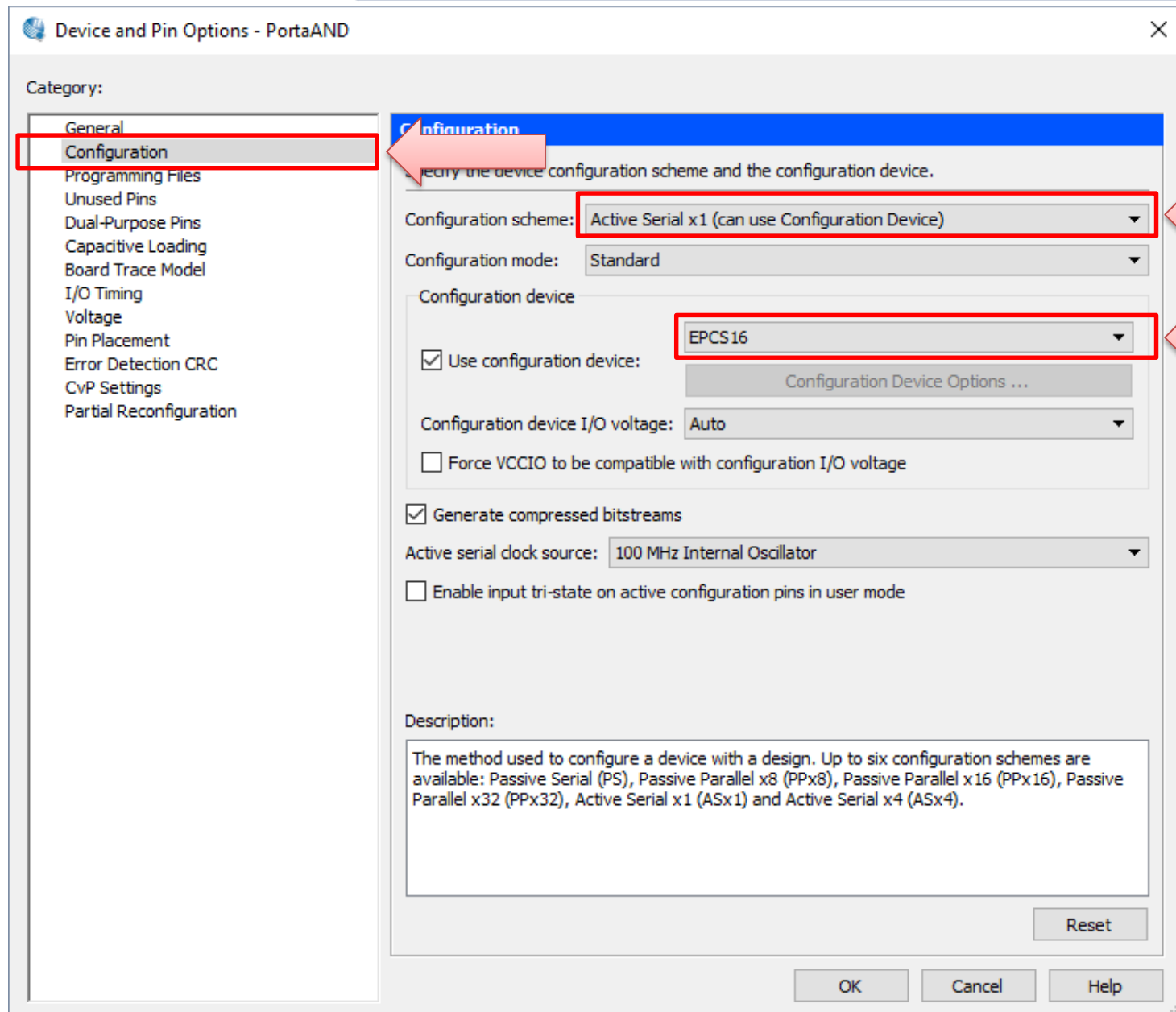
Device and Pin Options...

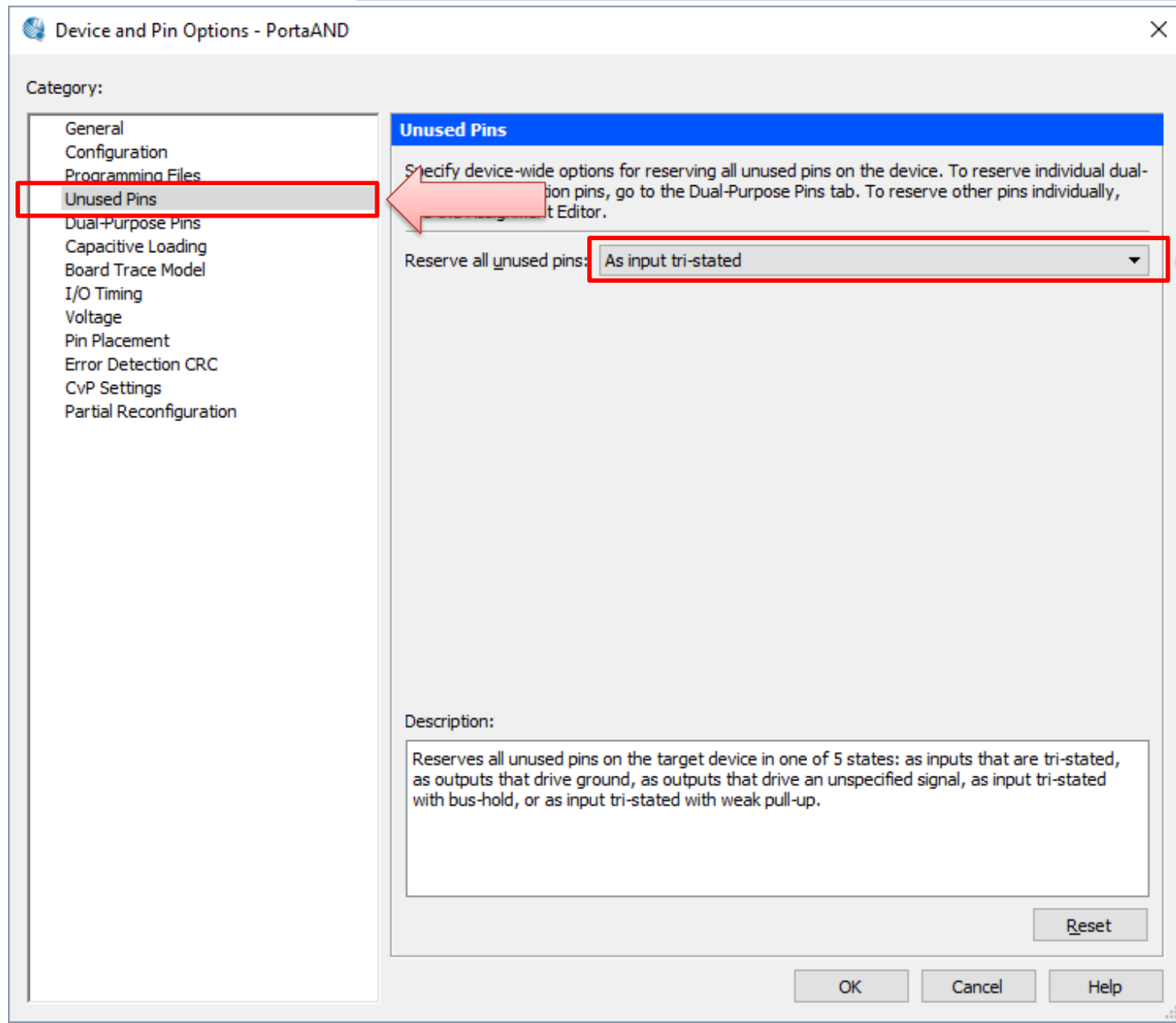
Available devices:

Name	Core Voltage	ALMs	User I/Os	GXB Channel PMA	GXB Channel PCS	PCIe I ^
5CEBA2U15C6	1.1V	9430	176	0	0	0
5CEBA2U15C7	1.1V	9430	176	0	0	0
5CEBA2U15C8	1.1V	9430	176	0	0	0
5CEBA2U15I7	1.1V	9430	176	0	0	0
5CEBA2U19C7	1.1V	9430	224	0	0	0
5CEBA2U19C8	1.1V	9430	224	0	0	0
5CEBA4F17A7	1.1V	18480	128	0	0	0
5CEBA4F17C6	1.1V	18480	128	0	0	0
5CEBA4F17C7	1.1V	18480	128	0	0	0
5CEBA4F17C8	1.1V	18480	128	0	0	0
5CEBA4F17I7	1.1V	18480	128	0	0	0
5CEBA4F23C7	1.1V	18480	224	0	0	0

Migration Devices... 0 migration devices selected

OK Cancel Help





Quartus II 64-Bit - C:/Users/5465381/Documents/Spatti/PortaAND - PortaAND

File Edit View Project Assignments Processing Tools Window Help

Stop Processing Ctrl+Shift+C

Start Compilation Ctrl+L

Analyze Current File

Start

Update Memory Initialization File

Compilation Report Ctrl+R

Dynamic Synthesis Report

PowerPlay Power Analyzer Tool

SSN Analyzer Tool

Receive Compilation Status Notifications

Project Navigator

Entity

Cyclone V: SCEBA4F23C7

PortaAND

Hierarchy Files Design UI

Tasks

Flow: Compilation Customize...

Task

Compile Design

Analysis &amp; Synthesis

Fitter (Place &amp; Route)

Assembler (Generate programming file)

TimeQuest Timing Analysis

EDA Netlist Writer

Program Device (Open Programmer)

Start Compilation Ctrl+L

Analyze Current File

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Update Memory Initialization File

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Dynamic Synthesis Report

PowerPlay Power Analyzer Tool

SSN Analyzer Tool

Receive Compilation Status Notifications

Start Compilation Ctrl+L

Analyze Current File

Start

Update Memory Initialization File

Compilation Report Ctrl+R

Dynamic Synthesis Report

PowerPlay Power Analyzer Tool

SSN Analyzer Tool

Receive Compilation Status Notifications

Start Compilation Ctrl+L

Analyze Current File

Start

Update Memory Initialization File

Compilation Report Ctrl+R

Dynamic Synthesis Report

PowerPlay Power Analyzer Tool

SSN Analyzer Tool

Receive Compilation Status Notifications

Start Compilation Ctrl+L

Analyze Current File

Start

Update Memory Initialization File

Compilation Report Ctrl+R

Dynamic Synthesis Report

PowerPlay Power Analyzer Tool

SSN Analyzer Tool

Receive Compilation Status Notifications

Start Compilation Ctrl+L

Analyze Current File

Start

Update Memory Initialization File

Compilation Report Ctrl+R

Dynamic Synthesis Report

PowerPlay Power Analyzer Tool

SSN Analyzer Tool

Receive Compilation Status Notifications

Start Compilation Ctrl+L

Analyze Current File

Start

Update Memory Initialization File

Compilation Report Ctrl+R

Dynamic Synthesis Report

PowerPlay Power Analyzer Tool

SSN Analyzer Tool

Receive Compilation Status Notifications

Start Compilation Ctrl+L

Analyze Current File

Start

Update Memory Initialization File

Compilation Report Ctrl+R

Dynamic Synthesis Report

PowerPlay Power Analyzer Tool

SSN Analyzer Tool

Receive Compilation Status Notifications

Start Compilation Ctrl+L

Analyze Current File

Start

Update Memory Initialization File

Compilation Report Ctrl+R

Dynamic Synthesis Report

PowerPlay Power Analyzer Tool

SSN Analyzer Tool

Receive Compilation Status Notifications

Start Compilation Ctrl+L

Analyze Current File

Start

Update Memory Initialization File

Compilation Report Ctrl+R

Dynamic Synthesis Report

PowerPlay Power Analyzer Tool

SSN Analyzer Tool

Receive Compilation Status Notifications

Start Compilation Ctrl+L

Analyze Current File

Start

Update Memory Initialization File

Compilation Report Ctrl+R

Dynamic Synthesis Report

PowerPlay Power Analyzer Tool

SSN Analyzer Tool

Receive Compilation Status Notifications

Quartus II 64-Bit - C:/Users/5465381/Documents/Spatti/PortaAND - PortaAND

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Entity

- Cyclone V: 5CEBA4F23C7
- PortaAND

Tasks

Flow: Compilation Customize...

Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming file)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)

Tools

- Run Simulation Tool
- Launch Simulation Library Compiler
- Launch Design Space Explorer II
- TimeQuest Timing Analyzer
- Advisors
- Chip Planner
- Design Partition Planner
- Netlist Viewers
- SignalTap II Logic Analyzer
- In-System Memory Content Editor
- Logic Analyzer Interface Editor
- In-System Sources and Probes Editor
- SignalProbe Pins...
- Programmer**
- JTAG Chain Debugger
- Fault Injection Debugger
- System Debugging Tools
- IP Catalog
- Nios II Software Build Tools for Eclipse
- Qsys
- Tcl Scripts...
- Customize...
- Options...
- License Setup...
- Install Devices...

Compilation Report - PortaAND

Summary	
Status	Successful - Mon Mar 12 16:08:59 2018
Quartus II 64-Bit Version	14.1.0 Build 186 12/03/2014 SJ Web Edition
Design Name	PortaAND
Level Entity Name	PortaAND
Device	Cyclone V
Device ID	5CEBA4F23C7
Design Models	Final
Logic Utilization (in ALMs)	1 / 18,480 (< 1 %)
Logic Registers	0
Logic Pins	3 / 224 (1 %)
Logic Virtual Pins	0
Logic Block Memory Bits	0 / 3,153,920 (0 %)
Logic DSP Blocks	0 / 66 (0 %)
Logic HSSI RX PCSs	0
Logic HSSI TX PCSs	0
Logic PLLs	0 / 4 (0 %)
Logic DLLs	0 / 4 (0 %)

IP Catalog

Installed IP

Project Directory

No Selection Available

Library

&gt; Basic Functions

&gt; DSP

&gt; Interface Protocols

&gt; Memory Interfaces and C

&gt; Processors and Periphera

Search for Partner IP

All Search

Type ID Message

293000 Quartus II Full Compilation was successful. 0 errors, 10 warnings

System (1) Processing (126)

Opens a Programmer window

184, 147 100%

Programmer - C:/Users/5465381/Documents/Spatti/PortaAND - PortaAND - [Chain1.cdf]

File Edit View Processing Tools Window Help

Search altera.com

Hardware Setup... USB-Blaster [USB-0] Mode: JTAG Progress:

☐ Enable real-time ISP to allow background programming when available

Start Stop Auto Detect Delete Add File... Change File... Save File Add Device... Up Down

File Device Checksum Usercode Program/Configure Verify Blank-Check Examine Security Bit Erase ISP CLAMP

Hardware Setup

Hardware Settings JTAG Settings

Select a programming hardware setup to use when programming devices. This programming hardware setup applies only to the current programmer window.

Currently selected hardware: USB-Blaster [USB-0]

Available hardware items:

No HardwareUSB-Blaster [USB-0]

Hardware	Server	Port	Add Hardware
USB-Blaster	Local	USB-0	Remove Hardware

Close

Windows taskbar with search bar and icons

16:12 12/03/20



Programmer - C:/Users/5465381/Documents/Spatti/PortaAND - PortaAND - [Chain1.cdf]

File Edit View Processing Tools Window Help

Hardware Setup... USB-Blaster [USB-0] Mode: JTAG Progress:

☐ Enable real-time ISP to allow background programming when available

File	Device	Checksum	Usercode	Program/Configure	Verify	Blank-Check	Examine	Security Bit	Erase	ISP CLAMP
------	--------	----------	----------	-------------------	--------	-------------	---------	--------------	-------	-----------

Start

Stop

Auto Detect

Delete

Add File...

Change File...

Save File

Add Device...

Up

Down

Select Programming File

Look in: C:\Users\5465381\Documents\Spatti\output\_files

Computer

5465381

PortaAND.sof

File name: PortaAND.sof

Files of type: Programming Files (\*.sof \*.pof \*.jam \*.jbc \*.ekp \*.jic)

Open

Cancel

Programmer - C:/Users/5465381/Documents/Spatti/PortaAND - PortaAND - [Chain1.cdf]\*

File Edit View Processing Tools Window Help

Search altera.com

Hardware Setup... USB-Blaster [USB-0] Mode: JTAG Progress: 100% (Success)

☐ Enable real-time ISP to allow background programming when available

	Device	Checksum	Usercode	Program/Configure	Verify	Blank-Check	Examine	Security Bit	Erase	ISP CLAMP
output_files/PortaAND.sof	SCEBA4F23	004DD387	004DD387	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Start

Stop

Auto Detect

Delete

Add File...

Change File...

Save File

Add Device...

Up

Down

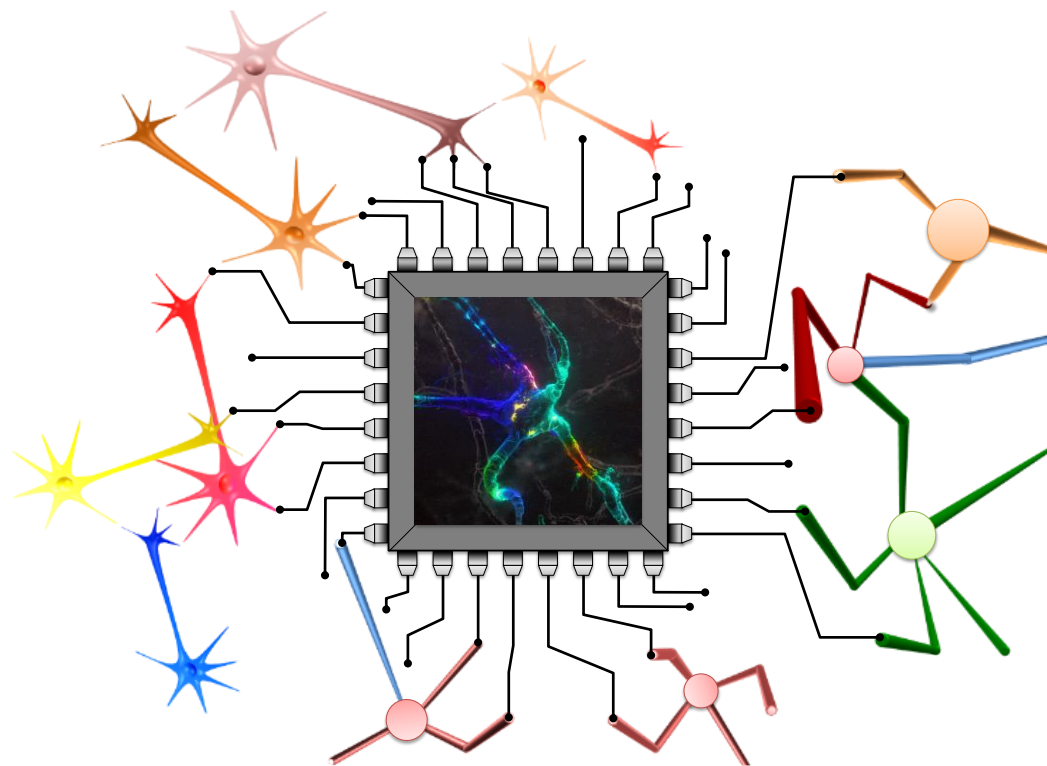
TDI

TD0

ALTERA

SCEBA4F23

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