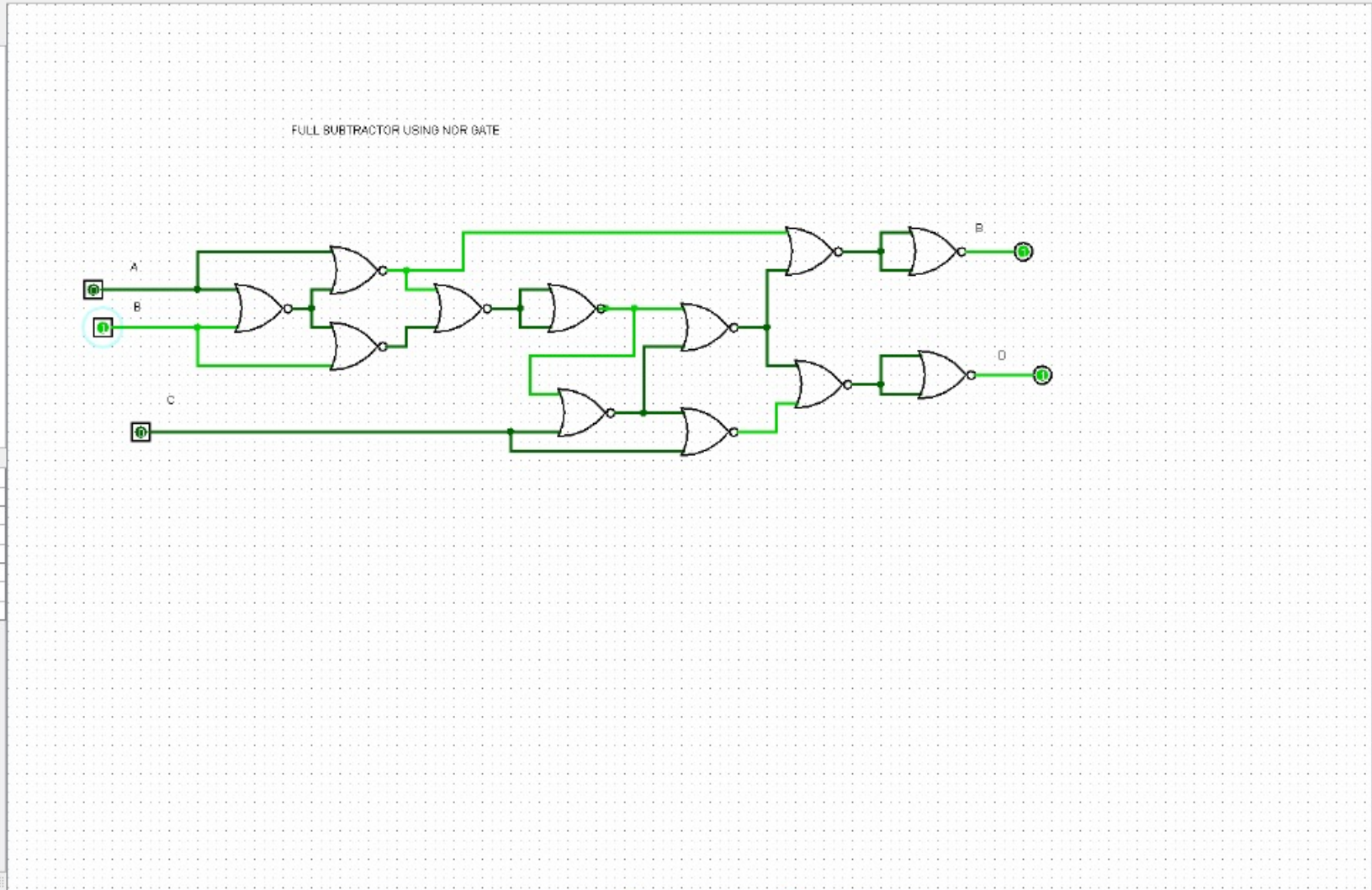


Facing	East
Output?	No
Data Bits	1
Three-state?	No
Full Behavior	Unchanged
Label	
Label Location	West
Label Font	SansSerif Plain 12



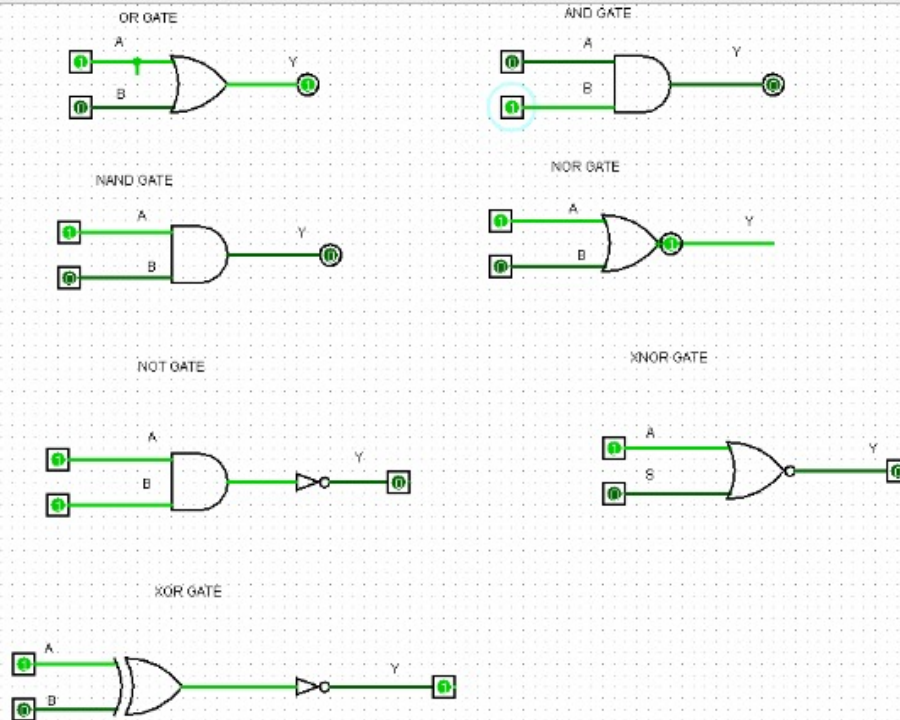


LOGIC GATES-7*

- main
- HALF ADDER
- HALD ADDER
- Wiring
- Gates
 - NOT Gate
 - Buffer
 - AND Gate
 - OR Gate
 - NAND Gate
 - NOR Gate
 - XOR Gate
 - XNOR Gate
 - Odd Parity
 - Even Parity
 - Controlled Buffer
 - Controlled Inverter
- Flexers
- Arithmetic
- Memory
- Input/Output
- Base

	Pin
acing	East
output?	No
ata Bits	1
three-state?	No
all Behavior	Unchanged
abel	
abel Location	West
abel Font	SansSerif Plain 12

100%



Logisim: main of HALF SUB USING NAND

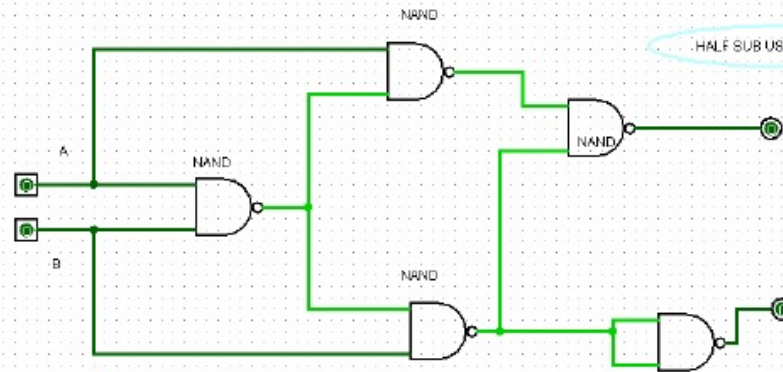
File Edit Project Simulate Window Help



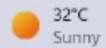
- HALF SUB USING NAND*
- main
- Wiring
- Gates
 - NOT Gate
 - Buffer
 - AND Gate
 - OR Gate
 - NAND Gate
 - NOR Gate
 - XOR Gate
 - XNOR Gate
 - Odd Parity
 - Even Parity
 - Controlled Buffer
 - Controlled Inverter
- Flexers
- Arithmetic
- Memory
- Input/Output
- Base

Label

Text	HALF SUB USING NAND GATE
Font	SansSerif Plain 12
Horizontal Alignment	Center
Vertical Alignment	Base



100%



32°C
Sunny



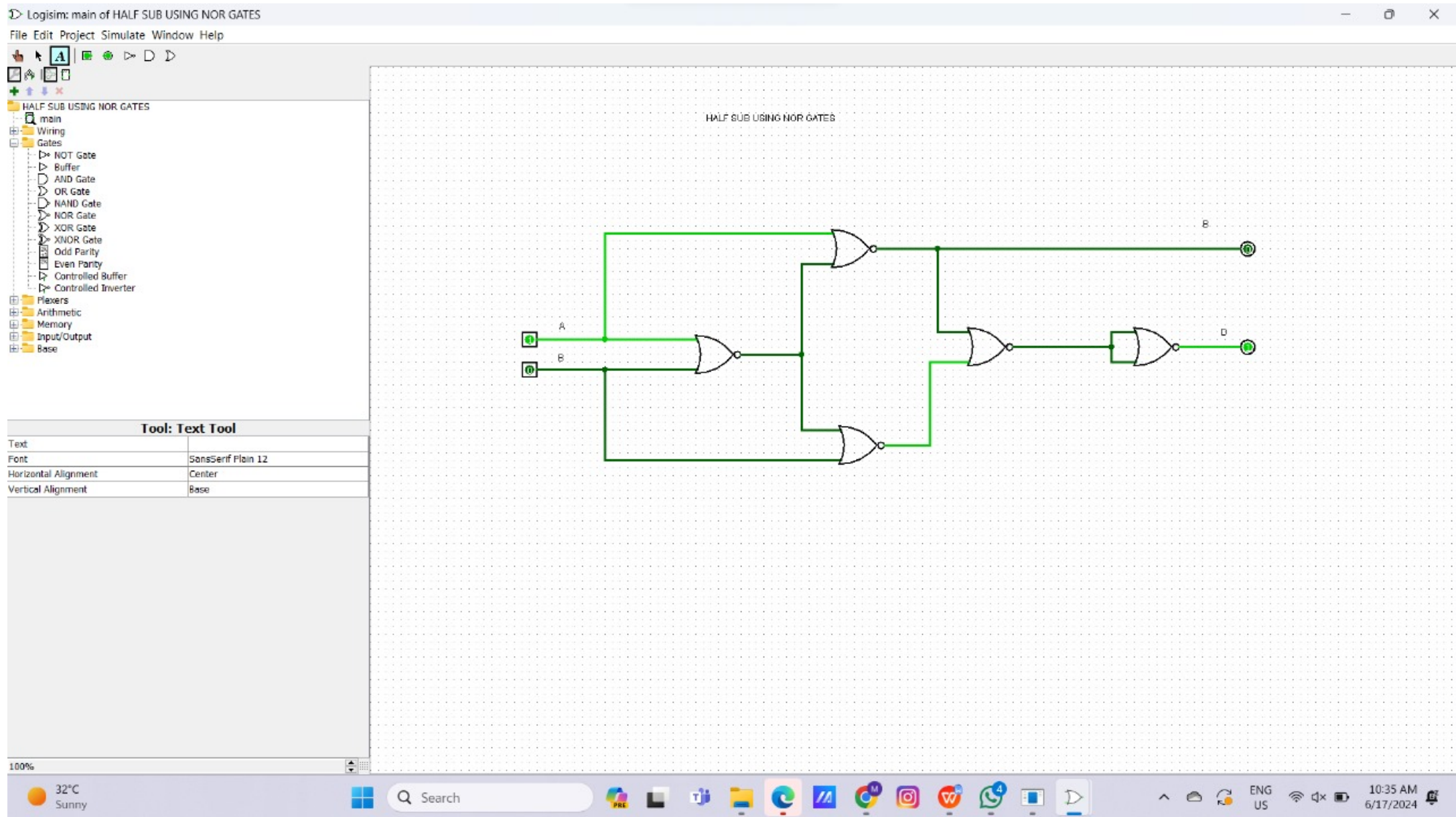
Search



ENG
US

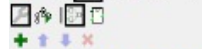


10:29 AM
6/17/2024



Logisim: main of HALD ADDER USING NOR GATE

File Edit Project Simulate Window Help



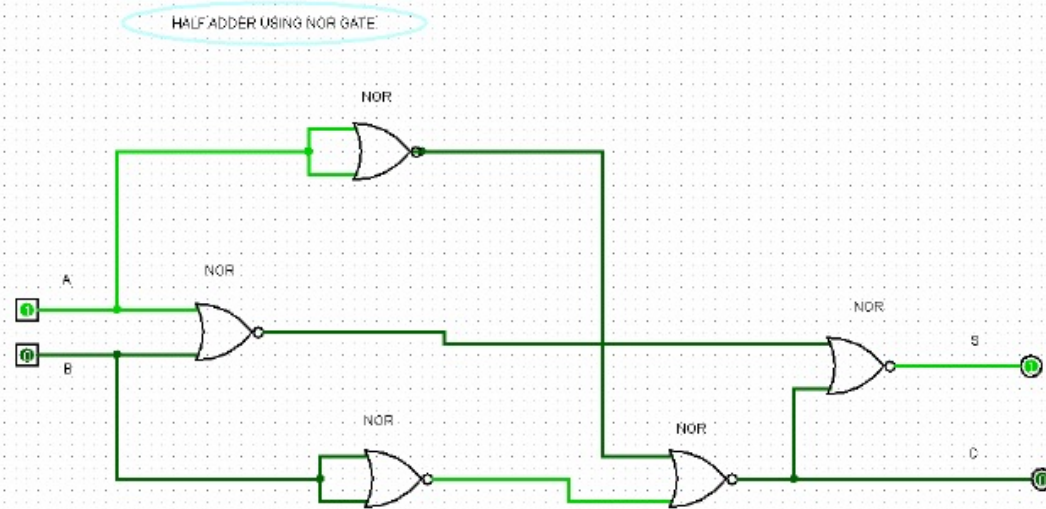
HALD ADDER USING NOR GATE*

- main
- Wiring
- Gates
 - NOT Gate
 - Buffer
 - AND Gate
 - OR Gate
 - NAND Gate
 - NOR Gate
 - XOR Gate
 - XNOR Gate
 - Odd Parity
 - Even Parity
 - Controlled Buffer
 - Controlled Inverter
- Flexers
- Arithmetic
- Memory
- Input/Output
- Base

Label

Text	HALF ADDER USING NOR GATE
Font	SansSerif Plain 12
Horizontal Alignment	Center
Vertical Alignment	Base

100%



32°C
Sunny



Search



ENG
US



10:16 AM
6/17/2024



Logisim: main of FULL SUBTRACTOR USING NAND GATES

File Edit Project Simulate Window Help



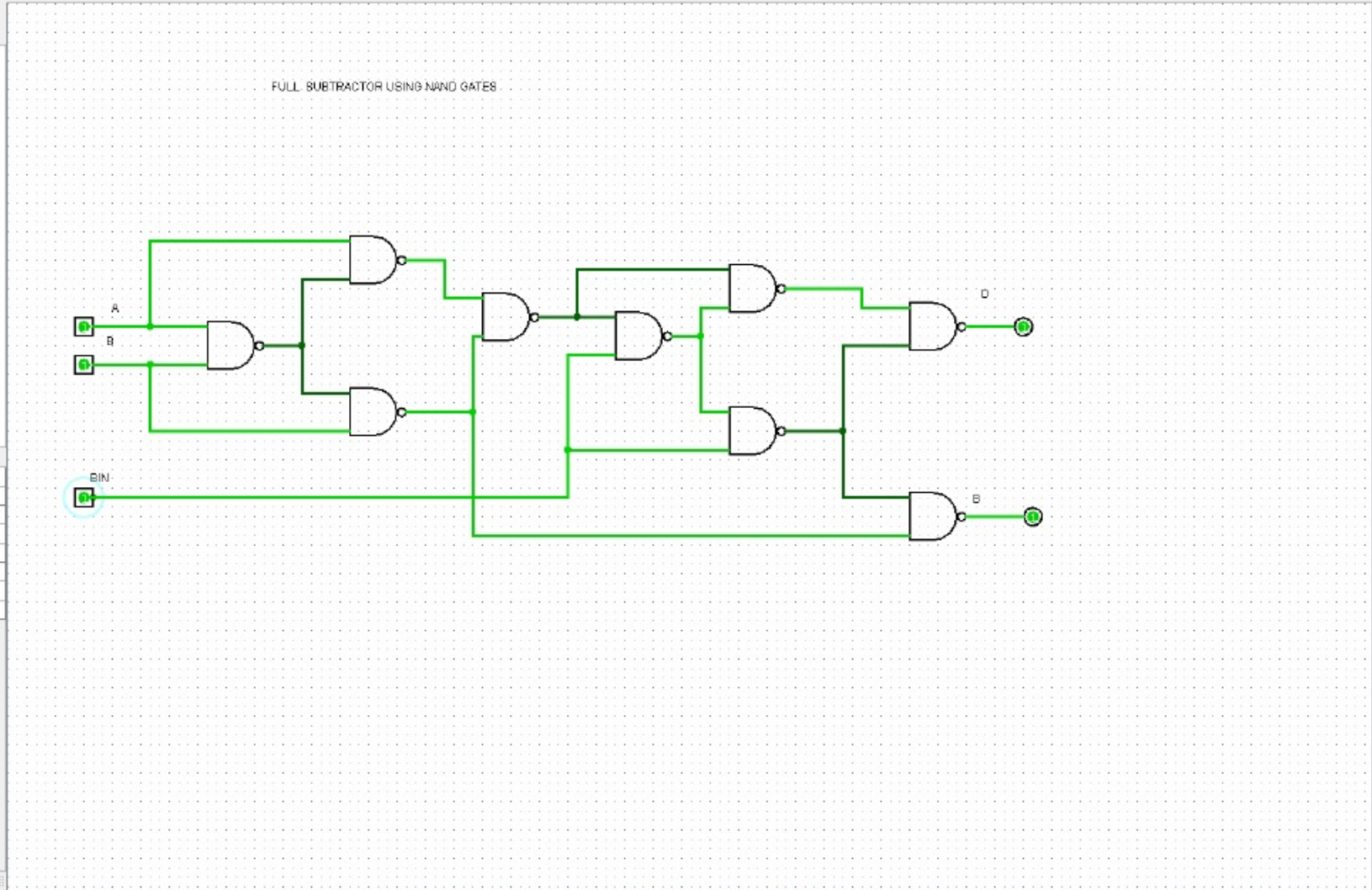
FULL SUBTRACTOR USING NAND GATES

- main
- Wiring
- Gates
 - NOT Gate
 - Buffer
 - AND Gate
 - OR Gate
 - NAND Gate
 - NOR Gate
 - XOR Gate
 - XNOR Gate
 - Odd Parity
 - Even Parity
 - Controlled Buffer
 - Controlled Inverter
- Flexers
- Arithmetic
- Memory
- Input/Output
- Base

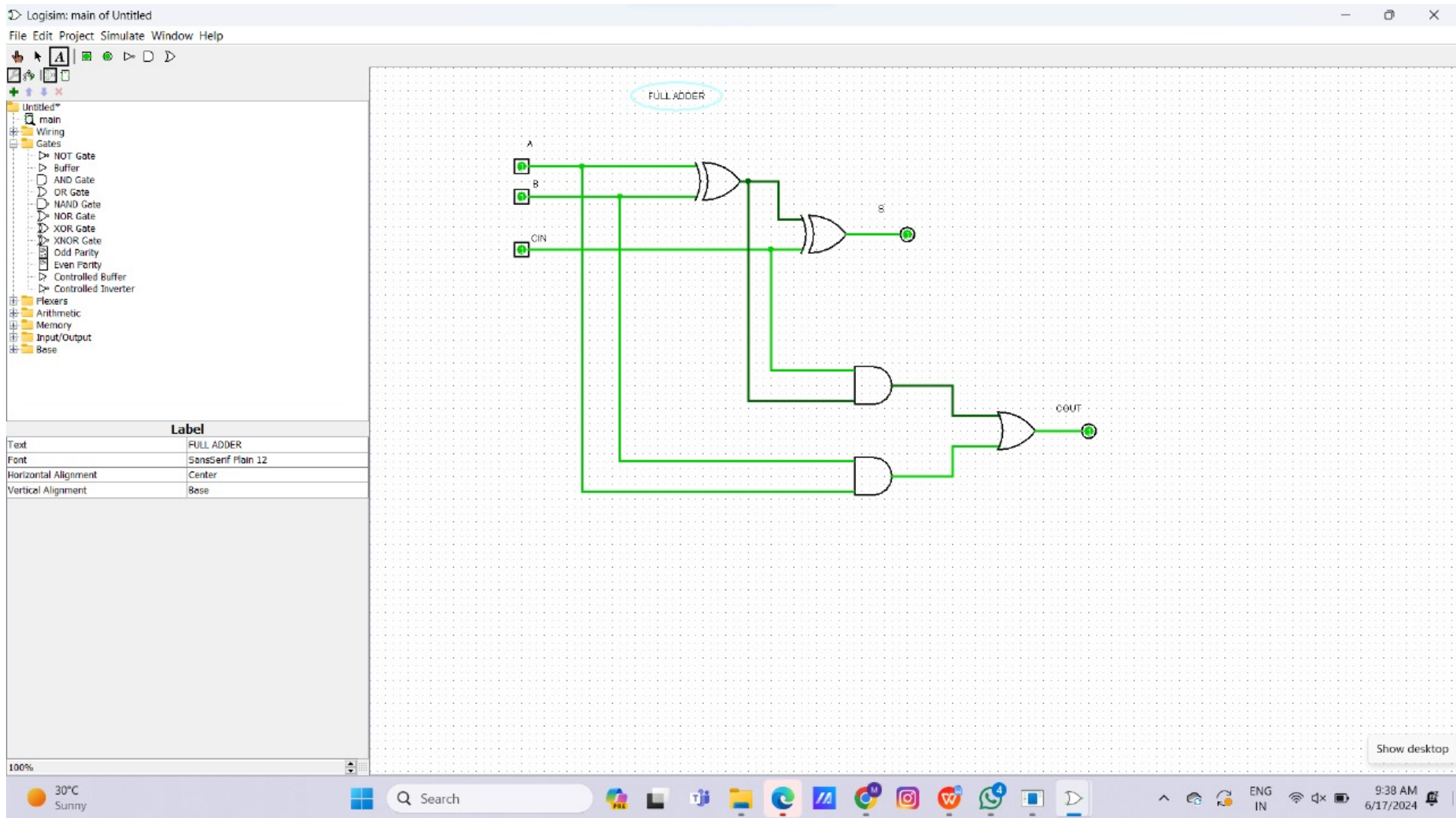
Pin

Facing	East
Output?	No
Data Bits	1
Three-state?	No
Full Behavior	Unchanged
Label	
Label Location	West
Label Font	SansSerif Plain 12

100%



30°C
Mostly clear



Logisim: main of FULL ADDER USING NOR AGTES

File Edit Project Simulate Window Help



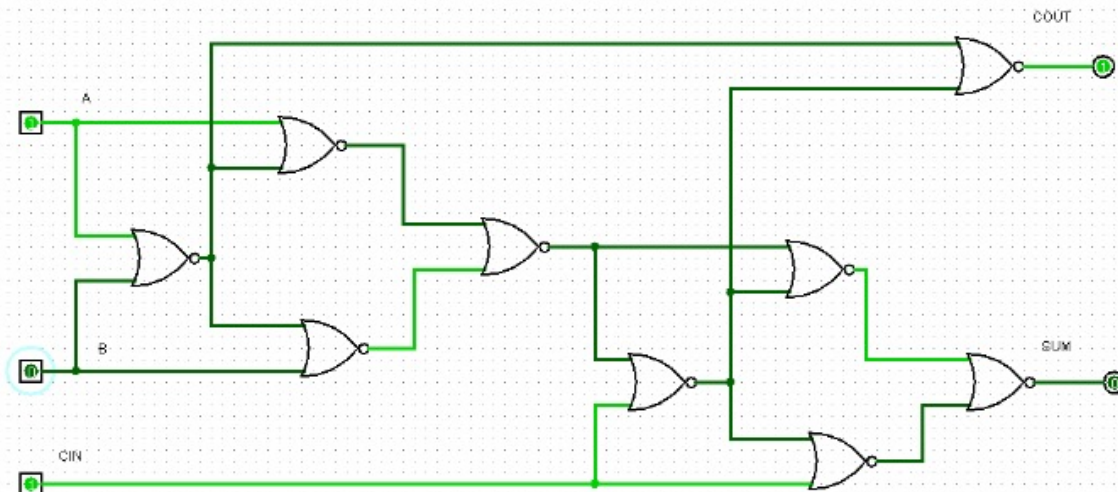
- FULL ADDER USING NOR AGTES
 - main
 - Wiring
 - Gates
 - NOT Gate
 - Buffer
 - AND Gate
 - OR Gate
 - NAND Gate
 - NOR Gate
 - XOR Gate
 - XNOR Gate
 - Odd Parity
 - Even Parity
 - Controlled Buffer
 - Controlled Inverter
 - Flexers
 - Arithmetic
 - Memory
 - Input/Output
 - Base

Pin

Facing	East
Output?	No
Data Bits	1
Three-state?	No
Full Behavior	Unchanged
Label	
Label Location	West
Label Font	SansSerif Plain 12

100%

FULL ADDER USING NOR GATES



30°C
Mostly clear

- New Ctrl+N
- Open... Ctrl+O
- Open Recent >
- Close Ctrl+Shift+W
- Save Ctrl+S
- Save As... Ctrl+Shift+S
- Export Image...
- Print... Ctrl+P
- Preferences...
- Exit Ctrl+Q

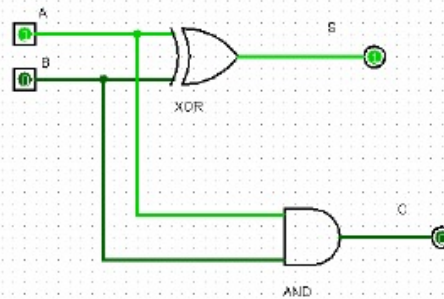
- Even Parity
- Controlled Buffer
- Controlled Inverter
- Flexers
- Arithmetic
- Memory
- Input/Output
- Base

Label

Text	HALF SUBTRACTOR
Font	SansSerif Plain 12
Horizontal Alignment	Center
Vertical Alignment	Base

100%

HALD ADDER



HALF SUBTRACTOR

