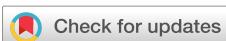


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ABSTRACT

The number of photonic components integrated into the same circuit is approaching one million, but so far, this has been without the large-scale integration of active components: lasers, amplifiers, and high-speed modulators. Emerging applications in communication, sensing, and computing sectors will benefit from the functionality gained with high-density active–passive integration. Indium phosphide offers the richest possible combinations of active components, but in the past decade, their pace of integration scaling has not kept up with passive components realized in silicon. In this work, we offer a perspective for functional scaling of photonic integrated circuits with actives and passives on InP platforms, in the axes of component miniaturization, areal optimization, and wafer size scaling.

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I. INTRODUCTION

Significant progress has been witnessed in the number of photonic components that can be packed into the same photonic integrated circuit (PIC), analogous in many ways to the trajectory observed in Moore’s law^{1,2} for microelectronics. Borrowing the concept from electronic integrated circuits (EICs),³ the circuit scale can be categorized as follows: small-scale integration (SSI) with 1–10 components; medium-scale integration (MSI) with 10–500 components; large-scale integration (LSI) with 500–20 000 components; very-large-scale integration (VLSI) with 2×10^4 – 10^6 components, and ultra-large-scale integration (ULSI) with a component count beyond 10^6 . VLSI PICs with more than 10^5 components are with us today.^{4,5} However, such circuits have a restricted set of components. Without the rich mix of active components, including lasers, semiconductor optical amplifiers (SOAs), and photodetectors (PD), the ultimate chip scalability, functionality, and flexibility of integrated photonics will not reach their full potential. The realization of active–passive LSI and VLSI requires a concerted effort on platforms where diverse types of components can be integrated at a high density.

Contemporary PIC platforms mainly include gallium arsenide (GaAs), indium phosphide (InP), silicon, silicon nitride (SiN), lithium niobate (LN), barium titanate (BTO), 2D materials, and polymers. GaAs has historically been used for discrete laser fabrication; mainly vertical-cavity surface-emitting lasers (VCSELs)

and, more recently, GaAs-based PICs operating around the 1030 nm wavelength are demonstrated.⁶ InP is a reliable material offering a comprehensive component portfolio for light generation, modulation, detection, and waveguiding at longer wavelengths and, particularly, in the O and C bands.⁷ These wavelength bands have been particularly important for the deployment of long-distance fiber optical communications and coherent integrated optical transmitters and receivers.^{8–10} Thin silicon on insulator (SOI) is a particularly prominent platform in Si photonics,¹¹ and its high index contrast in the cross section facilitates miniaturized passive components to be realized with the manufacturing tools in place for silicon electronics. However, the incorporation of native amplifiers and high-performance phase modulators has been challenging.^{12,13} SiN features a low absorption loss and a large transparency range, making it an excellent waveguiding material attractive for interferometers and delay lines in quantum information processing (QIP) and medical applications.¹⁴ However, efficient electrically driven modulators, electrically driven amplifiers, lasers, and detectors are absent in this material. LN has historically provided the gold standard for modulators,¹⁵ and to meet ever more stringent efficiency and bandwidth requirements, thin-film lithium niobate substrates are becoming available.¹⁵ It is also considered to be a near-pure passive material with limited amplitude modulation for the phase modulators. Materials such as 2D materials,¹⁶ BTO,¹⁷ and polymers¹⁸ are attracting considerable research interest, although manufacturability remains an area of study. Integrated circuits using these materials

alone are uncommon. Instead, they are more usually deposited and integrated into a more comprehensive PIC platform.

SOI and InP are the most commercially established PIC platforms at the time of writing. While active components are native to the InP platform, for SOI photonics, electrically driven light sources and amplifiers have required hybrid or heterogeneous integration with III-V materials,^{19,20} mostly InP due to the established market for telecommunications technologies. In one flavor, the InP active components are first fabricated, diced, and then integrated into SOI circuits as chiplets.²¹ A wafer-scale process can also be used after the InP material transfer, which potentially allows for more parallel fabrication and higher scalability. Such processes are currently realized by die bonding^{22,23} or transfer-printing.²⁴ Epitaxial growth of III-V materials on Si is researched as a wafer-scale solution in the long run, although the high process temperatures may prevent the most sophisticated levels of component integration. To date, the most successful approaches with electrically pumped demonstrations have used GaAs-based materials,^{25–27} which are unsuited to C-band light sources and the broadest range of active components. InP-based lasers directly grown on Si are still optically pumped.^{28–30}

The InP platform has demonstrated the versatility and flexibility required for PICs with the most diverse component types. With methods including regrowth,^{31,32} selective-area growth (SAG),³³ intermixing,³⁴ and vertical active-passive integration,³⁵ materials of different bandgaps, each individually and functionally optimized, can be integrated on the same substrate. The optical coupling between components can be seamless in the case of butt-joint interfaces. There are no mechanical conflicts that limit design density as might be seen in die-bonding or transfer-printing, providing the largest freedom in circuit floorplanning for LSI and VLSI. Mainstream monolithic integrated InP circuits do, however, have a waveguide cross-sectional area that is an order of magnitude larger than that of high-density SOI, resulting from the less strongly confined waveguides when using the native substrate.

In Sec. II, the PIC scaling trends are first investigated, emphasizing the contributing factors to die size and packing density, the same as in microelectronics as pointed out by Moore.³⁶ Then, we analyze opportunities for LSI and VLSI PICs with a rich mix of active and passive components leveraging the InP technology, particularly in two main axes described as the technological drivers of scale in Moore's law: component miniaturization (Sec. III) and areal optimization (elimination of unused chip areas) (Sec. IV). Finally, in Sec. V, we briefly discuss the opportunities for InP wafer-size scaling.

II. PIC SCALE DEVELOPMENT

A. Component count

In Moore's observation,^{1,37} the *scale* of the chip is quantified by the *component count*, which primarily includes transistors but not electrical (copper) interconnects. This is logical as it acknowledges that only the *functional components* contribute to the expansion of the integrated chip's capabilities. In photonic circuits, comparison studies^{8,10} have also counted only *functional components*, determined by the basic optical function they perform. The diversity can be extensive with components for light generation, amplification, attenuation, phase shifting/modulation, detection, (de)multiplexing, filtering, polarization rotation, out-of-plane coupling, etc. Here, similar to microelectronics, waveguide optics for interconnection,

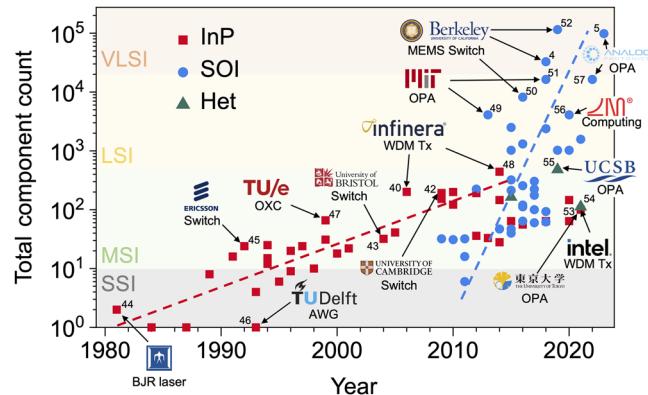


FIG. 1. Total functional component count per die for monolithic InP, SOI, and heterogeneous platforms, plotted as a function of the year the PIC is reported. Some representative examples^{4,5,40,42–57} are marked with the demonstrating institutes or companies.

including straight waveguides, adiabatic tapers, bends, crossings, star couplers, and splitters, are not counted. This may be revisited with the emergence of analog optical signal processing, including neuromorphic and quantum circuits, but we retain this approach for comparative purposes.

The evolution of PIC's component count is shown in Fig. 1 for InP, SOI, and InP/SOI heterogeneous integration platforms. As can be seen, InP has been the material of choice for more than 40 years.^{8,10,38} In its early phase, (InP) PIC scaling was driven by the development of individual components, with a focus on integrating active elements with passive elements using integration schemes, such as butt-joint regrowth.⁸ The chip scale is in the SSI regime. From the year 2000, large-scale deployments of fiber optics and high-capacity optical communication fueled the fast development of wavelength-division multiplexing (WDM), leading to rapid scaling with arrayed waveguide grating (AWG)-based multiplexing/demultiplexing^{9,35} and, later, systems-on-chip (SoC) for coherent communication.^{31,38} These InP PICs boast a rich mix of component types,^{39–41} including lasers, phase shifters, modulators, (de)multiplexers, and photodetectors (PD). Already a decade ago, a monolithic InP PIC $40 \times 57 \text{ Gb s}^{-1}$ WDM transmitter⁴⁰ was reported by Infinera, where 40 on-chip lasers are monolithically integrated with 40 in-phase-quadrature (IQ) phase modulators (PMs), 40 variable optical attenuators, and AWGs. This single chip was capable of delivering 2.25 Tb s^{-1} bandwidth. A need for advanced reconfigurability in the optical network drove research efforts into optical switches,^{42,43} which also integrated switch technology with AWG-based transceivers. These chips belong to the MSI regime and approach the LSI regime.

Emerging applications in optical communication, computation, and sensing drive the PIC scale toward LSI and VLSI. Data centers have relied on power-hungry electrical packet switches for exchanging massive data flows between millions of servers.⁵⁸ Research is now addressing switching and routing technologies with over 102.4 Tb s^{-1} capacity, requiring intimate photonic-electronic integration to meet the system's performance and power budget.⁵⁹ Large-scale and fast optical-domain switching^{4,58,60–62} holds

the promise to drastically reduce energy consumption and to provide full fiber bandwidth data capacity at the same time. The largest integrated optical switch demonstrated to date, a 240×240 optical switch with 57 600 switching units,⁴ each containing two vertical adiabatic couplers, is realized in the SOI microelectromechanical systems (MEMS) technology. Full channel testing has yet to be demonstrated.

The rise of machine learning (ML) and artificial intelligence (AI) is driving the demand for massively parallel matrix computations and brain-inspired neuromorphic hardware.⁶³ Integrated photonic methods based on nested interferometers, resonator arrays, or SOAs, resembling optical switch fabrics, are being proposed to enable energy-efficient computing with femtojoule-per-operation-level power consumption.^{64–68} Start-up companies, including Lightmatter,⁶⁹ Lightelligence,⁷⁰ and LightOn,⁷¹ are commercializing the photonic computing technology. An LSI 64×64 photonic matrix processor with 4096 compute elements⁶⁹ was reported by Lightmatter in 2020, while further scaling is being investigated.⁷² Similar or same matrix operations in ML and AI applications are also proposed as an essential part of photonic QIP,^{72–74} with additional emphasis on optical loss optimization.⁷⁵

Light detection and ranging (LiDAR) allows for remote sensing at an unprecedented spatial resolution and is believed to be one of the key technologies for advanced driver assistance systems (ADAS) and self-driving cars. Integrated optical phase arrays (OPAs)^{49,57,76–78} provide a promising route to full-solid LiDAR and potential production scalability with the planar integration technology. Recently, an integrated OPA with 49 152 integrated phase shifters has been demonstrated by Analog Photonics⁵ with the SOI platform, but with external light sources and without integrated optical amplifiers. In the long-term, on-chip light sources and distributed amplification may enable higher operating powers, reduced power penalty, streamlined manufacturing, and scalability.⁷⁹ The University of Tokyo has demonstrated the largest 100-channel InP-based OPA.⁵³

The LSI and VLSI PICs demonstrated at present are commonly based on replications of the same passive component in the circuit, limiting functionality and onward scalability. VLSI optical switches are based on the replication of individual switching units without on-chip gain and become loss-constrained.^{4,61,80} SOI switches based on electro-optic (EO) modulators (EOMs) or thermo-optic modulators (TOMs) nested in interferometers have not scaled beyond 32×32 , and the maximum path loss is in the order of 10 dB.^{61,81–83} Waveguide MEMS switches offer low loss in the off (decoupled) state to provide further scaling. The much larger 240×240 MEMS optical switch⁴ is reported to have a maximum path loss of 9.8 dB. However, the switching speed is mechanically limited. SOA integration provides the optical gain for onward scaling⁸⁴ while still allowing for a full solid-state realization. With an active-passive InP platform, a lossless operation is showcased in a 16×16 optical switch⁴² by the University of Cambridge (Fig. 1).

PIC-based machine learning accelerators face the same issue of loss-constrained scalability, as their circuit elements, connection types, and the number of connections are akin to those of integrated optical switches.⁶⁴ On-chip gain can facilitate further scaling. Implementations of neural network models by photonic chips, often referred to as neuromorphic or brain-inspired photonic computing, additionally call for the large-scale integration of nonlinear

activation functions.⁶⁷ This is not easy with the material optical nonlinearities as they are often weak and require a high optical input power.⁸⁵ On an SOI platform, all-optical activation is realized with ring-enhanced nonlinearities, but the power sensitivity of the reported device is +5 dBm.⁸⁶ Lasers and SOAs are considered competitive candidates for the required nonlinear activation^{87,88} to realize an all-optical neural network. In 2022, nonlinear activation with an on-chip input power as low as 0.06 mW (-12 dBm) is achieved using a membrane laser.⁸⁸ Unlike optical switches, which are supposed to send light out of the photonic chip, machine learning processors should ideally have all optical functions confined in their own package, motivating on-chip light source integration.⁶⁷

Long-range OPAs for the automotive sector require a detection distance of 200 m,^{78,89} indicating at least hundreds of milliwatt optical output from the emission aperture when considering coherent detection. For time-of-flight schemes, a peak power in the order of watts is required.⁹⁰ Amplifiers can be integrated to increase OPAs' output power and relax the power and heat management requirements of the light source. In a recent demonstration, 21.5 dB maximum gain is achieved using an InP-based OPA, delivering a maximum total output power of 35.5 mW.^{91,92} In another demonstration, up to 240 mW output power is achieved with an integrated master tunable laser feeding an on-chip SOA array.⁹³

B. Die size

Die size determines the available design area for the PIC. Figure 2 shows the die size evolution over the past three decades, categorized under the concerned PIC platforms. In the past, most of the PICs demonstrated had sizes smaller than one square centimeter. This is conveniently smaller than the scanner and stepper reticle size limit that is now mainstream for PIC production. As process yields have improved, it has become interesting to study larger area circuits. Recently, researchers from UC Berkeley and Analog Photonics individually showed the possibility of using widened waveguides for inter-reticle interconnection.^{4,5} As seen in Fig. 2, this innovation has led to the realization of $>10^3$ mm² VLSI circuits containing 10^5 -level components, as mentioned in Sec. II A. An ultra-large InP PIC occupying the entire 2-inch wafer was also demonstrated in 2010 by UC Davis,⁹⁴ although in this case, contact lithography was used, which has no reticle size limit. Here, the limit in the maximum circuit size comes from the wafer. Current commercial InP wafers have diameters up to 100 mm, and further scaling to 150 mm may technically allow larger PICs with an area of 10⁴ mm² and beyond. A detailed discussion on InP wafer size expansion can be found in Sec. V.

As shown in Fig. 2, there has been no push beyond the areal capability of non-contact lithography until the past decade. For low-complexity, small-scale chips, the sizes can be more determined by packaging and handling requirements rather than the photonic circuits themselves. If it is a research prototype, it may further have suboptimal areal utilization. Therefore, in the early days, there is no general relation between the number of components and the size of the chip. However, as PIC technology matures and approaches industrialization,⁹⁵ the economic dynamics of chip manufacturing^{36,37} require minimizing the cost per component, in other words, dense integration of photonic components. Advanced packaging, such as hybrid or heterogeneous assemblies, may also be necessary to reduce the packaging overhead for large-scale cir-

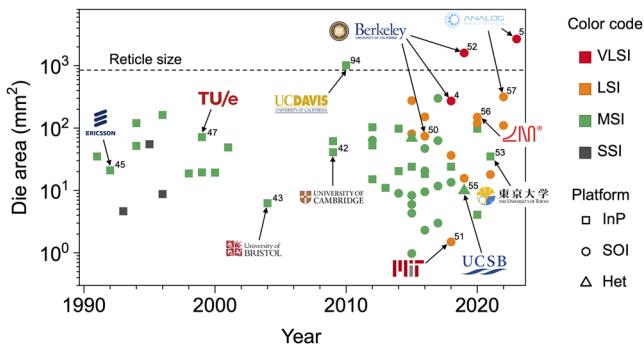


FIG. 2. Die area plotted as a function of year. The data points are based on the available information reported and, therefore, do not match one to one with those in Fig. 1. Some representative examples^{4,5,42,43,45,47,50–53,55–57,94} are marked with the demonstrating institutes or companies.

cuits. In the near future, densely integrated, large-scale circuits, even occupying an entire wafer,^{96,97} may be driven by demanding applications, such as neuromorphic and quantum computation, as well as larger-scale switching networks.

C. Packing density

Ever-denser integration offers an attractive perspective for functional enhancement and cost reduction for a given chip area. One key difference for PICs relative to (digital) microelectronics is that PICs consist of a richer variety of component types, each with its own footprint and density constraints. Figure 3 plots the packing densities in PICs, for passive components, MEMS components, EOMs, TOMs, and SOAs. The highest density is achieved for passive elements, such as surface grating antennas in an OPA from MIT, which exhibits an impressive component density of over 10^4 mm^{-2} and an individual antenna footprint of only $4 \times 4 \mu\text{m}^2$. Passive components scaling is currently bound by optical confinement, and circuit performance is bound by a lack of high-density active components. PICs with active tuning or modulation by TOMs or EOMs

show the highest component packing density of around 40 mm^{-2} , as demonstrated in actively tunable OPAs^{5,98} and photonic processors.⁵⁶ Although this is slightly lower than what is demonstrated with MEMS components that achieve a density in the order of 10^2 mm^{-2} , it should be noted that there is no electrical wiring to the tuning element in the high-density MEMS PICs.^{45,99} The highest density achieved for active components is around 10 mm^{-2} with SOA-based optical switches, as demonstrated by the University of Bristol,⁴³ University of Cambridge,⁴² and TU Eindhoven.¹⁰⁰ Comparing the different component types, it is evident that actives and modulators have not been able to scale at the same pace as passives.

Miniaturization of EOMs requires innovations in achieving higher modulation efficiency,^{13,102–104} expressed widely as the product of the half-wave modulation voltage and phase modulator length ($V_{\pi}L$). TOMs typically have a much smaller footprint due to the more effective (but slower) electrical-power tuning mechanism.^{105,106} Thermal crosstalk and power consumption impose challenges on the density and scale of TOMs.^{10,107,108} SOAs and many laser designs exhibit a low wall-plug efficiency (WPE), making them thermally constrained.^{2,32,109} Areal optimization will be required to enhance the packing density of miniaturized components, especially for components that require electrical wiring and active tuning. This aspect includes optimization of the integration technology, heat dissipation, and circuit floorplanning. Unlike in electronics, where multi-layer copper wiring with vertical vias is the standard, so far on-chip optical interconnection mostly relies on in-plane connectivity. Hence, compact waveguide floorplanning with ultra-sharp bends and butt-joint integration is important. Vertical optical vias are also being researched for 3D integration.¹¹⁰

III. COMPONENT MINIATURIZATION WITH InP TECHNOLOGY

A. A membrane-based approach

InP component miniaturization can be achieved through substrate removal for tighter confinement of the guided mode, and this is conceptually similar to the SOI technology. By replacing the cladding with a low-index dielectric, it is possible to confine light within a nanophotonic membrane with a remarkably slim thickness of only hundreds of nanometers.^{111–117} This approach was pioneered by several groups worldwide in the late 2000s.^{118–120} Figure 4(a) shows the waveguide cross sections for both a substrate-based InP technology and the membrane InP technology developed at TU Eindhoven. A typical single-mode waveguide dimension on this InP membrane platform is $300 \times 400 \text{ nm}^2$. Its cross-sectional area is only ~5% of those on conventional substrate-based platforms.¹⁰ The utilization of deep ultraviolet (DUV) scanner lithography and non-intentionally doped (n.i.d.) InP-based waveguide together enable 1 dB cm^{-1} -level propagation loss,¹²¹ comparable to the state-of-the-art passive SOI technology. The cross-sectional size reduction directly leads to the passive miniaturization to the same compactness levels achievable with high-confinement SOI technologies. Examples include ultra-sharp $1 \mu\text{m}$ -radius bends,¹²² ultra-short $4 \mu\text{m}$ -long polarization rotators,^{123,124} and $3 \mu\text{m}$ -long fully reflective photonic crystal reflectors,¹²⁵ as seen in Fig. 4(b). When compared to prior work with substrate-based components,¹⁰ this represents size reduction factors of 10–100.

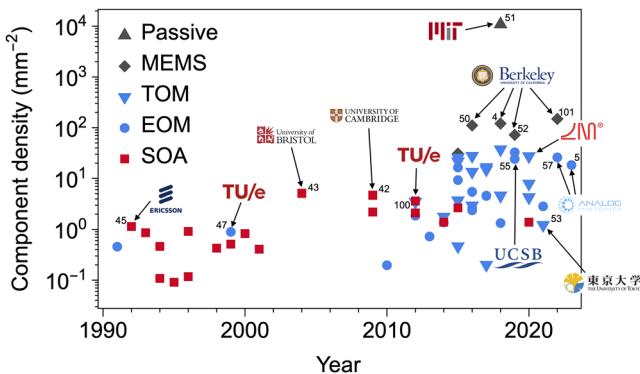


FIG. 3. Density per die for passive, MEMS, TOM, EOM, and SOA components plotted as a function of the year the PIC is reported. Some representative examples^{4,5,42,43,45,47,50–53,55–57,100,101} are marked with the demonstrating institutes or companies.

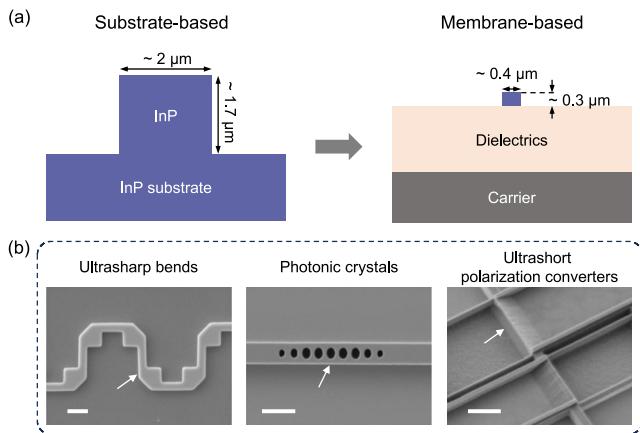


FIG. 4. (a) Waveguide cross sections of the substrate-based and membrane-based InP technologies. (b) Examples of miniaturized passives—bends, reflectors and polarization mode converters—with the InP membrane technology. The arrows indicate the devices of interest. Scale bar: 1 μm .

1. Active components miniaturization

The InP material system offers miniaturization opportunities beyond simple passives, by utilizing the mature epitaxy techniques for combining functional materials. A TOM based on an epitaxially grown n-InP heating layer directly on top of the waveguiding layer has recently been realized.¹²⁶ Figure 5(a) shows the schematics of such a TOM, which has an ultra-compact footprint of $13.3 \times 7.3 \mu\text{m}^2$ including the contact pads. The zero-distance placing of the heating element to the highly confined optical mode results in a high energy efficiency of $\sim 2.2 \text{ mW}/\pi$ and $P_\pi \cdot \tau$ of $28.6 \text{ mW } \mu\text{s}$. This is $>50\times$ more efficient compared to substrate-based InP TOMs. Further improvement to $1 \text{ mW}/\pi$ and $10 \mu\text{s}$ time constant is possible by reducing the functional volume even more to a single-mode waveguide.¹²⁶

Miniaturized modulators can be realized with the membrane-based approach. By inserting a thin layer of dielectric in the middle of two electrically biased semiconductor layers, forming a capacitor,^{127–131} efficient modulators by carrier accumulation are reported. This is not possible on substrate-based platforms since

the optical mode is deeply shielded by the claddings. Compared to silicon-insulator-silicon capacitor modulators, InP-based materials offer a much stronger carrier-induced index change,^{132,133} resulting in a significantly reduced footprint. Such modulators with InP-based materials are first demonstrated in 2017 by two individual research groups, one showing $0.47 \text{ V mm } V_\pi L$ with a length of $500 \mu\text{m}$ ¹²⁸ and the other one exhibiting a $V_\pi L$ of 0.9 V mm with a length of $250 \mu\text{m}$.¹²⁷ Initial results show modest GHz-level modulation bandwidths, but a recent study has predicted a route to higher bandwidths.¹²⁹

Amplifiers and lasers miniaturization benefit from optical confinement enhancement with the membrane structure. A conceptual illustration is shown in Fig. 5(b). With appropriate waveguide geometries, the strong index contrast offered by the membrane could mean $\sim 3\%$ confinement per quantum well (QW), which is a threefold improvement compared to thick-InP-clad waveguide designs. To efficiently inject carriers into this membrane gain section, lateral carrier injection schemes^{111,117,134–138} have been proposed, where the n- and p-doped claddings are grown by the side of the active core, as seen in Fig. 5(b). Lasers constructed from these high-confinement membrane structures exhibit superior performance concerning compactness and low-power operation. In 2022, a membrane distributed-reflector laser is demonstrated to have an ultra-low threshold of 0.13 mA ,¹³⁹ with continuous-wave operation measuring up to $46\times$ threshold. Moreover, the maximum external quantum efficiency is calculated to be 23% [wall-plug efficiency (WPE) 10%]. The footprint of the gain section is only $0.7 \times 30 \mu\text{m}^2$, an order of magnitude smaller than conventional DFB lasers. More recently, membrane SOAs with similar high-confinement cross sections are also realized and integrated into a PIC.^{137,140} The gain per unit device length can also be boosted by multipass in the same gain section. Mode-division multiplexing may be used to suppress resonance.¹⁴¹ A proof-of-concept double-pass SOA has recently been reported utilizing the InP membrane technology,¹⁴¹ which shows up to 87% more optical gain compared to a single-pass SOA with the same gain section length and injection current. This allows for a SOA length reduction with a given optical gain.

Double-sided processing—processing both before and after the InP wafer bonding to silicon—provides access to both sides of the high-confinement waveguiding layer for further design cleverness in miniaturization and performance enhancement. Figure 5(c) shows

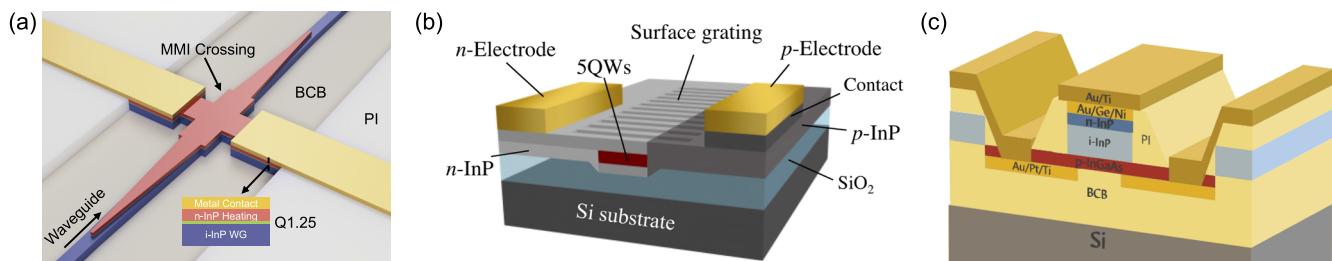


FIG. 5. Miniaturized membrane InP components with active functions. (a) A 13- μm -long phase shifter. Reproduced with permission from Wang *et al.*, *J. Lightwave Technol.* **41**(6), 1790–1800 (2023). Copyright 2023 IEEE. (b) A membrane laser with a surface grating-based cavity. From Takahashi *et al.*, 2022 *IEICE Society Conference Proceedings*. Copyright 2022 IEICE. Reproduced with permission from IEICE. (c) A miniaturized waveguide-coupled UTC-PD. de Graaf *et al.*, *IEEE J. Sel. Top. Quantum Electron.* **28**(2), 3802010 (2022). Copyright 2015 Author(s), licensed under a Creative Commons Attribution 4.0 License.

the cross-sectional structure of a waveguide-coupled uni-traveling-carrier (UTC) PD with an ultrasmall footprint of only $2 \times 5 \mu\text{m}^2$ and a decent responsivity of 0.6 A/W .¹⁴² Double-sided processing allows the metal contacts to be on both sides of the membrane, minimizing the junction-contact access distance from a few μm to below 100 nm and thereby reducing the device footprint. The decrease in such access distance additionally reduces series resistance and allows for a reduced RC time constant. An ultra-low 4 fF capacitance and $<10 \Omega$ series resistance have been achieved, enabling broadband operation of over 110 GHz .

2. Miniaturization of optical I/O

Optical input/output (I/O) options include both end-fire and out-of-plane couplings for membrane-based platforms. With high optical confinement, the opportunity is now to simplify off-chip optics by managing beamforming within the chip, emphasizing component miniaturization at the diffraction limit. Examples of out-of-plane-coupled I/O interfaces are shown in Fig. 6. Figure 6(a) shows SiO₂-on-InP grating antennas¹⁴³ developed for optical beam steering applications, e.g., LiDAR. Leveraging the high dry etching selectivity (>30:1) between SiO₂ and InP, robust critical dimension control is attained in the SiO₂ gratings on top of the InP waveguide. This enables mm-scale emission apertures and an ultra-narrow beam divergence of 0.05° with a 2-mm long antenna.¹⁴³ For optical fiber interfacing, grating couplers of around $10 \times 12 \mu\text{m}^2$ ^{113,115} footprint are designed to accommodate the mode size of a single-mode fiber. Metal reflectors placed beneath the membrane, fabricated via the double-sided processing technique, are designed to boost the coupling efficiency by reflecting and combining the downward emission in-phase with the upward emission. A $1.2 \text{ dB}/\text{interface}$ coupling loss is measured with the metal reflector,¹⁴⁴ as compared to 3 dB for the reflector-free designs.^{113,115} The techniques have been used for optical wireless wavefront receivers, where the interfacing elements are further downsized to $3 \times 4 \mu\text{m}^2$,¹¹³ as seen in Fig. 6(c).

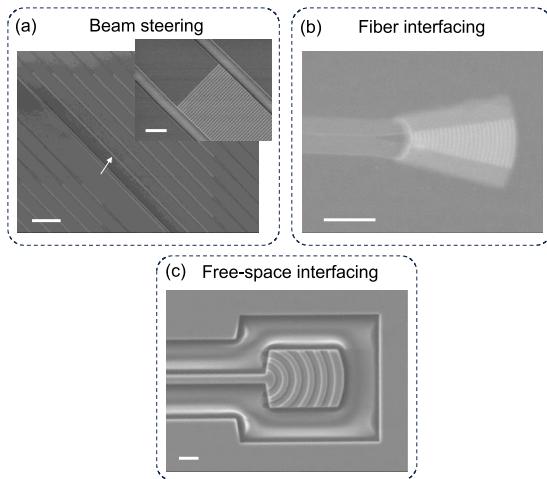


FIG. 6. SEM images of membrane-based miniaturized optical I/O elements. (a) Grating antennas for beam steering.¹⁴³ The arrow indicates the grating section. Scale bar: $200 \mu\text{m}$. Inset: Zoom-in image of the grating. Scale bar: $5 \mu\text{m}$. (b) A grating coupler for fiber interfacing.¹⁴⁴ Scale bar: $10 \mu\text{m}$. (c) A receiver element for free-space interfacing applications.¹¹³ Scale bar: $1 \mu\text{m}$.

B. Nanophotonic approaches

Apart from the size reduction in the waveguide cross section, nanophotonic approaches can also be employed for InP-based active components miniaturization. This can include the use of slot waveguides, plasmonics, and photonic crystals. Here, for comparison purposes, a state-of-the-art InP bulk waveguide-based component is first described, followed by possible miniaturization directions leveraging nanophotonics. Figure 7(a) shows a dense 100 GHz -class MZM array¹⁴⁵ on a semi-insulating InP substrate. Through the adoption of narrow coplanar stripline electrodes, the width of each MZM is only $17 \mu\text{m}$ and the array pitch is $27 \mu\text{m}$. A $V_{\pi}L$ of 7.5 V mm is measured with a device length of 1 mm , and optimizations in the active layer stack are expected to enable an efficiency of below 2 V mm .

Slot waveguides offer stronger light-matter interactions through enhanced confinement in the slot. Modulators based on slot waveguides filled with EO polymers can achieve sub-1 V mm-level $V_{\pi}L$.^{13,15} Chemical optimization of the polymers' EO activity strength further allows the realization of a $V_{\pi}L$ of 0.32 V mm ¹⁴⁶ and a short interaction length of $280 \mu\text{m}$ ¹⁴⁷ in separate experiments. An InP-based polymer slot waveguide modulator is shown in Fig. 7(b).¹⁴⁸ As a preliminary study, only an EO polymer focusing on thermal stability but with an order of magnitude lower EO activity is used, resulting in a measured $V_{\pi}L$ of 4.5 V mm with a device length of $500 \mu\text{m}$. From a performance perspective, the benefit of using InP slot waveguide instead of Si slot waveguide lies in InP's higher electron mobility and lower material loss induced by dopants. This potentially offers a lower access resistance to the EO slot, allowing for a higher RC bandwidth^{149,150} without compromising the component's insertion loss.

Plasmonic slot waveguides present one step further confinement enhancement, where >90% optical confinement is possible.¹⁴⁸ This is a nearly threefold improvement when compared to an InP slot waveguide on the same platform. The plasmonic slot waveguide also significantly improves the electrical field intensity and offers a conductivity far better than semiconductors, with which superior RC time constants can be expected. These features allow plasmonic-organic-hybrid modulators^{18,151–153} to approach a bandwidth as high as 500 GHz with a length of $20 \mu\text{m}$ ¹⁵¹ and a $V_{\pi}L$ of 0.04 V mm .¹⁵⁴ Figure 7(c) shows such a fabricated plasmonic MZM interfaced with InP membrane photonic circuits. As a first attempt and proof-of-concept, a slot width of 250 nm is used, and the same EO polymer is used as in the device shown in Fig. 7(b). A narrower slot can be achieved using high-resolution fabrication techniques, such as metal etching. The device measured a low $V_{\pi}L$ of 0.44 V mm with a short $10 \mu\text{m}$ -long plasmonic-organic section. Further iterations on the design parameters and polymer selection could potentially bring this to be on par with the state-of-the-art.¹⁴⁸ However, it is important to note that the performance of plasmonic modulators does not come at no cost—reducing the optical loss of the plasmonic mode remains an open challenge. The insertion loss of components has a significant impact on defining the maximum possible scale of the photonic circuit, and a poor optical performance will lead to additional energy used in the transceiver electronics. In this device, we measure a propagation loss of $0.43 \text{ dB } \mu\text{m}^{-1}$, which is similar to that of the state-of-the-art.^{18,153} This translates to $4\text{--}5 \text{ dB}$ loss for a $10 \mu\text{m}$ -long plasmonic-organic section, which is much higher than conventional EOMs. By employing resonating structures, amplitude

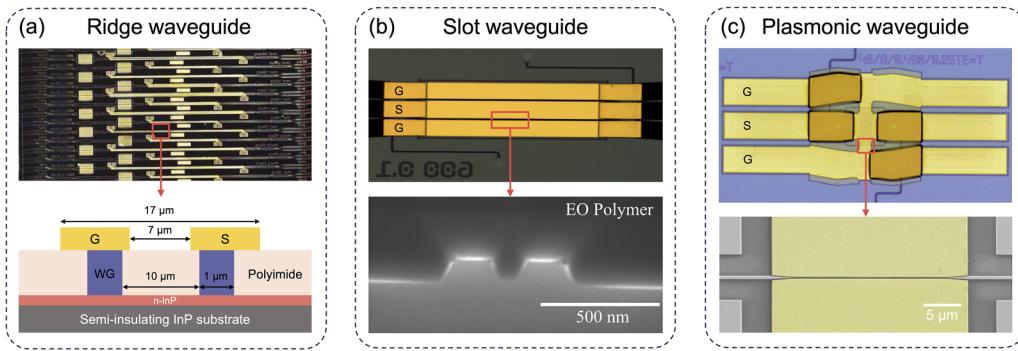


FIG. 7. Modulator miniaturization by efficiency enhancement. (a) Microscope image of an MZM array with schematic showing the ridge-waveguide-based cross section and layout optimization. (b) Microscope image of a fabricated slot-waveguide-based MZM with a zoom-in SEM image of the slot cross section. Reproduced with permission from Reniers *et al.*, IEEE J. Quantum Electron. **57**, 0600306 (2021). Copyright 2021 IEEE. (c) Fabricated plasmonic MZM and a zoom-in, false-colored SEM image of the 20 μm long plasmonic waveguide modulator.

modulation can be achieved with a much lower loss, where a 1.2 dB on-chip loss has recently been reported,¹⁸ but accurate wavelength alignment is needed to ensure the extinction ratio.

Metallic cavities potentially offer an opportunity for laser miniaturization into the plasmonic regime.¹⁵⁵ In addition, the excellent thermal conductivity of metals facilitates heat extraction from miniaturized devices, where hotspots are easier to form when compared to macroscopic devices. The first demonstration of such a nanolaser working in the hybrid photonic-plasmonic regime was realized in 2007, with gold-coated semiconductor nanopillars based on InP.¹⁵⁶ The pillar diameter is in the order of 200 nm. The nanolaser exhibited continuous-wave lasing under electrical pumping at 77 K temperature. Low-loss silver cladding enabled a nano-light-emitting diode with its optical output coupled to a waveguide in the same InP membrane.¹⁵⁷ For nanolasers, one challenge is the increased surface/body ratio lowering the carrier injection efficiency. Advanced surface passivation methods may enable room temperature continuous wave lasing. In 2017, an ultra-low surface recombination velocity of 260 cm s^{-1} is demonstrated by the combination of $(\text{NH}_4)_2\text{S}$ treatment and SiO_2 encapsulation. As a result, an 80-fold enhancement is observed in the photoluminescence strength of the gain medium as compared to the non-passivated case.

Photonic crystal structures can provide ultrahigh optical confinement in all directions via photonic bandgap engineering. This has already been pioneered for vertical cavity surface emitting lasers, but in-plane photonic crystal lasers, which are suited to planar integration, have been realized more recently utilizing suspended InP membrane structures.¹⁵⁸ Initially, only optical pumping was demonstrated,¹⁵⁶ but electrical pumping schemes are now also available through lateral current injection¹⁵⁹ or carrier injection along the light propagation direction,^{160,161} since the laser cavity is just a few micrometers long. Direct modulation on these microlasers shows 4.4 fJ bit^{-1} energy consumption with the laser operating at 10 Gbit s^{-1} .¹⁵⁹ Miniaturization of SOAs has also been demonstrated using photonic crystal waveguides. Enhanced by the slow-light effect, up to 8 times higher gain per unit length is achieved.¹⁶² So far, optical pumping has been demonstrated. Electrical pumping will require further reductions in the electrical resistance of the cur-

rent path, without introducing detrimental optical loss via doping or metal contacts.

IV. AREAL OPTIMIZATION

A. Active–passive integration

Butt-joint regrowth has been the most widely used industry approach to monolithic active–passive integration schemes in InP PICs due to its design flexibility and ability to combine multiple material bandgaps^{31,38} and component types. At high packing densities, the edge growth rate enhancement effect^{163,164} must be taken into account, which degrades the material quality near the interface by introducing topology and compositional (i.e., bandgap) variations.¹⁶⁵ This effect leads to design limits on the maximum regrown area and the minimum spacing between adjacent regrown areas and, therefore, generates nonfunctional chip areas and constrains the achievable packing density. In practice, less than 30 μm active stripe width and greater than 200 μm spacing are typically required in the regrown areas to achieve a sufficiently suppressed growth rate enhancement for onward lithography. The spacing has been reduced to 50 μm ¹⁶⁶ for Fabry–Perot lasers with low-optical confinement waveguides. Growth rate enhancement should be given particular attention in high-confinement components and waveguides, where the optical mode is more sensitive to topology variations.

A butt-joint regrowth technique has been developed for arbitrary active component separation using an innovative open-mask approach.^{167,168} The conceptual process flow of such open-mask butt-joint regrowth is illustrated in Fig. 8(a). Steps 1 and 2 are implemented as per prior butt-joint regrowth techniques to define the active mesa and remove unwanted active materials. In step 3, the center of the mask is now opened to trap the excess reactive species, which would otherwise contribute significantly to the growth rate enhancement through vapor-phase diffusion. In our approach, these species are deposited in a controlled manner in the opening, as depicted in step 4. A selective wet-etch can then be leveraged to remove the excessive material grown during the previous step. To achieve this, selective wet etch-stops may be inserted. Leveraging this approach, the growth rate enhancement constraints are lifted,

since the functional area size is decoupled from the actual masked size during epitaxy. As a preliminary verification, a $0.5 \times 1.7 \text{ mm}^2$ MQW-based active area is integrated with a passive i-InP material in the same horizontal plane using this technique.¹⁶⁷ Figure 8(b) shows the cross-sectional SEM image of such a butt-joint structure. The growth rate enhancement measured is of the same level as narrow stripes of $10 \mu\text{m}$ width. As this method involves “zero change” to the reactor parameters, it affords high flexibility in the circuit floorplan: normal masks for discrete components can be combined conveniently with open masks for high-density arrays. In the following process, both discrete and densely arranged components can be fabricated simultaneously, as seen in Fig. 8(c). From a purely topological perspective, an active component density of over 10^2 mm^{-1} may be achieved using this method.

B. Heat dissipation

Heat dissipation is a limiting factor to the packing density. Membrane photonic components have relatively poor thermal dissipation when low-thermal-conductivity bonding polymers

and dielectrics are used in the claddings. Thermal impedances of $500 \mu\text{m}$ -long membrane lasers and SOAs with dielectric claddings are measured to be in the range of $100\text{--}200 \text{ K W}^{-1}$ ^{135,169} while polymer-cladding-based devices can reach a thermal resistance of $300\text{--}500 \text{ K W}^{-1}$.^{170,171} This level of thermal resistance will typically result in an elevated core temperature if actives are densely packed and under high current injection. Figure 9 shows the simulated cross-sectional temperature distributions of a dense membrane SOA array of $10 \mu\text{m}$ pitch, under the injection current density of 2.3 kA cm^{-2} , in the cases of without and with thermal shunting to the Si substrate.¹⁷² The thermal shunt can be made with high thermal conductivity materials, such as metals. In this particular simulation, a 200 nm -thick shunt made of gold helps decrease the core temperature by 23 K , from 346 K (73°C) to 323 K (50°C). Direct bonding or bonding with a thin adhesion layer to a high-thermal-conductivity, low-index substrate has also been proposed as a viable solution to efficient heat sinking.^{173\text{--}175} It is worth noting that membrane active components often require less electrical power than their substrate-based counterparts, since they can offer higher

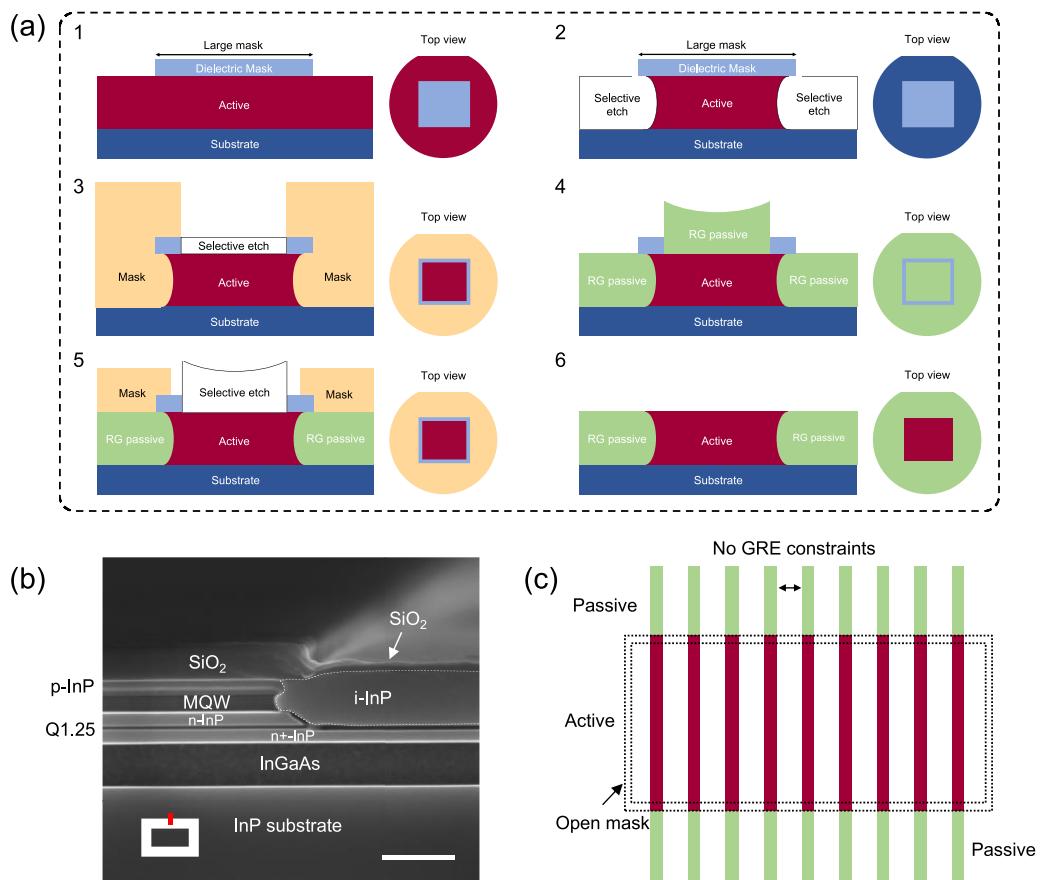


FIG. 8. Regrowth process for large-scale dense integration. Reproduced with permission from Wang *et al.*, Opt. Mater. Express 11(8), 2478 (2021). Copyright 2021 Optica Publishing Group. (a) Conceptual process flow. (1) Mask deposition. (2) Selective wet-etch. (3) Mask opening. (4) Regrowth. (5) Selective removal of excess material. (6) Mask removal. (b) Stain-etched cross-sectional SEM image at the interface of a $0.5 \times 1.7 \text{ mm}^2$ active area with regrown passive i-InP. The SiO₂ mask is still present. The cross section slice location is depicted in red at the bottom left inset. Scale bar: 500 nm. (c) Dense active–passive integration within a large regrown area.

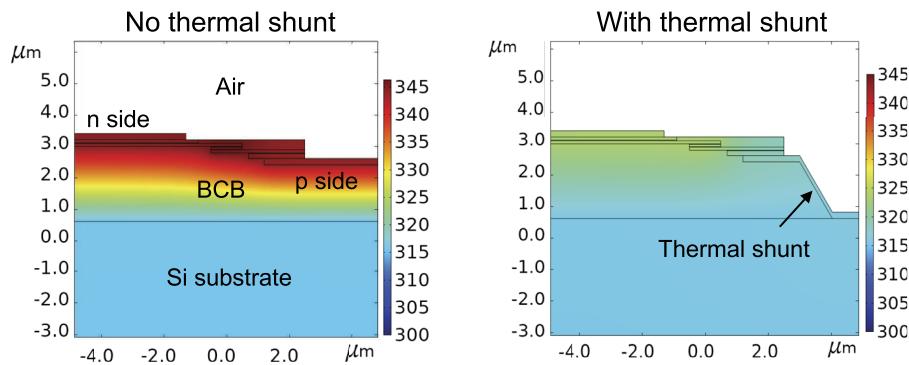


FIG. 9. Simulated temperature distributions of a membrane SOA without and with thermal shunt to the Si substrate.¹⁷²

efficiency through enhanced optical confinement. When combined with improved heat sinking, superior performance can be attained. One example is a membrane laser bonded to a SiC substrate with a thin 40 nm bonding layer.¹⁷³ Simulation shows sub-100 K W⁻¹ thermal resistance with a short length of 50 μm , facilitating the small differential gain reduction at high injection currents.¹⁷³ This further allows for the realization of the record-high 108 GHz bandwidth with direct modulation.

C. Electrical I/O

Electrical I/O density can be a limiting factor to the efficient use of chip area, especially with functionally complex active–passive PICs. Many VLSI applications are also I/O-intensive, e.g., photonic computing and switching. The microelectronics industry employs multi-layer metal interconnects with flip-chip packaging or hybrid assemblies.¹⁷⁶ The same method should also be leveraged to boost the interconnect density of InP PICs. Figure 10(a) shows the frontside multi-layer transmission lines¹⁷⁷ realized on an InP substrate for photonics devices. Apart from the extra degree of spatial freedom, the RF performance of the transmission lines could be improved since they are moved farther away from the lossy semiconductor. With the native substrate removed, the membrane-based cross section additionally allows for backside I/O, as depicted in Fig. 10(b). This is conceptually similar to the backside power delivery technology¹⁷⁸ for digital EICs and could further boost I/O density by separating the bias delivery from signal delivery. Electronic co-integration could potentially simplify electrical I/O by reducing the

number of connections to external electronic systems.¹⁷⁹ As a proof-of-concept, InP-based MZMs integrated with an on-chip driver made of InGaAs metal–oxide–semiconductor field-effect transistor (MOSFET) have been demonstrated.¹⁸⁰

V. WAFER SIZE

To date, InP PICs are manufactured on wafers with diameters up to 100 mm, while 150 mm wafers are transitioning from R&D to production.⁹⁵ In March 2024, the world-first 6-inch InP optoelectronics fab is announced by Coherent Corp. Current demand from the photonics market is satisfied with volume production on 100 mm wafers,^{95,181} but emerging VLSI applications may strengthen the transfer toward larger InP wafers. Apart from this economic driver, the technological motivation for wafer size scaling is the adoption of advanced process equipment used in microelectronics, with which better uniformity and process control can be achieved.¹⁸² High-quality membrane InP waveguides with loss figures¹²¹ comparable to that of SOI photonics⁷⁵ are now demonstrated with DUV scanner lithography on 75 mm wafers. However, with the emphasis having been on Si microelectronics, equipment innovation has primarily targeted wafer diameters of over 200 mm.

Various approaches have been proposed to expand InP PICs to 200 mm and beyond. Table I summarizes the state of the art and challenges for notable approaches. The most widely reported technologies are flip-chip bonding and heterogeneous die-to-wafer bonding (referred to as die-bonding hereafter). III–V die flip-chip

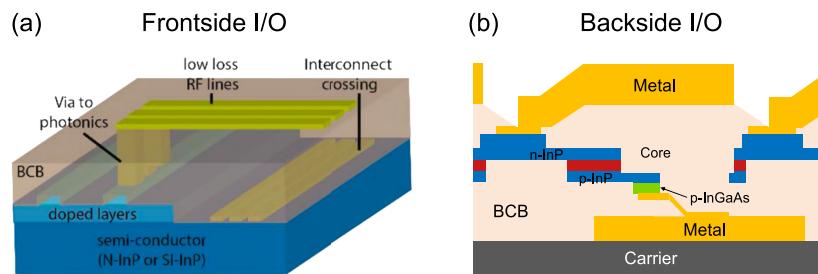


FIG. 10. (a) A multi-layer electrical I/O.¹⁷⁷ (b) Back-side electrical I/O with InP membrane technology.

TABLE I. Technologies for expanding InP PIC wafer sizes.

Technology	Readiness	Wafer size (mm)	Key current challenges
Flip-chip	High	300 ²¹	High topology, throughput, inter-die mechanical conflict
Die-bonding	High	200 ¹⁸⁴	Inter-die mechanical conflict
Wafer-bonding	Mid	75 ¹¹⁵	Demonstration of 100 mm and beyond
SmartCut™	Mid	200 ¹⁸⁵	Demonstration of epitaxy after substrate transfer
μTP	Mid	200 ¹⁸⁶	Mechanical alignment
Heteroepitaxy	Low	300 ³⁰	Electrically pumping and coupling to membrane waveguides

bonded to 300 mm wafers have been demonstrated by IMEC,^{21,183} while die-bonding has been primarily commercialized by Intel on its 200 mm platform.¹⁸⁴ Flip-chip bonding creates a high topology, which may hinder further 3D electrical packaging, an especially important technology for large-scale circuits. Flip-chip bonding also requires sequential alignment of each processed InP die, bringing challenges in throughput scaling. The die-bonding technology circumvents these challenges by removing the substrate to create a membrane-like cross section and then doing post-transfer lithography. However, it still had the same challenge of mechanical conflict between adjacent dies, limiting the density when a diverse range of active/passive components are to be integrated.

Technologies in the R&D phase include wafer-to-wafer bonding (referred to as wafer-bonding hereafter), micro-transfer printing (μTP), SmartCut, and III–V on Si heteroepitaxy. The wafer-bonding technology removes the risk of inter-die mechanical conflict by providing all photonic functions in one membrane,¹¹⁵ but current demonstrations are still limited to 75 mm. Further expansion would require larger donor wafers. The SmartCut technology,¹⁸⁷ which is used to manufacture SOI wafers, is a potential candidate to realize the expansion of InP membranes without needing larger native substrates. In this approach, multiple source InP wafers are first cut and tiled onto a larger substrate to produce a pseudo-donor wafer. Then, H⁺ ion implantation is performed to define an in-depth splitting layer in the InP tiles of the pseudo-donor. Afterward, the pseudo-donor is flipped and bonded to a receiver wafer. After annealing, in-depth splitting then happens at the implanted depth, leaving thin InP membranes on the large receiver wafer. Finally, polishing is performed on the receiver wafer to obtain a device-ready surface. The pseudo-donor can be recycled and utilized in the fabrication of a new wafer. The state-of-the-art demonstration of this technology is with 200 mm Si wafers.¹⁸⁷ To support active components, transfer after epitaxy or epitaxy after transfer is required. μTP²⁴ represents another effort to scale InP with the help of Si substrates. In this approach, active components are first fabricated on the donor InP wafer, and then, only the components themselves get transferred and printed to the receiver wafer with high parallelism, allowing for scalability and potential recycling of the III–V material. However, still fine mechanical alignment is required for the optical interfaces. This technology is explored by a few institutes across the globe, including Tyndall¹⁸⁸ and IMEC.²⁴ Our ongoing INSPIRE project^{186,189} aims at delivering a foundry-compatible 200-mm plat-

form with foundry InP actives combined with low-loss SiN passives. Leveraging coupon-based transfer, much higher integration densities can potentially be enabled, facilitating VLSI realizations. Finally, direct heteroepitaxy of a III–V material on Si, an approach believed to have potentially the highest scalability,¹⁹⁰ is an active area of research. From an epitaxy perspective, the biggest challenge is the mismatches in the lattice constants, thermal expansion coefficients, and crystal polarities between Si and III–V.¹⁹¹ Mitigation methods, such as buffer layers and growth in confined areas, create device-level challenges, such as electrical pumping if grown in confined areas and coupling to high-confinement waveguides if grown on thick buffer layers. Epitaxially grown InP lasers on 300-mm Si wafers have already been demonstrated with optical pumping in 2015,³⁰ but the aforementioned issues are still to be addressed at the present time. In summary, multiple approaches to creating InP membranes on 200 and 300-mm wafer sizes already exist at low to mid-readiness levels. Some of them, if not all, are expected to mature rapidly in the coming 5–10 years, facilitating high-volume, large-scale, and high-density applications.

VI. CONCLUSION

In this paper, we have reviewed the historical scaling trends for photonic integrated circuits. High levels of integration are appearing in the literature, but this has so far been constrained to circuits with functionally identical building blocks. In contrast, platforms with the most sophisticated and comprehensive range of building blocks are now lagging due to the challenges of onward scaling. Nonetheless, emergent use cases for complex combinations of active and passive components for communications, computation, and sensing are expected to drive renewed interest in high-complexity and high-performance integration platforms.

Emerging membrane-based platforms using indium phosphide are offering powerful scaling perspectives through cross-sectional miniaturization and areal optimization. Miniaturized modulators and lasers are now being developed with lengths in the order of tens of micrometers. Membrane SOAs and multipass SOAs show the potential for high optical gain and high efficiency with a reduced length. Areal optimization provides a systematic approach to enhance InP active integration density by orders of magnitude through advanced butt-joint regrowth, heat management, and I/O

optimizations. Wafer size expansion beyond the native substrate additionally offers a route toward high volume and sustained scaling.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Yi Wang: Conceptualization (lead); Data curation (lead); Investigation (lead); Visualization (lead); Writing – original draft (lead); Writing – review & editing (equal). **Yuqing Jiao:** Conceptualization (lead); Funding acquisition (lead); Supervision (lead); Writing – review & editing (lead). **Kevin Williams:** Conceptualization (lead); Funding acquisition (lead); Supervision (lead); Writing – review & editing (lead).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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