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Large-scale photonic processors and their applications

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Digital electronics have been essential in all technological breakthroughs over the past decades, from the advent of the internet to the miniaturization of portable devices with ever-increasing capabilities. While they continue to drive technological innovation, certain applications demanding extraordinary bandwidth and performance reveal the need for complementary emerging technologies. Photonics is particularly well-suited for this purpose, leveraging light to process large volumes of information with minimal latency. The scalability of photonic integrated circuits (PICs) is advancing rapidly, with increasing numbers of actuators improving performance and extending applicability across different domains. Analyzing two decades of development, this study extracts the scalability laws guiding photonics evolution, doubling every two years and predicting a transition from hundreds to 10^5 actuators in PICs within six years. We also tackle key challenges and emphasize the crucial synergy between electronics, software, and photonics, which will determine the market penetration and industry impact of large-scale photonic processors.

The unique combination of research, technology and economics has made the use and application of electronic chips universal and pervasive. Major technical breakthroughs over the last 60 years in architectures, design, and fabrication processes and the mutually reinforcing economic cycle of general-purpose technologies enabled the shift from application-specific integrated circuits to general-purpose electronic programmable devices with ever-increasing processing power[1,2]. However, during the last decade, current and emerging application fields have been pushing the limits of integrated electronics, demanding growing signal-processing and computing capabilities in terms of bandwidth, speed rates, low-form factor and power consumption, scalability, versatility, and adaptability. Some examples of driving technologies include 5 G/6 G communications[3], the Internet of Things (IoT)[4] car-to-car communication[5], high-tech medicine[6], artificial intelligence[7], neuromorphic and quantum processing[8].

While electronic integration has advanced steadily for over five decades, fundamental physical limits at the nanoscale—such as quantum effects—are increasingly challenging its cost-effective future evolution. This has led to a re-transition towards complex application-specific engines like Graphic Processing Units (GPUs) or custom Artificial Intelligence (AI) hardware. Furthermore, most of these applications will require electronics to symbiotically team up with complementary technologies to meet short and mid-term requirements[9]. Integrated photonics is an ideal option for this. The technology that enables the generation, processing, distribution and detection of light signals brings complementary features (large bandwidth, low latency, low losses, and parallelism via wavelength multiplexing) and can be integrated on chip[10]. Through the integration of optical sources, waveguides, modulators, passive components and photodetectors, integrated circuits have been proven successful for a myriad of applications but only a few fields such as transceivers and data center interconnection have shown enough fabrication volume to justify the high non-recurring engineering costs, including fab infrastructure, assembly process development, and yield optimization[11,12].

Similar to the trajectory of electronics, software-defined photonics emerges as an innovative paradigm in hardware configuration. By orchestrating the control of many actuators, these systems exert precise control over the path and properties of light within a chip[13,14]. This versatility engenders a spectrum of architectures, designed to suit distinct applications, capitalizing on their intended functionality and adaptability. Notably, moderate-scale processors have showcased considerable promise in realms such as microwave photonics, signal acceleration for machine learning inference hardware, and quantum and optical signal processing processing[15–17]. However, current moderate-scale photonic processors often fall short of the system-level complexity and functional flexibility required by emerging applications. This gap stems from a combination of hardware and software constraints—such as limited optical port counts, signal degradation, reconfiguration speed, easy-integration Application Programming Interfaces—that vary significantly depending

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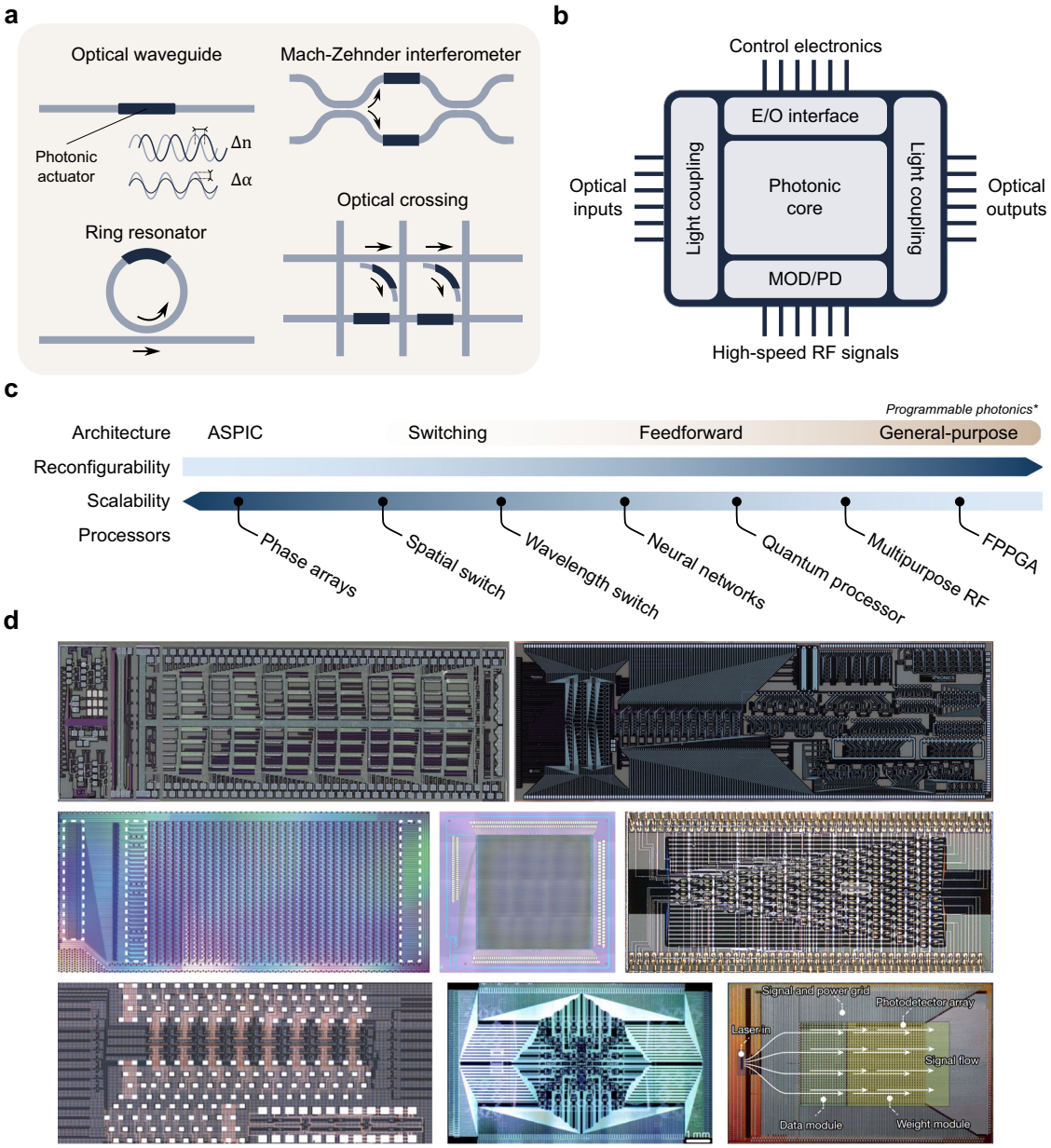

Fig. 1 | Photonic integrated circuits description. a Definition of a photonic actuator and different types of programmable unit cells. **b** Schematics of the photonic processor, including both optical I/O and electronics for driving, monitoring and high-speed processing. **c** Architectures of photonic processors as a function of their level of reconfigurability and scalability. **d** Examples of photonic chips for various applications, arranged from left to right and top to bottom, tunable beamformer[34] (160 PAs), general-purpose radio-frequency processing[35] (576 PAs), polarization-insensitive switching[38] (2048 PAs), large-scale LIDAR[39] (12480 PAs), neuromorphic computing[7] (176 PAs), wavelength selective switch[37] (64 PAs), programmable topological processor[36] (300 PAs) and matrix multiplier[40] (8320 PAs). Images taken with permission from the given references.

on the use case. Bridging this gap will require the transition to large-scale integration—i.e., photonic processors with tens of thousands of actuators, scalable performance, calibration strategies, and software-defined control stacks tailored to specific application domains in communications, networking, and computing[18].

In this work, we aim to provide insight into the scalability laws that will shape the photonics evolution in the coming years, as well as the potential applications where this anticipated level of integration will meet market demands. First, we define the photonic actuator as the key primitive element shared among all processors, and next we outline scaling ranges for medium, large, and very large-scale photonic circuits. In this context, we foresee a transition from circuits currently integrating hundreds of actuators to those accommodating 10^5 actuators within the next six-year period. Lastly, we identify and analyze the primary challenges that photonics technology must confront, along with the implications of this trend across several markets and use cases.

Results

Photonic integrated processors

Photonic circuits can be reconfigured by suitable control of their photonic actuators (PA). In these components, light waves can be phase-shifted or attenuated depending on modifications to either the real or imaginary part of the material refractive index[19,20]. Photonic actuators can be combined with power splitters and combiners to form programmable unit cells[21] (PUCs) such as 2 × 2 Mach-Zehnder interferometers (MZI), ring resonators (RR) or crossing arrays (see Fig. 1a). Together with other passive

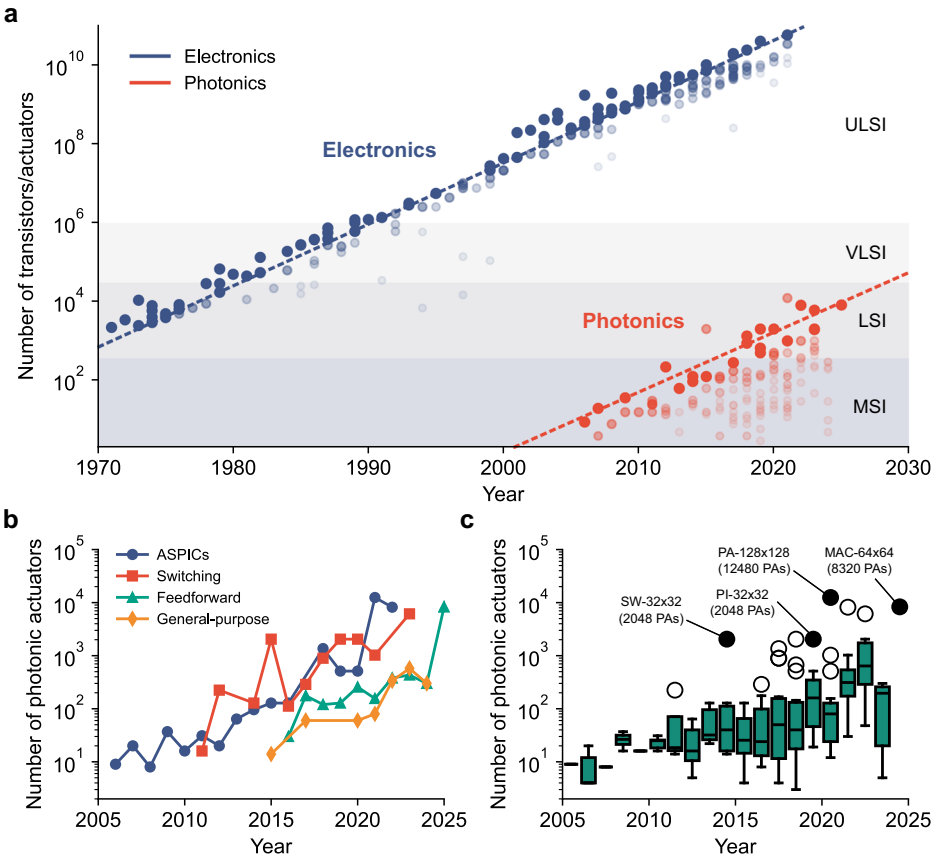

Fig. 2 | Timeline of photonic processors. **a** Evolution in the number of photonic actuators per year and exponential fitting of the progression versus electronics. We observe that the number of photonic actuators doubles every 24 months. A maximum of three actuators per year for the fitting is considered for the fitting. Integration margins of medium-scale integration (MSI) from 10 to 500 actuators, large-scale integration (LSI) from 500 to 20,000 actuators, very large-scale integration (VLSI) from 20,000 to 1,000,000 actuators and ultra-large-scale integration (ULSI) more than 1,000,000 actuators are highlighted in shaded area. **b** Evolution over the years in the number of actuators for different types of photonic processor architectures and **c** a boxplot showing the annual distribution of photonic actuators. Four notable examples are highlighted: (1) the first large-scale 32 × 32 switch[56] (SW-32 × 32 with 2048 PAs), (2) the first large-scale polarization-insensitive 32 × 32 switch[38] (PI-32 × 32 with 2048 PAs), (3) the largest integrated phased array to date, featuring a 128 × 128 configuration[39] (PA-12480 with 12,480 PAs), and (4) the highest matrix size multiplier, a 64 × 64 mesh[40] (MAC-64 × 64 with an extrapolated total of 8320 PAs).

components, they serve as fundamental blocks for building more intricate photonic circuits within the core of a comprehensive optical system. In this study, we focus on the number of PAs, as they play a crucial role in adding functionality and enabling the reconfiguration of PICs. This analysis also offers valuable insights into how electrical input and output (I/O) and packaging strategies need to evolve to address scalability challenges effectively. A generalized view of a photonic integrated processor is illustrated in Fig. 1b, comprising optical fan-in and fan-out stages where light is coupled into the chip, along with optional interfaces for high-speed radiofrequency (RF) signals utilizing modulators and photodetectors[22]. Control electronics are responsible in these systems for the overall orchestration by directly controlling each photonic actuator to provide the system-level functionality. It should be emphasized, however, that each PA has a different tuning control and precision, which can impact the performance of the photonic system and limit its scalability.

Photonic processors can be classified into four main types based on architecture, reconfigurability, and intended functionality: application-specific photonic integrated circuits (ASPICs), switches, feedforward meshes, and general-purpose processors (see Fig. 1c). ASPICs are not designed for reconfigurability but for fixed functions such as beamforming, filtering, or microwave photonic links. While generally rigid, some like optical phased arrays, offer high scalability through dense integration of phase shifters[23,24]. Other examples of ASPICs include beamformers, microwave photonic links and reconfigurable filters[25–28]. Switches provide higher reconfigurability by enabling dynamic light routing through fixed mesh architectures. These systems mimic electronic switching fabrics and are programmed to control signal paths without modifying core hardware[29,30]. Feedforward meshes implement mathematical transformations using cascaded interferometers with controllable amplitude and phase. They support complex signal processing tasks but require sophisticated calibration and control systems[31,32]. General-purpose processors offer the highest flexibility, capable of emulating other architectures through programmable, often recirculating, photonic meshes of interferometers. While versatile, they face scalability challenges due to increased control complexity and hardware overhead[33]. Figure 1d presents representative chip examples across all four categories including tunable beamformers[34], general purpose RF and topological processors[35,36], large-scale switches[37,38], densely integrated phase arrays[39], and matrix multipliers for AI acceleration hardware[7,40], with an integration density ranging from few hundreds of actuators to several thousands.

Scalability trends

Similar to the evolution seen with transistors in electronics, photonic actuators are shrinking in size, which allows for high-density integration and enhanced functionality of large-scale processors. Figure 2a shows this temporal evolution, revealing a pronounced exponential surge in the count of photonic actuators over the past two decades, doubling approximately every two years. This trend mirrors the trajectory observed in electronics, as described by Moore's Law more than 5 decades ago[41,42]. Today, photonic processors fall within the so-called large-scale integration (LSI) process, employing between 500 and 20,000 actuators in a single chip. According to the trend, it is anticipated that very large-scale integration (VLSI), exceeding 20,000 actuators, will be reached before the end of the decade, around 2028. Furthermore, by approximately the year 2032, photonics technology is projected to support the integration of up to 10^5 functioning actuators, which would be a significant advancement of the whole ecosystem.

Figure 2b illustrates the progression of processor architectures, showcasing their direct influence on the proliferation of photonic actuators throughout the years. Between 2005 and 2010, simple PICs emerged, integrating fewer than 50 actuators, with limited reconfigurability and primarily focused on applications such as optical filtering, tunable delay lines, and low-scale phase arrays[43–46]. Over the next five years, switching architectures garnered increasing attention

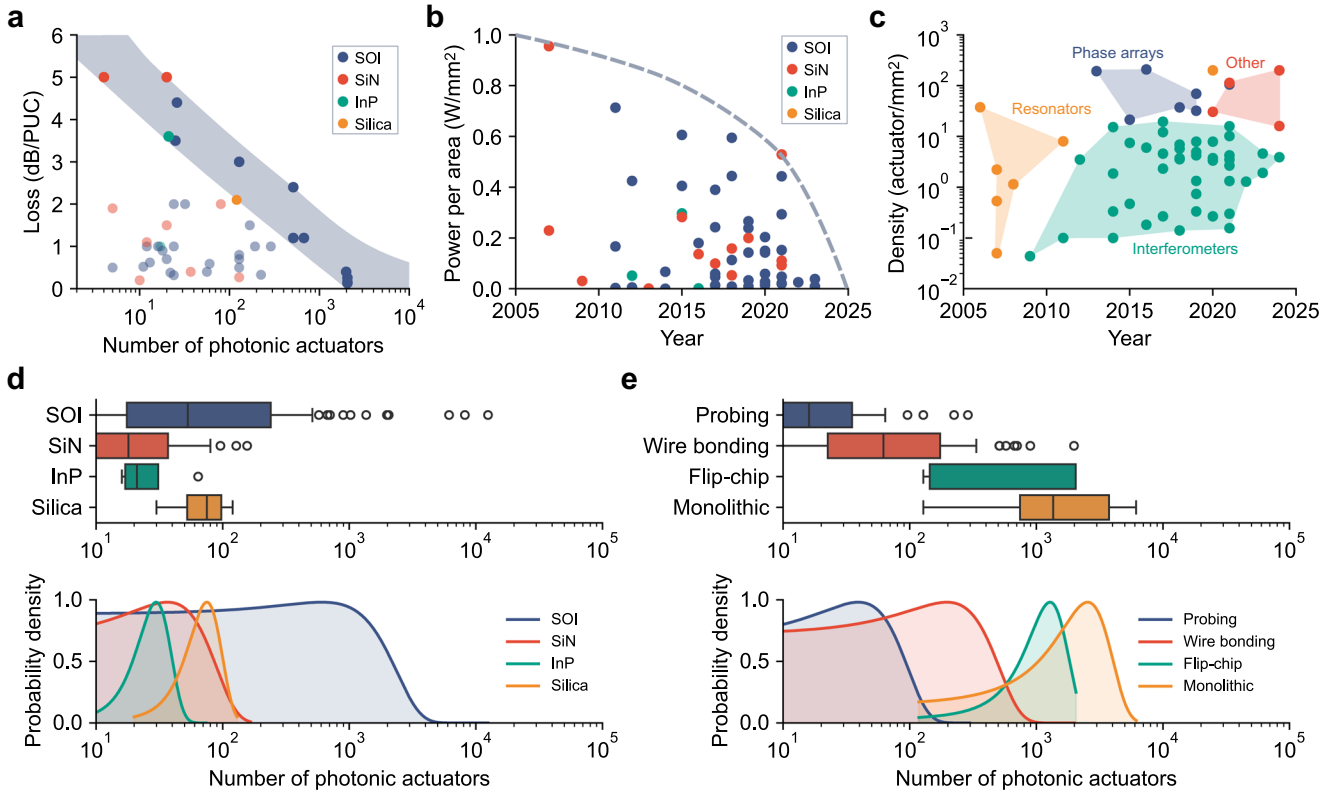

Fig. 3 | Trends of photonic processors. a Insertion loss of the programmable unit cell per number of photonic actuators. The two data points with the highest values relative to the number of actuators are highlighted. An improvement in the loss is observed as the number of actuators increases. **b** Power consumption of the processor per square millimeter. A reduction in the power per area is observed by the dashed envelope line as a result of the improvement in the energy efficiency of the actuators. **c** Actuator density per year for different PUCs based on resonators, Mach-Zehnder interferometers, high-density phase arrays and other: MEMS-based crossing arrays, PCM and bimodal waveguides. **d** Box plot of the material platforms as a function of the number of actuators and probability density representation, upper and lower graphs, respectively. **e** Box plot for different electrical driving technologies as a function of the number of actuators and probability density representation, upper and lower graphs, respectively.

and rapidly became the PICs with the highest numbers of integrated actuators[47–55]. In 2015, Tanizawa et al. demonstrated a 32 × 32 on-chip optical switch with 1024 tunable MZIs and 2048 integrated actuators[56]. By the same year, two new processor architectures emerged, employing feed-forward meshes and general-purpose architectures. The degree of programmability has significantly increased, enabling new applications such as optical matrix multiplication for hardware accelerators or quantum information processing[57,58]. In 2017, Shen et al. published the first paper on neuromorphic computing using a programmable PIC with a feed-forward processor containing 176 thermo-optic actuators[7]. More recently, in 2023, Wang et al. reported a quantum photonic device with over 4000 passive and active components and 216 actuators[59]. Similarly, in 2023 Pérez-López et al. introduced the largest-scale general-purpose processor to date, featuring an array of 304 photonic actuators, and demonstrating its prowess in advanced radio-frequency applications[35]. So far, to the best of our knowledge, the programmable processor with the highest number of photonic integrated actuators is a phase array with 12,480 MEMS-based devices reported by Zhang et al.[39]. However, it is worth noting that scalability is more significant in some applications than others, for example, in achieving large-size matrix multiplications for computing, high-radix switches in optical networks or large-scale quantum processors. Therefore, following this trend is of major importance, particularly in those areas where advanced integration will allow the penetration of photonics technology into new markets. On the other hand, the timeline of the data point collection as a box plot is detailed in Fig. 2c where four examples are highlighted in the outliers as representative works of large-scale integration. The most commonly employed configuration is the thermo-optic actuator as it provides low-loss, reliability, and mass volume fabrication[60]. It is also worth noting that MEMS-based vertical couplers can be integrated along with crossing arrays and phase change materials (PCM), allowing for high density integration, although they are less robust and lack reliability[61,62].

Challenges and limitations

To keep up with the pace of the photonics trend, several aspects and challenges must be carefully considered and overcome. One of the main concerns in photonics is the optical loss that can occur due to chip coupling, propagation, and the insertion loss of photonic components[63]. Figure 3a illustrates the current evolution of the PUC loss as a function of the number of photonic actuators. The material platforms, such as silicon-on-insulator (SOI), silicon nitride (SiN), indium phosphide (InP), and silica, are shown. The results suggest that the loss per PUC decreases as the number of actuators increases, which is crucial for achieving high-density integration. Specifically, most processors involving more than 10^3 actuators report a PUC-loss between 0.3 and 0.5 dB. In the upcoming years, for some applications, it is imperative to reduce PUC loss below 0.15 dB for the integration of more than 10^4 photonic actuators, although its effect on overall system performance is architecture-dependent. Additionally, fabrication processes need to be further optimized to reduce propagation loss in optical waveguides and improve fiber-to-chip coupling[18].

Regarding energy consumption, Fig. 3b illustrates the power per area of photonic processors. The data does not reveal a clear trend in energy consumption per unit area. However, it is worth highlighting that thermo-optic actuators have become increasingly efficient over the years, with energy requirements now reaching sub-milliwatt levels. Despite these

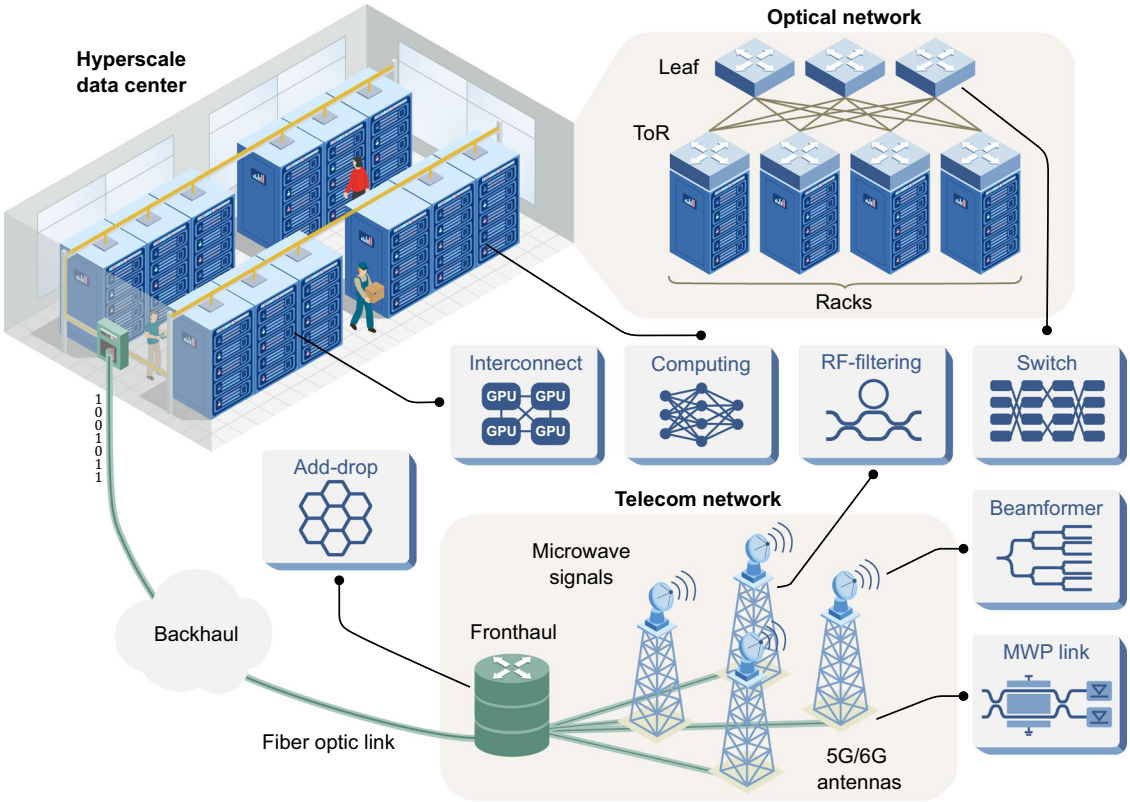

Fig. 4 | Photonic processors applications, scalability demand and markets. Figure 4 Two principal areas are represented: datacom and telecom. The former involves data centers and the use of photonic processors within optical networks as interconnects switches, and digital/quantum computing (10^4–10^5 actuators). The second is focused on telecom networks for 5G-6G communications, RF-processing (10^2-10^4 actuators) and beamforming (10^3–10^4 actuators)."

advancements, thermal stabilization systems represent the main energy overhead due to the continuous power draw of thermal tuning and stabilization systems. Furthermore, as more actuators are integrated into a single area, precise temperature control becomes increasingly important for architectures relying on resonant structures, presenting a significant challenge for future developments. However, power per area levels remain far below those currently employed in electronics, which can exceed hundreds of watts per square millimeter[48,60]. Figure 3c illustrates the integration density of photonic actuators per square millimeter for diverse types of PUCs. Mach-Zehnder interferometers (MZIs) have a lower integration density, around 20 actuators per square millimeter, although they offer broadband operation, which is crucial for most applications[64]. Resonators are more compact and can be integrated into smaller footprints, but their operating bandwidth is limited to a few nanometers[65] and suffer from thermal instabilities in the chip. Phase arrays, along with PCM and MEMs in crossing waveguides and bimodal waveguides, provide the highest actuator density, around 200 actuators per square millimeter[66–69]. Figure 3d, e show the material platforms and the electrical driving as a function of photonic actuators, respectively. Silicon-on-insulator (SOI) and silicon nitride (SiN) are the platforms that more miniaturization of photonic components, allowing for higher integration[70]. Additionally, hybrid integration of silicon with novel materials as thin-film lithium niobate, offers a promising avenue for mitigating some of these limitations, facilitating significant size reduction, or serving as a reliable alternative to the thermo-optic effect[71,72]. Regarding electrical packaging, probing enables the testing of processors with a few hundred actuators, followed by wire bonding for thousands, and flip-chip and monolithic packaging, which allow for driving a higher number of actuators, exceeding 10^4 on a chip[73]. Scalability is not merely about integrating more components into a chip but doing so while maintaining the desired overall system performance. Several approaches have been proposed to enhance the scalability and stability of large-scale processors, including advancements in innovative 2.5D packaging and the development of new matrix-addressing schemes for IO reduction[74,75]. The co-integration of photonics and electronics is of significant interest, particularly for the direct integration of electrical drivers within the photonic die, which can enhance signal integrity and reduce I/O complexity[76]. An alternative 3D integration of drivers onto the substrate also helps balance system-level complexity and fabrication process maturity. Others challenges stem from intrinsic fabrication errors, fluctuations in the operating values, signal degradation and noise, which call for dynamic control and monitoring of the circuit responses containing ever increasing unit cells[77,78]. In this regard, there are several approaches to develop fabrication-tolerant and fault-tolerant processors by employing component designs that tolerate fabrication deviations[79], circuit-level implementations[80] and reconfigurable components components[81,82].

Telecommunications and sensing applications

The progress of 5/6 G communications is pushing the limits of conventional networks towards higher bandwidth, lower latency and reduced energy consumption (Fig. 4). In this context, integrated microwave photonics (MWP) for distribution and processing of the spectrum offer remarkable advantages such as tunability, broadband operation, electromagnetic immunity, energy reduction and weight gains. Other systems such as lidar, optical spectroscopy or integrated logic gates for fast signal processing can also be integrated on-chip with promising results in latency, resolution and sensitivity[83,84].

For these applications, the most employed architecture of photonic processors are ASPICs based on optical phase arrays, optical beamforming networks and MWP links, making solutions with 10 s to 1000 s actuators market-ready. There are several examples of very large-scale photonic chips acting as phase arrays, one of them implementing more than 10,000 actuators, and compact-size low-power reconfigurable beam formers with high aperture angles[34,39]. The low complexity of phase arrays allows for very high dense integration as only phase shifters are needed and in most cases

these can be implemented with very compact-size doped silicon heaters[23]. In contrast, beamforming networks and MWP links require true-time delay lines and large optical high-speed modulators, respectively, which hinder dense integration and large-scale development. Finally, another application that will potentially benefit from this scalability is software-defined networks where future coherent-compatible products demand programmable optical switching and reconfigurable optical add-drop multiplexers with advanced programmability.

Optical networking and interconnects applications

The number and scale of data center networks and AI infrastructure have grown exponentially, driven by the continuous processing demand of generative models in cloud-based applications and big data analytics. The core of each data center relies on thousands of servers and their interconnection layer. Depending on the selected architecture, the network aggregates hundreds of thousands of electro-optical transceivers to interconnect electronic switches through point-to-point connections. In addition, the power consumption of data centers is expected to grow from 3% of total world power generation (0.6% associated to data movement) to 10% (3% data movement) in 6 years. In this context, optical interconnects (Fig. 4) have emerged as a solution to be introduced in hybrid networks, progressively conquering a portion of the communication channels from inter-data center to intra-data center (rack-to-rack and intra-rack).

Chip-to-chip interconnects have gained increasing attention in the last years as they provide large bandwidth connections between electronic cores. Although it provides a scale-up alternative when single core performance is limited, co-design with electronic cores needs to be addressed which limits its market penetration in the short-term. Moreover, there are existing electronic solutions capable of intra-rack connections between GPU units with very large bandwidth which also hinders the development of photonic solutions in the immediate future. Conversely, many works have addressed the benefits of optical circuit switching to complement existing datacom and AI systems to support big data flows over a more flexible, upgradable, and reliable infrastructure[85,86]. While electronic switches and transceivers have steadily advanced to support rising data rates, the growth in channel speed has lagged behind the pace of demand[87]. As a result, modern systems increasingly rely on both wavelength and space-division multiplexing, which require a high number of optical and electrical ports. This introduces significant cost and scalability challenges, including limited port density and reduced flexibility to adapt to future data rate and modulation format requirements.

To see integrated optics penetrating in the data centers and AI systems interconnects, there are 3 key coupled challenges. First, optical loss should be reduced at the component, circuit, and system level to match the 1 dB loss of existing MEMS-based solutions. While we envision this to happen in 8–10 years, to get an earlier zero-loss solution, an optical amplification array introducing moderate gain (4 to 10 dB) and low noise (<5 dB NF) could enable scalable growth. Secondly, to support higher radix (128–256 ports) while supporting non-blocking switching schemes, circuits need to integrate around 10^4–10^5 photonic actuators imposing a challenge on system integration and control handling. While we anticipate this in the mid-long term, lower radix switches (32–64 ports) in the order 10^3 actuators, are a real solution in the short–term, and they can find application in several areas within a data center. Third, coupled with the prior point, these actuators can work at μs or even ns reconfiguration speed to meet the performance requirements in intra-data center reconfiguration. On the software side, the ecosystem needs to evolve to accommodate the coexistence of optical circuit switching and electronic package switching to benefit from the higher speed reconfiguration and thus increase the overall data processing and network performance.

Optical computing applications

Over the past decade, both industry and academia have invested considerable effort into the development of light-driven integrated computer processors (Fig. 4), seeking benefits in low-latency and low power consumption[88]. However, the results show that the technology has not yet matched electronics in integration density, reconfigurability, and throughput scaling trends[89].

In most cases, the core of a photonic hardware accelerator for computing is an optical matrix multiplier. Several architectures have demonstrated capability in this regard including feedforward interferometers, ring-based array networks, and diffractive neural networks, among others[90,91]. Feedforward meshes are the most commonly employed configuration for computing, as they can reliably multiply large matrix sizes. Nevertheless, competing with digital electronic multipliers presents a fundamental trade-off between speed and matrix size. Achieving practical performance levels requires multiple processing cores capable of handling matrices larger than 256×256 or 512×512, which in turn demands the integration of 10^4 to 10^5 photonic actuators. This introduces significant development challenges, including complex packaging, precise calibration of optical components, and the need for sub-microsecond reconfiguration speeds alongside high-speed (1 GHz) modulation arrays. As shown in the trend projection, photonics technology is not capable of implementing such levels of dense integration in the short and mid-term. The current integration density of electronics exceeds that of current photonic solutions by 4 to 5 orders of magnitude and allows parallelization in multiple cores like GPUs. Furthermore, photonics does not offer considerable savings in power consumption, as it is dominated by memory data movement and optical solutions in that field are yet to be proven successful. The number of floating-point operations per second has scaled by a factor of 3 every two years, while memory interconnection bandwidth has only increased by a factor of 1.5 in the same period. Furthermore, the size of cutting-edge AI models has drastically surpassed GPU memory capacity, making data centers the new standard for compute units[92]. Lastly, the bit precision in optical computing is highly limited to 4 or 8 bits due to excess loss, optical power budgets and signal-to-noise ratio, compared to flexible precision configuration in most electronics. This is practical only for specific cases in AI inference, as other applications—such as training, image processing, and quantum computing—demand higher accuracy levels exceeding 16 bits. Training solutions such as fine-tuning, quantization-aware training, and pipelining are essential for addressing the challenges of low precision and computational limitations in photonic AI processors[93,94]. PIC scalability and resulting performance remains a key challenge of photonic processor for digital-computing tasks. For this type of processors, most of the limitations come from the encoding-decoding strategies and end-nodes based on fast modulators and photodetectors. Mitigating some of this challenges requires both architectural and algorithmic strategies that in some cases dilute the inherent advantage of photonic processors. It is worth noting that photonic encoding differs from conventional digital electronics, as its precision is determined by a separate control system. However, this work focuses on directly comparing photonic hardware components across various applications.

All in all, there are certain application spaces that could avoid direct competition with digital electronic computing[95]. First, applications where the input/output signal is on the radiofrequency or the optical domain like base-station computing or satellite-ground stations, respectively[96]. Secondly, specific-purpose quantum computers and Ising machines are still trying to find their niche applications space[97]. The extremely low loss requirement calls for platforms with beyond-state-of the art performance in low-loss design and wafer manufacturing[98,99]. Certainly, far from competition with electronic solutions, we anticipate niche applications where analog inputs and small-scale multipliers can truly leverage the advantages of optical computing. Moreover, nonlinear optical processing plays a critical role in optical networks handling complex signals and high-speed fiber communications, as well as in implementing activation functions within optical neural networks[100–103].

Discussion

In this work, we analyzed the evolution of large-scale photonic processors over the past two decades, unveiling the most promising application markets and their requirements. Photonic chips are following a similar exponential

trend to that of electronics decades ago, reaching an impressive trend of 2x in the number of actuators every two years. These levels of integration offer clear advantages in bandwidth density, energy efficiency, and latency, positioning photonic processors as strong complementary candidates for next-generation communication and processing system integration. Specifically, we anticipate optical interconnects as one of the main application areas where photonics can play a crucial role, particularly in next-generation data centers and AI/ML infrastructure. Optical circuit switches can provide transparent solutions to accommodate ever-increasing large bandwidth demands and modulation formats. Moreover, the maturity of photonics technology is progressing fast to develop large-scale processors of thousands of actuators that can be deployed at scale. The advancement of photonics is not solely dependent on the growth in the number of actuators. The synergy between electronics, software and photonics is key in advancing the technology's penetration into the market. This symbiosis will ultimately dictate the role of large-scale photonic processors for industry-wide solutions to contemporary challenges.

Methods

Data processing

Figure 2a presents the data points alongside a linear interpolation illustrating the evolution of both electronic and photonic technologies. Figure 2c displays the interquartile range (IQR) between the 25th and 75th percentiles, highlighting the most representative examples as outliers. Figure 3c shows the clustering of the dataset based on different types of PUC mechanisms. Figure 3d, e provide boxplot representations similar to Fig. 2c. All data visualizations were processed and generated using Python scripts, which are available in the Code Availability section.

Data availability

The datasets generated and analysed for this study are available at https://github.com/LuisTorrijosMoran/LS-Photonic-Processors-Survey.

Code availability

The python scripts used for this study are available at https://github.com/LuisTorrijosMoran/LS-Photonic-Processors-Survey.

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Author contributions

D.P.L. conceived the original idea of the article. All authors processed the data and wrote the main manuscript text. All authors reviewed the manuscript. L.T.M. prepared the figures.

Competing interests

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