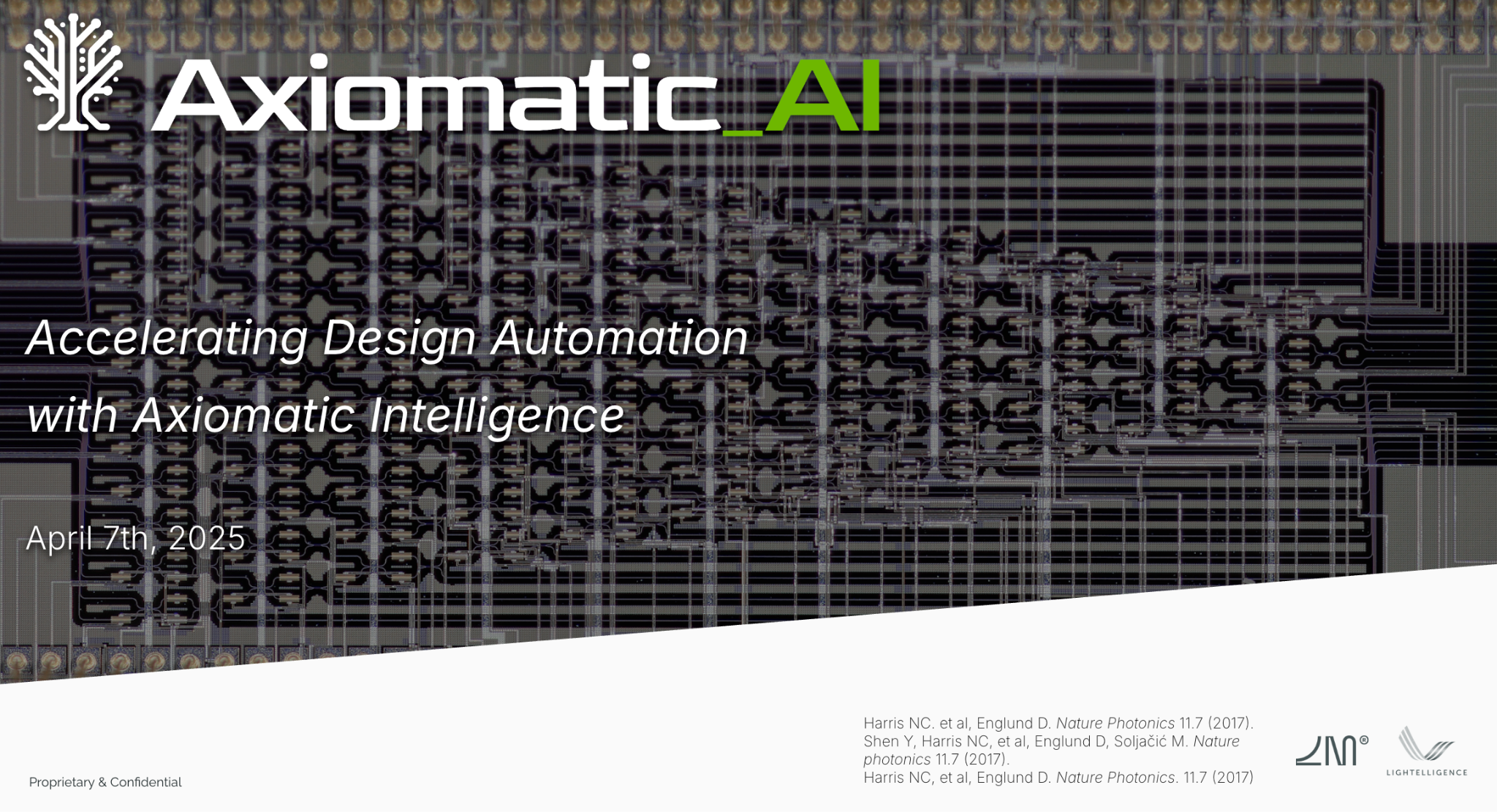
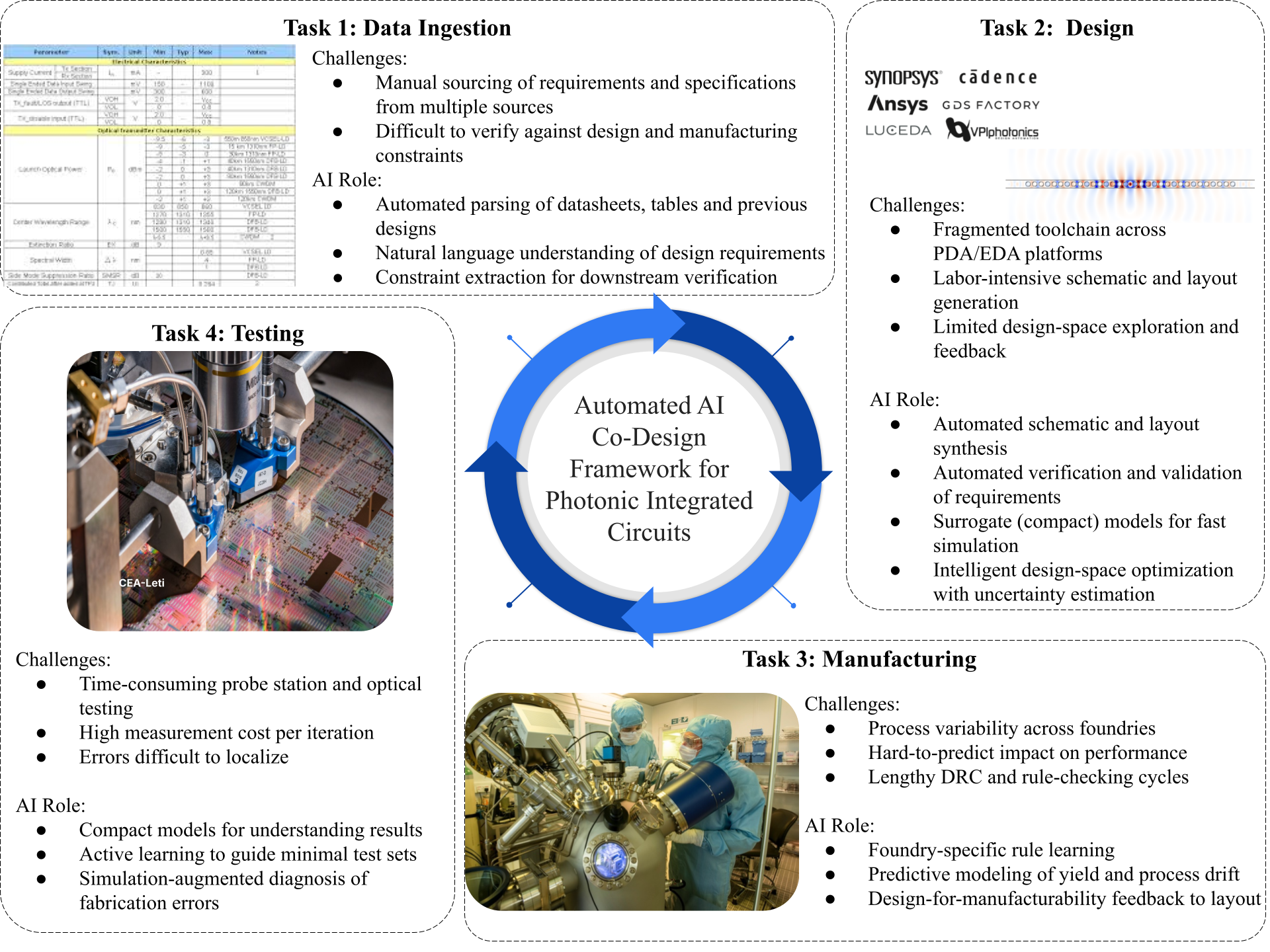
**AI-enabled Photonic Design Automation for Very Large-Scale Photonic Integration (VLPI):** Agentic AI tools with a natural language interface and simulation-integrated design engine for scalable VLPI photonic circuits.

| **Company Name** | Axiomatic\_AI |
| --- | --- |
| **Company UEI Code** | YXU5B26YLV49 |
| **Solicitation Number** | DARPA-SN-25-88  Very Large-scale Photonic Integration (VLPI) |
| **Submission Type:** | Request for Further Information (RFI) for  Very Large-scale Photonic Integration (VLPI) |
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| **Research Area** | Technical Area 2: Design Automation for VLPI |
| **Submission Date** | July 15, 2025 |

**Technical Area 2: Manufacture-Aware Automated VLPI Design Flow & Large-Scale Simulation**



[**Figure 1**](#figur_axiomatic_products_v01)***: Overview of Axiomatic\_AI approach:*** *To meet the growing demands of scalable photonic integrated circuit (PIC) development, we are building an* ***automated AI co-design framework*** *that spans the entire hardware development lifecycle—from data ingestion and design to manufacturing and testing. Each phase of this pipeline presents unique challenges: fragmented design ecosystems, process variability across foundries, labor-intensive data verification, and costly, time-consuming testing cycles. Our integrated suite of AI-driven tools — The Axiomatic AI platform including the* ***PIC Designer****,* ***Model Builder****,* ***AX ingestion assistants (AxToys)*** *—addresses these pain points by automating routine tasks, learning from data, and incorporating verification, validation, uncertainty quantification and optimization techniques (VVUQO). Together, these components form a feedback-driven system that not only accelerates development but also improves robustness, yield, and scalability for increasingly larger and more complex photonic integrated circuits. The result is a unified and adaptive framework that automates photonic co-design enabling the development of VLPI. Image credits: All wafer and photonic circuit images used in Task 3 and Task 4 are courtesy of CEA-Leti.*

**2a. Capabilities & Challenges Addressed**

Very-Large-Scale Photonic Integration (VLPI) demands the seamless synthesis of circuits containing 10⁵–10⁶ optical elements—orders of magnitude beyond today’s typical 10³–10⁴ device layouts. Current photonic-CAD platforms excel at small-scale design but falter when stretched to VLPI due to multiple challenges [[1]](https://paperpile.com/c/WiX4Bu/FOOp):

* **Scaling EM Solvers:** Mesh-based full-wave solvers (FDTD, FEM) grow super-linearly in runtime and memory as element count increases, capping practical simulation domains at ~10³ devices and forcing designers to manually partition layouts into sub-blocks—losing global fidelity [[2,3]](https://paperpile.com/c/WiX4Bu/Y2yr+rto7) .
* **Maintaining Physics Fidelity:** Reduced-order methods (eigenmode expansion, coupled-mode theory) trade off scattering, polarization effects, and substrate coupling—errors that accumulate across large WDM filters or resonator arrays and undermine yield predictions [[2,4]](https://paperpile.com/c/WiX4Bu/LRYV+Y2yr).
* **Embedding Manufacturing Variability:** Most flows assume nominal PDK parameters; discrete corner analyses via manual or brute-force Monte Carlo campaigns can require days to capture the impact of ±10 nm waveguide width or thickness variations on resonance shift and loss [[5–10]](https://paperpile.com/c/WiX4Bu/uOpN+43yN+fok5+pTLQ+gCmP+kQSq) .
* **Co-Simulating Multi-Physics:** Thermal, electrical, and optical phenomena interact in dense PICs (e.g., thermo-optic tuning, carrier effects), yet existing toolchains serialize between separate simulators, incurring significant I/O overhead and limiting co-optimization loops [[11–16]](https://paperpile.com/c/WiX4Bu/HseY+j0Bs+cWKs+v72w+ZQyL+PHDF).
* **Ecosystem Fragmentation & Manual Integration:** Layout editors, EM solvers, circuit simulators, variability engines, and measurement tools each use different formats and APIs. Engineers spend extensive time writing and debugging ad-hoc scripts to convert between GDSII, OpenPDK, HDF5 logs, and simulator inputs—an error-prone, labor-intensive process that breaks down entirely at VLPI scale [[17–20]](https://paperpile.com/c/WiX4Bu/ajWQ+slu6+nRT8+7HjM).

**Proposed Solution: Axiomatic Intelligence platform**We will deploy an **agentic, data-driven design backbone that weaves together five core capabilities**:

1. **AxToys** agents ingest and semantically interpret multimodal engineering data—PDKs, GDSII layouts, SEM/AFM imagery, plots, tables, equations—into a unified, machine-readable knowledge graph.
2. **Model Builder** agents consume experimental and simulation datasets to automate construction of compact, physics-based surrogate (compact) models that faithfully reproduce element-level behavior.
3. **PIC Designer** employs generative AI to synthesize end-to-end PIC layouts from high-level specifications, orchestrates automated simulations, and drives multi-objective optimization (insertion loss, footprint, yield).
4. **Automated Verification & Validation (VV)** agents leverage embedded formal checks to guarantee model correctness, enforce fabrication rules and performance constraints, and provide corrective suggestions in-line.
5. **Uncertainty Quantification & Optimization (UQ&O)** modules optimize the design performance incorporating manufacturing variabilities and propagating uncertainties in the process — identifying robust design parameters and interpreting experimental variability to maximize yield.

Together, these agentic AI and AI-assisted frameworks eliminate manual orchestration, bridge fragmented toolchains, and ensure every design decision is grounded in provable physics and calibrated data—directly addressing VLPI’s core challenge of scaling PIC design pipelines beyond manual limits while guaranteeing accuracy and manufacturability. [Figure 2](#fig_pic_designer_v01) demonstrates a prototype implementation of this language-to-layout workflow, highlighting early progress across all four tasks.

**2b. Theoretical & Simulation Discussion**

Our platform integrates agentic orchestration with a multi-tier surrogate strategy:

* **Element-Level Surrogates (Model Builder for Compact Models):** Automatically generated neural-symbolic or regression-based models capture wavelength-dependent S-parameters of primitives (waveguides, bends, couplers) with high accuracy, replacing individual FDTD runs.
* **Uncertainty Workflows** (UQ&O - *Uncertainty Quantification and Optimization*): UQ&O modules propagate fabrication and model uncertainties through surrogate networks, compute performance distributions, and drive optimization loops to identify robust design points under real-world variability. We will also incorporate an initial design-for-measurement step to identify and capture key sources of variability.
* **Global simulation and optimization:** Simulation engines assemble million-node photonic circuits by linking element surrogates, solving for global transmission, crosstalk, and dispersion behavior in O(N log N) time.

**Agentic Orchestration:** Autonomous agents monitor solver loads and accuracy targets—dynamically selecting between physics-based solvers and surrogates, configuring multi-physics co-simulation workflows (optical/thermal/electrical) over in-memory data buses to eliminate file I/O, and pivoting strategies in real time to meet turnaround requirements.

**AI-Assisted EDA Modernization:** Agents continuously refactor legacy solver code—injecting GPU acceleration, pruning unused modes, and auto-vectorizing kernels—to extend each tool’s capacity commensurate with VLPI scale.

**Generative Design Loop (PIC Designer):** Generative AI models generate initial GDS layouts from system-level specs (filter order, bandwidth, footprint). Adjoint optimization techniques, based on traditional optimization or improved with reinforcement learning approach then refines designs in parallel, exploring thousands of candidates to balance performance metrics.

**2c. Development Strategy**

We propose developing and testing the AI-driven capabilities around a curated set of design challenges of increasing size and complexity in three phases as described in the table below. This will allow us to quantitatively evaluate the scalability of AI-driven design and simulation workflows.

| **Phase** | **Objectives** | **Key Activities** |
| --- | --- | --- |
| Phase 1  (M1–M8) | Data & Surrogate Foundation | • Deploy AxToys across PDKs, GDSII, SEM/AFM archives to build a database of existing components and devices.  • Develop element-level surrogates via Model Builder |
| Phase 2  (M4–M16) | Generative & Validation Workflows | • Fine tune the PIC Designer for layout generation of increasingly larger PICs.  • Embed Automated VV and integrate UQ&O modules into flow. |
| Phase 3  (M12–M24) | Scaling workflow to larger devices | • Orchestrate closed-loop: surrogate ↔ test-chip measurements  • Validate full VLPI workflow at wafer scale, for increasingly larger PICs. |

Overlapping phases accelerate feedback: surrogate and UQ&O insights from Phase 1 inform generative and verification loops in Phase 2. We then work in scaling the foundation established in Phases 1 and 2 to larger systems in Phase 3 .

**2d. Estimated Time to Availability & Risk Assessment**

| **Deliverable** | **ETA** | **Key Risks** | **Mitigation Strategies** |
| --- | --- | --- | --- |
| AxToys Data Ingestion | Month 7 | Heterogeneity of PDKs, layout formats and measurement logs may lead to incomplete parsing | Pre-fine-tune LLM parsers on a diverse corpus; build modular adapters for each file format |
| Element-Level Surrogates & UQ&O Modules | Month 12 | Surrogate models may under-represent nonlinear scattering or fabrication-induced effects; uncertainty workflows may misestimate real-world variability | Benchmark against high-fidelity FDTD and measured test-chip data; iteratively retrain surrogates and UQ modules on residual errors |
| Generative Layout & Automated VV Integration | Month 16 | Generative-AI based layout generators might produce non-fabricable geometries; formal rule sets may be incomplete | Conduct human-in-the-loop pilots on midsize PICs; expand VV rule library using feedback from foundry partners |
| Global Graph Solver & Modeling Loop | Month 20 | Test-chip measurement noise and variability could destabilize closed-loop calibration; *large simulation instances may exceed available compute resources* | Implement Bayesian filtering to reject outliers; progressively scale solver to larger graphs and optimize memory via sparse algorithms |

* **By Month 7:** The platform will support manufacture-aware yield prediction and surrogate-augmented simulation for circuits with **100+ functional components** (e.g., couplers, modulators, detectors).
* **By Month 16:** We aim to enable full AI-driven design, verification, and UQ&O workflows on circuits with **~1,000 functional components**, leveraging a design repository and layout automation through tools such as PIC Designer.
* **By Month 20**: We will validate the complete end-to-end VLPI workflow on benchmark circuits with 10⁴+ interdependent elements, including calibration against wafer-scale test-chip data. This final milestone demonstrates manufacturability, physical realism, and readiness to scale toward the 10⁵–10⁶ component range in subsequent phases, aligning with DARPA’s VLPI vision.



[Figure 2](#figur_pic_designer_v01) *Prototype implementation of our AI-augmented workflow for designing photonic integrated circuits (PICs), demonstrating progress toward a full language-to-layout stack. In* ***Task 1****, the user specifies design intent using natural language (e.g., “Design a 1×4 MZI interleaver centered at 1550 nm”).* ***Task 2*** *generates the corresponding architectural schematic. In* ***Task 3****, a physical layout is created and simulated to evaluate metrics like insertion loss.* ***Task 4*** *runs an optimization loop to refine the design under fabrication constraints and target performance specs. This demonstration bridges high-level intent with manufacturable, optimized PICs.*

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