Force-voltage analogy

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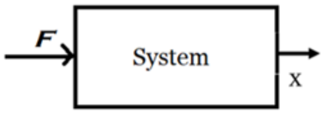
In experiment 1 we have analysed spring mass damper system and in experiment 2 we have analysed RLC circuit as a system. In both the case we got the second order transfer function and if we look at the both system and transfer function we can see that they both are comparable.

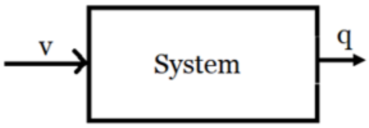
For the mechanical system (SMD):

$$\frac{1}{m*s^2 + c*s + k}$$



For electrical system (RLC)

$$\frac{1}{Ls^2 + sR + 1/c}$$



Now comparing both the system we can find some things are analogous as below:

Force → Voltage
Mass → Inductance
Damper constant → Resistance
Spring constant → 1/capacitance
Displacement → Charge
Velocity → Current

But the question arises that why this analogy is required than the reason is we are more familiar with electronics system and troubleshooting and problem solving is much comfortable with the electronics system. So by converting mechanical system in to the representative electronics system using force to voltage analogy then it becomes easier for us to interpret and solve it.

1 Time domain characteristics:

Till now we have also plotted time domain characteristic graphs, the step response of systems defines system parameters. Actually in system designing we knows only what kind of response we requires from system and accordingly we tunes our design parameters.

Here we have described time domain characteristics and parameters for second order system.

In fig 3 we have also shown these parameters on the graph we have plotted in scilab.

2 Rise time

The time required for response to rising from 10% to 90% of final value, for an overdamped system and 0 to 100% for an underdamped system is called the rise time of the system.

3 Peak time

The time required for the response to reach the 1st peak of the time response or 1st peak overshoot is called the Peak time.

4 Maximum overshoot

The difference between the peak of 1st time and steady output is called the maximum overshoot.

5 Settling Time (t$_s$)

The time that is required for the response to reach and stay within the specified range (2% to 5%) of its final value is called the settling time.

6 Steady State Error (e$_{ss}$)

The difference between actual output and desired output as time't' tends to infinity is called the steady state error of the system.