VLSI LAB REPORT

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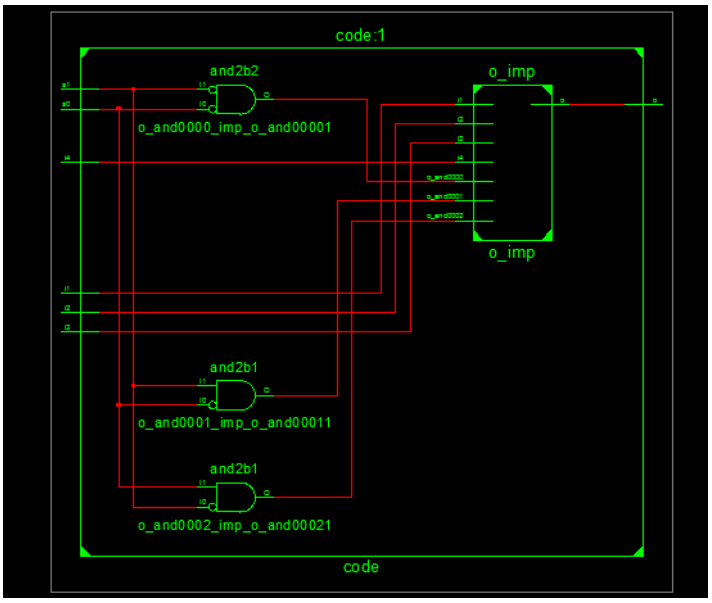
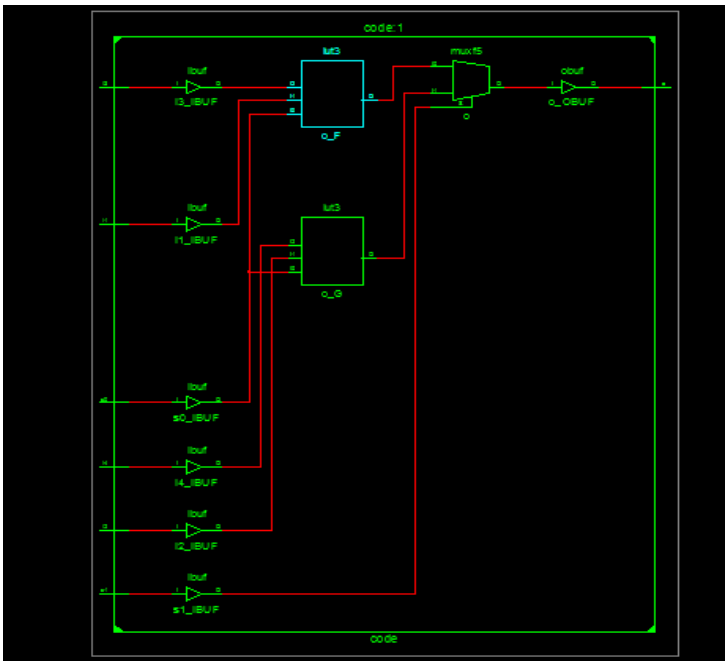
XILINX

Experiment 1: 4x1 MUX

RTL Schematic



Technology Schematic

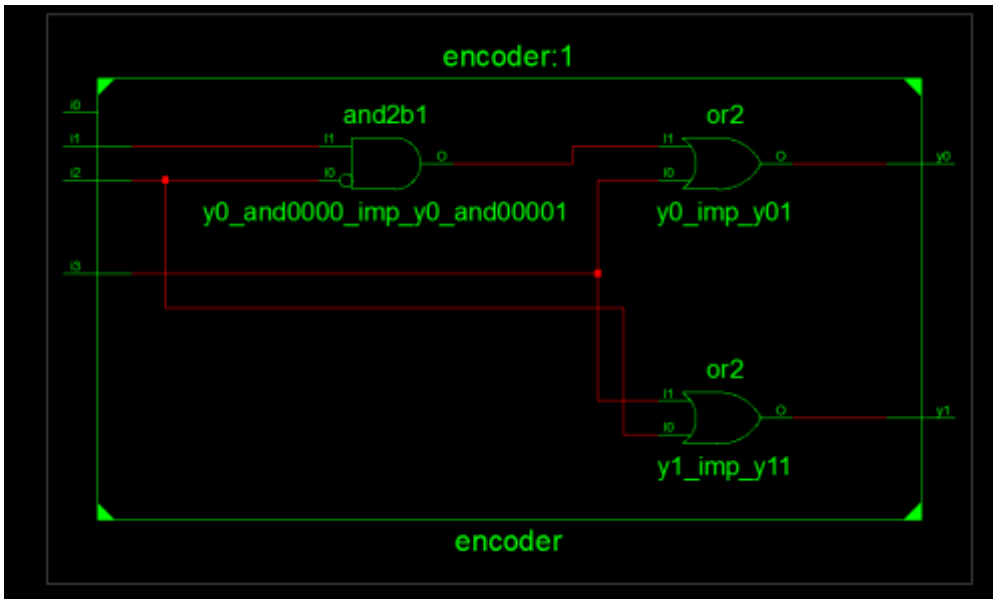


Design statistics:

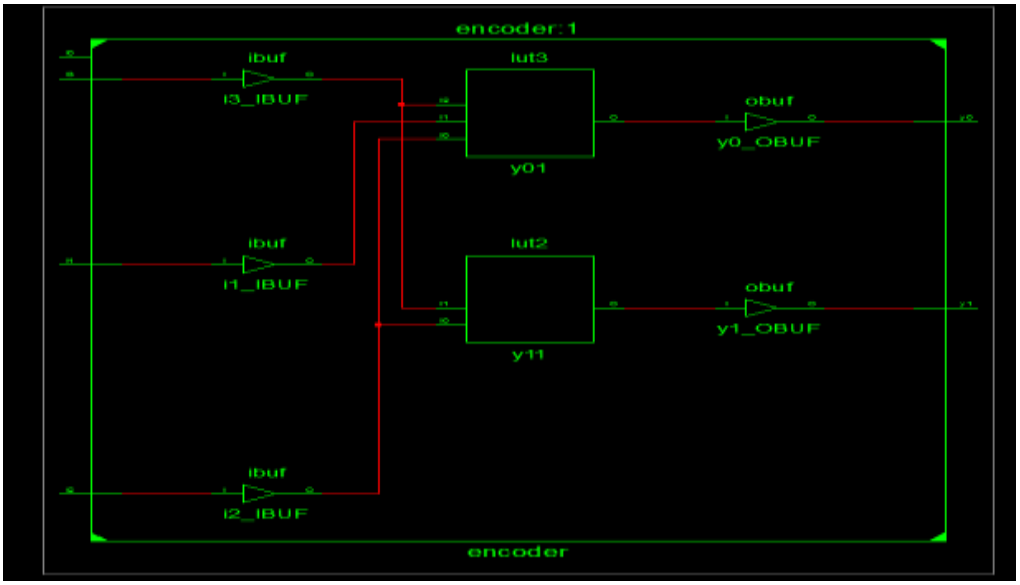
Number of Slices	:	1
Number of 4 input LUTs	:	2
Number of IOs	:	7
Number of bonded IOBs	:	7
Delay	:	6.054ns (Levels of Logic = 4)

Experiment 2: Priority Encoder

RTL Schematic



Technology schematic

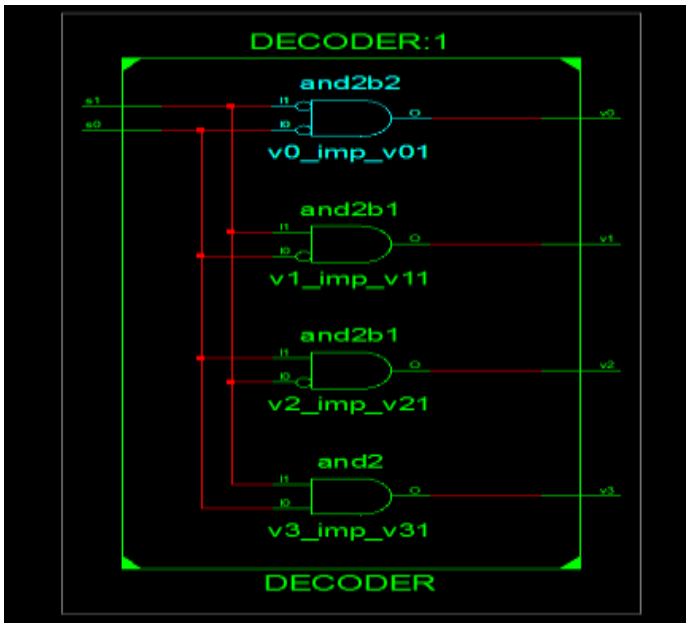


Design Statistics:

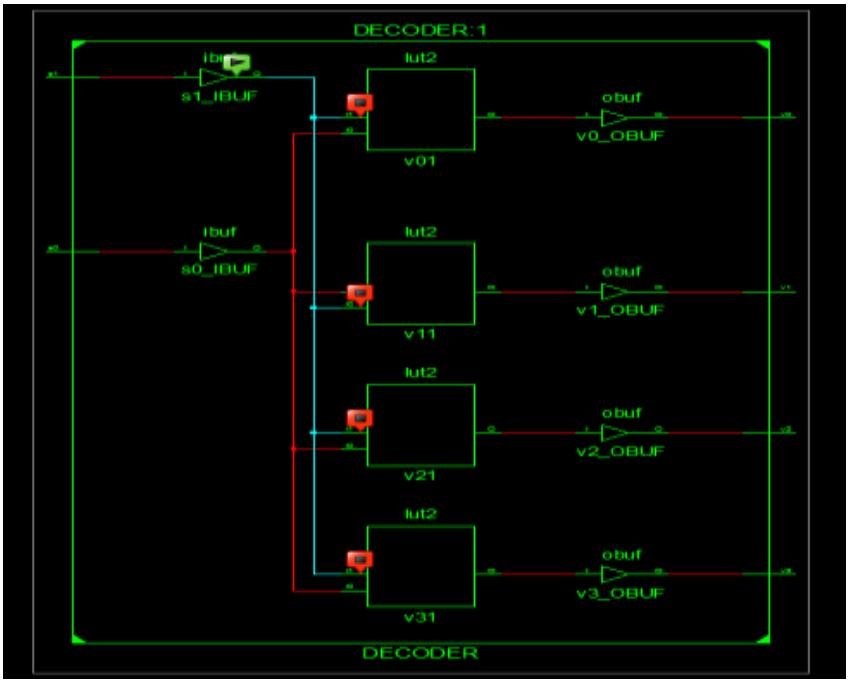
Number of Slices	:	1
Number of 4 input LUTs	:	2
Number of IOs	:	6
Number of bonded IOBs	:	5
Delay	:	5.776ns (Levels of Logic = 3)

Experiment-3: Decoder

RTL Schematic



Technology Schematic

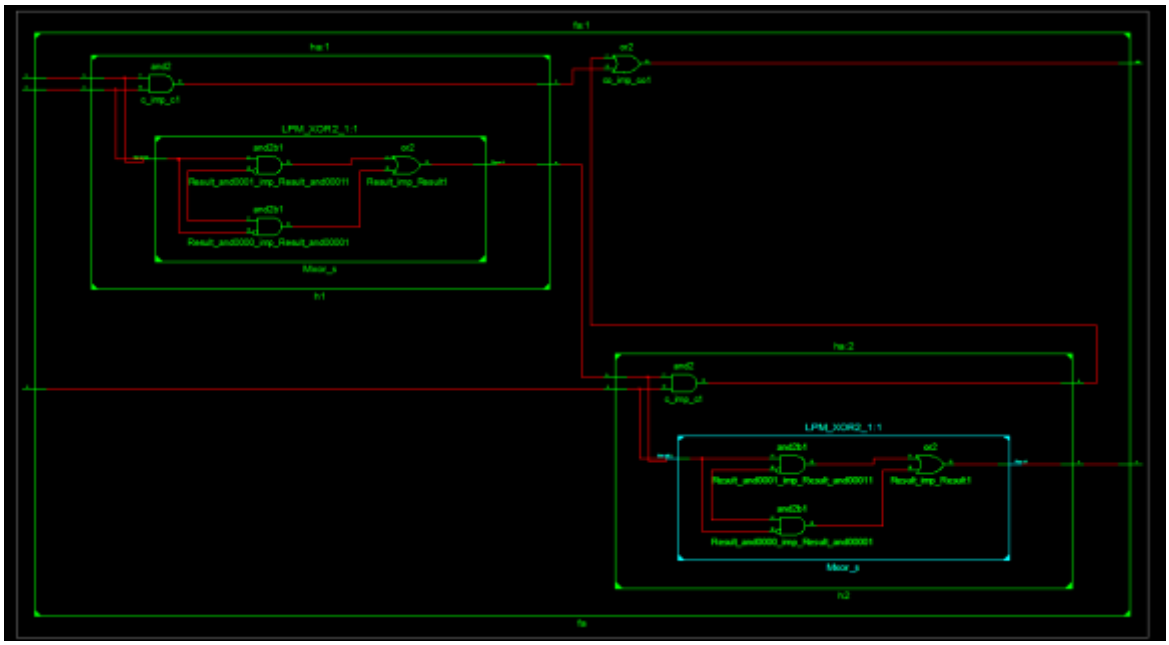


Design statistics:

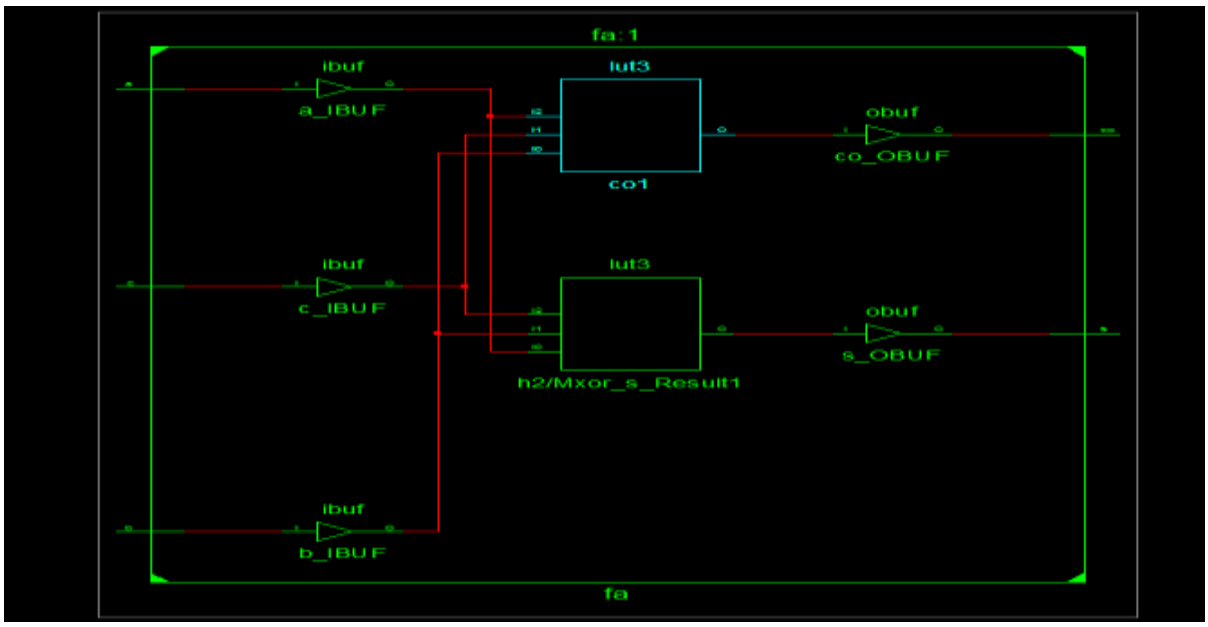
Number of Slices	:	2
Number of 4 input LUTs	:	4
Number of IOs	:	6
Number of bonded IOBs	:	6
Delay	:	5.895ns (Levels of Logic = 3)

Experiment-4: Full adder using half adders

RTL Schematic



Technology Schematic

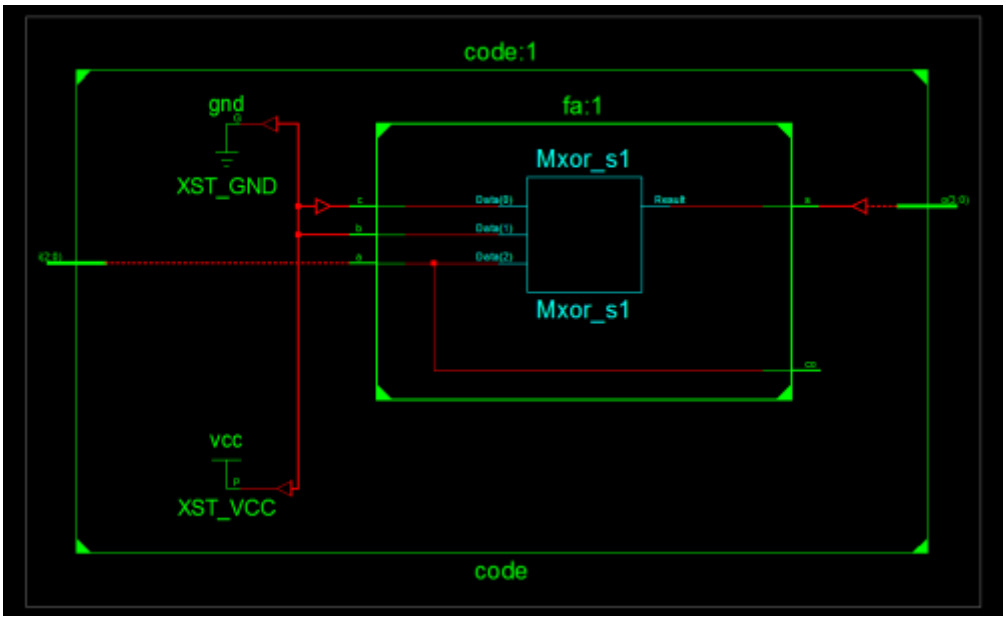


Design statistics

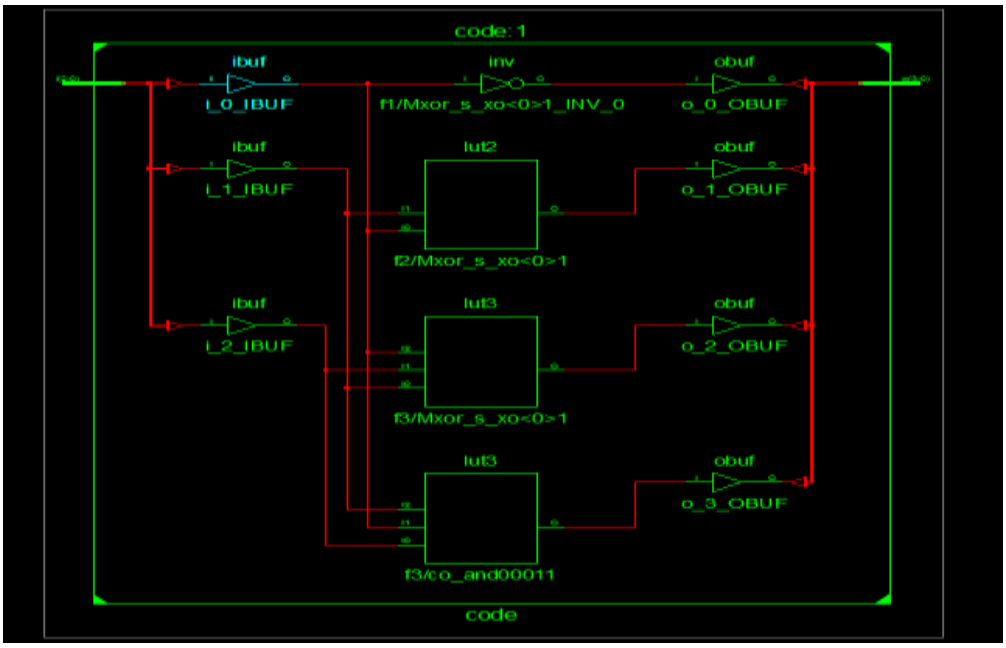
Number of Slices	:	1
Number of 4 input LUTs	:	2
Number of IOs	:	5
Number of bonded IOBs	:	5
Delay	:	5.776ns (Levels of Logic = 3)

Experiment 5: Binary to XS 3 Converter

RTL Schematic



Technology Schematic

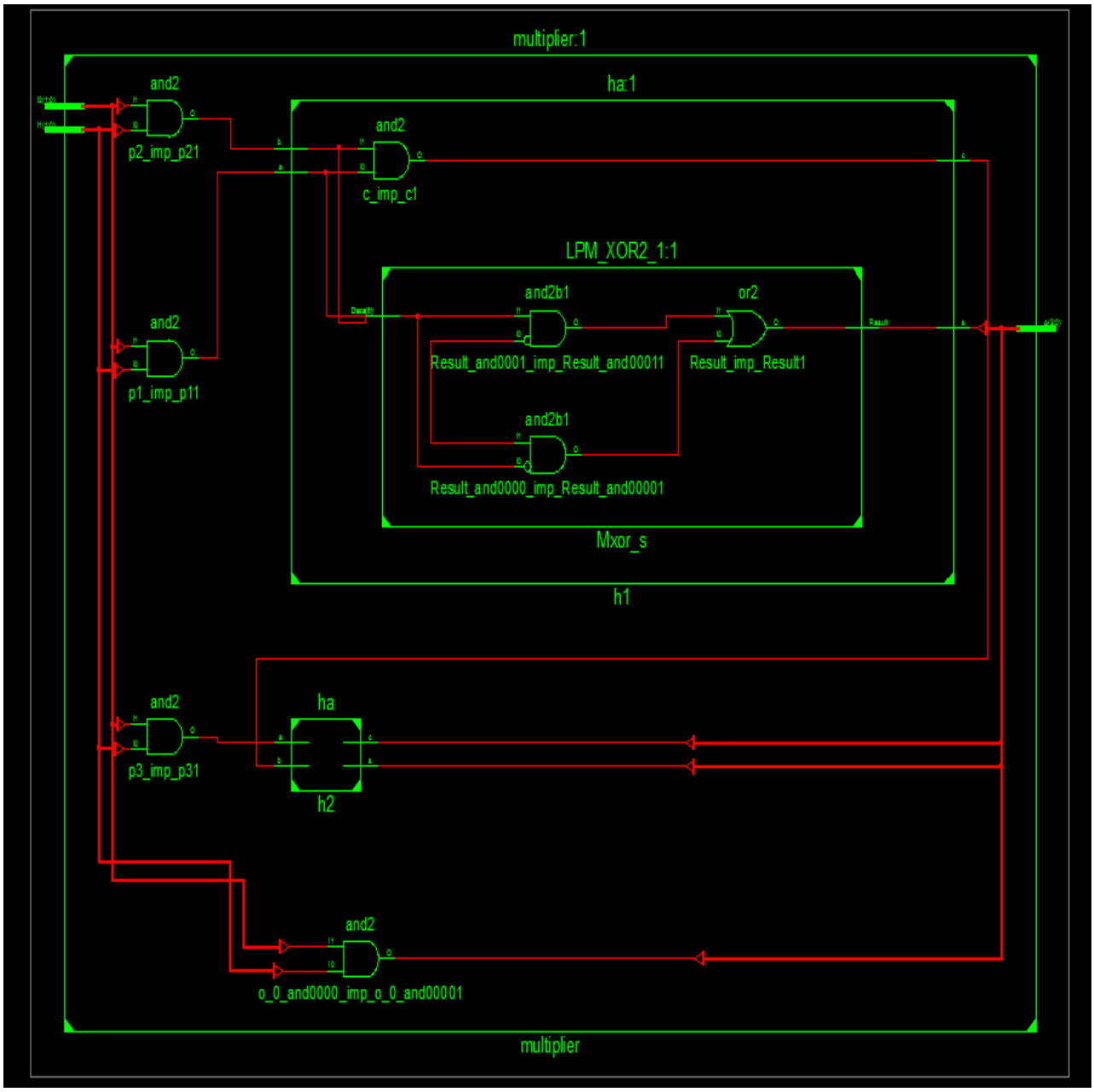


Design statistics

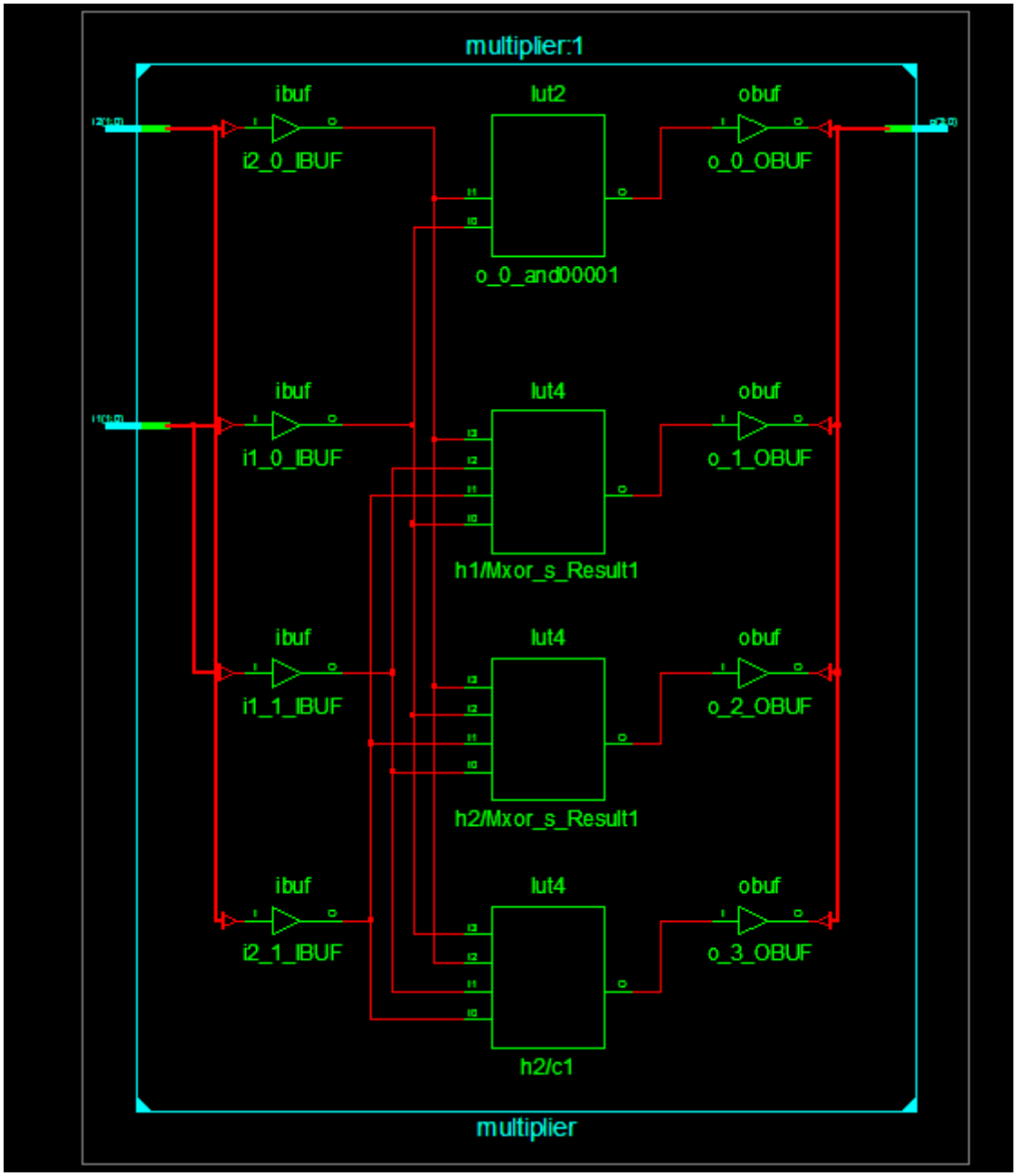
Number of Slices	:	2
Number of 4 input LUTs	:	4
Number of IOs	:	7
Number of bonded IOBs	:	7
Delay	:	5.895ns (Levels of Logic = 3)

Experiment 6: 2 bit multiplier

RTL Schematic



Technology Schematic

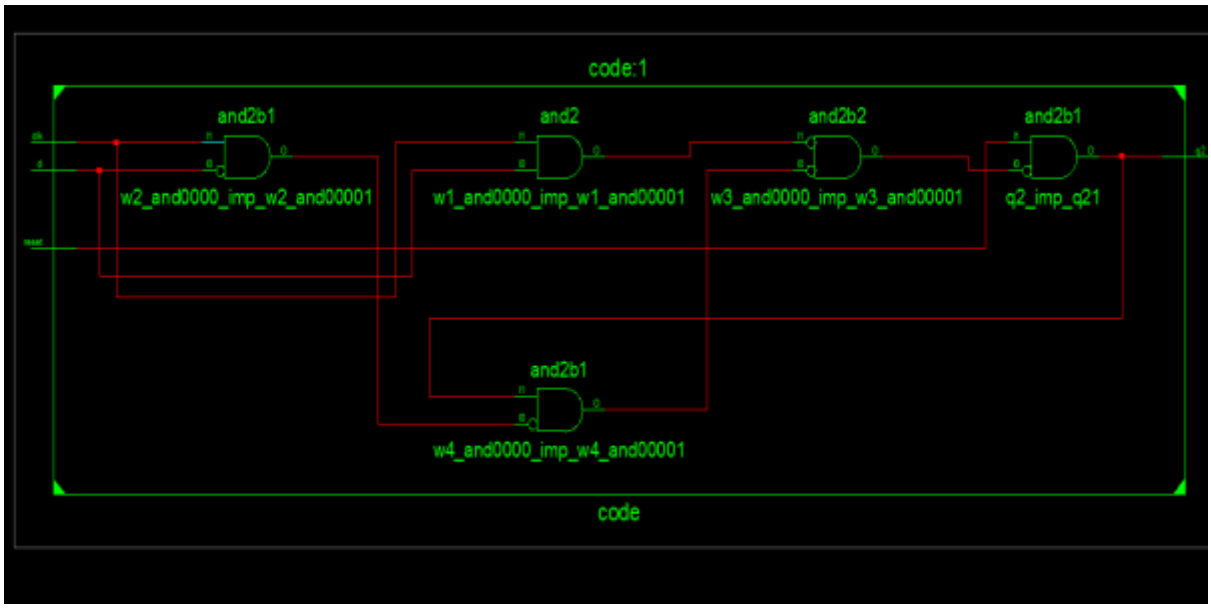


Design statistics:

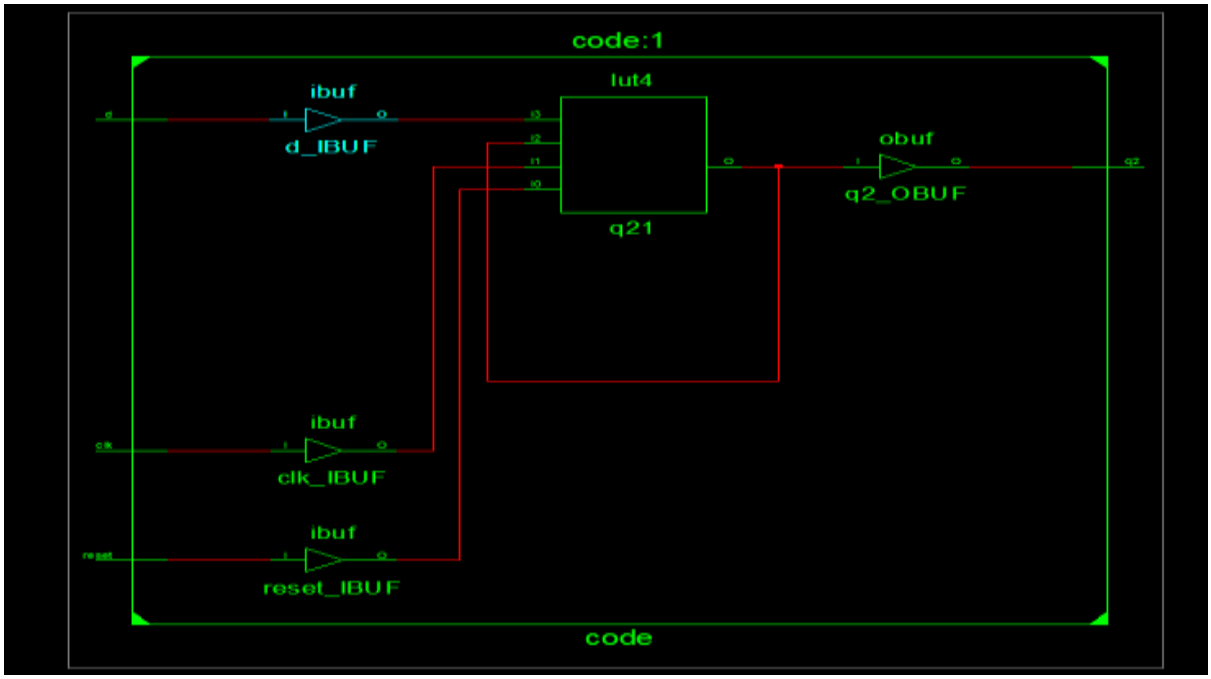
Number of Slices	:	2
Number of 4 input LUTs	:	4
Number of IOs	:	8
Number of bonded IOBs	:	8
Delay	:	5.895ns (Levels of Logic = 3)

Experiment 7: Latch

RTL Schematic



Technology Schematic

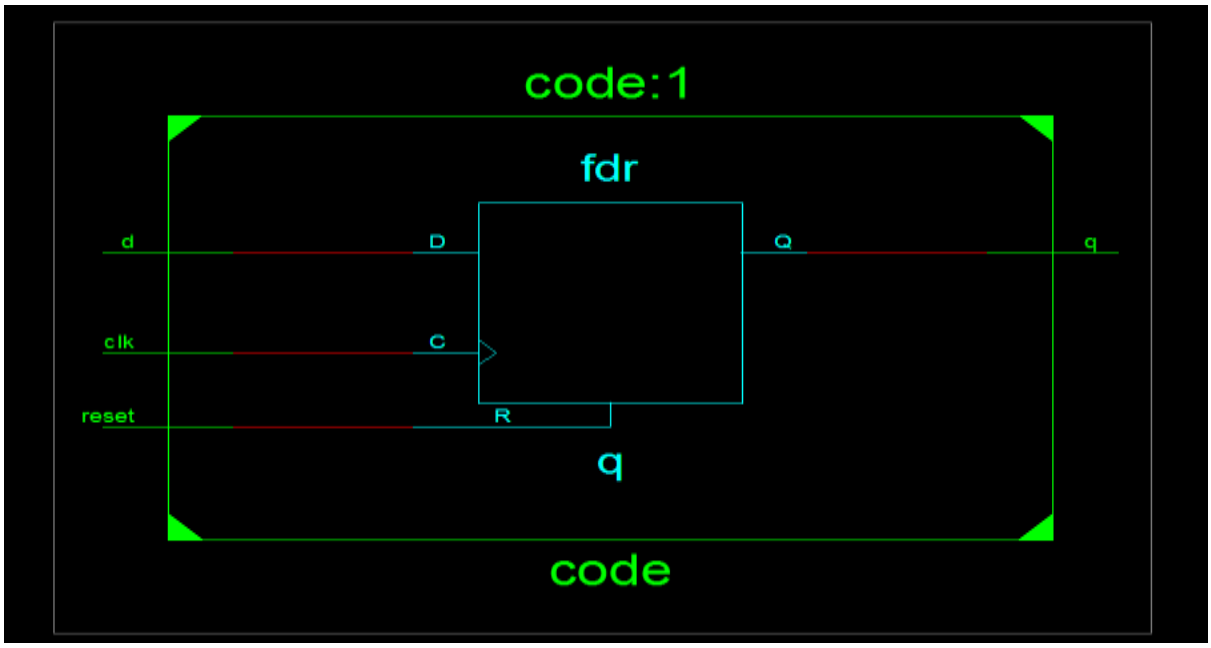


Design statistics

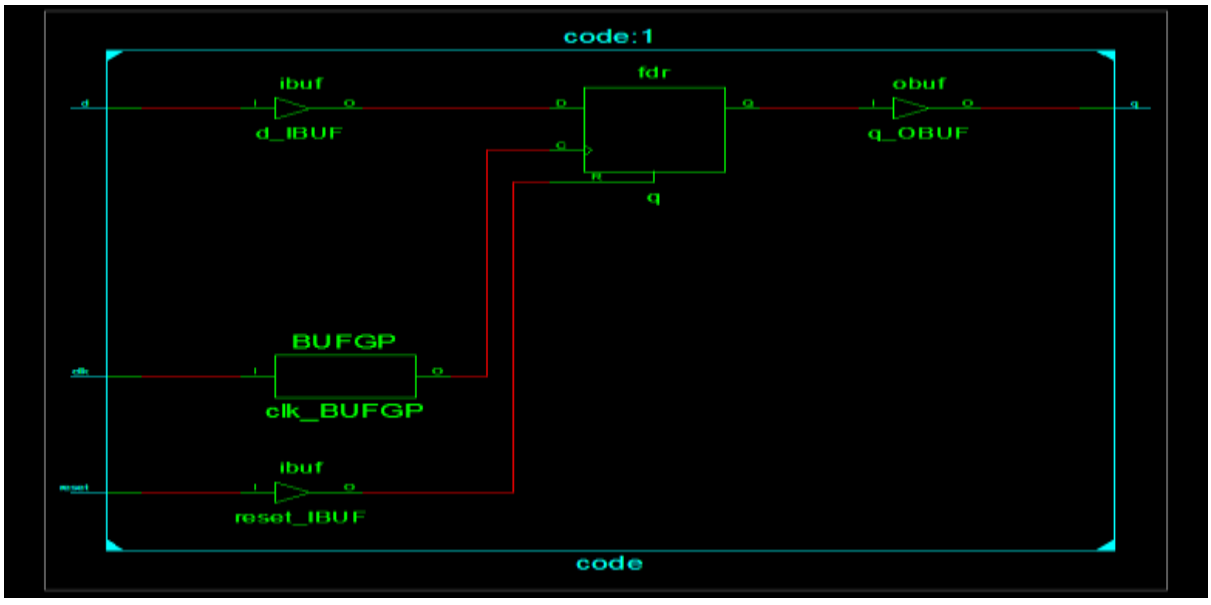
Number of Slices	:	1
Number of 4 input LUTs	:	1
Number of IOs	:	4
Number of bonded IOBs	:	4
Delay	:	5.776ns (Levels of Logic = 3)

Experiment-8: D Flip flop

RTL Schematic



Technology Schematic

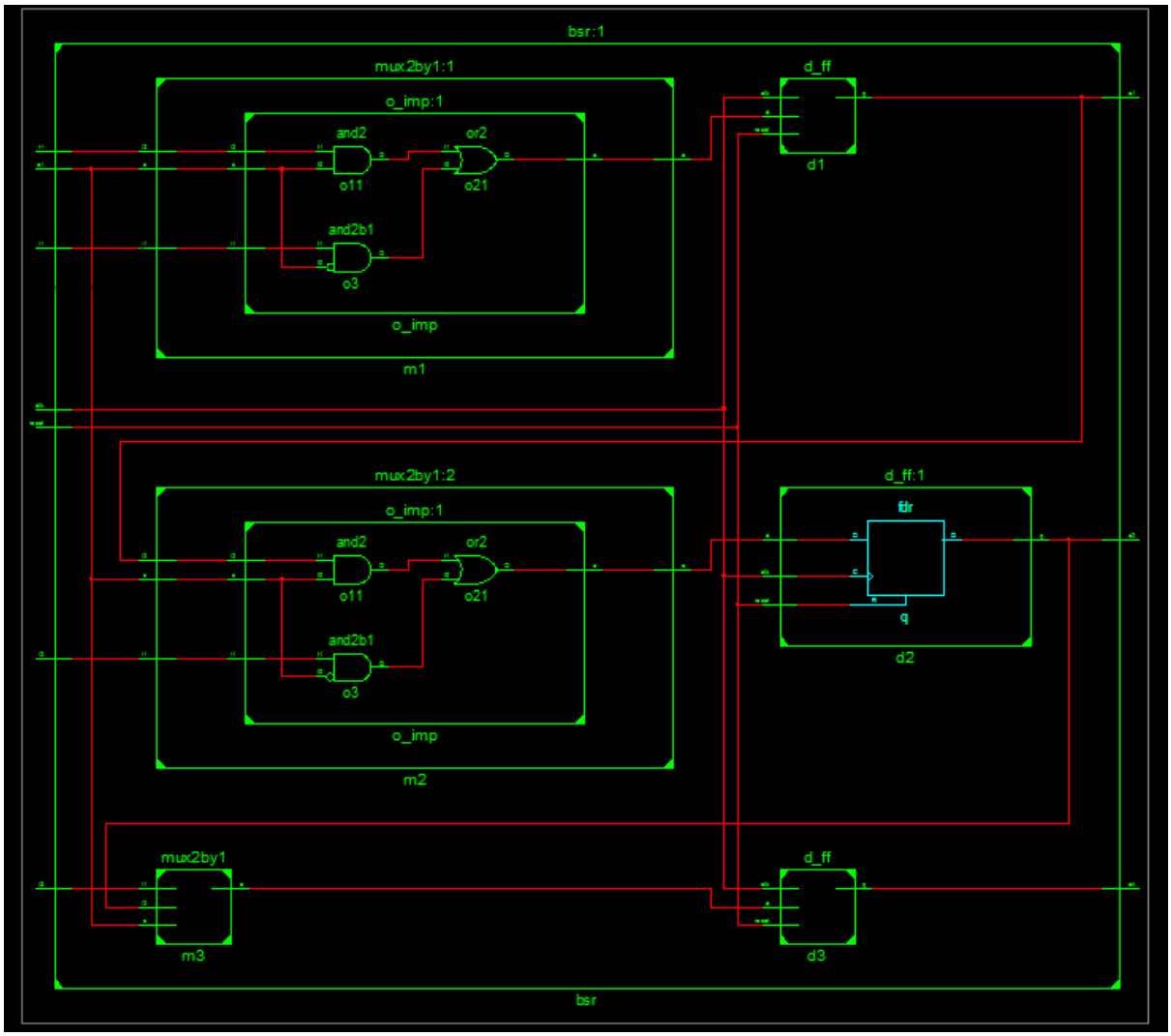


Design Statistics

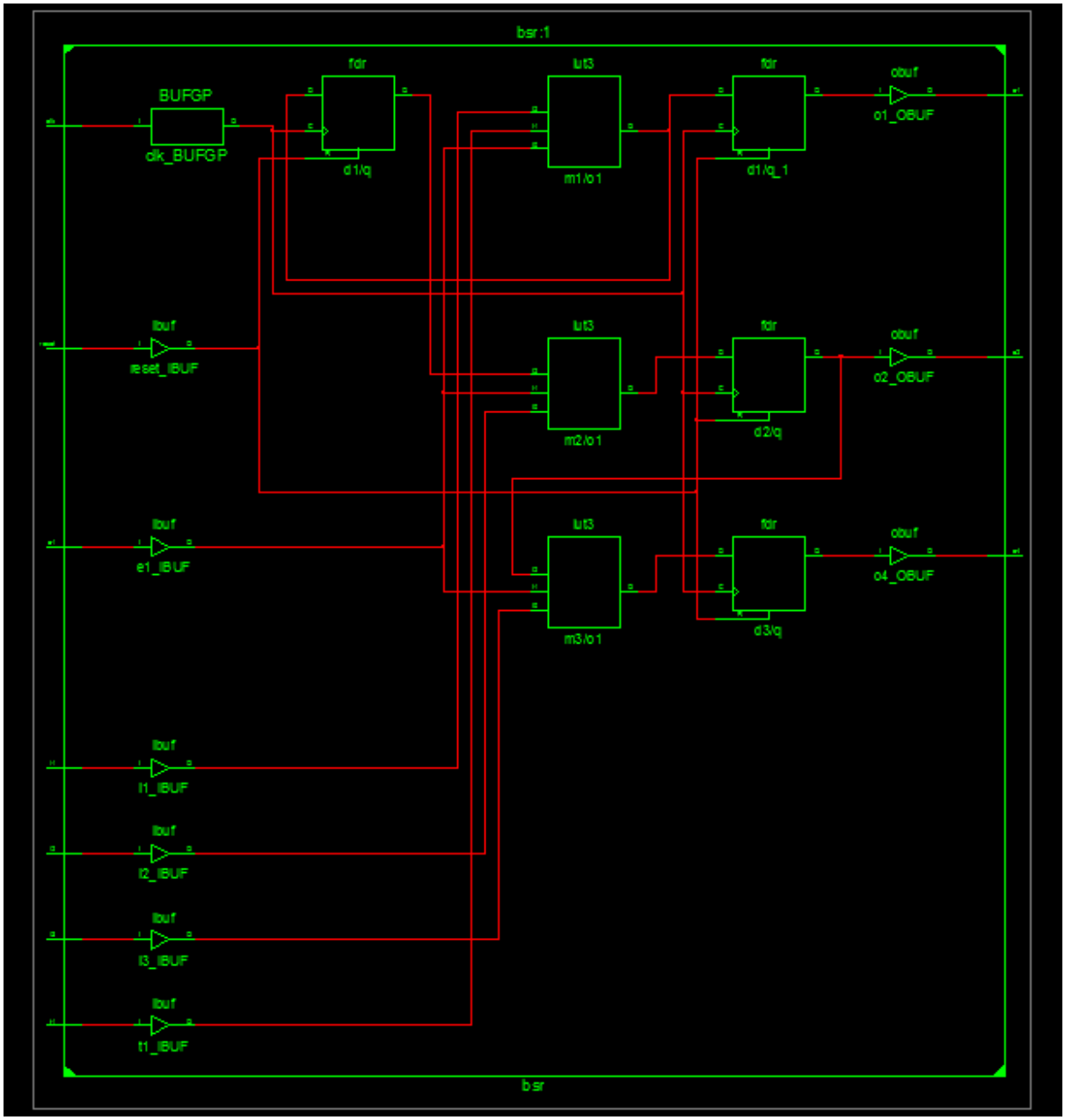
Number of Slices	:	0
Macros	:	1 Registers, 1 Flip-flops
Number of IOs	:	4
Number of bonded IOBs	:	4
Delay	:	Before clock: 2.258ns, after clock: 4.04ns

Experiment-9: Boundary scan register

RTL Schematic



Technology Schematic

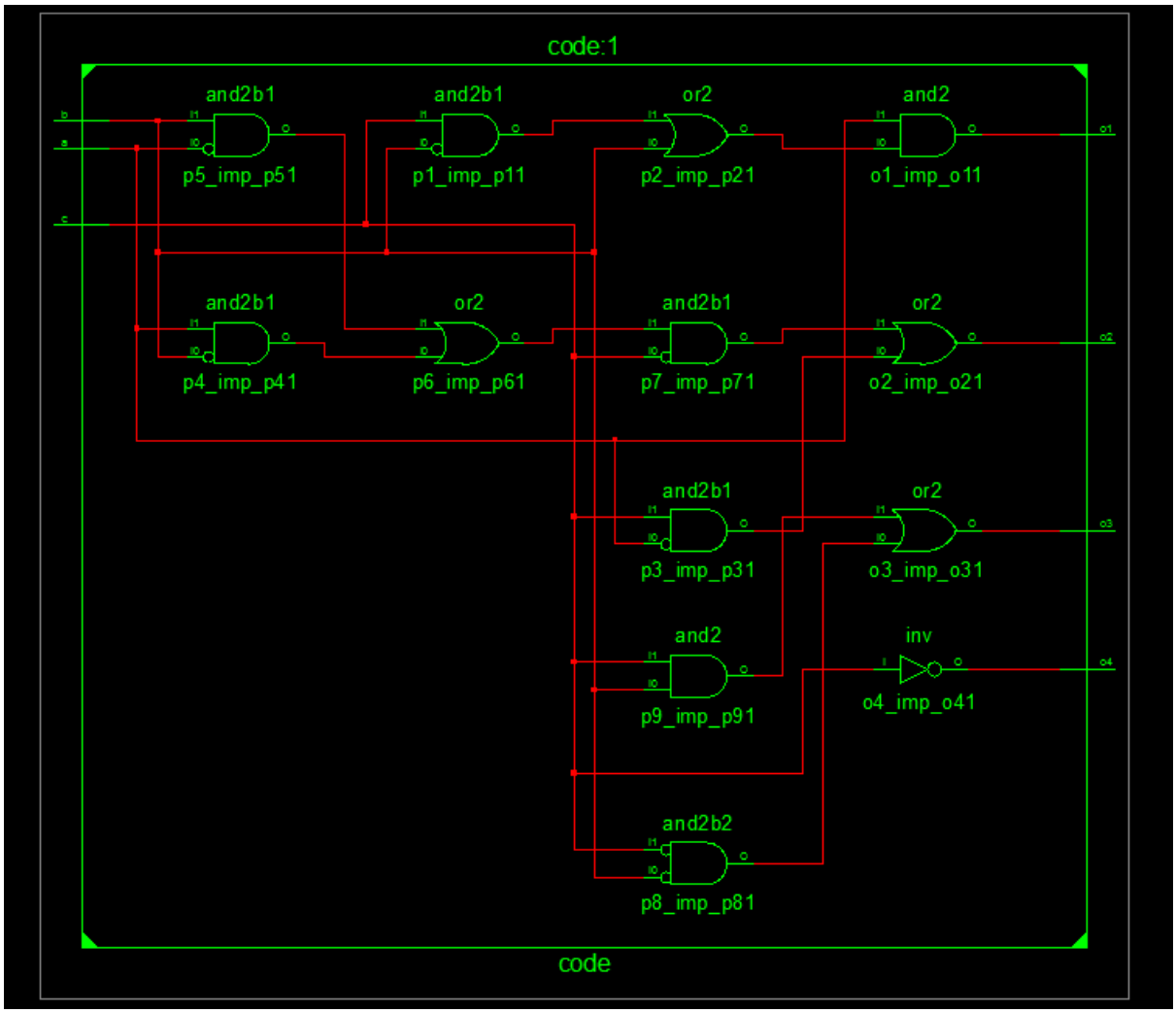


Design statistics

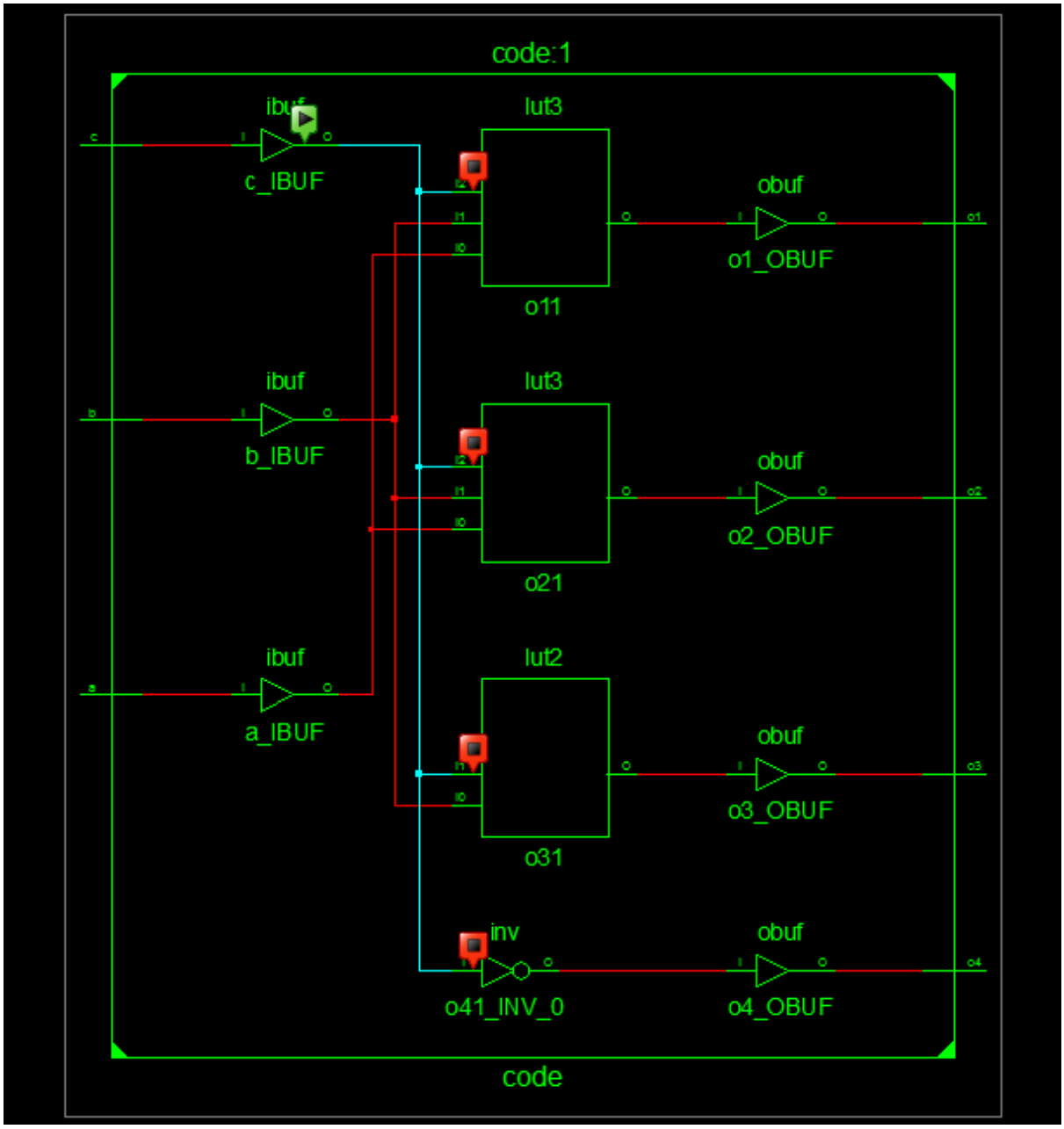
Number of Slices	:	2
Number of 4 input LUTs	:	3
Number of IOs	:	10
Number of bonded IOBs	:	10
Macros	:	4 Register, 4 Flip-Flops
Delay	:	Before clock: 2.589ns, after clock: 4.063ns

Experiment-10: Binary to XS 3 Parallelization

RTL Schematic



Technology Schematic

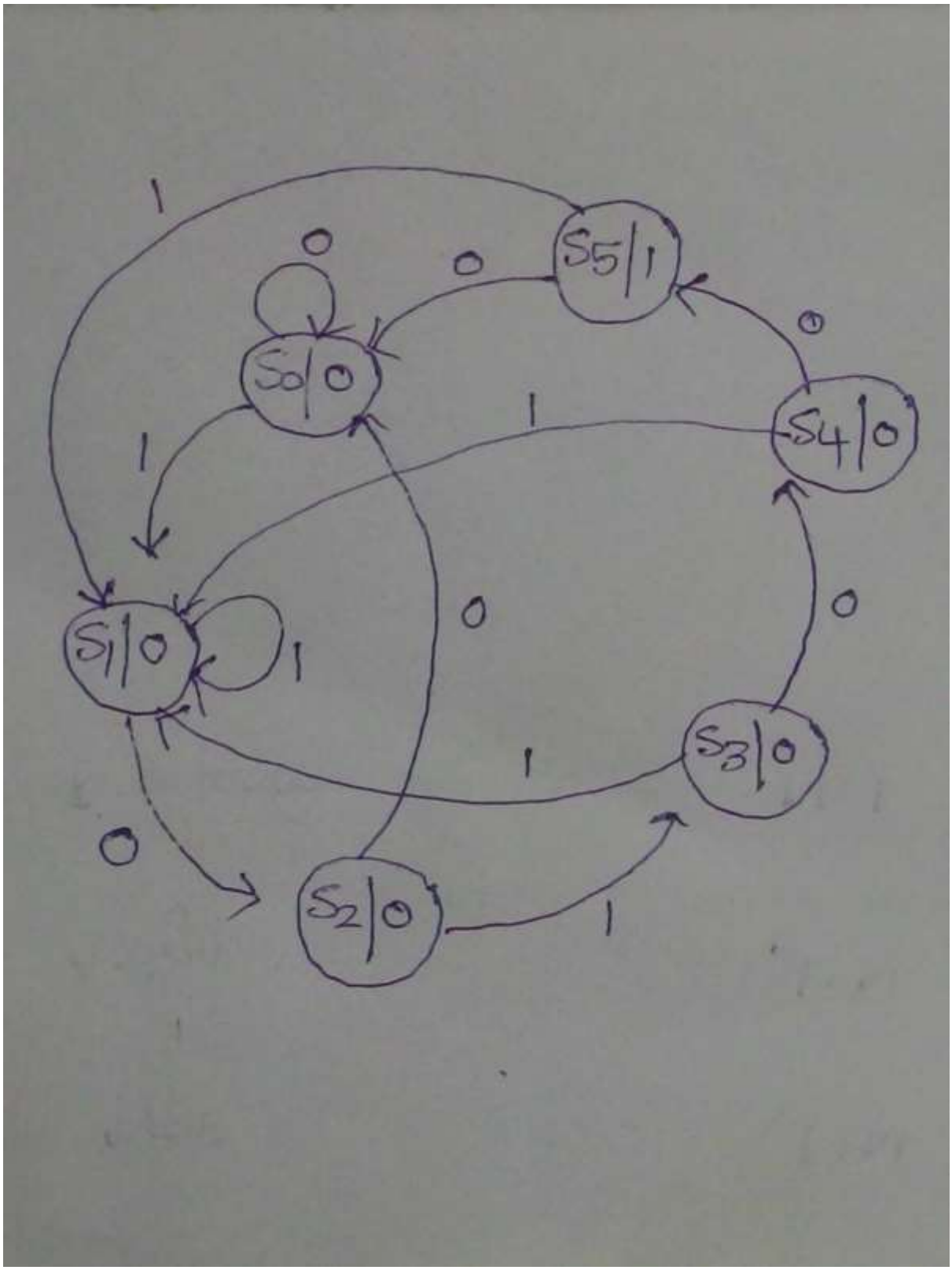


Design Statistics

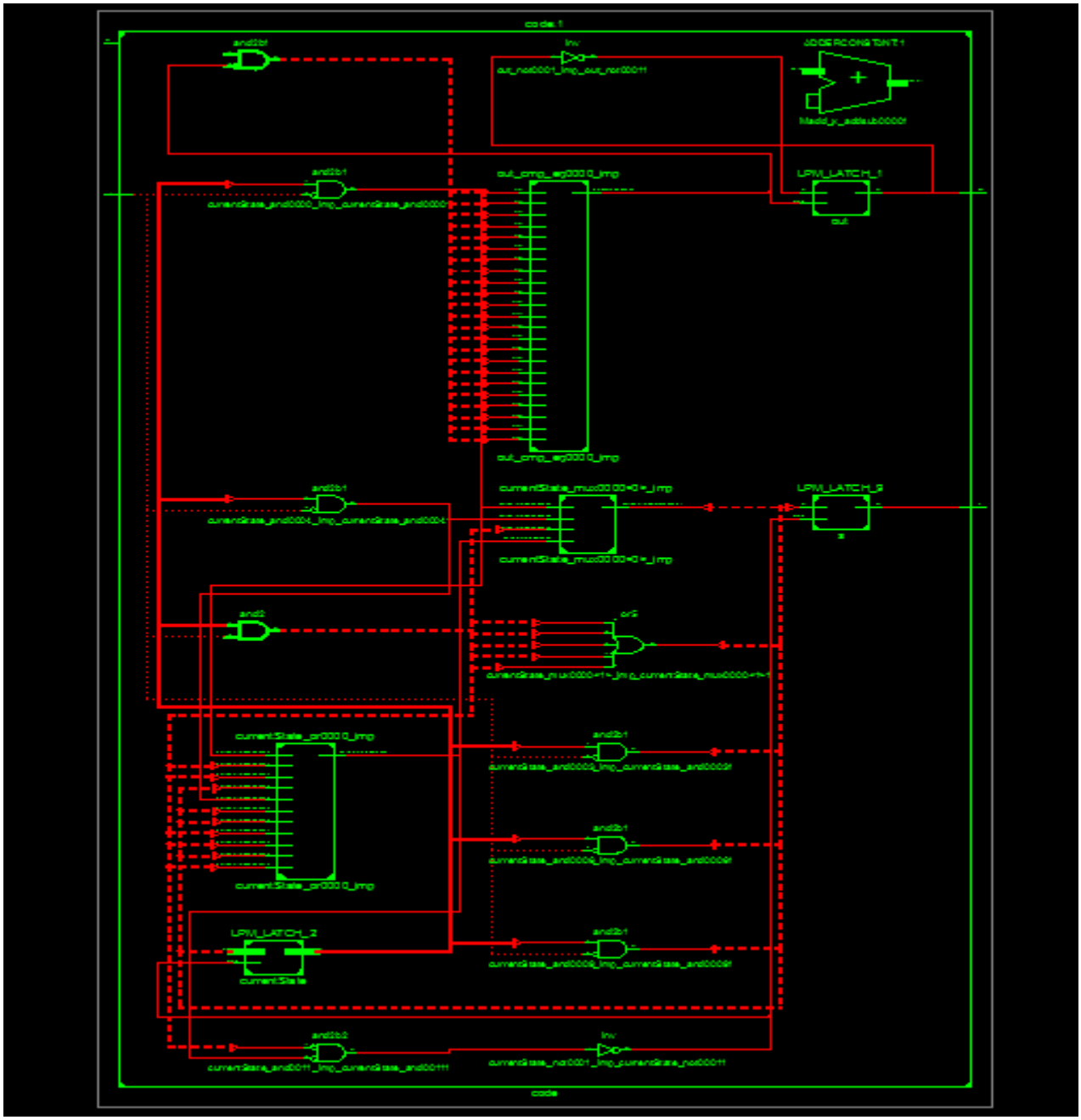
Number of Slices	:	1
Number of 4 input LUTs	:	2
Number of IOs	:	7
Number of bonded IOBs	:	7
Delay	:	6.054ns (Levels of Logic = 4)

Experiment-11: Moore finite state machine (Sequence 10100)

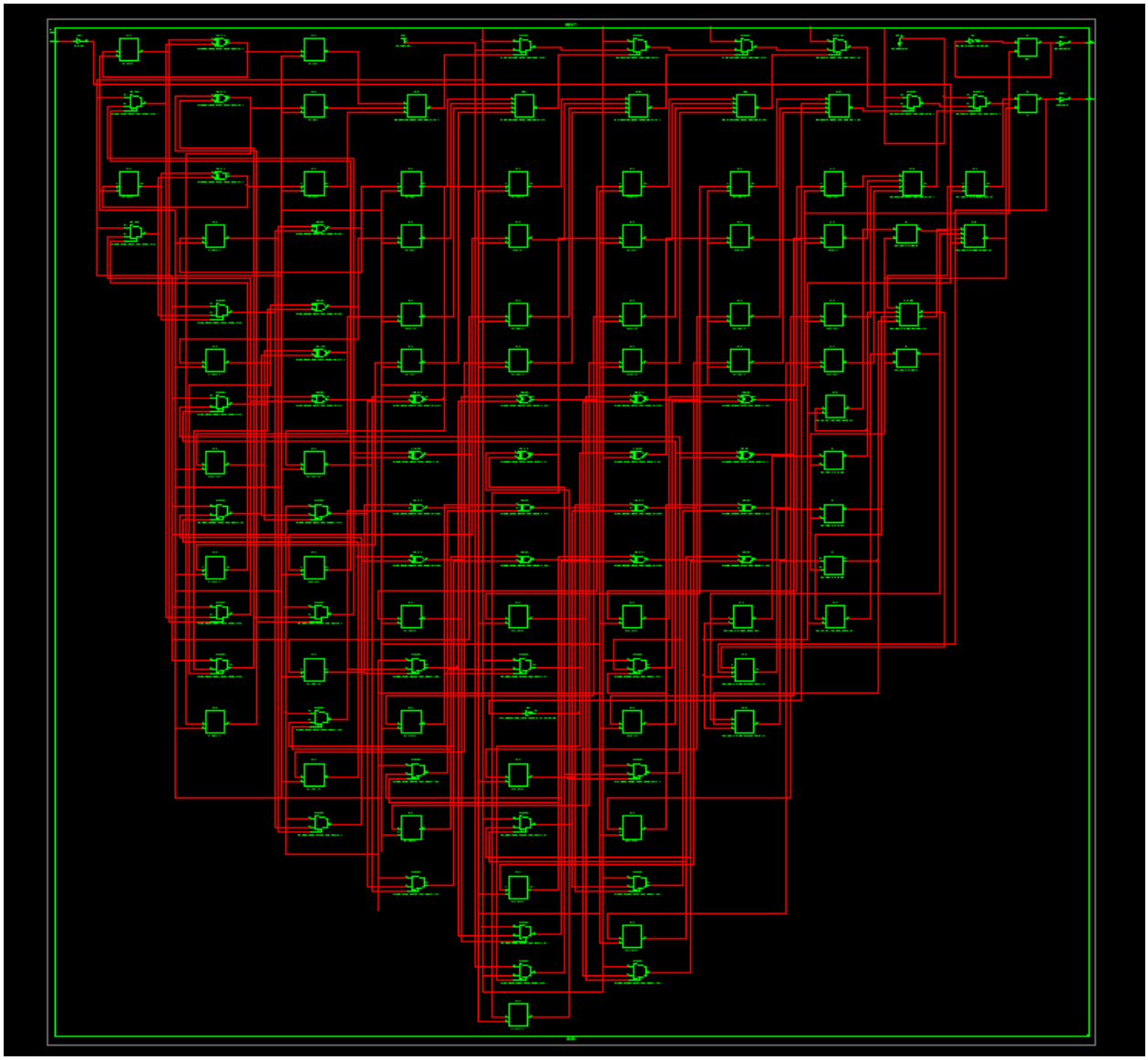
State Diagram



RTL Schematic


code 1
and2b1
inv
out_cmp_eg0000_imp
LPM_LATCH_1
out
and2b1
and2b1
LPM_LATCH_9
and2
or5
and2b1
and2b1
LPM_LATCH_2
and2b1
and2b2
inv
code

Technology Schematic

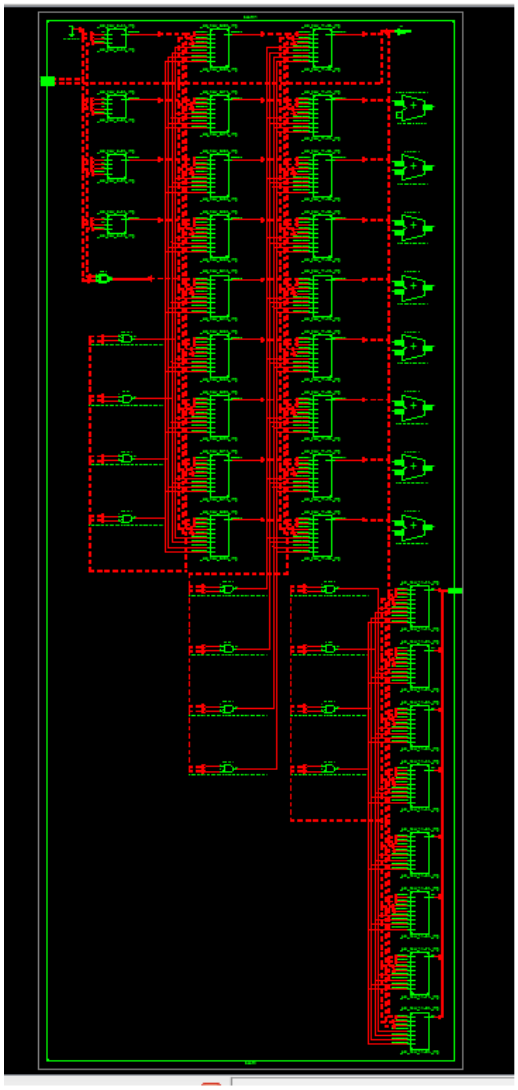


Design Statistics

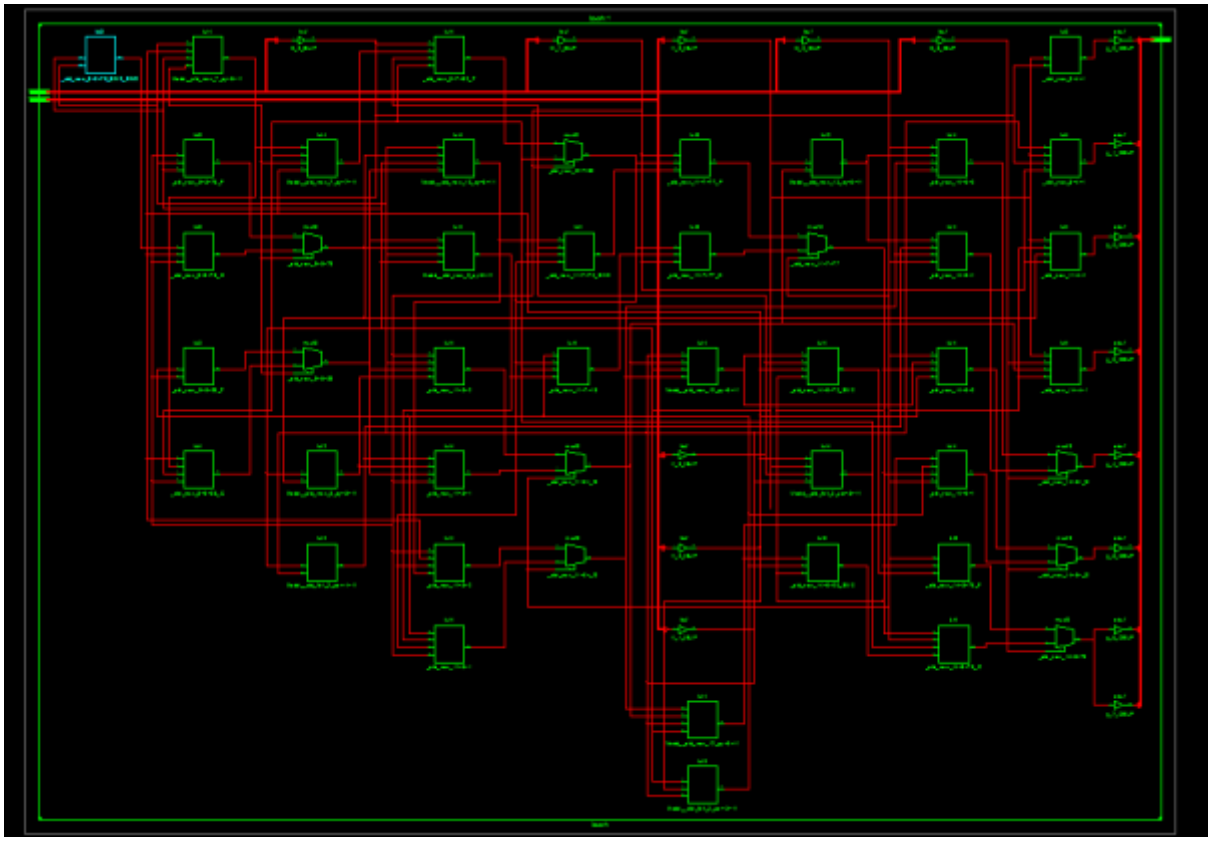
Number of Slices	:	33
Number of 4 input LUTs	:	61
Number of IOs	:	4
Number of bonded IOBs	:	4
Delay	:	Before clock: 2.054ns, after clock: 4.208ns

Experiment-12: Booth multiplier (4 Bit)

RTL Schematic



Technology schematic

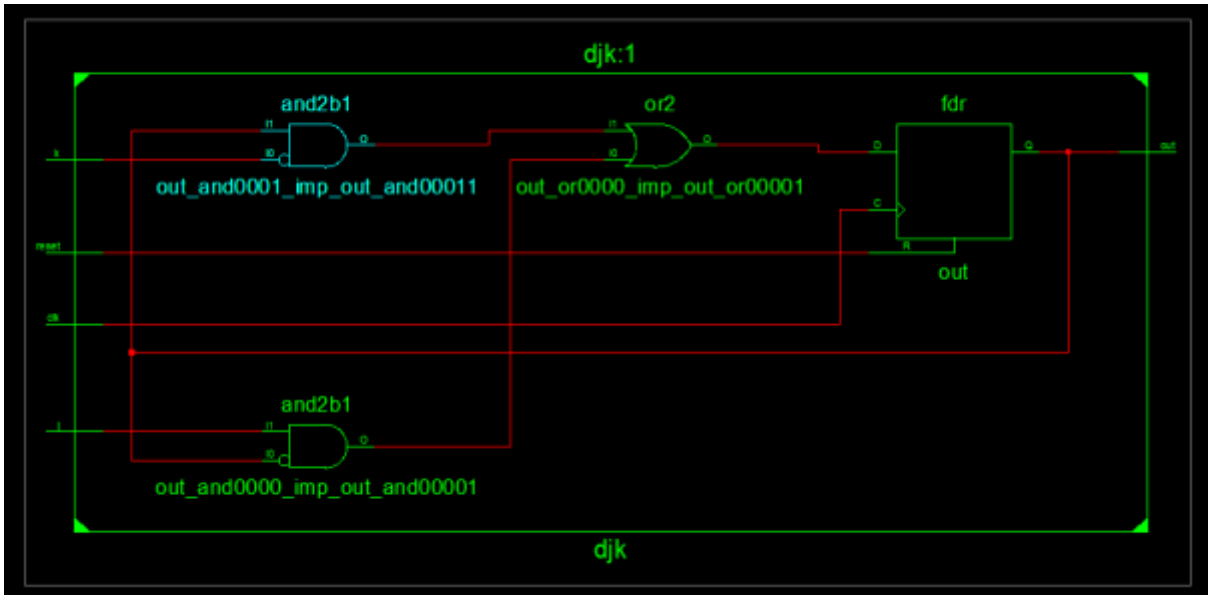


Design Statistics

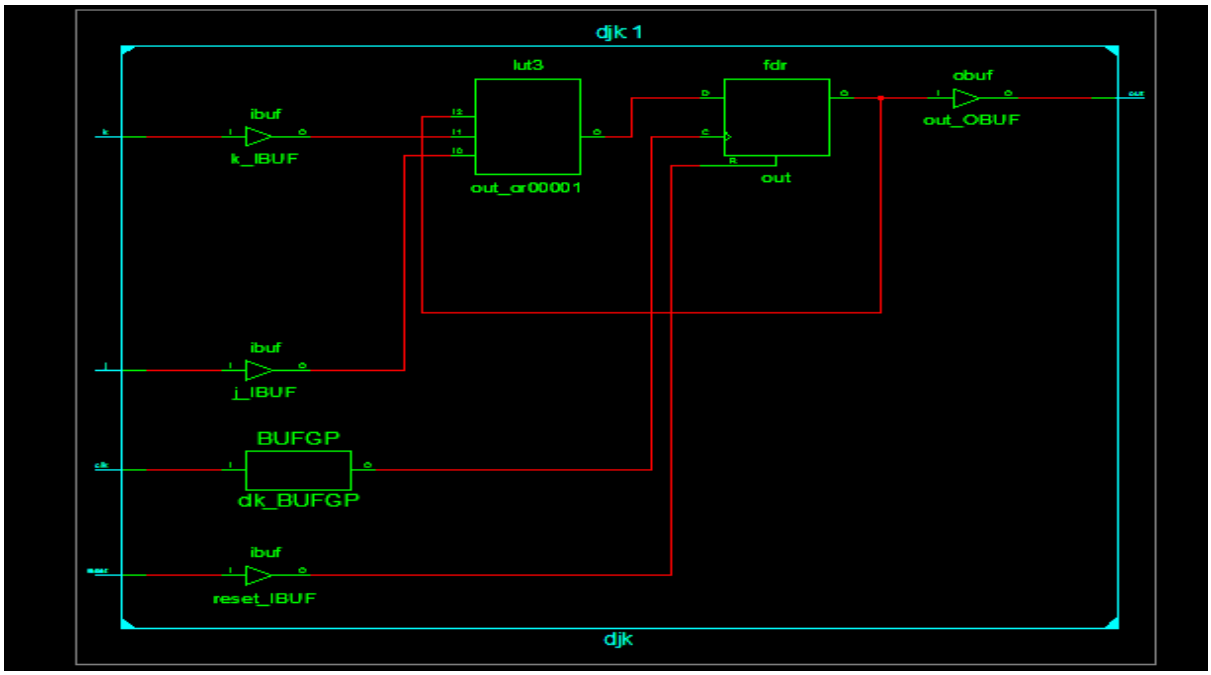
Number of Slices	:	21
Number of 4 input LUTs	:	37
Number of IOs	:	16
Number of bonded IOBs	:	16
Delay	:	14.205ns (Levels of Logic = 12)

Experiment 13 D_TO_JK Flip-flop

RTL Schematic



Technology Schematic

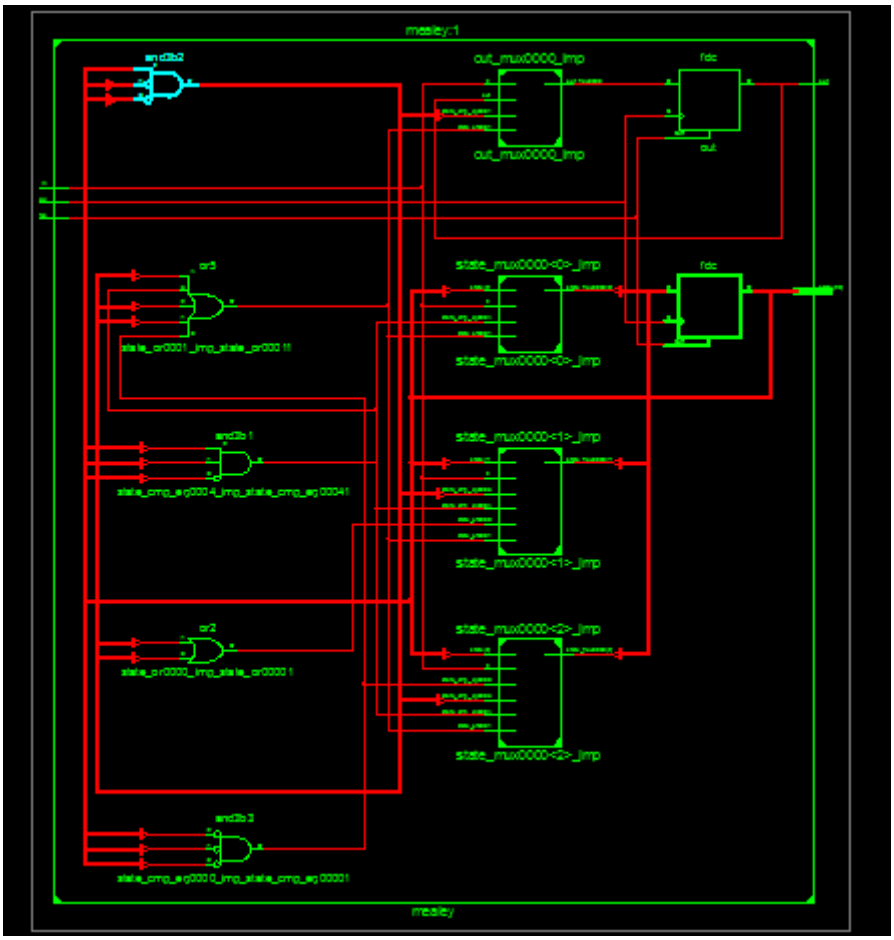


Design statistics

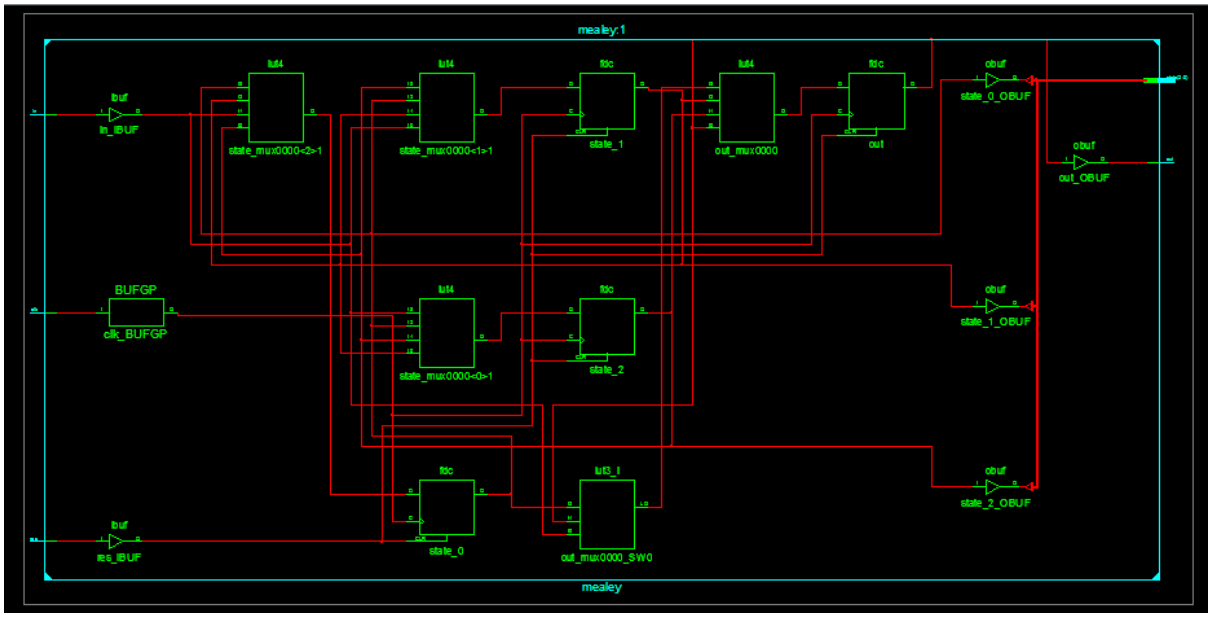
Number of Slices	:	1
Number of 4 input LUTs	:	1
Number of IOs	:	5
Number of bonded IOBs	:	5
Macros	:	1 Register, 1 Flip-Flops
Delay	:	Before clock: 2.495ns, after clock: 4.063ns

Experiment-14: Mealy machine

RTL Schematic



Technology Schematic



Design statistics

Number of Slices	:	3
Number of 4 input LUTs	:	5
Number of IOs	:	7
Number of bonded IOBs	:	7
Macros	:	4 Register, 4 Flip-Flops
Delay	:	Before clock: 2.677ns, after clock: 3.352ns