**COA Course Activity pattern**

Design and simulate a **2-stage pipelined processor**, which can perform Load/Store, Arithmetic & Logical operations on a set of data. Design for a Harward Architecture, separate code memory & separate data memory to store program instructions and operands respectively. Include all the control & status registers like PC (to hold address of instruction), MAR (to hold the memory address), MBR (to hold the data from memory), PSW (to hold status of condition codes) and IR (to decode the instruction). Include a **Register file of 16 Registers** (R0—R15). Include a data memory and code memory of suitable size.

* Fetch the instruction using the contents of PC and update PC
* Decode the instruction from IR
* Fetch the operands (wherever applicable)
* Execute the operation
* Write the result back in the destination (wherever applicable)

Each team needs to implement the problem statement using given addressing mode. The addressing modes to be implemented are:

1. Direct addressing
2. Indirect addressing
3. Register addressing
4. Immediate addressing

**Specifications to be followed for design**

**Instruction Set**

|  |  |  |
| --- | --- | --- |
| **Inst.No** | **Opcode** | **Operation** |
| 1 | 0000 | Load |
| 2 | 0001 | Store |
| 3 | 0010 | Add |
| 4 | 0011 | Subtract |
| 5 | 0100 | Multiply |
| 6 | 0101 | Divide |
| 7 | 0110 | Increment |
| 8 | 0111 | Decrement |
| 9 | 1000 | And |
| 10 | 1001 | Or |
| 11 | 1010 | Not |
| 12 | 1011 | Exchange |
| 13 | 1100 | Shift Right |
| 14 | 1101 | Shift Left |
| 15 | 1110 | Rotate right |
| 16 | 1111 | Rotate left |

|  |  |  |
| --- | --- | --- |
| **2- address format** | | |
| **Opcode(4 bits)** | **Register address (4 bits)** | **Mem loc (8-bits) /Register(4-bits) /Immediate (8-bits) / Indirect address (8-bits)** |

|  |  |  |  |
| --- | --- | --- | --- |
| **3-address format** | | | |
| **Opcode(4 bits)** | **Destination Register address (4 bits)** | **Source Register address (4 bits)** | **Mem loc (8-bits) /Register (4-bits) /Immediate (8-bits) / Indirect address (8-bits)** |

|  |  |
| --- | --- |
| **1-address format** | |
| **Opcode(4 bits)** | **Mem loc (12-bits) /Register(4-bits) /Immediate (12-bits) / Indirect address (12-bits)** |

**Evaluation plan (Final evaluation will be carried out for 20 marks)**

* Each team will be assigned a problem statement based on the given pattern and addressing mode
* Each team is expected to design the processor architecture for the given problem **(05 marks)**
* Each team is expected to write an assembly code snippet **(05 marks)**
* The code snippet is to be simulated and output shown in the team **(05 marks)**
* Each team should write a brief report on **(05 marks)**
  + Challenges faced
  + How you overcame them
  + Brief Comparative study of contemporary processors

**Assessment Rubrics for Activity**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Parameters** | **Excellent** | **Good** | **Scope for improvement** | **PI** |
| Architecture & Design phase  **(05 M)** | Able to innovate in the design of the processor for the chosen instruction set.  **(4-5M)** | Able to design the processor for the chosen instruction set.  **(2-3M)** | Able to design the processor, but works for only few instructions.  **(0-1 M)** | 2.1.2 |
| Implementation of Datapath  **(05 M)** | Proposes an optimal solution in a manner that thoroughly addresses multiple contextual factors of the problem.  **(4-5M)** | Proposes the solution in a manner that superficially addresses multiple contextual factors of the problem. **(2-3M)** | Proposes the solution in a manner that ignores multiple contextual factors of the problem**.**  **(0-1 M)** | 3.3.1 |
| Simulation  **(03M)** | Able to simulate designed processor datapath and the simulation shows output for all possible inputs.  **(3M)** | Able to simulate the processor datapath partially.  **(1-2M)** | Unable to simulate.  **(0 M)** | 5.3.1 |
| Teamwork & collaboration.  **(02M)** | There was an indication of high level of collaboration, communication and good teamwork.  **(2M)** | There was indication of some level of collaboration, communication and good teamwork.  **(1M)** | There was indication that team did not collaborate and communicate well. **(0M)** | 9.3.1 |
| Comparative study of contemporary processors  **(05 M)** | Details are complete and comprehensive. Areas of comparison have been thoroughly addressed.  **(4-5M)** | Comparisons with some details complete and comprehensive.  **(2-3M)** | Details of the comparison are lacking.  **(0-1 M)** | 12.3.1 |