Lab 3: The Arithmetic Logic Unit

Frederick Meneses

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Part I

2. Export the subcircuit schematic as an image and include it in your report.

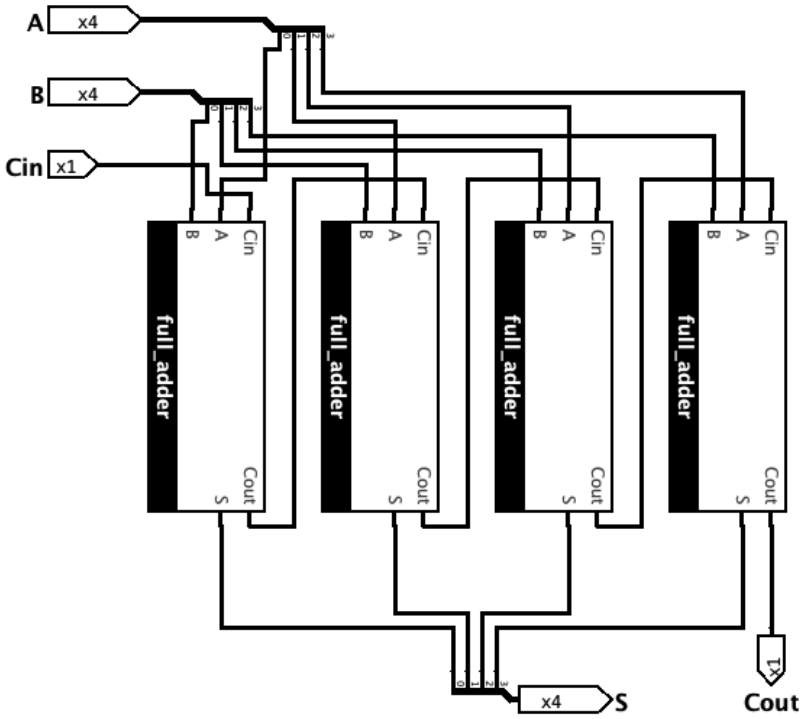

Figure 1: A schematic of ripple_carry4.

3. Include a screenshot of your simulated test vector for the 4-bit Ripple Carry Adder.

Part II

1. Export the subcircuit schematic of each operation as an image and include it in your report.
2. Include a screenshot of your simulated test vectors for op3, op4, and op5.
3. Export the ALU schematic as an image and include it in your report.

Test Vector ripple_carry4 of lab3

Passed: 4 Failed: 0

Status	A	B	Cin	Cout	S
pass	0000	0000	0	0	0000
pass	0111	0111	0	0	1110
pass	1111	0111	0	1	0110
pass	1111	1111	0	1	1110

Figure 2: A simulation ripple_carry4.

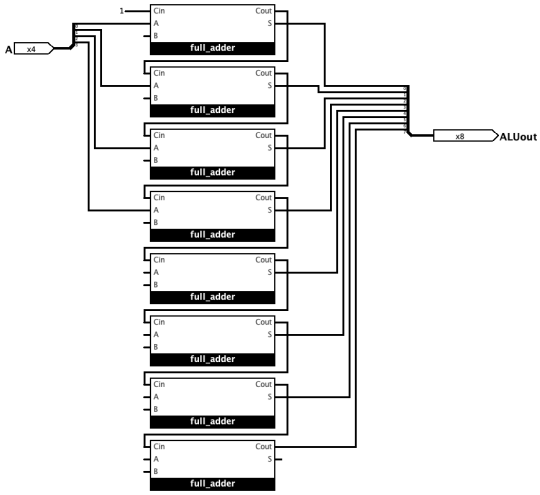

Figure 3: A schematic of op0.

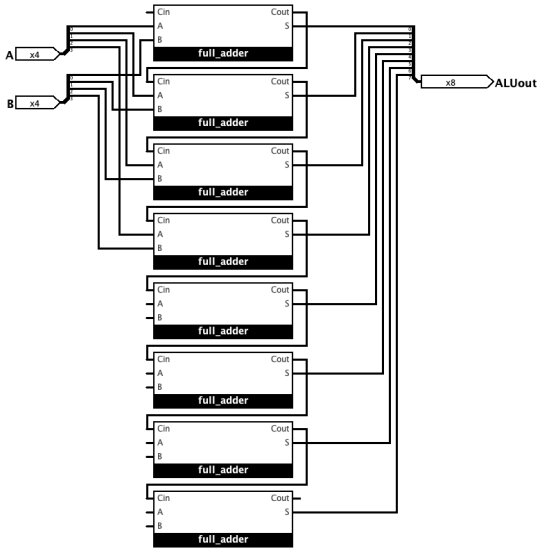

Figure 4: A schematic of op1.

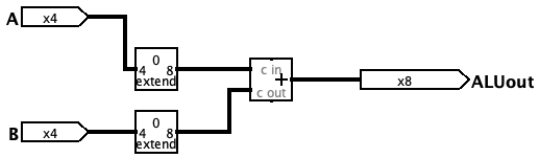

Figure 5: A schematic of op2.

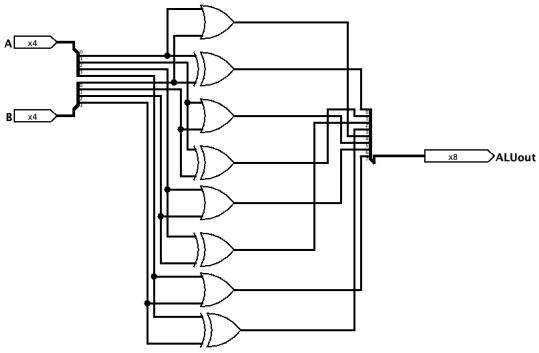

Figure 6: A schematic of op3.

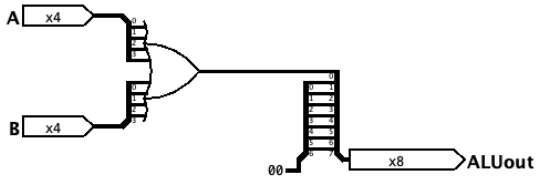

Figure 7: A schematic of op4.

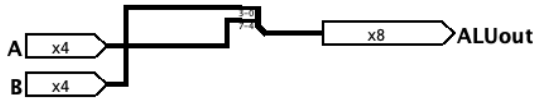

Figure 8: A schematic of op5.

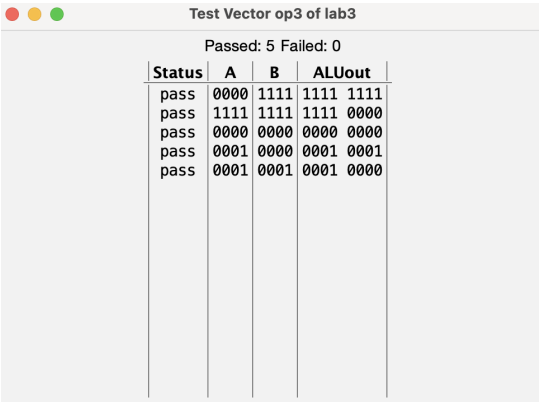

Figure 9: A simulation of op3.

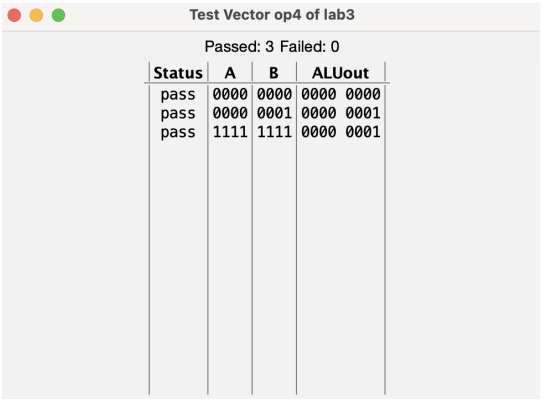

Figure 10: A simulation of op4.

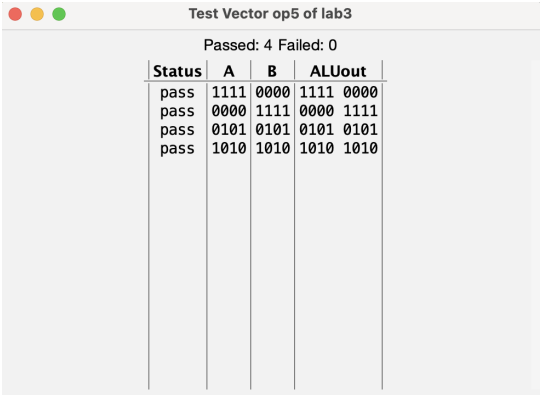

Figure 11: A simulation of op5.

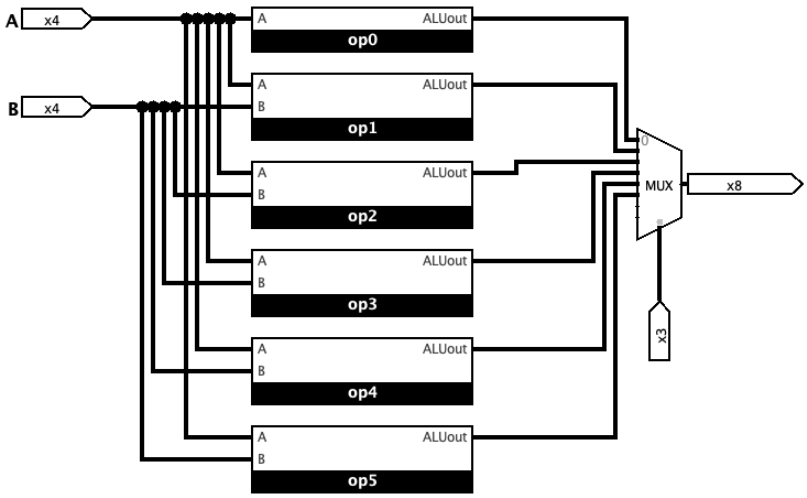

Figure 12: A schematic of the ALU.