

# Lab 6: Finite State Machines

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## 1 Part I

1. Complete Table 1 below.

Table 1: State Encodings

State	Encoding
A/0	101
B/0	001
C/0	000
D/0	011
E/0	110
F/1	111
G/1	100

2. Complete Table 2 below.

Table 2: Encoded State Transition Table for Robo-Snail

<i>curr_state</i> [2..0]				<i>w</i>	<i>next_state</i> [2..0]		
0	0	0	0	0	1	1	0
0	0	0	1	1	0	1	1
0	0	1	0	0	1	0	1
0	0	1	1	1	0	0	0
0	1	0	0	0	—	—	—
0	1	0	1	1	—	—	—
0	1	1	0	0	1	1	0
0	1	1	1	1	1	1	1
1	0	0	0	0	1	0	1
1	0	0	1	1	0	0	0
1	0	1	0	0	1	0	1
1	0	1	1	1	0	0	1
1	1	0	0	0	1	0	1
1	1	0	1	1	1	0	0
1	1	1	0	0	1	1	0
1	1	1	1	1	1	1	1

3. Derive equations for each of your next state outputs below.

$$\begin{aligned}
S'_0 &= next\_state_0 \cdot \overline{next\_state_1} \cdot next\_state_2 + \overline{next\_state_0} \cdot \overline{next\_state_1} \cdot next\_state_2 \\
S'_1 &= next\_state_0 \cdot \overline{next\_state_1} \cdot next\_state_2 + \overline{next\_state_0} \cdot \overline{next\_state_1} \cdot next\_state_2 \\
S'_2 &= next\_state_0 \cdot next\_state_1 \cdot \overline{next\_state_2} + \overline{next\_state_0} \cdot next\_state_1 \cdot next\_state_2 \\
S'_3 &= next\_state_0 \cdot next\_state_1 \cdot \overline{next\_state_2} + next\_state_0 \cdot next\_state_1 \cdot next\_state_2 \\
S'_4 &= next\_state_0 \cdot \overline{next\_state_1} \cdot next\_state_2 + next\_state_0 \cdot \overline{next\_state_1} \cdot \overline{next\_state_2} \\
S'_5 &= next\_state_0 \cdot next\_state_1 \cdot \overline{next\_state_2} + next\_state_0 \cdot next\_state_1 \cdot next\_state_2 \\
S'_6 &= next\_state_0 \cdot \overline{next\_state_1} \cdot next\_state_2 + \overline{next\_state_0} \cdot \overline{next\_state_1} \cdot \overline{next\_state_2}
\end{aligned}$$

4. Export the subcircuit schematic as an image and include it in your report.

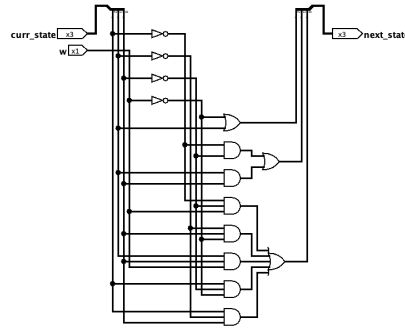


Figure 1: A schematic of part1\_state.table.

5. Complete Table 3 below.

Table 3: Encoded Output Table for Robo-Snail

State	Output
101	0
001	0
000	0
011	0
110	0
111	1
100	1

6. Derive the equation for your output logic below.

$$Z = F + G = curr\_state_0 \cdot curr\_state_1 \cdot curr\_state_2 + curr\_state_0 \cdot \overline{curr\_state_1} \cdot \overline{curr\_state_2}$$

7. Export the subcircuit schematic as an image and include it in your w

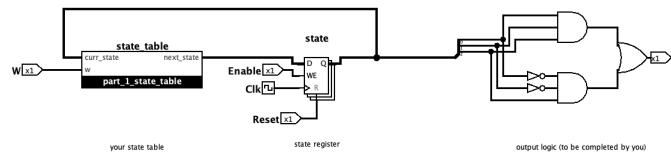


Figure 2: A schematic of part1.FSM.

## 2 Part II

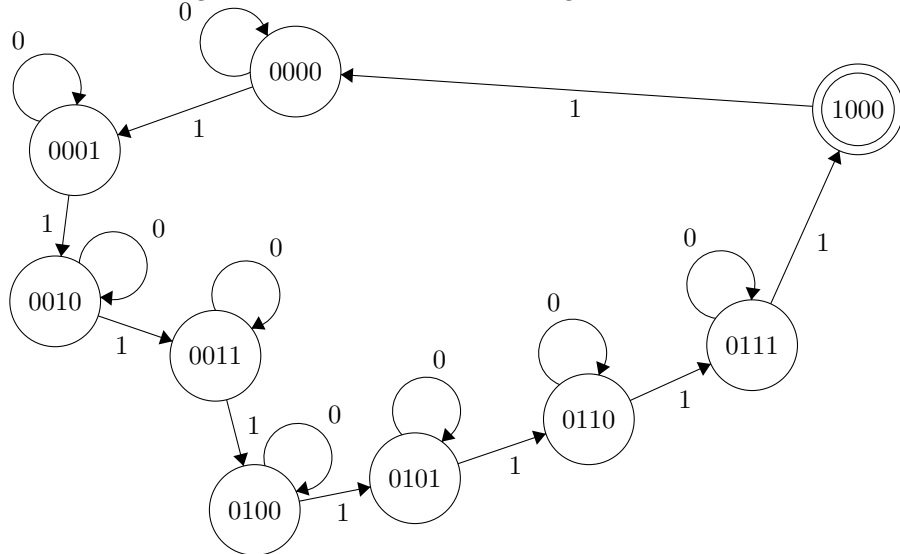
1. Complete Table 4 below.

Table 4: Encoded State Transition Table for Part II

$state[3..0]$	$ld_a$	$ld_b$	$ld_c$	$ld_x$	$alu\_select_a[1..0]$	$alu\_select_b[1..0]$	$ld\_alu\_out$	$alu\_op$	$ld_r$	$next\_state[3..0]$
0 0 0 0	1	0	0	0	0	0	0	0	0	0 0 0 1
0 0 0 1	0	1	0	0	0	0	0	0	0	0 0 1 0
0 0 1 0	0	0	1	0	0	0	0	0	0	0 0 1 1
0 0 1 1	0	0	0	1	0	0	0	0	0	0 1 0 0
0 1 0 0	0	1	0	0	0	1	1	1	1	0 0 1 0
0 1 0 1	0	1	0	0	0	0	0	1	0	0 0 1 1
0 1 1 0	1	0	0	0	1	0	1	1	0	0 1 1 1
0 1 1 1	1	0	0	0	0	1	1	1	0	1 0 0 0
1 0 0 0	0	0	0	0	0	0	1	0	0	0 0 0 0
1 0 0 1	0	0	0	0	0	0	0	0	0	0 0 0 0
1 0 1 0	0	0	0	0	0	0	0	0	0	0 0 0 0
1 0 1 1	0	0	0	0	0	0	0	0	0	0 0 0 0
1 1 0 0	0	0	0	0	0	0	0	0	0	0 0 0 0
1 1 0 1	0	0	0	0	0	0	0	0	0	0 0 0 0
1 1 1 0	0	0	0	0	0	0	0	0	0	0 0 0 0
1 1 1 1	0	0	0	0	0	0	0	0	0	0 0 0 0

2. Draw the state transition diagram and include it in Figure 3.

Figure 3: The state transition diagram for Part II



3. Simulate your circuit using a variety of input settings.

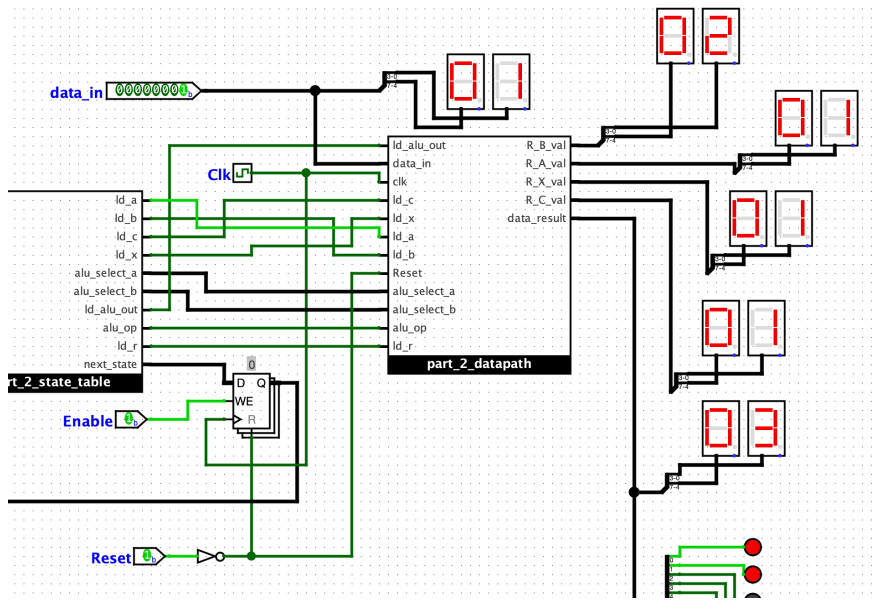


Figure 4: Test Case for Part 2.

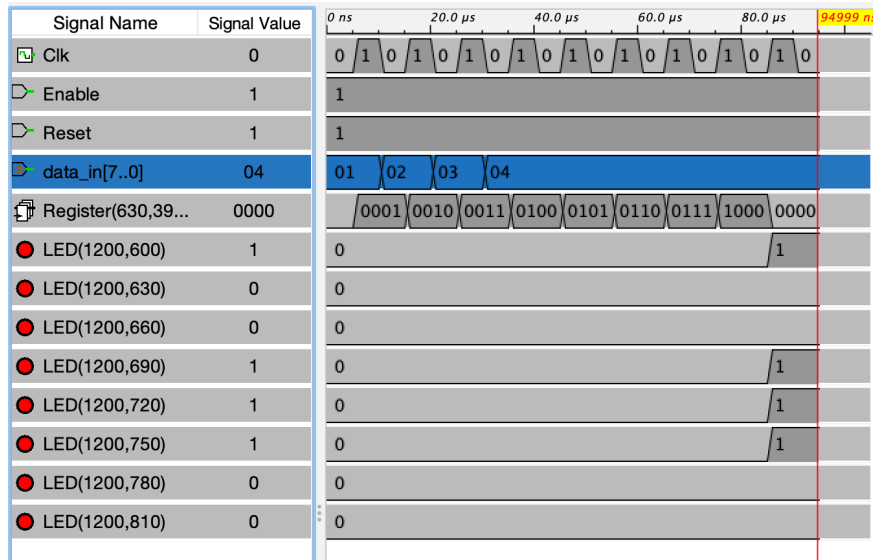


Figure 5: Test Case for Part 2.

### 3 Part III

1. Draw a schematic for the datapath of your circuit. It will be similar to the handout. You should show how you will initialize the registers, where the outputs are connected, and include all the control signals that you require.
2. Draw the state diagram that controls your datapath.

Figure 6: State diagram that controls the datapath in Part 3.

3. Draw the schematic for your controller module.

Figure 7: Controller Module in Part III.

4. Draw the top-level schematic showing how the datapath and controller are connected as well as the inputs and outputs to your top-level circuit.

Figure 8: Top level schematics schematic in Part III.

5. Simulate your circuit using a variety of input settings.

Figure 9: Test Case for Part 3.

Figure 10: Test Case for Part 3.