Lab 5: Counters and Clocks

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1 Part I

1. Export the subcircuit schematic as an image and include it in your report.

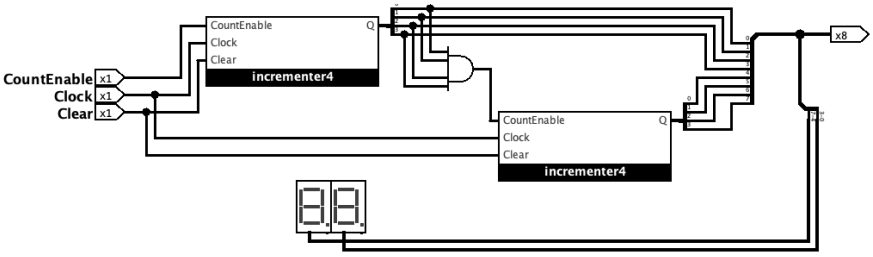

Figure 1: A schematic of counter8.

2. Include a screenshot of your simulation.

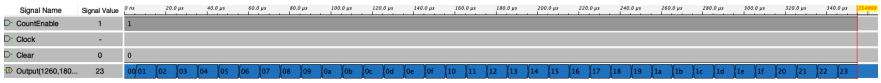

Figure 2: A timing diagram for counter8.

2 Part II

1. The check for the maximum value is not necessary in the example above. Explain why in your prelab report. It is not necessary because the CounterOut will rise to 1 when it hits the maximum value and reset the counter.
2. If you wanted this 4-bit counter to count from 0-9, how would you adjust the circuit above? Add a comparator to the output of the counter where its output is connected to the input of the counter, comparing the counter's memory to the 4-bit value 1001, resetting the counter if it reaches 9.
3. In Properties there is a setting called Action On Overflow. Explain how each value for this setting responds to overflow by experimenting with this setting and describing the results.
   Wrap around: if counting up, then the next value after overflow is 0. If counting down, then the next value after overflow is the maximum value.
   Stay at value: At overflow, if counting up, then the counter stays at the maximum value. If counting down, then it stays at 0. They stay at this value until bit width is reached. After which, it stays at the loaded value until it continues.
   Continue counting: At overflow, If counting up, then the counter's memory resets itself but keeps counting until it hits the maximum number of bit allotted. If counting down, then counts from the maximum until the maximum allotted bit is reached. Whatever is loaded in the bit input load, is saved for the next cycle.
   Load next value: Loads the next value from the bit input load.
4. Export the subcircuit schematic as an image and include it in your report.
5. Export the timing diagram as an image and include it in your report.

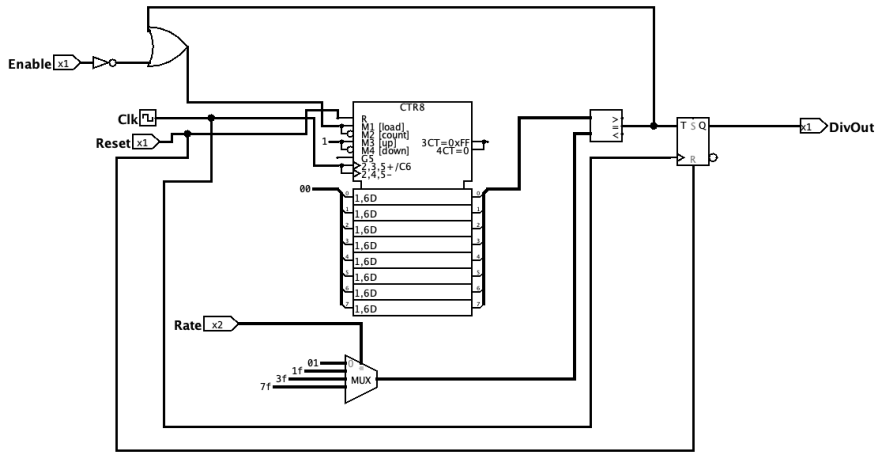

Figure 3: A schematic of rate_divider.

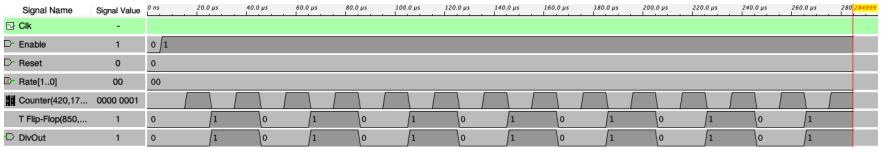

Figure 4: A timing simulation of rate_divider.

3 Part III

1. Fill in a table with your binary representation of each letter from S to Z.

Letter	Morse Code	Pattern Representation (pattern length is 14 bits)
S	• • •	10101000000000
T	—	11100000000000
U	• • —	10101110000000
V	• • • —	10101011100000
W	• — —	10111011100000
X	— • • —	11101010111000
Y	— • — —	11101011101110
Z	— — • •	11101110101000

Table 1: Morse Pattern Representation with fixed bit-width

2. Export the subcircuit schematic as an image and include it in your report.

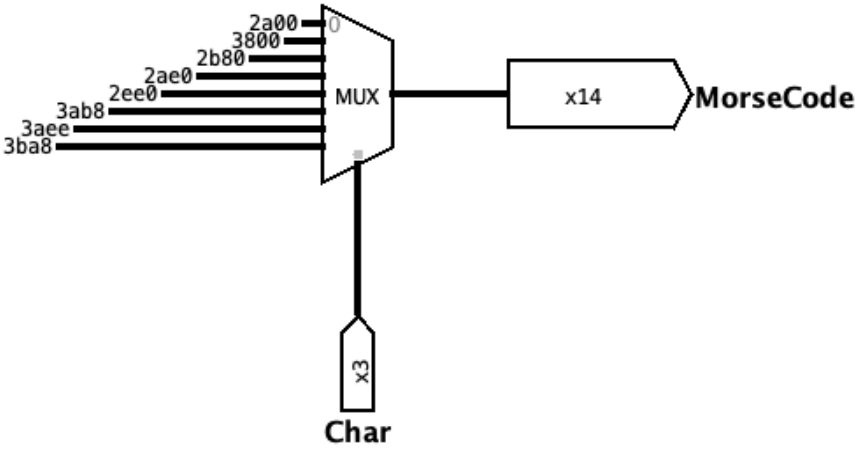

Figure 5: A schematic of MORSE_LUT.