Lab 2: The Design Hierarchy

Frederick Meneses

January 22, 2023

Part I

1. If the truth table in Table 2.1 of the handout was given in full, how many rows would it have?

   2^6 rows.

2. Export the schematic of the mux4to1 subcircuit as an image and include it in your report.

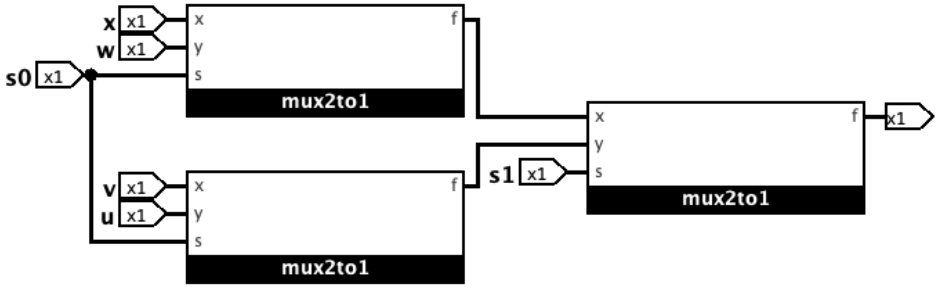

Figure 1: A schematic of the 4-to-1 multiplexer

Part II

1. Derive seven truth tables, one for each segment of the 7-segment decoder.

$D_{3:0}$	Character	S_0	S_1	S_2	S_3	S_4	S_5	S_6
0000	0	1	1	1	1	1	1	0
0001	1	0	1	1	0	0	0	0
0010	2	1	1	0	1	1	0	1
0011	3	1	1	1	1	0	0	1
0100	4	0	1	1	0	0	1	1
0101	5	1	0	1	1	0	1	1
0110	6	1	0	1	1	1	1	1
0111	7	1	1	1	0	0	0	0
1000	8	1	1	1	1	1	1	1
1001	9	1	1	1	1	0	1	1
1010	A	1	1	1	0	1	1	1
1011	b	0	0	1	1	1	1	1
1100	c	0	0	0	1	1	0	1
1101	d	0	1	1	1	1	0	1
1110	E	1	0	0	1	1	1	1
1111	F	1	0	0	0	1	1	1

2. Use Karnaugh maps to write seven Boolean functions for each segment so that they are optimized.

$$S_0 = \overline{vx} + \overline{u}w + \overline{u}vx + vw + u\overline{vw}$$
$$S_1 = \overline{uv} + \overline{uwx} + \overline{vx} + \overline{u}wx + u\overline{w}x$$
$$S_2 = \overline{uw} + \overline{u}x + \overline{w}x + \overline{u}v + u\overline{v}$$
$$S_3 = \overline{uvx} + \overline{u}w\overline{x} + \overline{v}wx + v\overline{w}x + u\overline{w} + uv\overline{x}$$
$$S_4 = \overline{vx} + w\overline{x} + uw + uv$$
$$S_5 = \overline{uwx} + \overline{u}v\overline{w} + \overline{u}v\overline{x} + u\overline{v} + uw$$
$$S_6 = \overline{v}w + v\overline{w} + v\overline{x} + u$$

3. Use the naming scheme `HEX0`, `HEX1`, ..., `HEX6` for each subcircuit. Export each subcircuit schematic as an image and include it in your report.

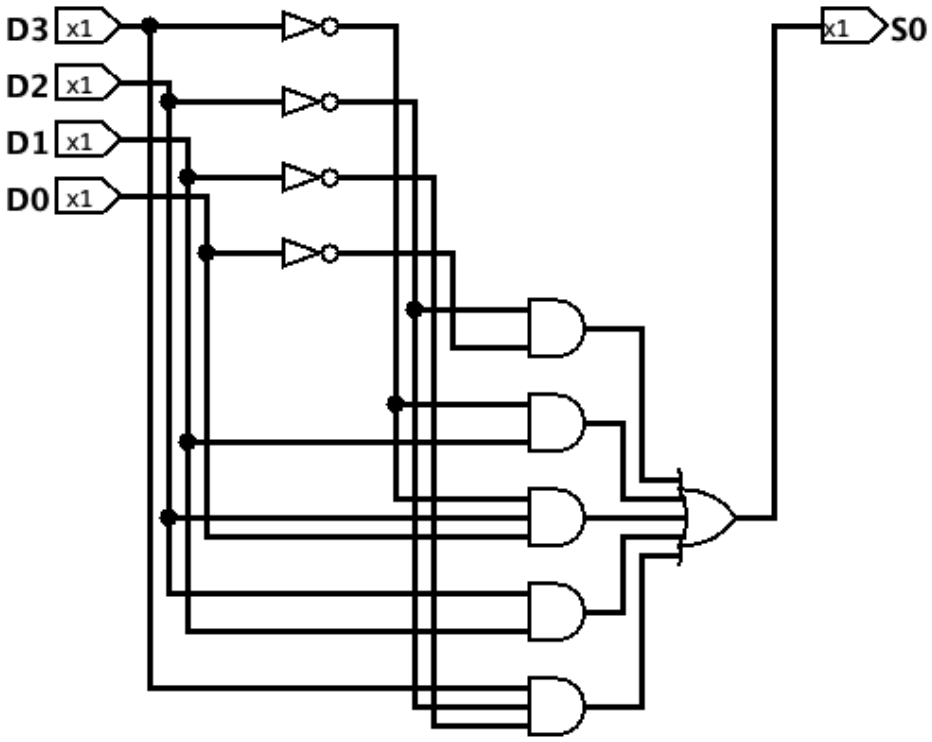

Figure 2: A schematic of HEX0

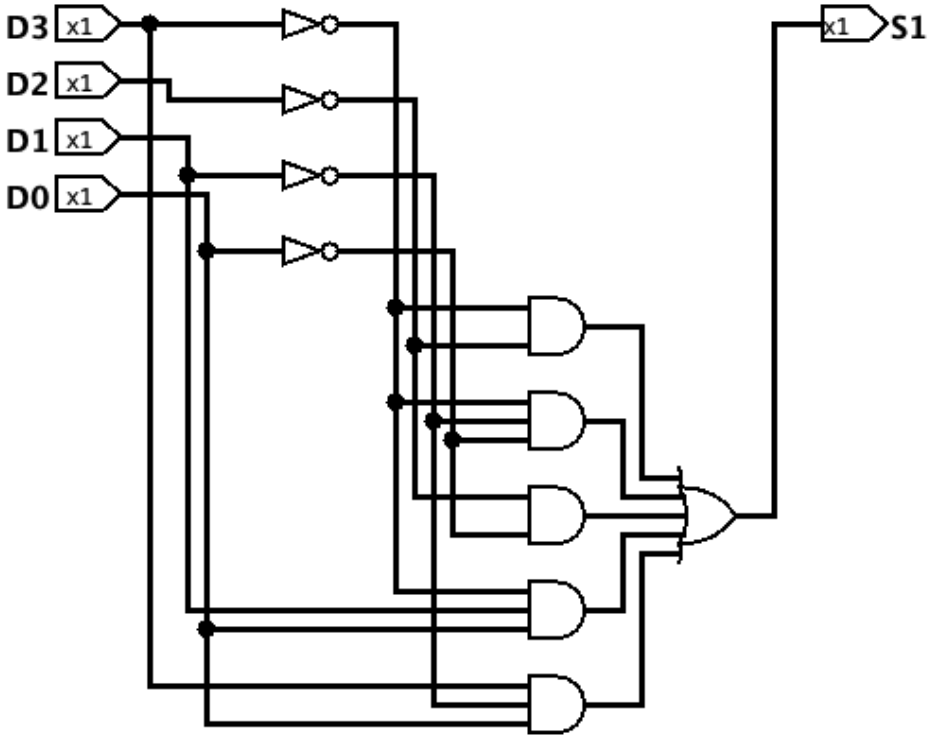

Figure 3: A schematic of HEX1

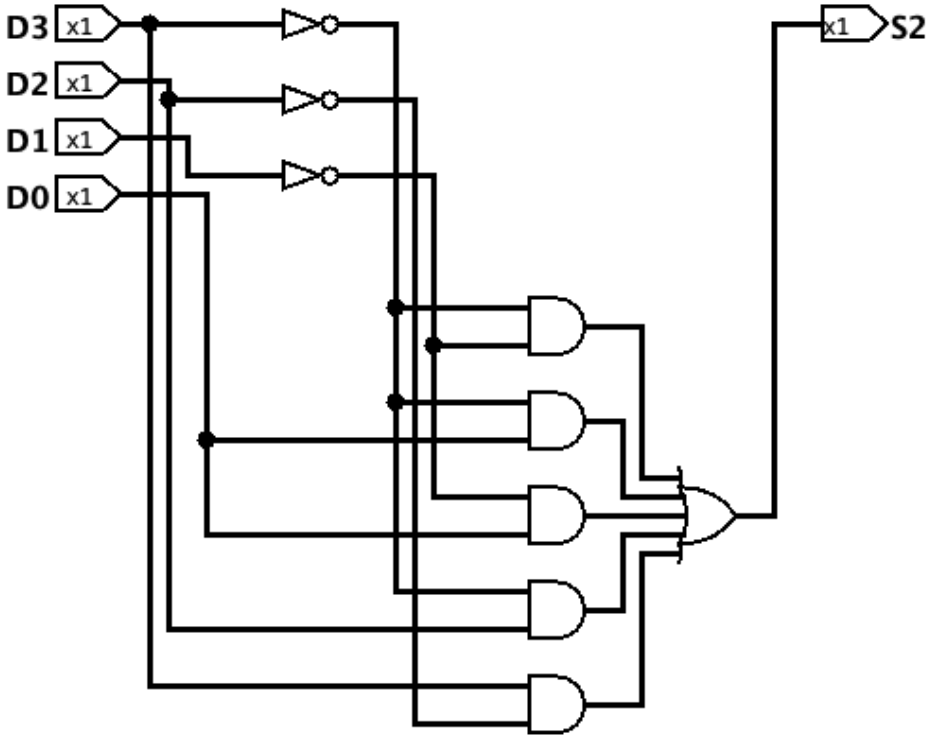

Figure 4: A schematic of HEX2

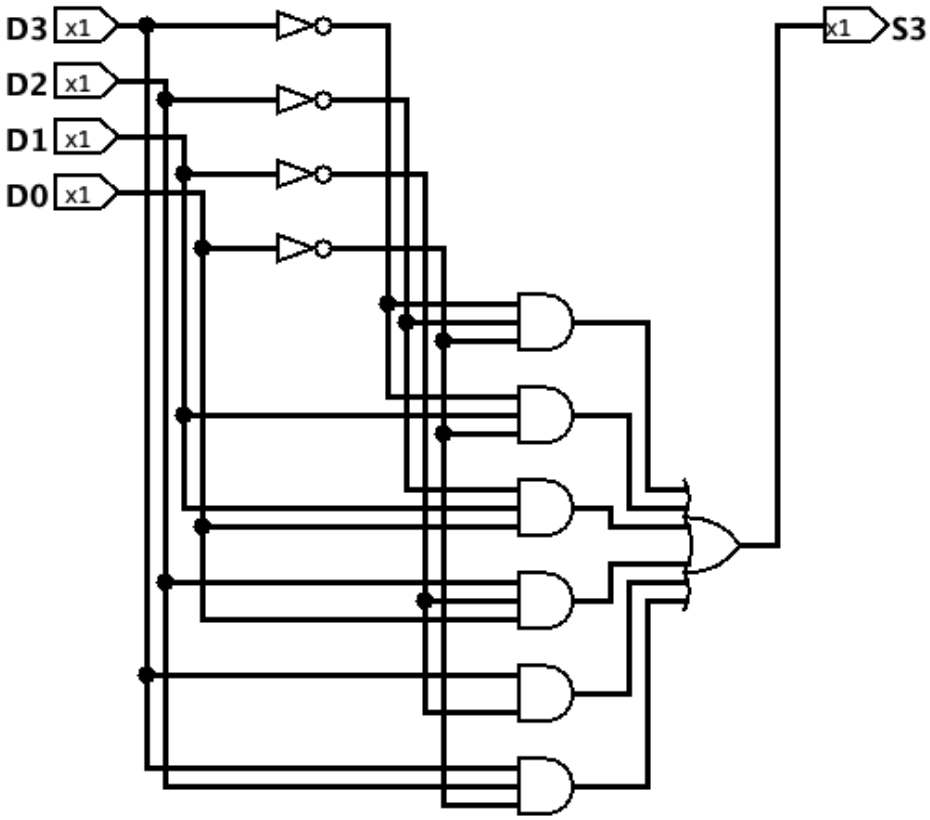

Figure 5: A schematic of HEX3

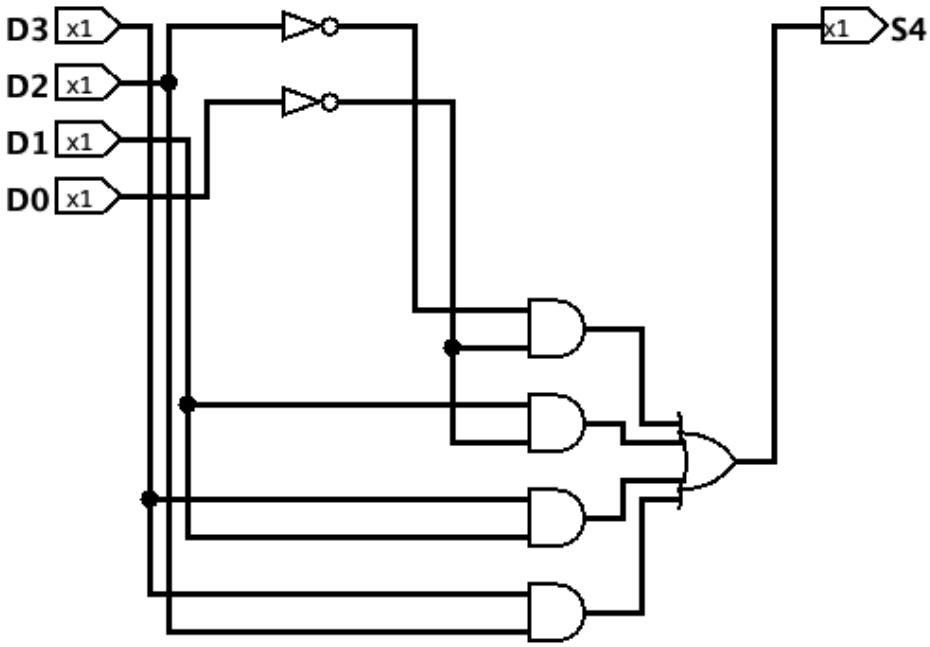

Figure 6: A schematic of HEX4

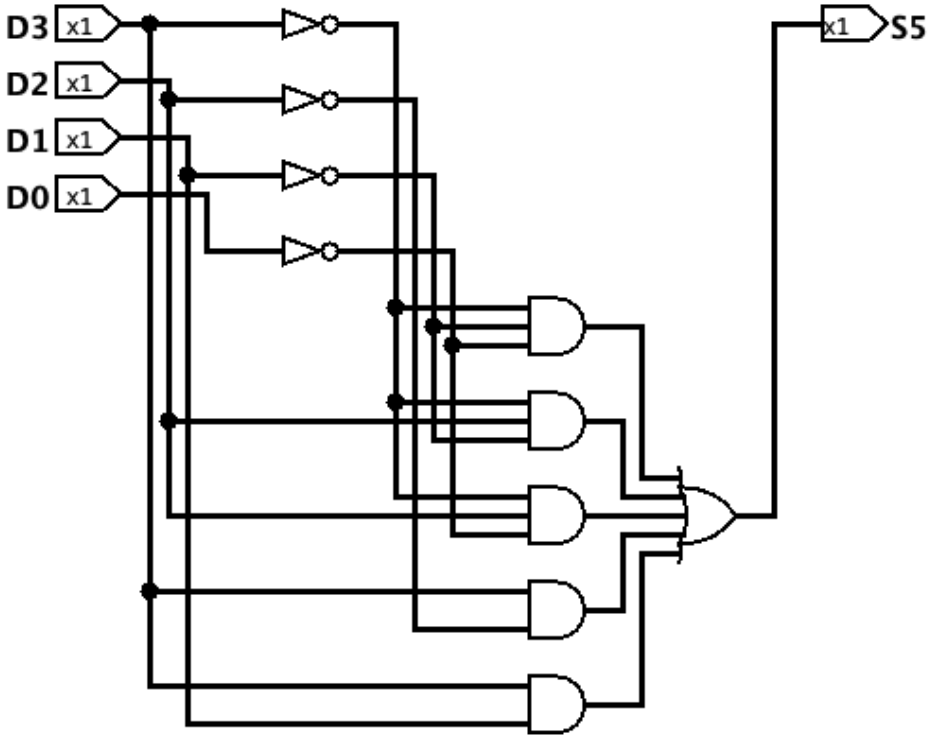

Figure 7: A schematic of HEX5

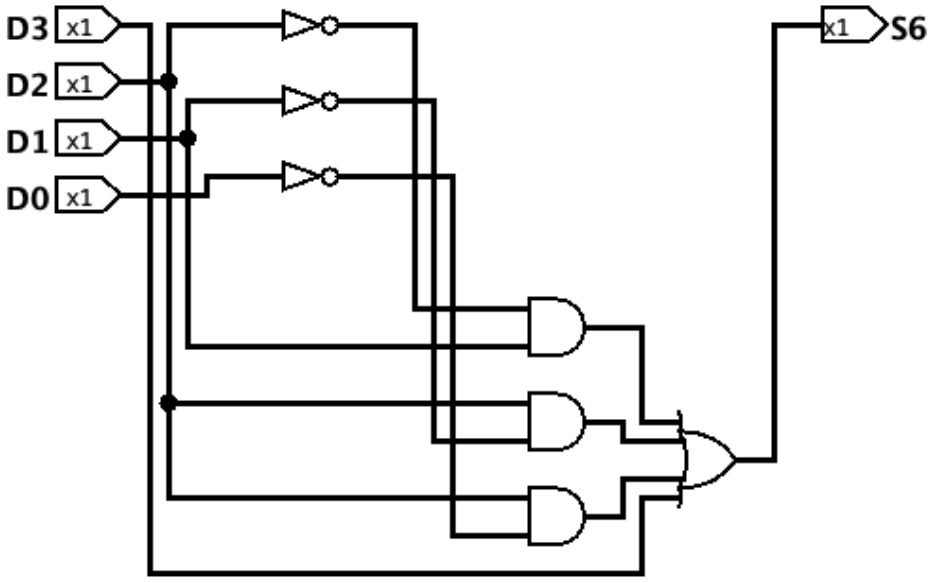

Figure 8: A schematic of HEX6