Lab 4: Synchronous Sequential Circuits

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Part I

2. Export the subcircuit schematic as an image and include it in your report.

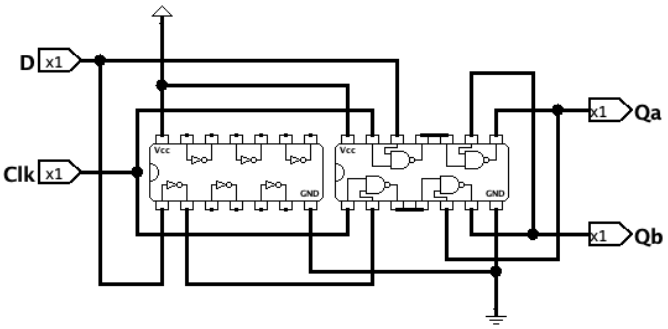

Figure 1: A schematic of the gated D-latch.

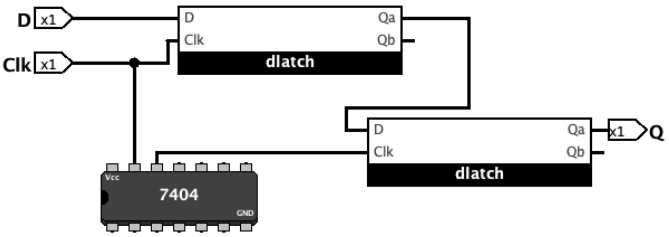

Figure 2: A schematic of the D flip-flop.

3. For the D latch and the flip flop, are there any input combinations of Clk and D that should NOT be the first you test with the *Poke* tool? List them if applicable.
   - D = 0, Clk = 0
   - D = 1, Clk = 1

Part IIa

2. Export the subcircuit schematic as an image and include it in your report.

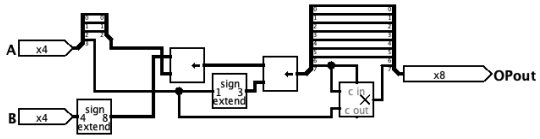

Figure 3: A schematic of op5.

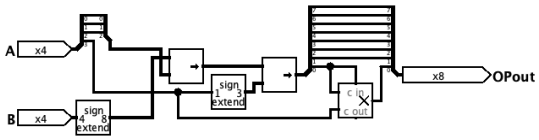

Figure 4: A schematic of op6.

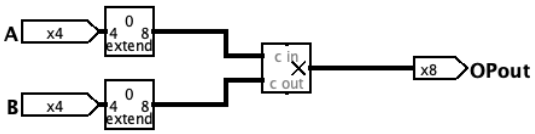

Figure 5: A schematic of op7.

3. Include a screenshot of your simulated test vectors for op5, op6, and op7.

Test Vector op5 of lab4_part2

Passed: 9 Failed: 0

Status	A	B	OPout
pass	0000	0000	0000 0000
pass	0001	0000	0000 0000
pass	0010	0000	0000 0000
pass	0111	0000	0000 0000
pass	0001	1111	1111 1110
pass	0100	1111	1111 0000
pass	0111	1111	1000 0000
pass	1000	1111	0000 0000
pass	1111	1111	0000 0000

Figure 6: A simulation of op5.

Part IIb

3. Include a screenshot of your simulated timing diagram demonstrating ALUreg starting at 0x0 and increasing by 1 until 0x0f.
4. Include a screenshot of your simulated timing diagram demonstrating a shifting operation where ALUreg goes from at 0x01 and doubling until 0x00.

Test Vector op6 of lab4_part2

Passed: 9 Failed: 0

Status	A	B	OPout
pass	0000	0000	0000 0000
pass	0001	0000	0000 0000
pass	0010	0000	0000 0000
pass	0111	0000	0000 0000
pass	0001	1111	0111 1111
pass	0100	1111	0000 1111
pass	0111	1111	0000 0001
pass	1000	1111	0000 0000
pass	1111	1111	0000 0000

Figure 7: A simulation of op6.

Test Vector op7 of lab4_part2

Passed: 14 Failed: 0

Status	A	B	OPout
pass	0000	0000	0000 0000
pass	0001	0000	0000 0000
pass	0010	0000	0000 0000
pass	0100	0000	0000 0000
pass	1111	0000	0000 0000
pass	0001	0001	0000 0001
pass	0010	0001	0000 0010
pass	0100	0001	0000 0100
pass	1111	0001	0000 1111
pass	1111	0010	0001 1110
pass	1111	0100	0011 1100
pass	1111	1000	0111 1000
pass	1111	0101	0100 1011
pass	1111	1111	1110 0001

Figure 8: A simulation of op7.

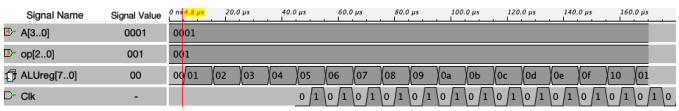

Figure 9: A timing simulation demonstrating incrementing.

Part III

2. What is the behaviour of the 8-bit shift register when *Load_n = 1* and *ShiftRight = 0*? Briefly explain in your prelab.

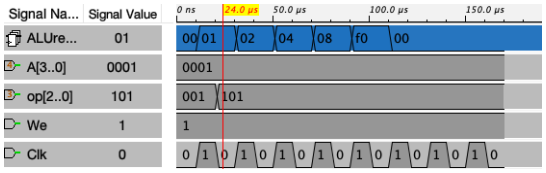

Figure 10: A timing simulation demonstrating doubling.

Since *Load_n = 1*, the bits from the previous clock cycle is parallel loaded into the register. However, since *ShiftRight = 0*, the flip flop in each bit is not changing it's value for the bit on it's right to load.

Export the subcircuit schematic as an image and include it in your report.

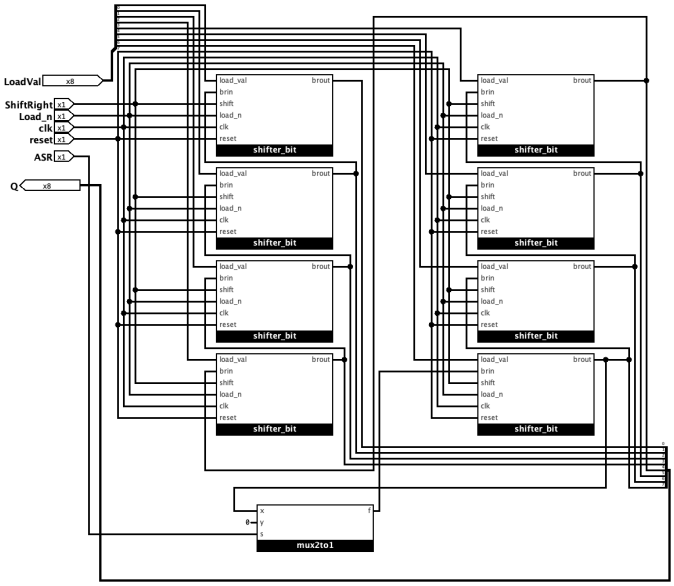

Figure 11: A schematic of the 8-bit shift register.

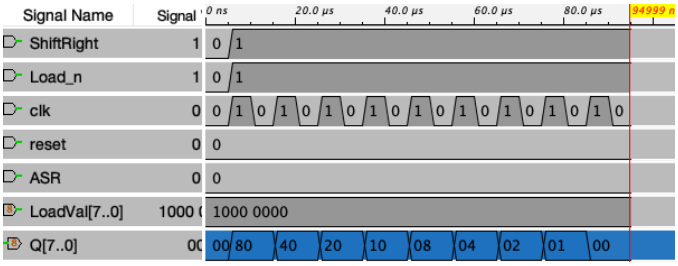

Figure 12: 8-bit shift register's shift right one bit.

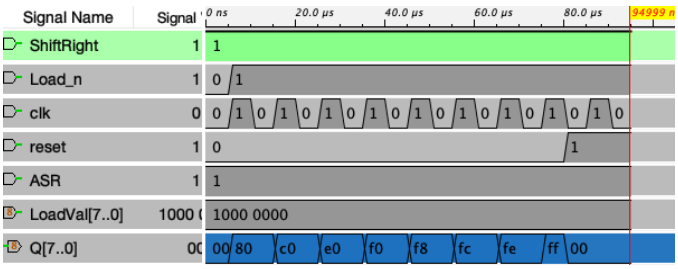

Figure 13: 8-bit shift register's shift right asr one bit with reset.

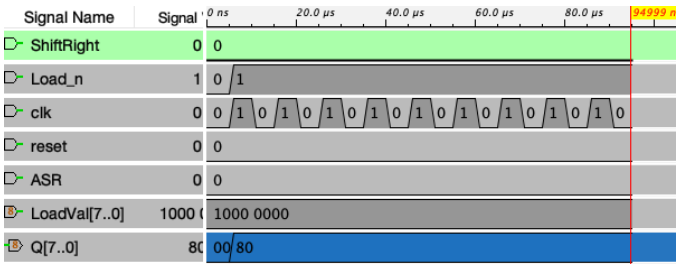

Figure 14: 8-bit shift register's no shift load n one bit.