Lab 7: Memory and Video

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1 Part I

1. What happens if both signals are off when the clock goes high? What happens when both signals are on? Experiment with these signals to confirm your guess and write the behaviour in your prelab report. When both write and output enable signals are off, then RAM moves to the next memory address without writing to it or reading the value at the memory address when the clock is high. When write enable is on and output enable is off, then the value of A is written to the current memory address, then RAM moves to the next memory address. When output enable is on and write enable is off, then a value is read from the current memory address, then RAM moves to the next memory address. When both are on, the value at A is written to and read from the current memory address and RAM moves to the next memory address.

2. Draw a schematic describing this circuit as part of your preparation.
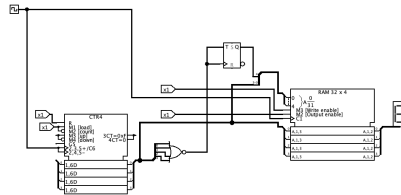

Figure 1: Schematic of Part 1.

3. Test your modules with *Poke* and the Logisim clock to verify its correctness. Include a few screenshots that shows the contents of the memory unit during your simulation.
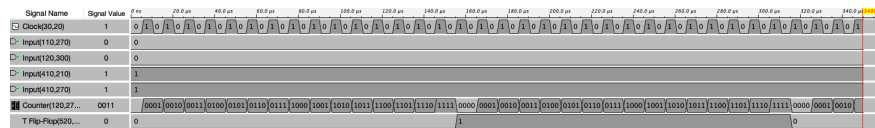

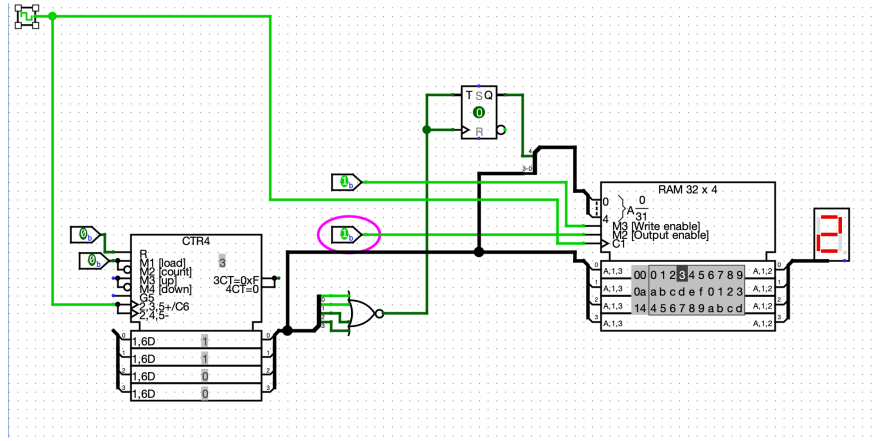Figure 2: A simulation of the Memory.

Figure 3: A simulation of the Memory part 2.

2 Part II

- What happens if you don't turn Enable off before updating X and Y? The square will break and resume drawing at the new X, Y coordinate with some offset determined by the counters in the datapath.

- What happens if you turn Enable off before 256 clock cycles have passed? The square will be completed and no new changes will be made. The counters will still cycle through each (X, Y) coordinate in the 16x16 square.

- What happens if you turn Reset on while Enable is on? While enable and reset are on, the first pixel at the (X, Y) coordinate will keep attempting to change colour when the clock is high and the counters will not cycle through the indices.
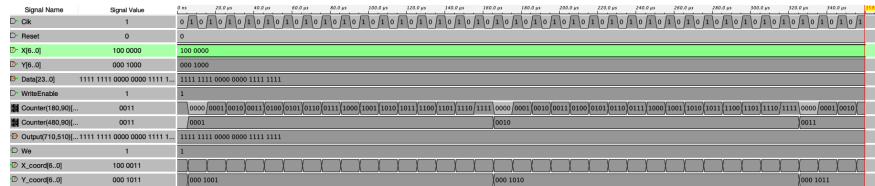

Figure 4: A simulation of datapath.

Figure 5: A simulation of controlunit.

Figure 6: A simulation of statetable.

3 Part III (Bonus)