Single-cycle processor

A microarchitecture

Introduction

Processor elements

Datapath and control

Conclusion

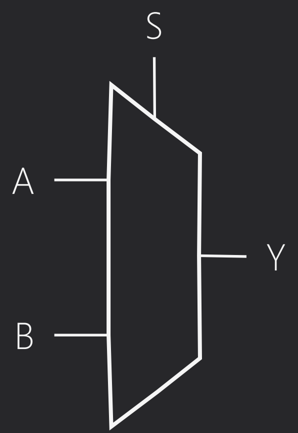
The elements of a processor

Some common combinational and state elements

Combinational elements

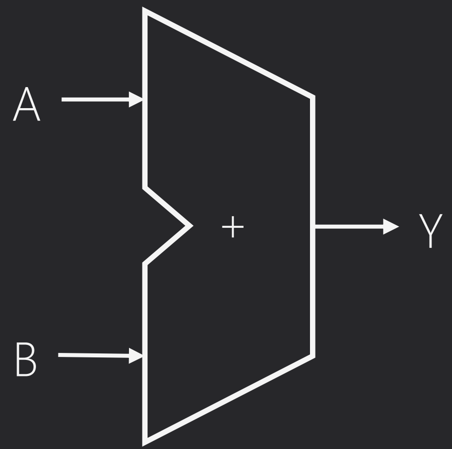
- Output of a combinational element depends only on the current input
- Operations take time (latency, propagation delay)

Multiplexer



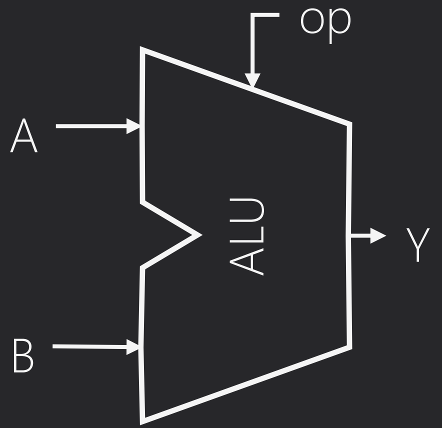
- The hardware analog to an if-statement
- If S == 0, then Y = A
- If S == 1, then Y = B

Adder



- Simply, Y = A + B

Arithmetic Logic Unit

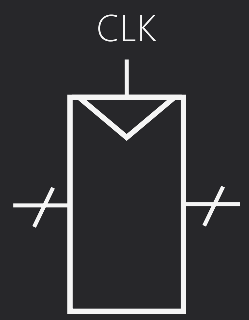


- Y = A (op) B
- Where op is, e.g.,
  - Add, Subtract
  - Multiply, Divide
  - Shift

State elements

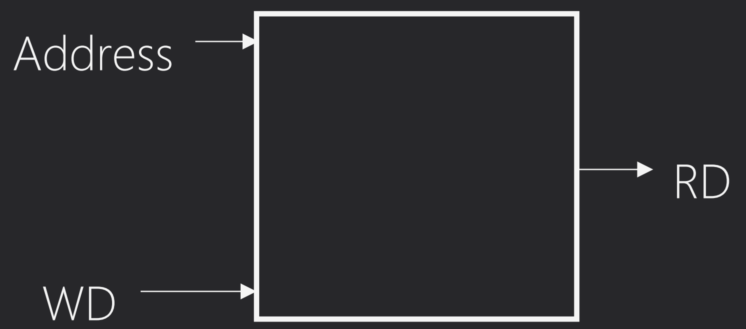
- Retains data
- Can be read from or (usually) written to
- Read/Write Enable: control whether to read and/or write

Register



- Very small (32-bit, 64-bit)
- e.g., the *program counter* (PC) is a register

Memory



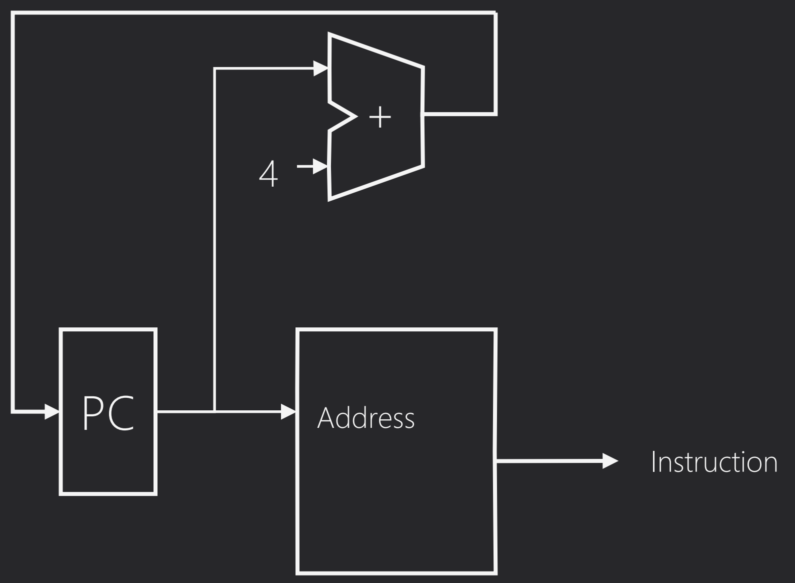
- Small (KB) to very large (GB)
- Address can be, e.g., a register or memory location
- e.g., the register file, instruction cache, and data cache are memories

Building a processor

Connecting elements together to build a single-cycle processor

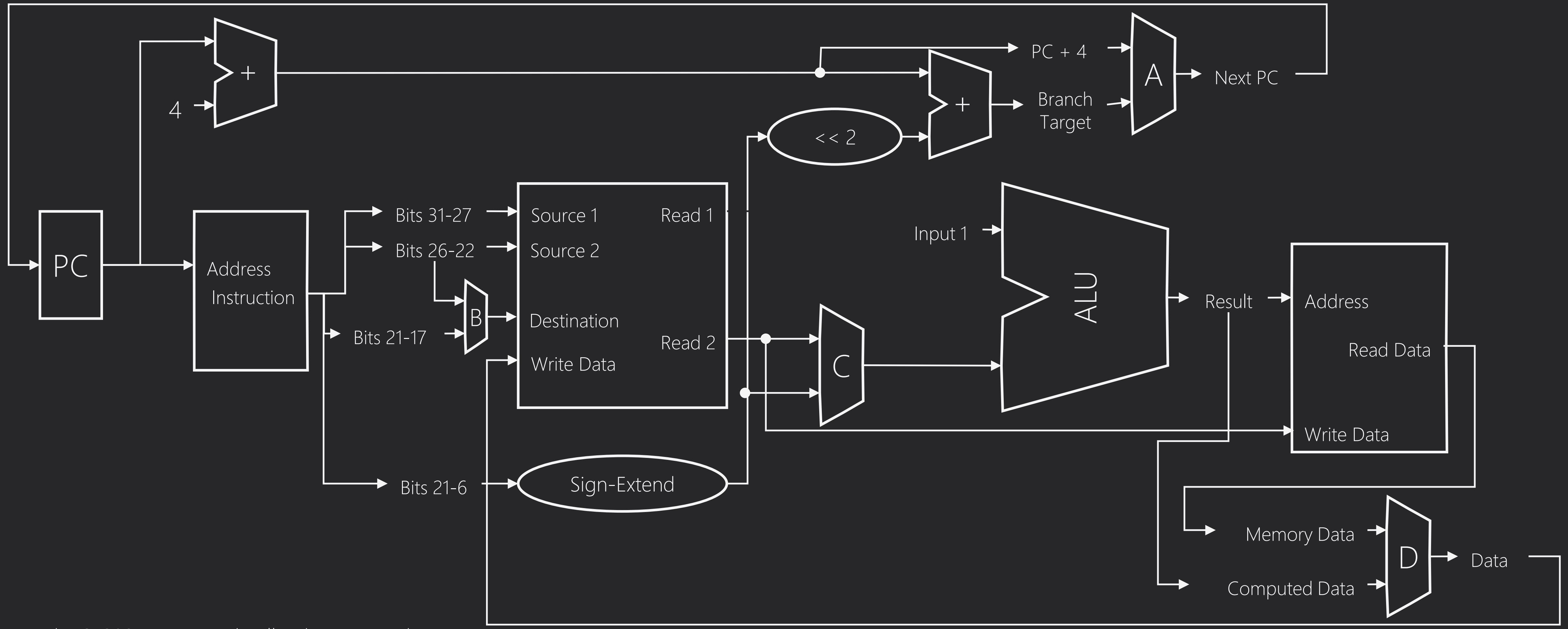
Sequential execution

- The program counter (PC) contains the address of the next instruction
- Read the data at PC from instruction memory
- Next: the instruction data must be decoded



The datapath

- Operates on data of some size (e.g., 32-bit, 64-bit)
- Contains both combinational and state elements
- Multiplexers and ALU are missing inputs!



The control unit

- Tells the datapath *how* to execute the current instruction
  - e.g., connects to the "S" input of the datapath's multiplexers
  - e.g., connects to the "op" input of the datapath's ALU

- A: What is the next instruction address?
- B: Does this instruction update the register file?
- C: Does the ALU's second operand come from the register file or an immediate value?
- D: Does the data written to the register file come from the ALU or was it loaded from data memory?

The “single cycle”

- Each instruction takes one cycle

- How long is the cycle?
  - Need to consider the worst-case
  - The longest path through the datapath is for a load instruction

Conclusion

Recapping the important points

Improving single-cycle performance

- There is no parallelism in a single-cycle microarchitecture
    - No spatial parallelism
    - No temporal parallelism (pipelining)
- Processors can be pipelined; how many stages?
    - Some modern, low-power processors use 2- or 3-stage pipelines
    - The Pentium 4 (circa 2006) used a 31-stage pipeline
- What about spatial parallelism?
    - Stay tuned for “superscalar” processors
    - P.S. superscalar processors are pipelined, combining temporal and spatial parallelism