# WEEKLY REPORT 1 : CLASS B OUTPUT STAGE ( AMPLIFIER)

1. **Circuits using both BJT and MOS ( 180nm ) technology**
    a) **BJT**
    b) **MOS**

2. **Expected Voltage Characteristics and Simulation using LTSpice**
    a) **Vout vs Vin for BJT**
    b) **Vout vs Vin for MOS**
    c) **Waveform for Sinusoidal Input for BJT**
    d) **Waveform for Sinusoidal Input for MOS****

3. **Effect of parameters such as Load Resistance , Frequency , Input Voltage on Waveforms and study of Harmonic Distortion**
    a) **Load Resistance on BJT ****
    b) **Load Resistance on CMOS ****
    c) **Frequency ( discussed in more detail in 4)**
    d) **Harmonic Distortion due to increase in input voltage ( discussed in more detail in 6)**

4. **Reducing Crossover Distortion and studying effects 3c and 3d**

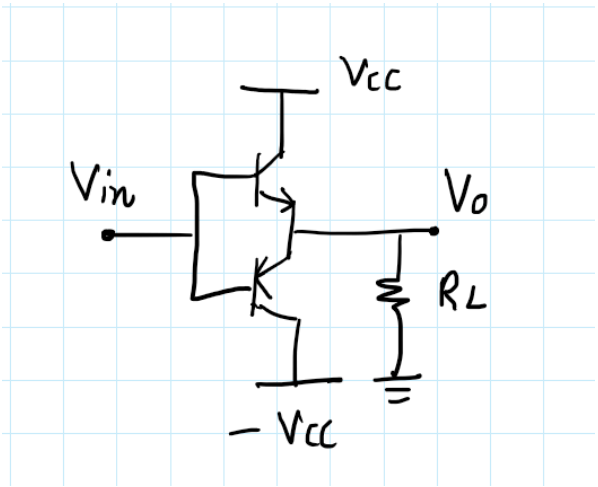
5. **Efficiency analysis ( After reducing crossover distortion )**

6. **Power Dissipation****

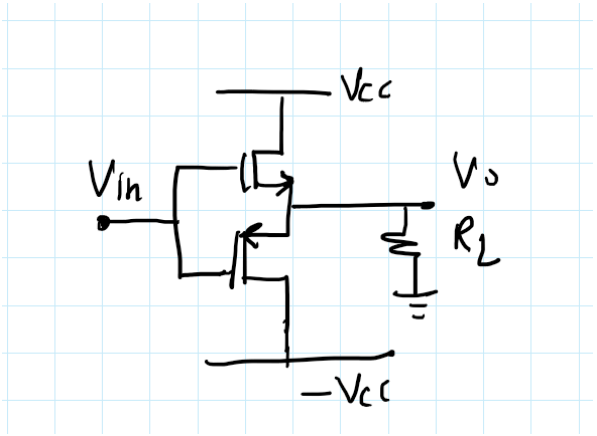
** Indicates interesting observations

## 1. Circuit Diagrams :

a) BJT :




b) MOS :




## 2. Expected Voltage Characteristics :

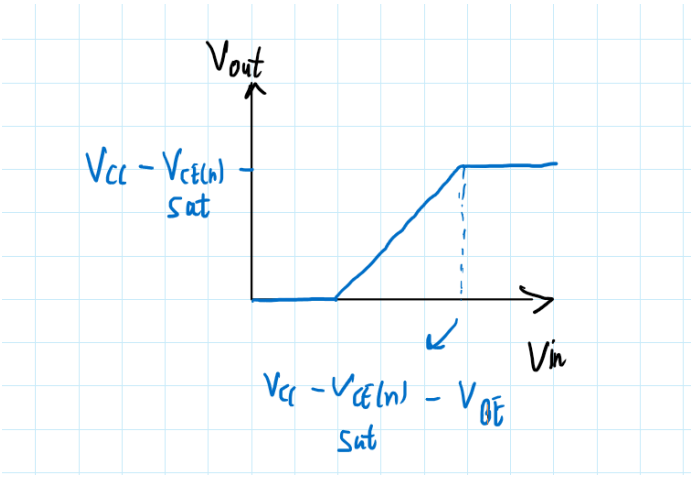
a) Voltage Characteristics for BJT :

When Vin > 0 , the PNP transistor will be OFF and the NPN transistor will conduct in the Forward Active Region  when Vbe (Vin as Vout = 0V) is approximately 0.7-0.8V .

We can write  Vo = Vin - Vbe(n) ( n for NPN)
Where we can assume Vbe(n) is fairly constant across the operation as Vbe(n) = Vt ln(Ic/Is) , i.e. Vbe(n) has a weak dependence on Ic , it changes by 60mV when Ic changes by about 10.

Also since the input is applied at the base and output taken at the collector we observe that it is Emitter follower topology .The increase in Vout is limited by the VCE(n), sat ( Value of VCE for which the transistor enters saturation ) . Thus the maximum value of Vout we can get is Vcc - VCE(n),sat.

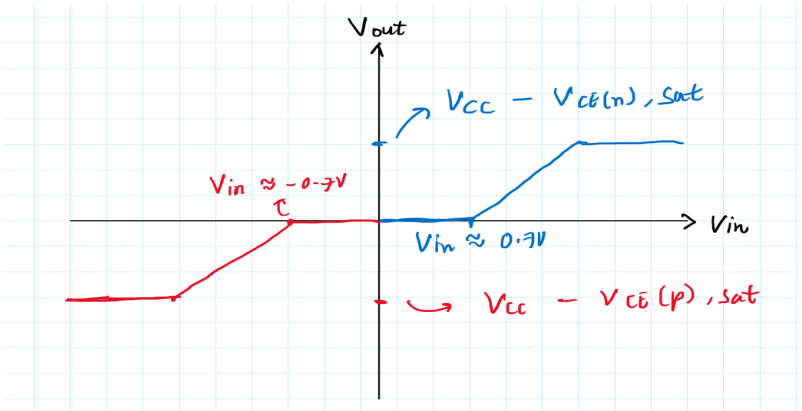
Expected Voltage Characteristic for Vin > 0 is as shown :



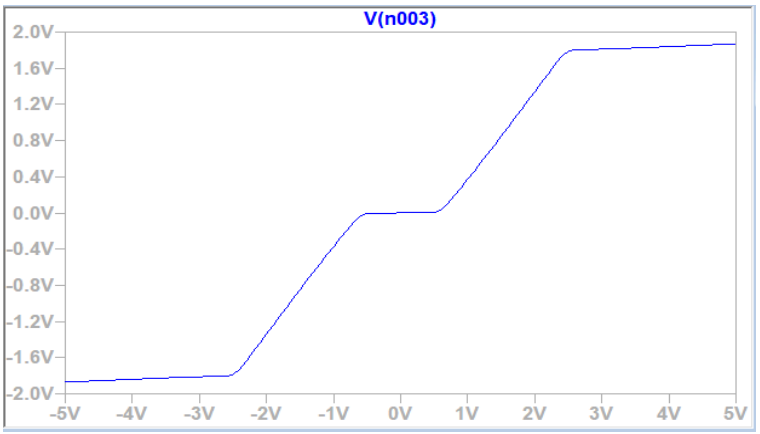

Since the PNP is OFF . We can say Ic(n) = I(L) ( Load current )

Similarly for Vin < 0 , we have the  NPN transistor that is OFF and PNP gets on when Vin < (-0.7V) ( Approximately). As above we can write

Vout = Vin - Vbe(p) and I(L) = - Ic(p) . We just have to produce the graph backwards to get the complete picture as shown below :

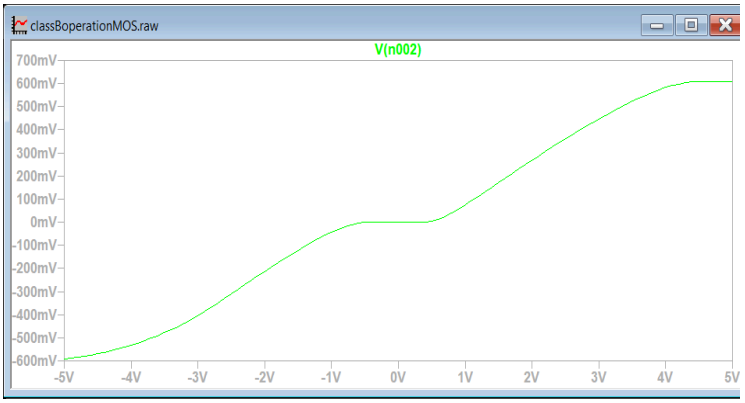



On LTSpice we get the following Characteristic :

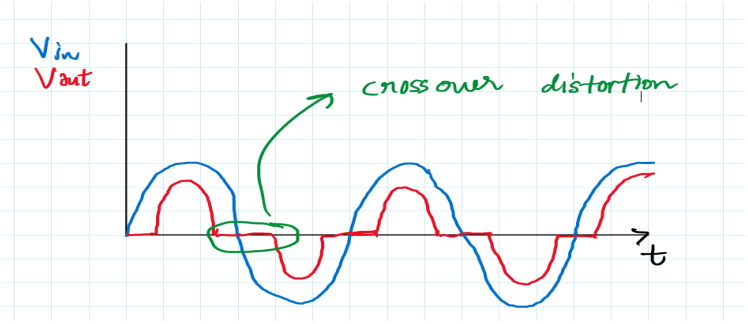



b) Voltage Characteristics for MOS

For MOS there will be source follower action as well but only when Vin > Vth(n) ( 0.4V ) or Vin < Vth(p) ( -0.4V) ( One of the transistors goes into saturation and the other is off). But as Vin continues to increase the device may go into triode , then cutoff . So we expect a similar characteristic as BJT but slightly less flat region about the origin as Vth < Vbe .

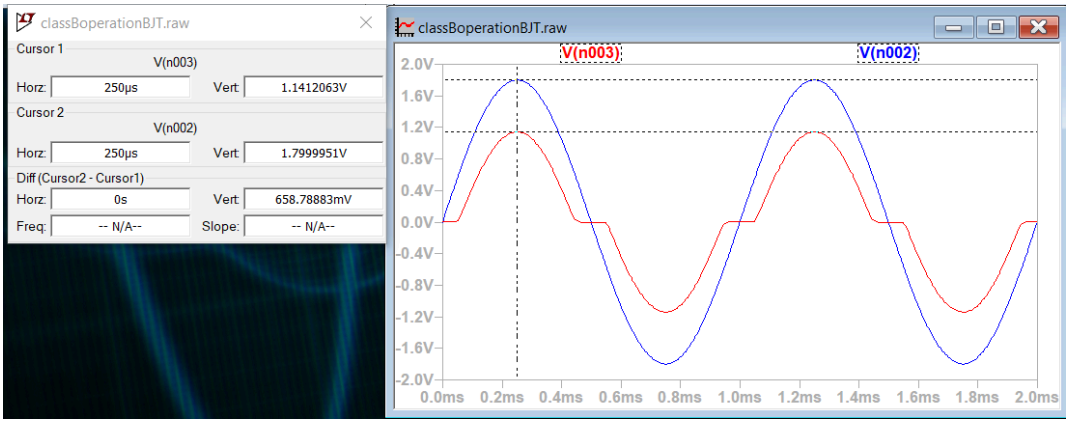


c) Sinusoidal Input response for BJT Class B :




Expected response by studying Voltage Characteristics

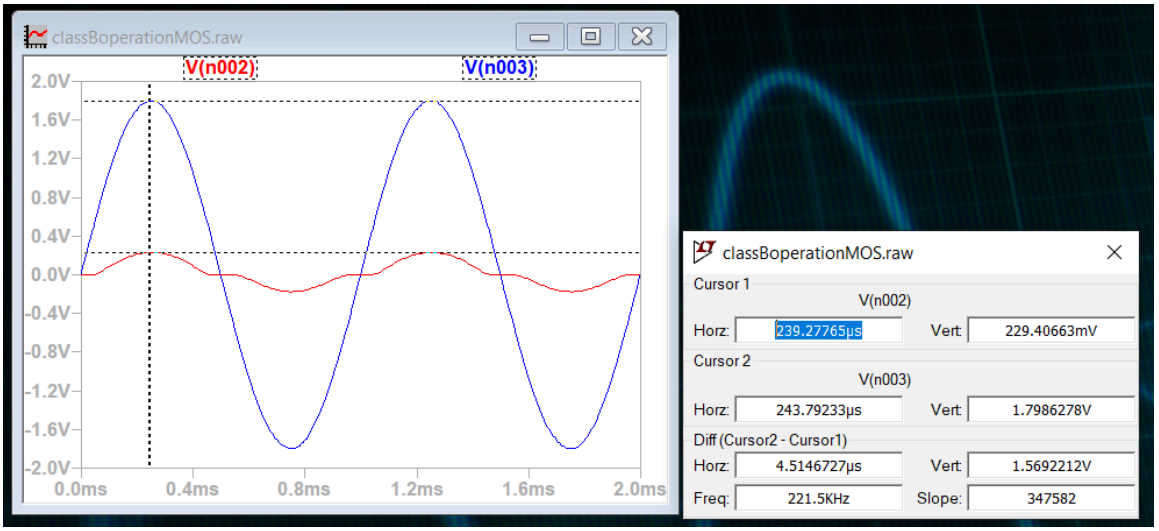
Simulation on LTspice :




Inline with the expected output, we can also observe that the difference between the peaks is almost equal to Vbe(n) (658mV).

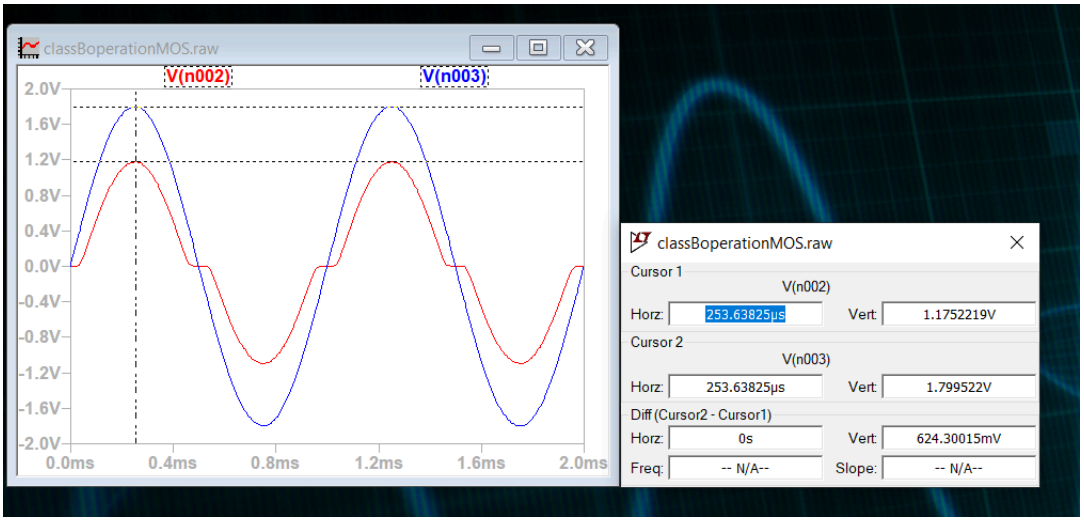
d) Sinusoidal Input Response to CMOS Class B :

We expect a similar response here as well



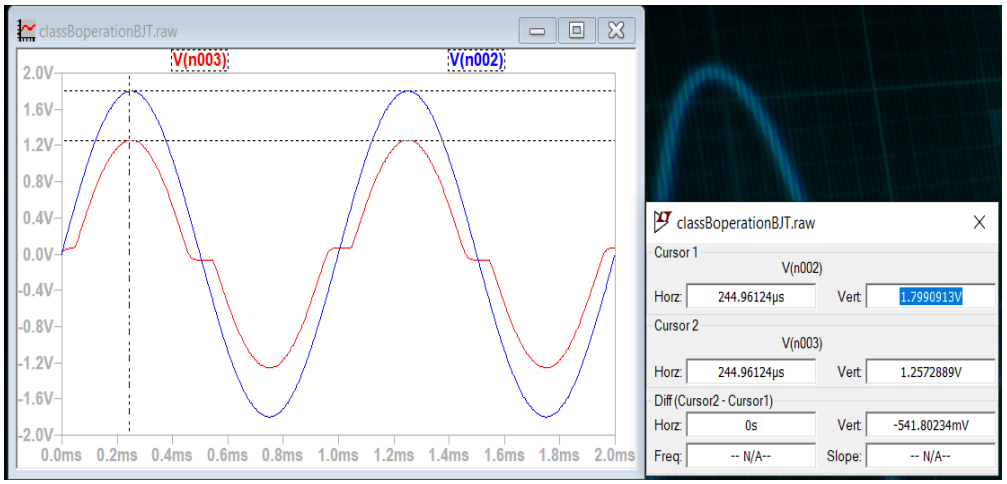
But we run into something interesting i.e. the gap between the peaks is much more than that of BJT Class B (1.56V)

This means we are experiencing poor Source following . This can be improved by increasing Rload  from 1000 to a much larger value , say 100k. Response is shown below .(Peak gap = 624 mV)




So we managed to increase the performance of the source follower , but one question arises . Why is it that varying  Rload in BJT has little to no effect on the gap between peaks but in MOS it is a significant effect ?

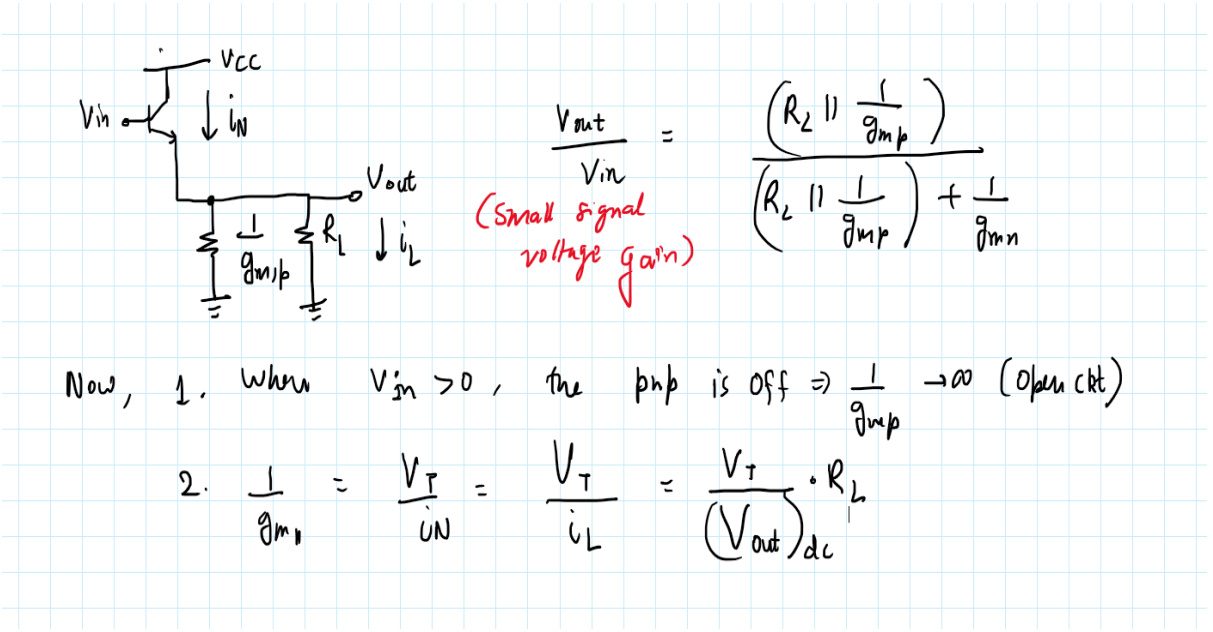
For example BJT Response at R = 100k

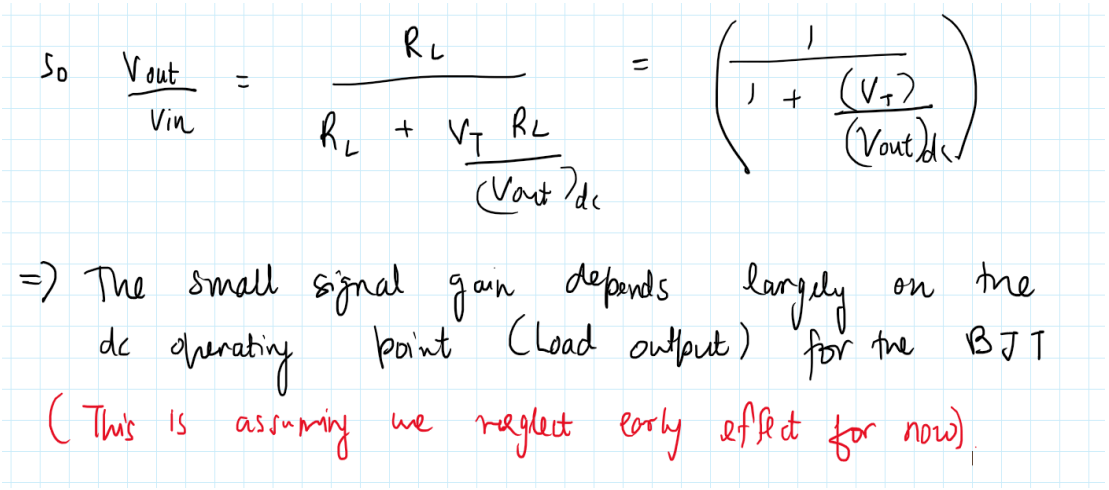


## 3. Effect of parameters such as Load Resistance , Frequency , Input Voltage on Waveforms and study of Harmonic Distortion :

a) Load Resistance : ( We follow up from the last point made about gap between the peak voltages )

Small Signal Analysis for BJT :



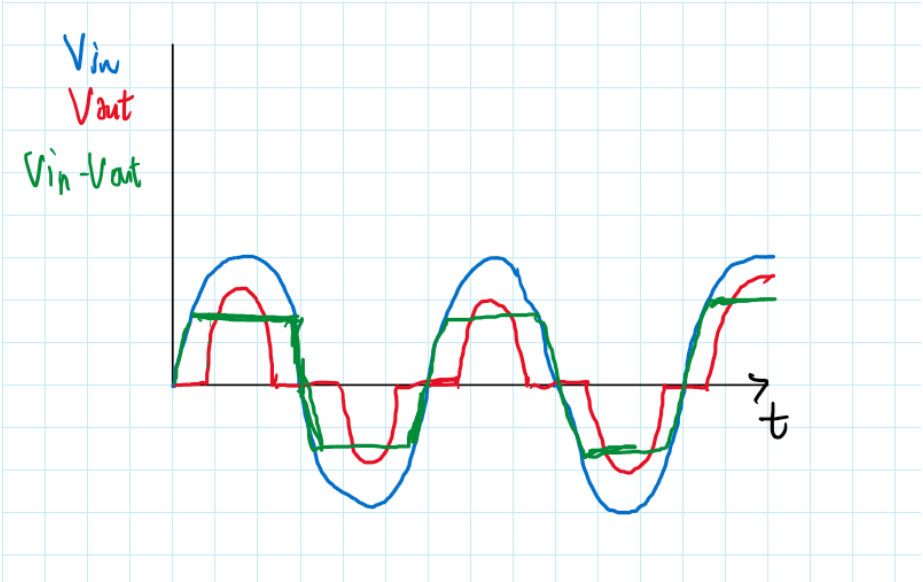



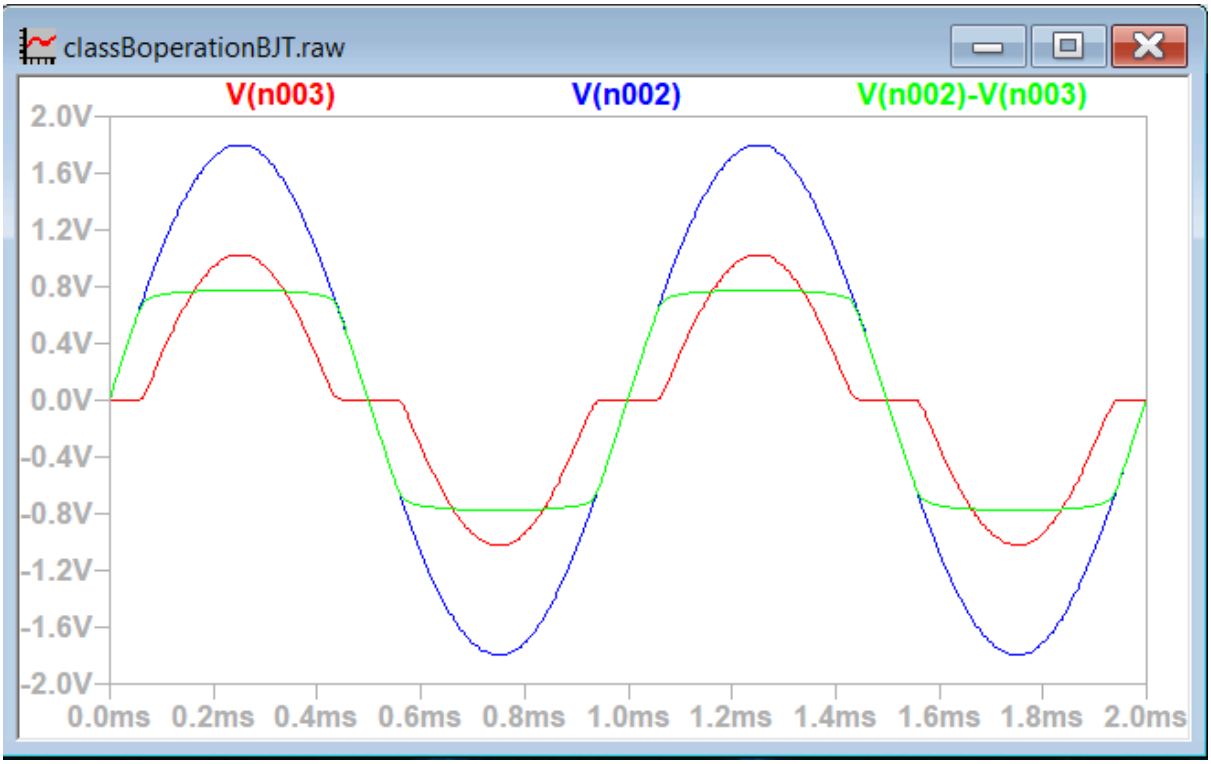

We observe that if we neglect early effect ( output resistance of the BJT to be infinite ) The Small Signal gain depends only on the output load voltage as VT = 26mV .

So when (Vout)dc >> 26mV say 100mV or more we can expect small signal gain to be approximately equal to 1 . Thus by the equations

Vout(dc) = Vin - Vbe(n) _____(1)
del(Vout) = del( Vin) _____(2) ( Small signal gain for Voutdc> 100mV)

From (1) and (2) .. Vin - Vout is expected to be relatively flat for a large region . Let us see whether the simulation result matches with our expectation )




b) Load Resistance effect on CMOS Class B :

Since the voltage gain expression is same for both emitter and source follower,

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{R_L}{R_L + \frac{1}{g_{mn}}} = \frac{R_L}{R_L + \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)\left((V_{in}-V_o)_{dc} - V_{th}\right)}}$$

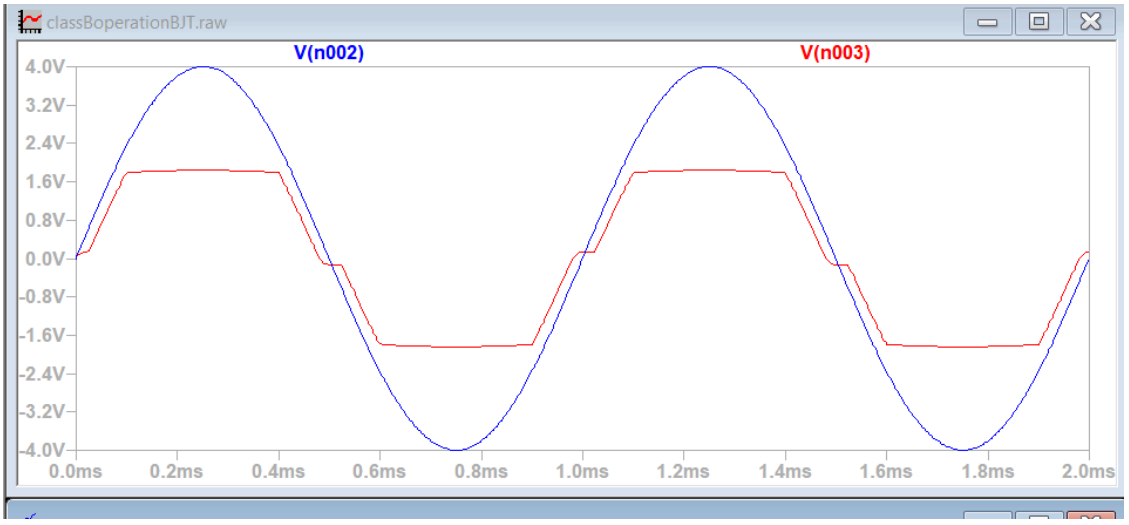
We observe that there is a strong dependence of RL for the small signal voltage gain . Thus only for large loads we can expect the output to try to follow the input .

c) Frequency

The CMOS class B is expected to produce much lesser distortion as compared to the BJT Class B output stage , this is because charge collection occurs in the base of BJTs , thus making switching a slow process . Will discuss this point further when I try to reduce crossover distortion )

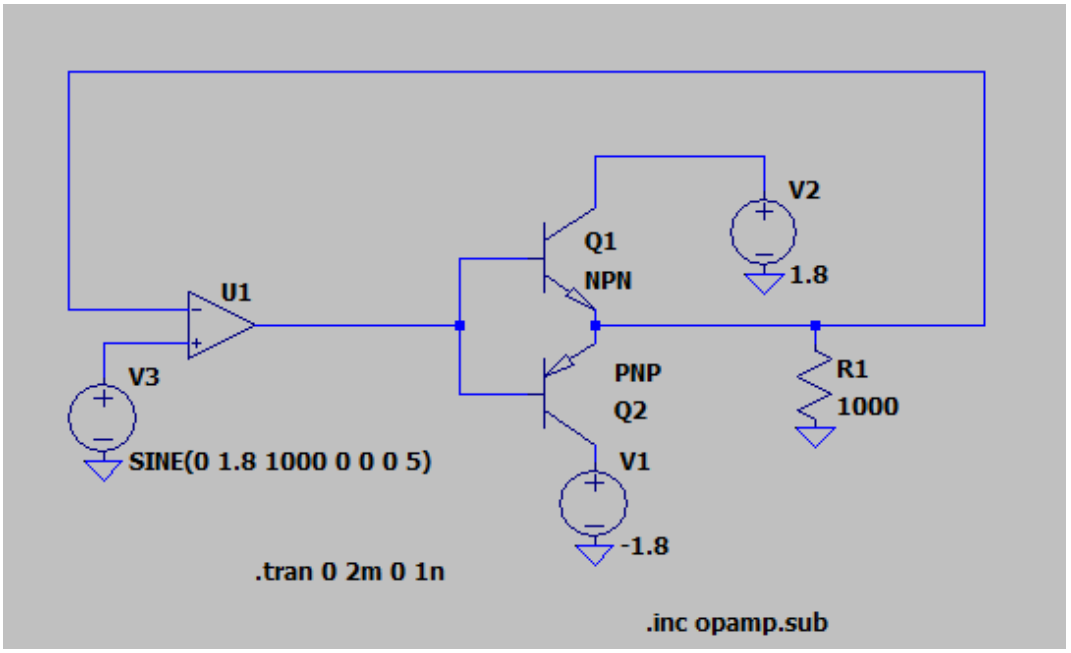
d) Harmonic Distortion due to Increase in Input Voltage

This is expected in both BJT and CMOS as increase in input voltage leads to a corresponding increase in output voltage this limiting the swing due to saturation in BJT and triode ( or cutoff ) in CMOS .

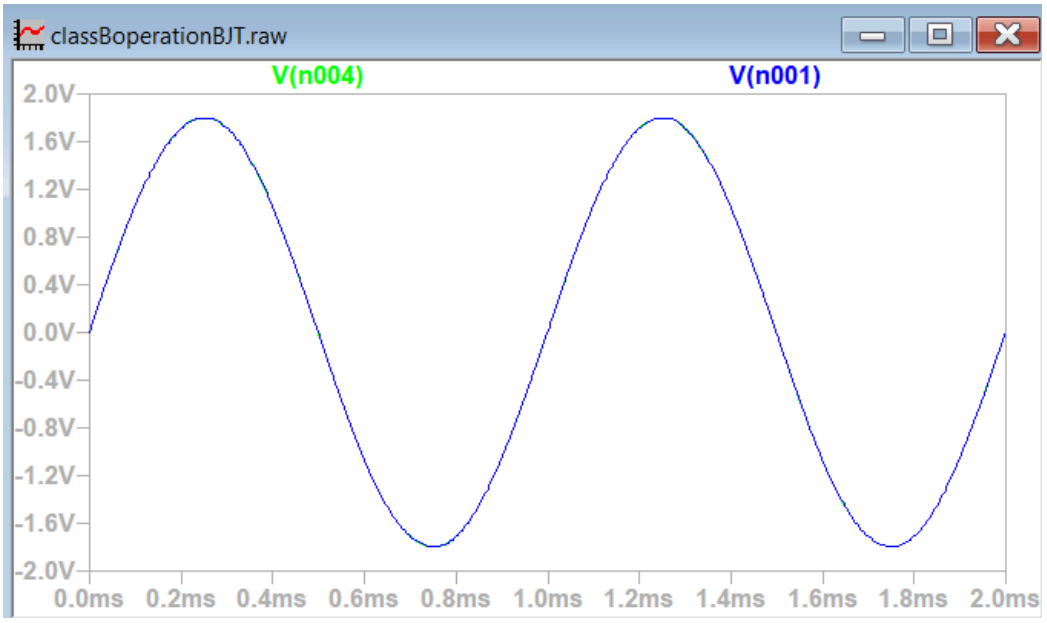



## 4. Reducing Crossover Distortion :

We can put a high gain op amp in feedback as shown below . This reduces the Crossover distortion to 0.7/A0 ( BJT ) and 0.4/A0 for (CMOS) where A0 is the dc gain of the opamp. It also improves linearity of the Voltage Transfer Characteristic

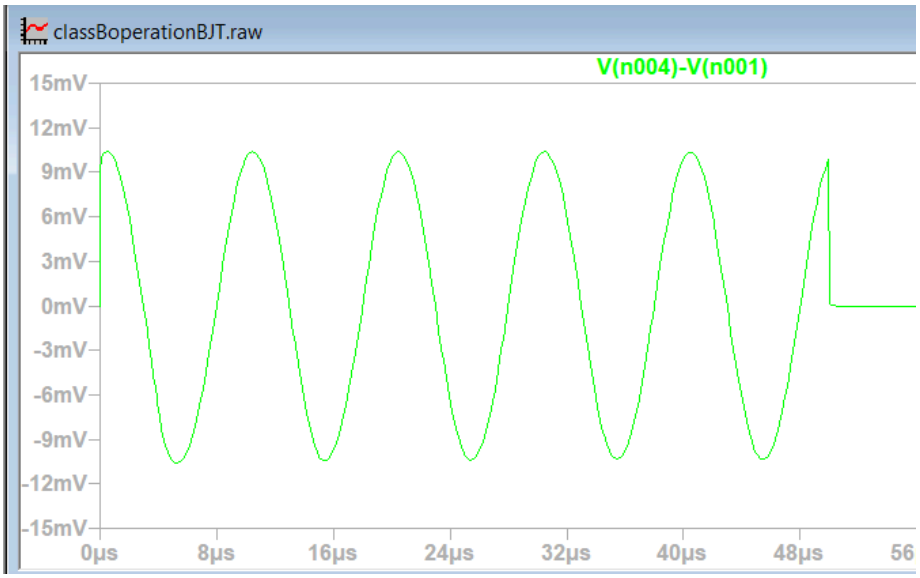



We have taken the DC gain to be 10k . The plot for sinusoidal response is as shown :

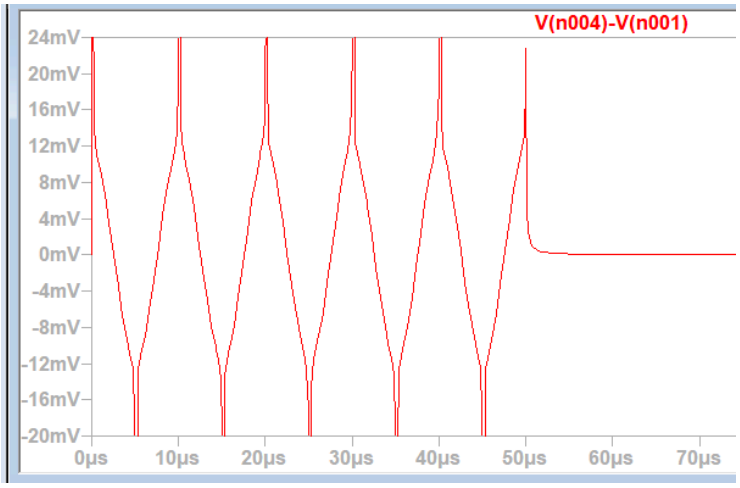



We obtain coincident plots ( crossover distortion is almost 0) . Output follows Input completely .

Now let us increase the frequency to 100k ( next page )




Blue ( output ) .. Notice the ripples at 0V . This is due to charge collection at the base . We try the same for CMOS and observe




This is a surprising point . It seems BJT Class B has lesser error when frequency is increased . This is a contradiction from what is generally taught in VLSI . CMOS being better at switching ( High frequencies).

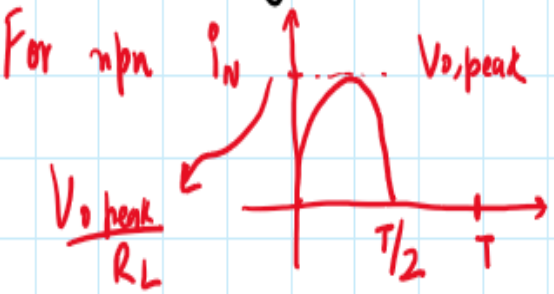
## 5. Efficiency Analysis :

$$\text{Power Conversion Efficiency } (\eta) = \frac{(P_{load})_{avg}}{(P_{supply})_{avg}}$$

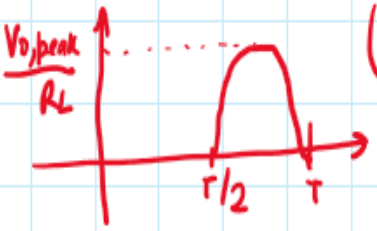
$$(P_{load})_{avg} = \frac{V_{o,peak}^2}{2R_L}$$

$$(P_{supply})_{avg} = 2V_{CC} I_{avg} = 2V_{CC}\left(\frac{V_{o,peak}}{\pi R_L}\right)$$

For npn $i_N$




$$(i_N)_{avg} = \frac{V_{o,peak}}{\pi R_L}$$




$$(i_P)_{avg} = \frac{V_{o,peak}}{\pi R_L}$$

$$\text{So } \eta = \frac{V_{o,peak}}{2R_L} \cdot \frac{\pi R_L}{2V_{CC} V_{o,peak}} = \frac{\pi}{4}\frac{V_{o,peak}}{V_{CC}}$$

Typical values of $V_{CE(sat)} = 0.2\,V$ so, $V_{o,peak} \approx V_C$

So we have $\eta \approx \frac{\pi}{4} \Rightarrow \boxed{78.5\%}$

## 6. Power Dissipation :

$$(P_D)_{avg} = (P_{supply})_{avg} - (P_{load})_{avg}$$

$$= \frac{2 V_{cc} V_{o,peak}}{\pi R_L} - \frac{V_{o,peak}^2}{2 R_L}$$

$$\frac{dP_D}{dV_{o,peak}} = \frac{2 V_{cc}}{\pi R_L} - \frac{V_{o,peak}}{R_L}$$

for $(P_D)_{avg}$ to be max, $\frac{(dP_D)}{dV_{o,peak}} = 0$

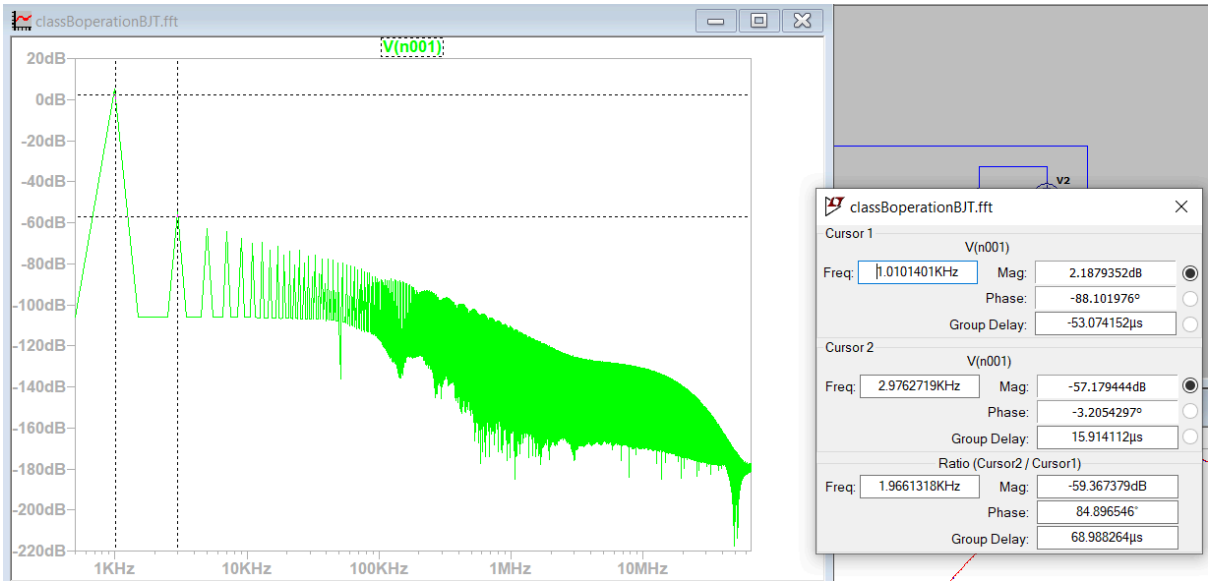
$$\Rightarrow V_{o,peak} = \frac{2 V_{cc}}{\pi}$$

for max power dissipation

$$\eta_{P_D,max} = \frac{\pi}{4} \cdot \frac{2 V_{cc}}{2 \pi V_{cc}} = 50\%$$

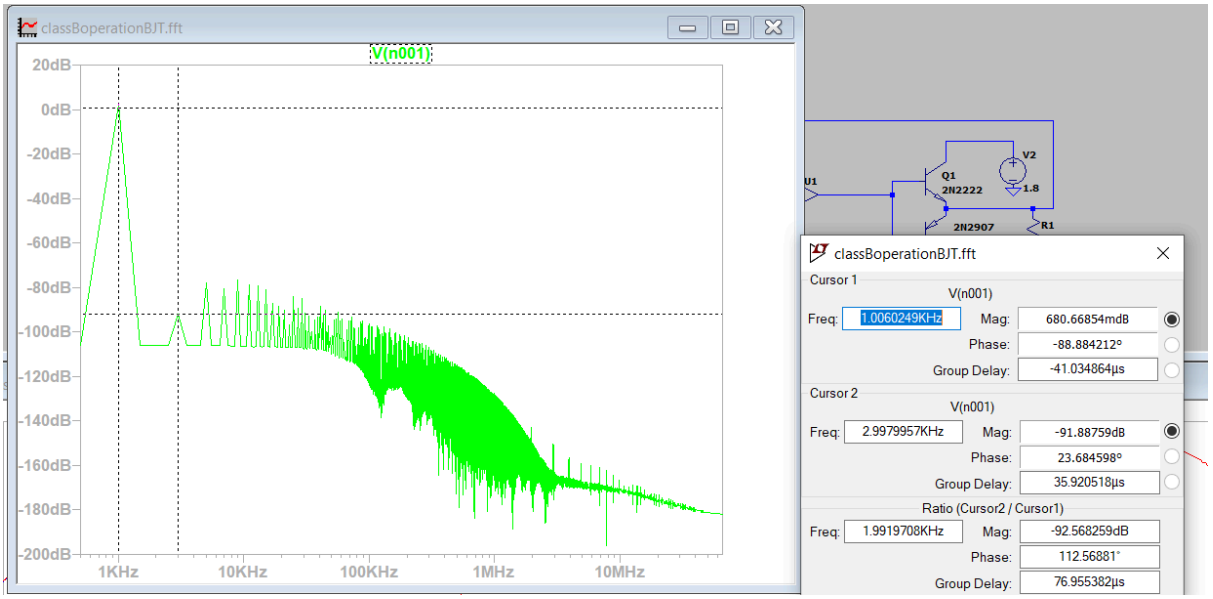
So at max power dissipation, $\eta = 50\%$

So to improve efficiency, we must have $V_{o,peak} > \frac{2 V_{cc}}{\pi}$ but the problem is increase in harmonic distortion




First we check the FFT for Vin = 2.5Vsin(wt) ( This should be the point for maximum power conversion efficiency) . The third harmonic is -57.179dB .

For Vin = 1.84Vsin(wt) , we have lower power conversion efficiency and lower power dissipation but much lower Harmonic Distortion ( see below)




The Third Harmonic has rms value -91.88dB . So we try to chase for maximum efficiency but pay price as far as THD is concerned