HAUSHALYA ANIL CHANDANSHIVE

CAREER OBJECTIVE:

An Enthusiastic VLSI Trainee with highly motivated and technical skills having masters of engineering degree in VLSI and Embedded system and seeking a responsible job with an opportunity for professional challenges.

CONTACT DETAILS:

Room 401, B-wing, Swarup Residency, New Kopare, Uttam Nagar Pune:411023

haushalya@gmail.com

9960257982

VLSI DOMAIN SKILLS:

- **HDL:** Verilog,VHDL
- **HVL:** System Verilog.
- **EDA Tools**: Modelsim, Questasim-mentor Graphics, ISE-Xilinx,LDRA,HDL designer.
- **Domain:** ASIC and FPGA Front End Design and Verification
- **Knowledge:** RTL coding, Simulation, Synthesis, FSM based Design
- **TB Methodology:** UVM

WORK EXPERIENCE:

◆ **GVR Technolabs pvt.ltd. [March24 to still]**

- Deputed at DRDO lab, Armament R&D Establishment, Pashan Pune
- Review Documents and prepare report.
- Prepare code as per document
- Prepare testcases for given code and Prepare report.
- Doing verification by software tool of questa-sim simulation

◆ **M/s Mahesh Dadaji Bachchav [sept 23 to March24]**
Designation: Verification And Validation Engineer

- Deputed at DRDO lab, Armament R&D Establishment, Pashan Pune
- Review Documents and prepare report.
- Prepare code as per document
- Prepare testcases for given code and Prepare report.
- Doing verification by software tool of questa-sim simulation

◆ **Visheshwer Enterprises [1 jan 22 to 31 aug 2023]**
Designation: Verification And Validation Engineer

- Deputed at DRDO lab, Armament R&D Establishment, Pashan Pune
- Review Documents and prepare report.
- Prepare code as per document
- Prepare testcases for given code and Prepare report.
- Doing verification by software tool of questa-sim simulation

◆ **Rubix Technologies Pune [16 sept.2020 to 31 Dec.2021]**
Designation: Jr. R&D Engineer

- Making Schematic in Altium Software
- Procurement of R&D component

PERSONAL DETAILS:

- **Gender**: Female
- **Birth Date**: 20th March 1992
- **Language**: English, Hindi, Marathi
- **Strength**: Hardworking, Quick learner, Positive Attitude, Self-Motivated
- **Hobbies**: Playing chess, Cooking, Traveling

Advanced VLSI and Verification Course **7 months**

- Maven Silicon VLSI Training Institute.
- Bangalore- 29-dec-21 to 28-jul-22

ACADEMIC EDUCATION:

Master of Engineering in VLSI and Embedded System :8.2

- Sinhgad College Of Engineering, Pune
- Savitribai Phule Pune University

Bachelor In Electronics and Telecommunication :65%

- Fabtech Technical Campus, Sangola
- Solapur University (Year 2013-1016)

Diploma In Electronics and telecommunication :73%

- Shivaji Polytechnique College, Sangola
- Maharashtra State Board of Technical Education(Year 2010 – 2013)

Senior Secondary Education :76%

- Anand Vidyalaya Kamalapur, Sangola
- SSC board(Year 2008)

ACADEMIC PROJECT:

- **"RFID BASED ATTENDANCE SYSTEM". Year-2016**
- **"Wireless communication by using Phase Locked Loop" Year-2023 .**

DECLARATION:

I hereby declare that all information mentioned above is true and correct to the best of my knowledge.

Place:

Date:

Haushalya Anil Chandanshive