AREA OF INTEREST

- Analog IC Design
- RFIC design
- VLSI Design
- Neuromorphic circuits

SCHOLASTIC ACHIEVEMENTS

- 2019: Secured AA grade in **Course Seminar**, IIT Bombay.
- 2019: Secured AB grade in **VLSI design Lab** and **Solid State Microwave Devices and Application** IIT Bombay.
- 2011: Secured **1811 rank** in the GATE Exam in Electronics and Communication in 2011.
- 2015: Achieved **100% result** while teaching in AISSMS IOIT

RELEVANT COURSES

- CMOS Analog VLSI Design
- VLSI Design
- SSM Devices and Applications
- RF Microelectronics Chip Design
- VLSI Design Lab
- Electronics System Design

KEY ACADEMIC PROJECTS AND ASSIGNMENT

- **Two stage single ended OTA design and Layout** Course: CMOS Analog VLSI Design [Sep'18-Nov'18]
  Guide- Prof. Rajesh Zele, Dept. of EE IIT Bombay
  - Designed OTA circuit using **CMOS 180nm** technology. VDD =1.8V
  - Designed a Layout of OTA using **CMOS 180nm** technology
  - It is compare for schematic and post layout simulation for DC gain, UGF, PM, input referred noise and power consumption.

- **Three Assignment on Digital Design** Course: VLSI Design [Aug'18-Nov'18]
  Guide- Prof. D. K. Sharma, Dept. of EE IIT Bombay
  - Design of Circuit and Layout for Minimum sized CMOS INV, gamma = 1 CMOS 180nm SCL technology.
  - Delay parameter evaluation with INV and 2 i/p NAND gate using as a load circuit in CMOS 180nm technology
  - Logic Implementation with Domino AND and OR in CMOS 180nm technology and Brent Kung adder in VHDL

- **Synchronous Visible Light Tx/Rx using PRBS Manchester Encoding and CDR Technique**
  Guide- Prof.P. C. Pandey, Dept. of EE IIT Bombay Course: VLSI Design [Oct'18-Nov'18]
  - Complete circuit is designed on PCB
  - PRBS Manchester Encoder is Designed

- **Three Assignments and 2 Projects** Course: RF Microelectronics chip design [Feb'19-Apr'19]
  Guide- Prof.Rajesh Zele, Dept. of EE IIT Bombay
  - **Assignment: UMC 65 nm Technology VDD =1.2V**
    - **Design of a LNA** taking only matching and gain into consideration for different source impedance
    - Design of L,T and π matching for different frequencies and 0.2 nH Inductor in ASITIC for minimum area
    - **Design of a wide-band LNA** for 0.5GHz - 2.5GHz frequency band, Av =10 dB , NF (≤ 2.8 dB) IIP3 (+4 dBm) P1dB (-9.5 dBm) and PDC (17 mW)
    - **Design of an active double-balanced direct down-conversion mixer** for Conversion gain 10 dB @ 10 MHz, NF (≤ 15 dB) IIP3 (≥ 0 dBm) P1dB (-10 dBm) PDC (≤ 4 mW) and RF frequency 2.492 GHz.
  - **Project 1: UMC 65 nm Technology VDD =1.2V**
    - Design of a Narrow Band LNA Design (2.49GHz) for Bandwidth of 100MHz, Differential gain 24 dB and centre frequency 2.49 GHz.

- **Project 2: UMC 65 nm Technology VDD =1.2V**
  - Design of a 4.5 to 5.5 GHz Differential CC VCO and PLL and its Layout

- **Design a power amplifier using AFIC901N** Course: Solid State Microwave Devices and Applications
  Guide- Prof.Jayanta Mukherjee, Dept. of EE IIT Bombay [Mar'19-Apr'19]
  - It is designed for the minimum gain of 20 dB at 520 MHz and fabricated on FR-4 substrate with $\varepsilon r = 4.4$, h = 1.6 mm, $\tan\delta = 0.02$ and matching networks and bias-tee for $S11 \leq -10$ dB and $S12 \leq -60$ dB.

MS RESEARCH PROJECT AND SEMINAR

- **MS Thesis** [Dec'20-Till date]
  Title: Design of Oscillatory Neural Network (ONN) to solve combinatorial optimization problems (COPs)
  Guide- Prof. Jayanta Mukherjee, Prof.Udayan Ganguly, Dept. of EE IIT Bombay
  Objective: To design a low power, low area, fast ONN circuit to solve COPs suitable for neuromorphic circuits
  Ongoing work:
  - Schmitt trigger based 5 nodes ONN chip measurement of 45 nm GF for in and out of phase synchronization and ordering of the oscillators based on initial condition.

  Previous work:
  - Design of PCB Schematic and Layout to perform testing of 5 nodes ONN circuit
  - Tape out of the 5 nodes ONN circuit to perform in and out of phase synchronization between oscillator, ordering of the oscillators based on initial condition. and 2 nodes ONN circuit with different coupling capacitor configuration and variable frequency option in 45 nm GF.
  - Power supply noise influence analysis on use of maximum number of readable oscillators with size of ONN.
  - Analysis of the charging and discharging currents in an oscillator cycle to demonstrate the concept of in phase and out of phase settling.
  - Different oscillators design analysis to find the suitability of ONN.
  - Basic modules design of LNA, Mixer and LC oscillators for 60 GHz Transceivers for Short range [July'19-Apr'20] non-contact vital signs monitoring in **65 nm UMC technology.**
  - 4-bit Pipeline ADC design for ISRO in **65 nm UMC technology.**
- **MS Seminar** [May'19]
  Title: 60 GHz Transceiver design for Non-Contact Vital Signs Monitoring
  Guide- Prof. Jayanta Mukherjee, Dept. of EE IIT Bombay
  - Design Challenges and applications of 60 GHz oscillator and devices is explored

TECHNICAL SKILLS

- **Programming & Scripting Languages:** MATLAB, Verilog, Verilog-A, VHDL
- **Tools and Technologies:** Cadence, ADS, Ngspice, LTspice, XCircuit

PROFESSIONAL EXPERIENCE

- Assistant professor at Electronics Department, **AISSMS IOIT** campus, Pune [July'13 to May'17]
- Assistant professor at Electronics and Communication Department, **AIT Pune** Campus. [June'17 to May'18]

TECHNICAL EXPERIENCE

- Worked at **CMC LTD (A Tata Enterprise)**, Mumbai as an **Engineer Trainee** [June'08 to May'09]
  - Maintains SUN Solaris/UNIX Servers and control panels of simulators including electronic instruments.
  - Maintains Router trouble shooting and n/w monitoring at Central Bank of India Mumbai.
- Worked at Cad Track Digital System, Bhopal as an **O&M Engineer** [Aug'09 to Jan'11]
  - Maintains flow, pressure, humidity and temp. of Isolators, assign work to ITI workers.

POSITIONS OF RESPONSIBILITY

- **Executive Member** in PGAC, IIT Bombay [May'20 to Apr'21]
- TA Duty in every semester, IIT Bombay [July'19 to May'23]
  - PC Lab Prof. Nair Jayakrishnan and EE207 Prof. Saha Dipnkar
  - EE101 Prof. M. B. Patil and EE101 Ashwin Talapurkar
  - PC Lab Prof. Subhnand and EE214 Prof. Madhav Desai
- NPTEL Duty for Analog Circuit IIT Bombay [Jan'20 to Mar'20]
  - Prof. Jayanta Mukherjee, Detp. of IIT Bombay