Department of Electronic & Telecommunication Engineering

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Heart ECG Monitor

Group 27

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Abstract

This report is based on the Analog based Heart ECG monitoring device project completed for the EN2091 - Laboratory Practice and Projects module. The report covers the designing process starting from ECG signal acquisition to displaying the waveform to the final device prototyping. Due to the lower amplitude of the signal, proper amplification was done and details of several standard circuit modularities such as instrumentation amplifiers and filters are discussed in the report too. All the testing procedures starting from computer simulation to PCB testing were done to identify and mitigate any distortions and improve the quality of the signal. All the other details including PCB and enclosure design are mentioned in the report as well.

Contents

1 Introduction

A heart ECG monitor is a device capable of displaying an electrical measurement of the human heart in real time. It is a non-invasive method of diagnosing many diseases related to the cardiac system of the body such as arrhythmia. The device takes as input, a 3-lead ECG signal using electrodes placed on the left shoulder, right shoulder, and the bottom side of the left abdomen. Then, the effect of the noise of the input signal is minimized by noise filtering using an instrumentation amplifier. The effect of the 50 Hz noise from the power supply is further reduced by the addition of a notch filter. The signal obtained after noise filtering is sent through a low-pass filter with a cut-off frequency of 150Hz and a high-pass filter with a cut-off frequency of 0.05Hz in order to obtain the relevant ECG signal. The amplified ECG signal can be displayed on either the oscilloscope or Matlab software. A detailed description of the project is given below.

2 Design

The following specifications were taken into consideration when designing the Heart ECG monitor to amplify and display ECG signals with minimum distortion and superior signal quality.

- Standard 3 Lead signal acquisition should be used.
- Multiple stages of amplification are needed due to the lower magnitude of the body's electrical signal.
- Higher CMRR is needed to remove the noise. Otherwise, it is difficult to identify a clear ECG waveform.

2.1 Signal Acquisition

Three electrodes are placed on the right shoulder, left shoulder, and bottom left side of the abdomen to get the signal. In some cases, electrodes are placed on the right arm (RA), left arm (LA), and right leg (RL). RA and LA connect to the instrumentation amplifier and RL connects to the leg drive circuit. The physiological basics related to this placement are discussed in *Eithoven's triangle* formation.
In this device, three external electrode wires are connected to the main circuit.

Figure 1: ECG Electrodes with connecting wires

2.2 Noise Filtering

2.2.1 Instrumentation Amplifier

Instrumentation amplifier plays a major role in our ECG Device by improving the common mode rejection ratio of the circuit and stabilizing the device by providing high input gain to the circuit. It is composed of 2 stages.

1. Buffering Amplifier
2. Differential Amplifier

Buffering Amplifier

Peak to peak voltage of the input signal is about 4 mV, and hence in order to take the input signal without distortion, the input current has to be limited. For that purpose, we have used buffering amplifiers at the input stage of the instrumentation amplifier. Resistors R_1 and R_2 determine the amplifying ratio.

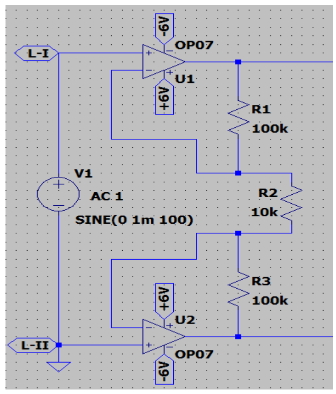


Figure 2: Buffering amplifier

$$\text{Buffer stage gain} = \left(\frac{2 \times 100\,\mathrm{k\Omega}}{10\,\mathrm{k\Omega}} + 1\right) = 21$$

Differential Amplifier

As the name implies, in this stage the difference in the input is amplified by the circuit. Resistors R_4 and R_6 determine the amplifying ratio.

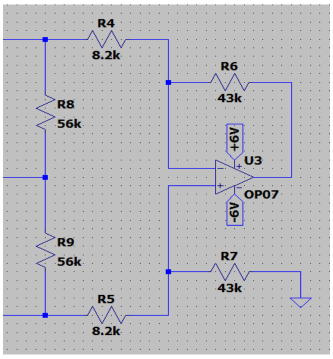


Figure 3: Differential amplifier

$$\text{Differential stage gain} = \frac{43\,\text{k}\Omega}{8.2\,\text{k}\Omega} = 5.244$$

So the complete instrumentation amplifier can be obtained by cascading these two stages .

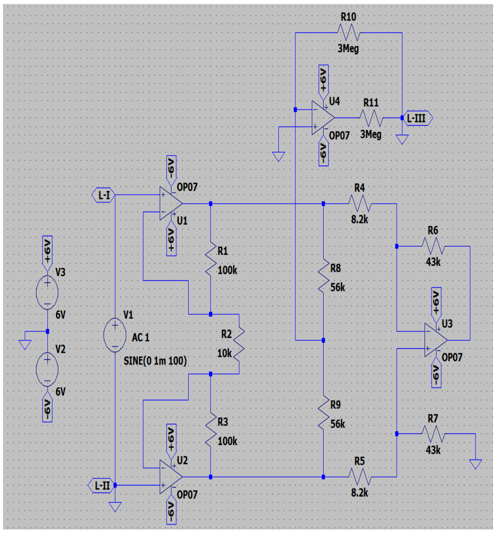


Figure 4: Instrumentation Amplifier

So the final gain of the Instrumentation amplifier when in differential mode is as follows;

$$\text{Total gain} = 21 \times 5.244 = 110.04$$

Since this circuit amplifies the difference of the inputs, common mode noise is canceled out at this stage. The gain of the Instrumentation amplifier when in common mode is 2.38407×10^{-6}.

2.2.2 Low Pass Filter

There are two topologies for a second-order low-pass filter: the Sallen-Key and the Multiple Feedback (MFB) topology. The MFB topology is commonly used in filters that have high-quality factors and require a high gain. But since our filter has a lower gain, we used the Sallen-key topology.

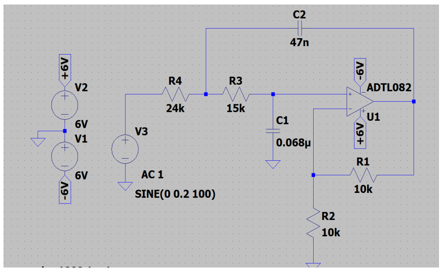


Figure 5: Second order Low Pass Filter

$$f_c = \frac{1}{2\pi\sqrt{R_3 R_4 C_1 C_2}}$$

$$\text{LPF Gain} = 1 + \frac{R_1}{R_2}$$

As a rule of thumb, it is recommended to keep the passband gain of a filter below 3. Since we needed to amplify the signal in multiple stages, a passband gain of 2 was selected for the LPF. To achieve that, the following capacitors and resistor values were used.

$$\begin{aligned} R_1 &= 10\,\text{k}\Omega & R_2 &= 10\,\text{k}\Omega \\ R_3 &= 15\,\text{k}\Omega & R_4 &= 24\,\text{k}\Omega \\ C_1 &= 0.068\,\mu\text{F} & C_2 &= 47\,\text{nF} \end{aligned}$$

Simulation results are as follows:

- Gain = 2
- Cutoff frequency = 147.678 Hz

2.2.3 High Pass Filter

Low ECG signals contain a lot of noise. Among those noises baseline wander is a low-frequency noise that can be seen in common ECG signals. Baseline wander noise is the noise added to the ECG signal due to respiration, subtle motions, and changes in electrode impedance.

This noise has a frequency range from 0-0.05/0.06Hz. Hence to remove that noise we have to use a high pass filter (HPF) with a cutoff frequency lying within the range of 0.05-0.06Hz.

Since the cut of frequency is very small and transmission bandwidth (about 0.01) is very narrow we have to proceed with a second-order low pass filter. Even though higher-order filters improve the steepness of the transmission band to avoid unnecessary complications we didn't use filters with very high orders.

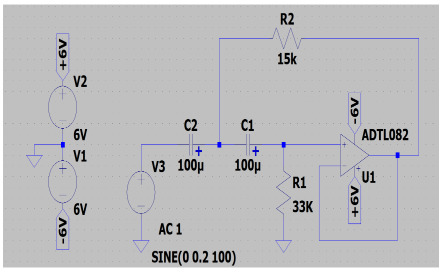


Figure 6: Second order Low Pass Filter

$$f_c = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

To obtain the required cutoff frequency, component values were chosen as follows. $R_1 = 33\,\mathrm{k}\Omega$, $R_2 = 15\,\mathrm{k}\Omega$ and $C_1 = C_2 = 100\,\mu\mathrm{F}$. Simulation results are as follows:

- Gain = 1
- Cutoff frequency = 68.3582 mHz

2.2.4 Notch Filter

The 50Hz noise, also known as power line noise, is a main factor that interferes with the ECG signals. As a result, a notch filter (band rejection filter) must be used to minimize its effect on the signal. A band-rejection filter is used to suppress a certain frequency rather than a range of frequencies. Two of the most popular band-rejection filters are the active Twin-T and the active Wien-Robinson circuit, both of which are second-order filters. In comparison to the Twin-T circuit, the Wien-Robinson filter allows modification of the passband gain without affecting the quality factor. Hence, an active Wien-Robinson filter was used in the design process.

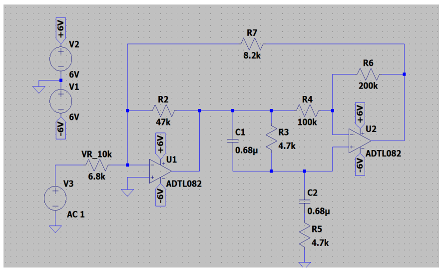


Figure 7: Notch filter

$$\alpha = \frac{R_2}{R_7} \qquad \beta = \frac{R_2}{\mathrm{VR}}$$

$$mid-frequency: \quad f_m = \frac{1}{2\pi R_5 C_2}$$

$$passband\ gain: \quad A_0 = \frac{\beta}{1+\alpha}$$

$$rejection\ quality: \quad Q = \frac{1+\alpha}{3}$$

As per the standard component values available in the market, R_3/R_5, R_4, R_2, R_7, VR, and C_1/C_2 values were selected as $4.7\,\mathrm{k}\Omega$, $100\,\mathrm{k}\Omega$, $47\,\mathrm{k}\Omega$, $8.2\,\mathrm{k}\Omega$, $6.8\,\mathrm{k}\Omega$, and $0.68\mu F$, respectively, such that the mid-frequency has a value of 49.79817 Hz. The quality (Q) factor and the pass band gain (A_0) have values of 2.244 and -1.02675 (inverted signal), respectively. Simulation results are as follows:

- Gain = -1
- Upper Cutoff frequency = 39.9 Hz
- Lower Cutoff frequency = 62.1 Hz
- Mid Cutoff frequency = 51 Hz

2.2.5 Right Leg Driven Circuit

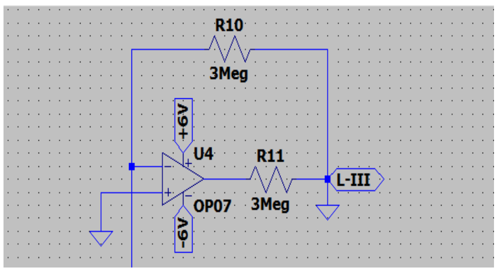


Figure 8: Right Leg drive circuit

The Right leg-driven circuit was designed to reduce interference from the amplifier. Two averaging resistors measure the common-mode voltage on the body. It is then inverted and returned fed back to the right leg via R_{11}. To equalize the displacement currents circulating in the body, this circuit drives a very little current (less than $1\,\mu$A) into the right leg. As a result, the body becomes a summing junction in a feedback loop, and the negative feedback from this circuit reduces the common-mode voltage. This circuit also contributes to the patient's safety. If an abnormally high voltage appears between the patient and the earth due to electrical leakage or other factors, the right leg circuit's auxiliary op-amp saturates. Therefore, since the amplifier can no longer drive the right leg, the patient is effectively ungrounded. The patient is protected because the resistance R_{11} between the patient and the earth is considerable. The amplifier will saturate at 0.5 µA current with a 3 MΩ resistor and a supply voltage of 6V.

2.3 Signal Displaying

2.3.1 Summing Amplifier (For signal displaying)

This includes the final amplifying stage of the circuit design.

- Minimum gain - 1.04853
- Maximum gain - 21.603

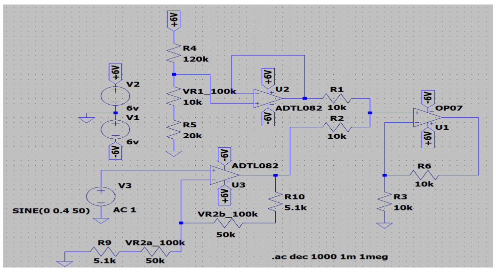


Figure 9: Summing Amplifier

For the display part, we need only a positive-sided voltage signal. Therefore, an offset DC voltage must be added to the varying output signal. This summation of the signal and the offset is done using an op-amp, which acts as a voltage adder.

In the final step, ***ESP32-WROOM module*** was used to display the signal on the monitor. Due to the restrictions of resources, serial communication is used at the initial stage of the product. However, with the proper resources, this could be used as an IoT device in the future by transmitting real-time data to a server and plotting the data on a screen.

2.4 Power Circuit

In order to power up op-amps, +6V, GND, and -6V are required. Therefore, a simple regulator circuit was used to obtain +6V, GND, and -6V. Further, a $Li - ion$ battery was used to power up the circuit and to minimize the effect of 50 Hznoise. This increases the portability of the device as well.

2.5 Component Selection

Initially, a few op amps were selected based on their CMRR and slew rate. Since having a higher value for the CMRR is essential in medical devices; LTC 1052 and LTC 1043 were initially selected. But due to their high cost and the unavailability of stocks in the local market, they were disregarded from the component selection.

OP07

OP07CP is a single op-amp Precision amplifier with the following parameters,

- Common Mode Rejection Ratio (CMRR) of 120 dB
- Power Supply Rejection Ratio (PSRR) of 108 dB
- Unity Gain Bandwidth of 0.6 MHz
- Input Offset Voltage of 60 mV
- Slew rate of 0.3 V/ μs

Due to the above values, this op-amp was used for the implementation of the Instrumentation amplifier.

TL072 Dual Op Amp

For the filter implementations, a higher number of operational amplifiers would be required if the single operational amplifier IC OP07CP was used, and the size of the Main PCB of the device would significantly increase. Due to these

reasons, the TL072 Dual op-amp which is commonly available in the market was selected to implement the high pass and low pass filters.
The typical parameters of the TL072 op-amp are as follows,

- Common Mode Rejection Ratio (CMRR) of 105 dB
- Power Supply Rejection Ratio (PSRR) of 100 dB
- Unity Gain Bandwidth of 5.25 MHz
- Input Offset Voltage of 1 mV
- Slew rate of 20 V/ μs

2.6 Schematic & PCB Design

PCB and schematic designs were done using Altium software. Two separate PCBs were done for the power and main circuit. The main circuit was done as a double-layer PCB. For +6V, -6V, and GND power nets, 10mil width was used and for other connections, 5mil was applied. Since the main PCB was printed by a foreign manufacturer (JLCPCB), several other rules and restrictions were also added. The power supply circuit which is used to power up all the ICs was done as a single-layer PCB and was manufactured locally.

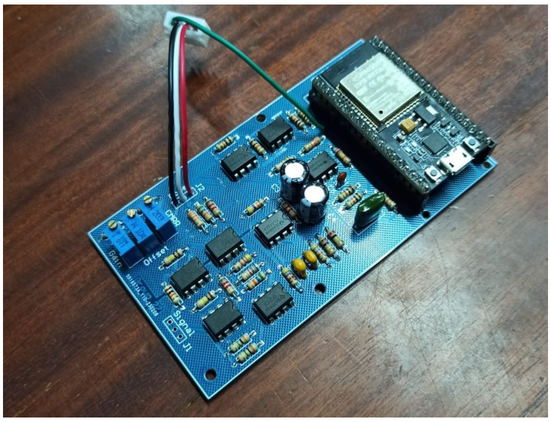


Figure 10: Main PCB board

2.7 Enclosure Design

The enclosure of the Heart ECG Monitor was designed using the SOLIDWORKS software and it comprises,

- MTS-1 series toggle switch for switching the device on/off
- Port for 3.5mm connector for signal input from the electrodes
- Port for Micro USB cable to connect the device to the laptop computer and obtain the output ECG waveform using Matlab software.
- Port for connecting the device to the oscilloscope
- Ventilation holes in order to avoid overheating of the device
- Battery compartment compatible with 4 rechargeable $Li-ion$ batteries (18650)

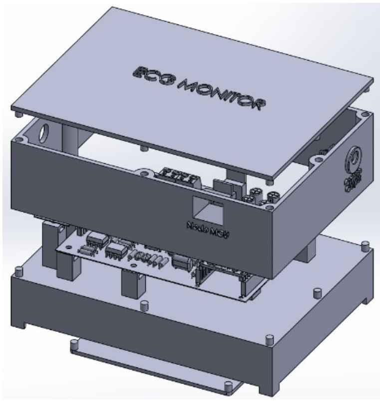


Figure 11: Enclosure designed using SOLIDWORKS

Figure 12: 3D printed enclosure

3 Results & Discussion

3.1 Testing and Results

Initially, the circuit was designed and simulated using *LTspice* software and the same was used for debugging purposes.

Next, the circuit was implemented on a breadboard and the tests were carried on until the required ECG signal was obtained. The resistor values were changed accordingly, fine-tuning the ECG waveform, and the selected resistor values were added to the *LTspice* simulation as well. The process was done repetitively until an ECG signal of sufficient accuracy was received.

After the testing of the breadboard implementation was finished and the results were verified to be accurate, the PCB was designed and made. After soldering the components on the PCB, tests were again carried on in order to confirm the functionality of the PCB.

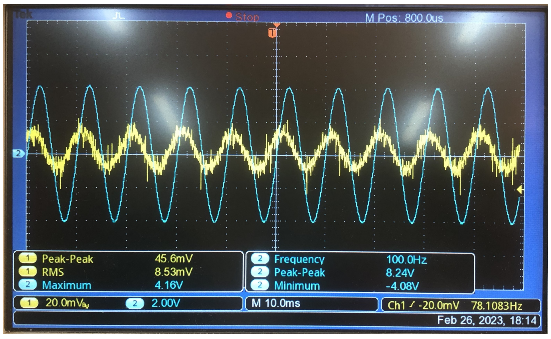


Figure 13: Signal filtering and amplification of a 10 mV sine wave

Here a 10 mV sine wave (yellow) was given as the input to the circuit. Then a sine wave (blue) of about 4 V was obtained as the output. Then the heart ECG signal was obtained using the circuit.

Figure 14: Obtained ECG signal

3.2 Discussion

Even though almost all the noise of the input signal in the range of the frequencies less than 0.05 Hz and greater than 150 Hz were removed by the high-pass and low-pass filters, the 50 Hz powerline noise was sometimes visible in the obtained output waveform. This was reduced as much as possible by the use of batteries as the power supply and the 50 Hz notch filter.

A clear ECG output waveform with much lower noise interference was obtained for some of the electrodes that were used for testing. The noise was significant for some of the used electrodes. However, with the same electrodes, the noise interference was much lower when the positive and negative input leads were interchanged resulting in an inverted ECG waveform.

Future improvements

- In-built display could be added in order to increase the portability of the device.
- Surface Mount Device (SMD) components could be added in order to reduce the size of the PCB resulting in a reduction of the enclosure.
- The output ECG waveform could be remotely sent to mobile devices developing the device further into an IOT device.
- The device could be modified to facilitate the charging of the device without the removal of batteries by the addition of an in-built charging system.

4 Contribution

Name.	Contribution
Amarasekara A.T.P. (200023C)	Regulator PCB design, Enclosure design
Herath H.M.E.A.C. (200212F)	Main schematic design, Notch/Low pass filter design, Soldering, Other circuit designs
Morawaka M.D. (200400F)	Main PCB design
Tharuka K.P. (200641T)	High pass filter design, Regulator schematic design

5 Components list

Component Value	Component Name	Quantity
1uF	Capacitor	2
10uF	Capacitor	2
0.68uF	Capacitor	2
100uF	Capacitor	2
68nF	Capacitor	1
47nF	Capacitor	1
10uF	Capacitor	2
1uF	Capacitor	2
100k	Axial Resistor 1/4W	5
10k	Axial Resistor 1/4W	7
56k	Axial Resistor 1/4W	2
3M	Axial Resistor 1/4W	2
8.2k	Axial Resistor 1/4W	3
43k	Axial Resistor 1/4W	1
33k	Axial Resistor 1/4W	2
6.8k	Axial Resistor 1/4W	1
47k	Axial Resistor 1/4W	1
200k	Axial Resistor 1/4W	1
4.7k	Axial Resistor 1/4W	2
15k	Axial Resistor 1/4W	2
24k	Axial Resistor 1/4W	1
5.1k	Axial Resistor 1/4W	2
100K	Resistor Cermet Trimmer	2
20K	Resistor Cermet Trimmer	2
LM7806CT	Voltage Regulators	2
OP07CP	OPAMP	5
TL072BCP	OPAMP	3
3.5 mm Jack		1
DPDT Switch		1
LM7806CT		2
ECG Probes		1
Lithium Ion battery		4

Figure 15: Components list

6 References

1. J.G.Webster, *Medical Instrumentation Application and Design*,4th ed., John wiley & Sons, 2009.

2. Analog Devices,"Ultralow Offset Voltage Operational Amplifier",op07. https://www.analog.com/media/en/technical-documentation/data-sheets/op07.pdf

3. Texas Instrument,"TL07xx Low-Noise FET-Input Operational Amplifiers",TL074 datsheet. https://www.ti.com/lit/ds/symlink/tl074.pdf?ts=1677302090812

4. Texas Instrument,"LM741 Operational Amplifier",LM741. https://www.ti.com/lit/ds/symlink/lm741.pdf

5. Linear Technology,"Zero-Drift Operational Amplifier",LTC1052. https://www.analog.com/media/en/technical-documentation/data-sheets/1052fa.pdf

6. Linear Technology,"Dual Precision Instrumentation Switched Capacitor Building Block",LTC1043. https://www.analog.com/media/en/technical-documentation/data-sheets/1043fa.pdf

7. Texas Instrument(August,2022),*Op Amps For Everyone*. Available:https://web.mit.edu/6.101/www/reference/op_amps_everyone.pdf

7 Appendix

7.1 Filter responses

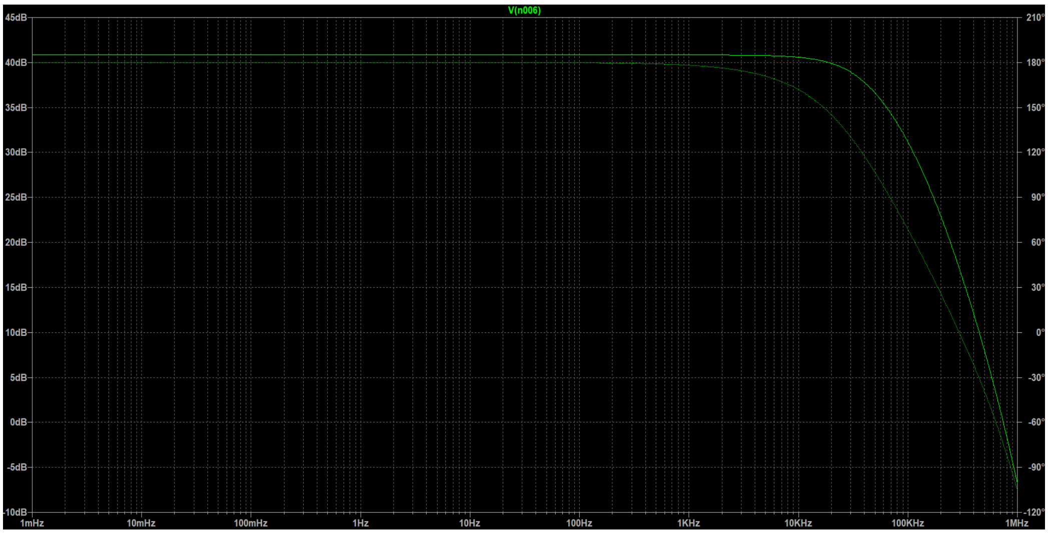


Figure 16: Instrumentation Amplifier Differential Mode Response

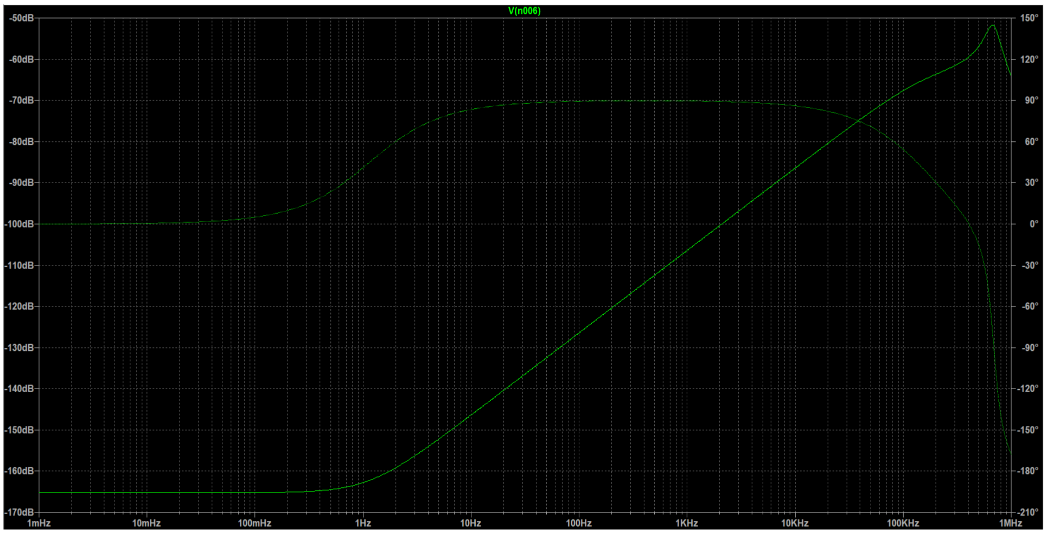


Figure 17: Instrumentation Amplifier Common Mode Response

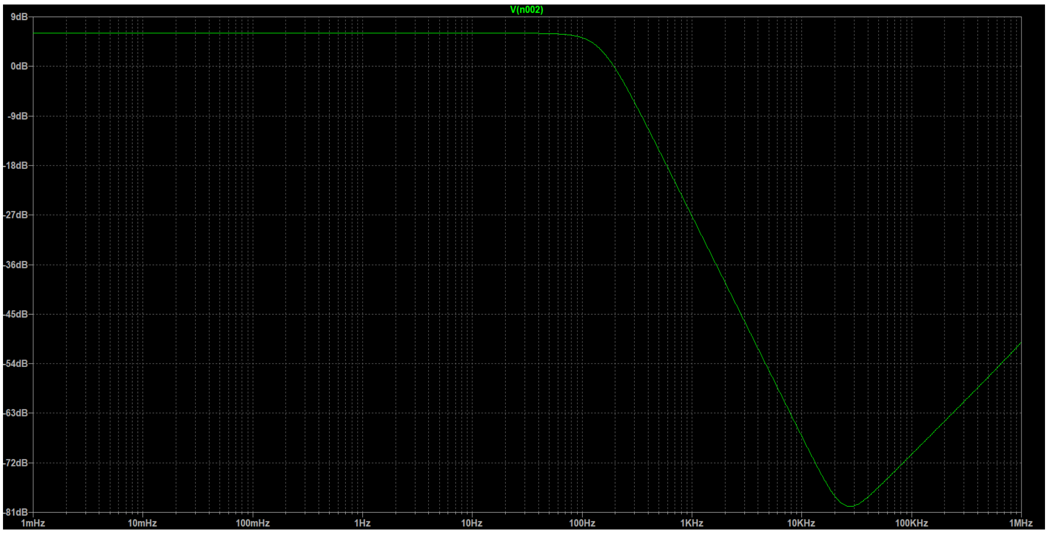


Figure 18: Lowpass filter response

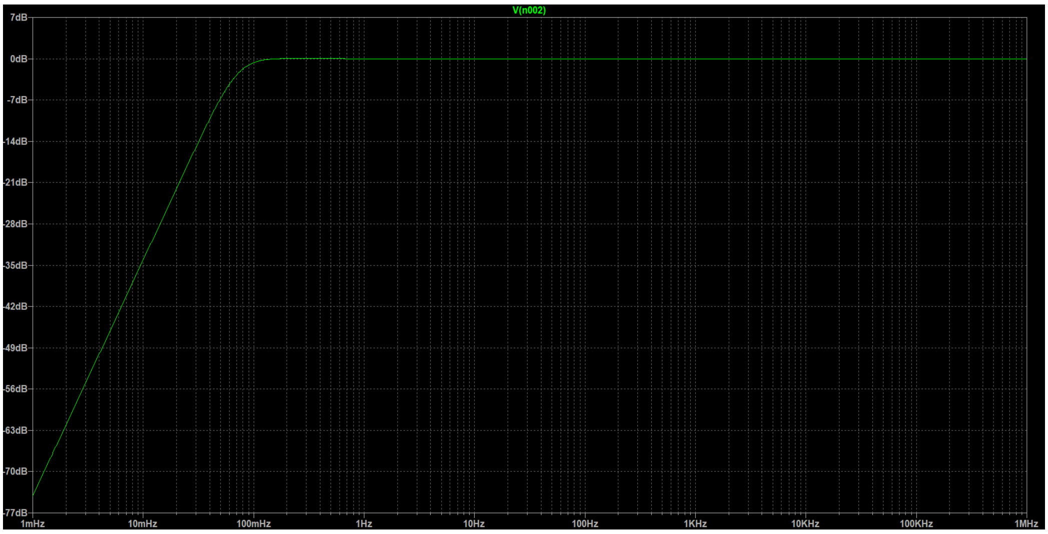


Figure 19: High pass filter response

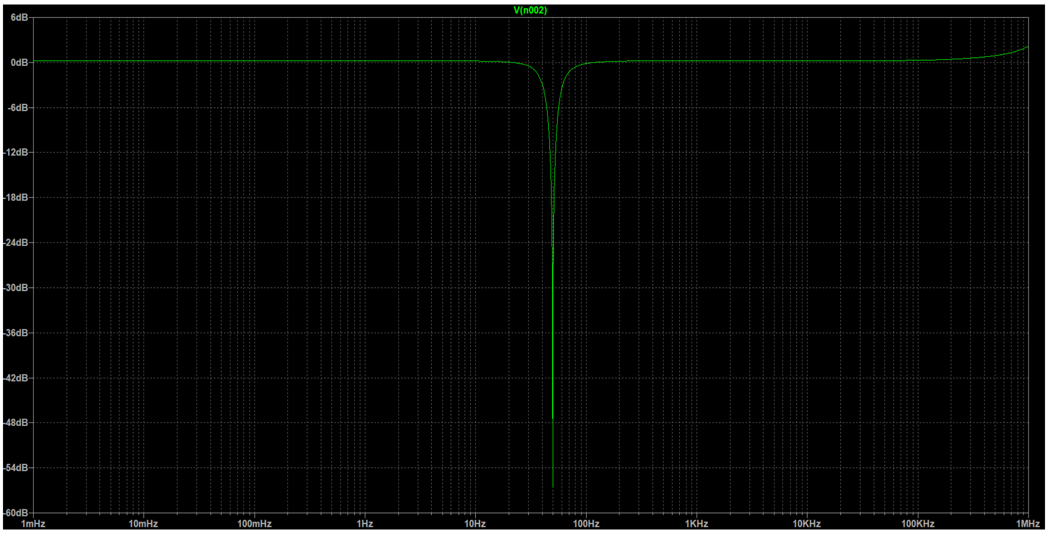


Figure 20: Notch filter response

7.2 LTspice circuit diagram

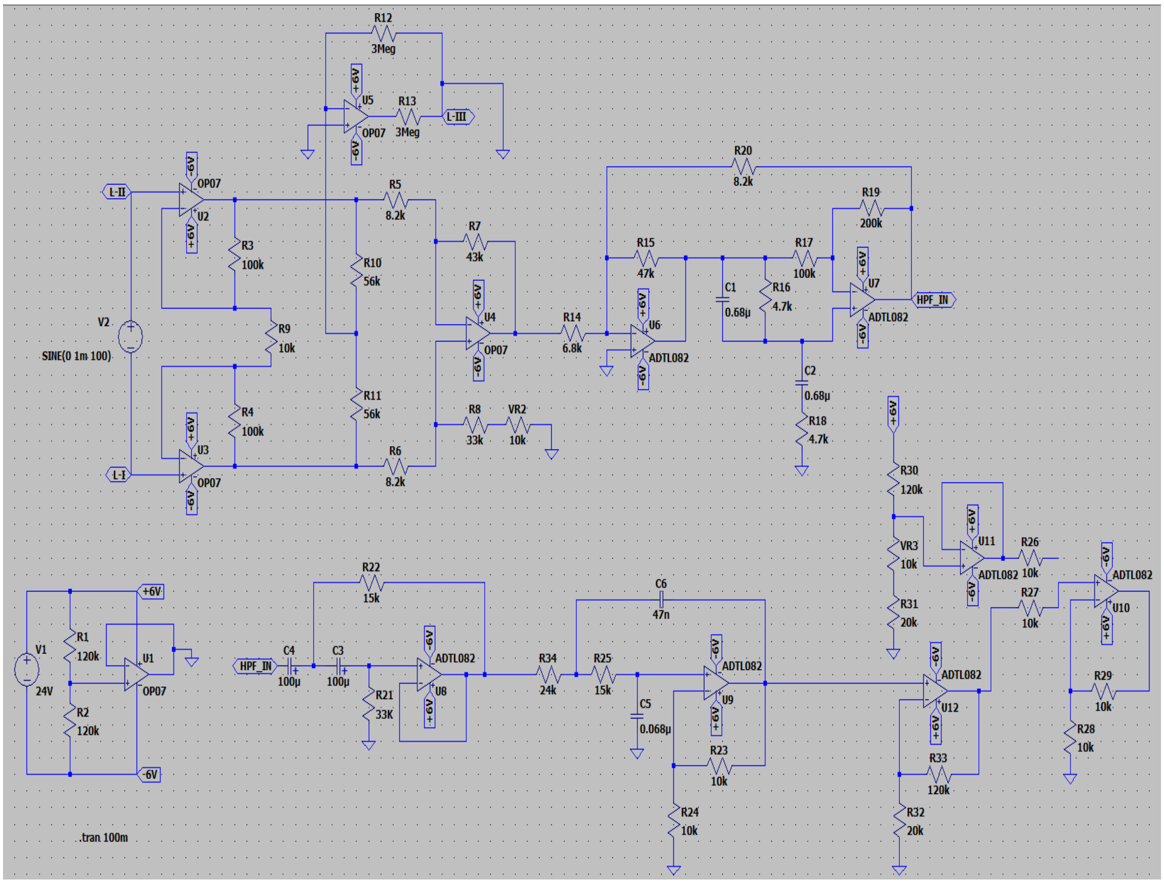


Figure 21: Final circuit design for LTspice simulation

7.3 Schematic Design

7.3.1 Main circuit

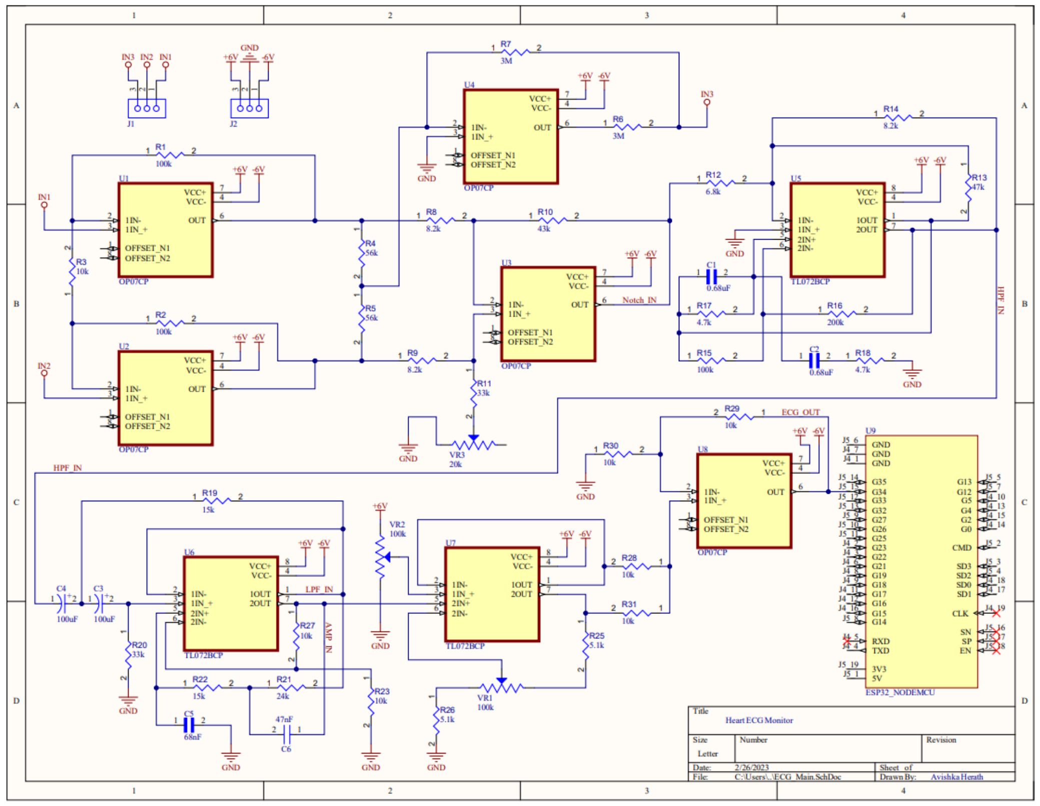


Figure 22: Schematic of main circuit

7.3.2 Power circuit

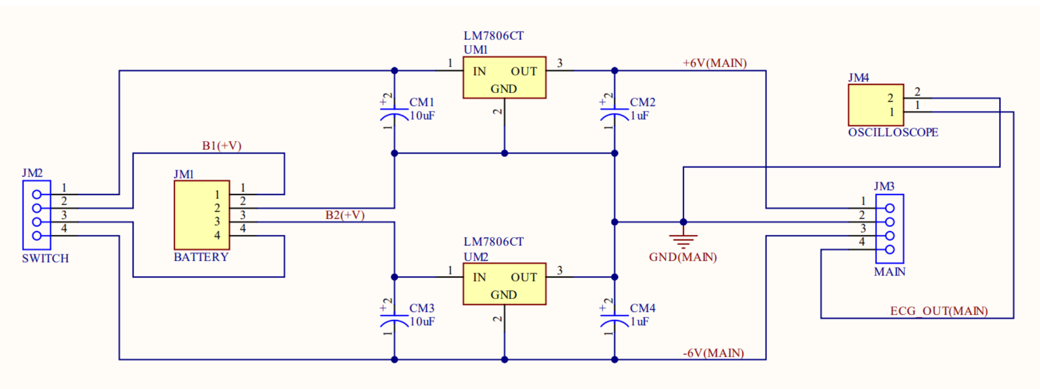
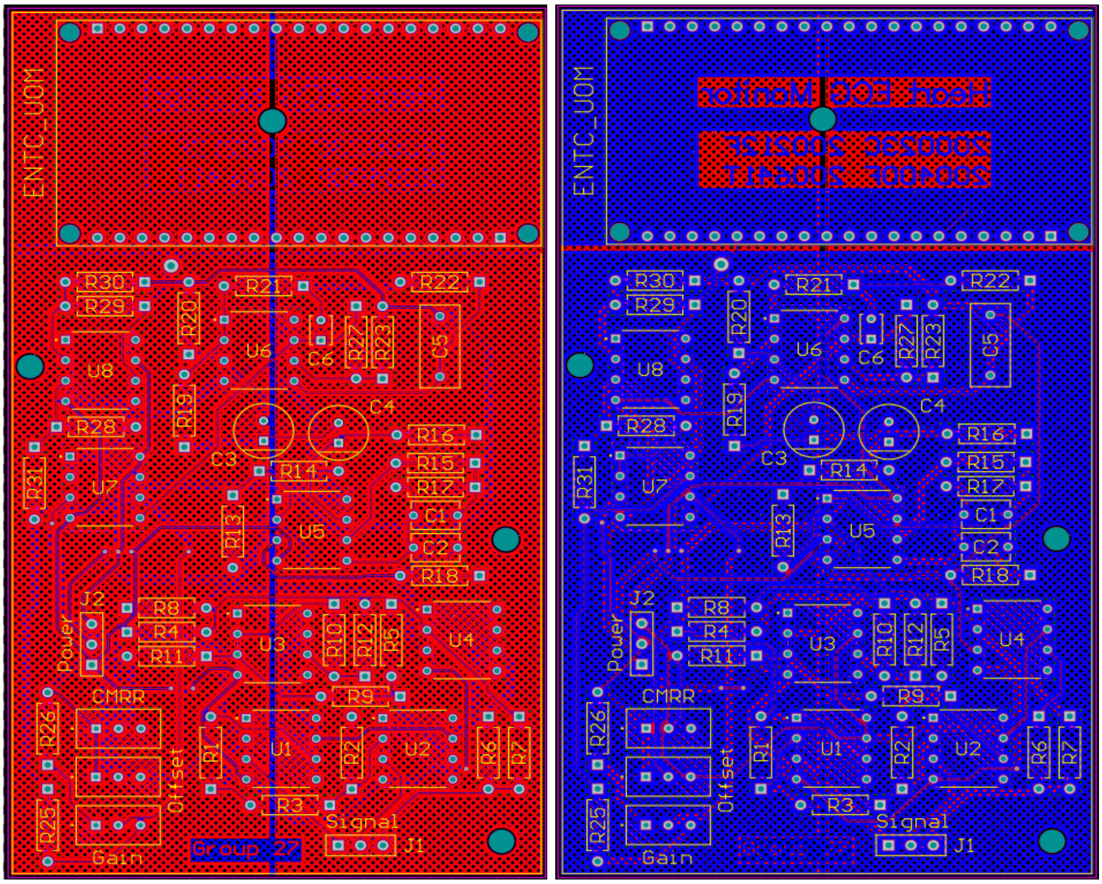


Figure 23: Schematic of power regulator circuit

7.4 PCB Layout Design

7.4.1 Main circuit



(a) Top layer of main PCB (b) Bottom layer of main PCB

7.4.2 Power circuit

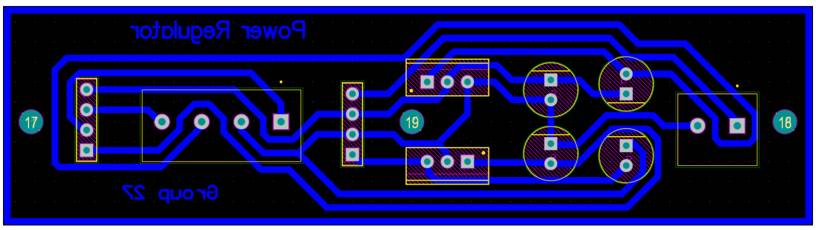


Figure 24: Power regulator PCB - Bottom Layer

7.5 3D view of PCB

7.5.1 Main circuit

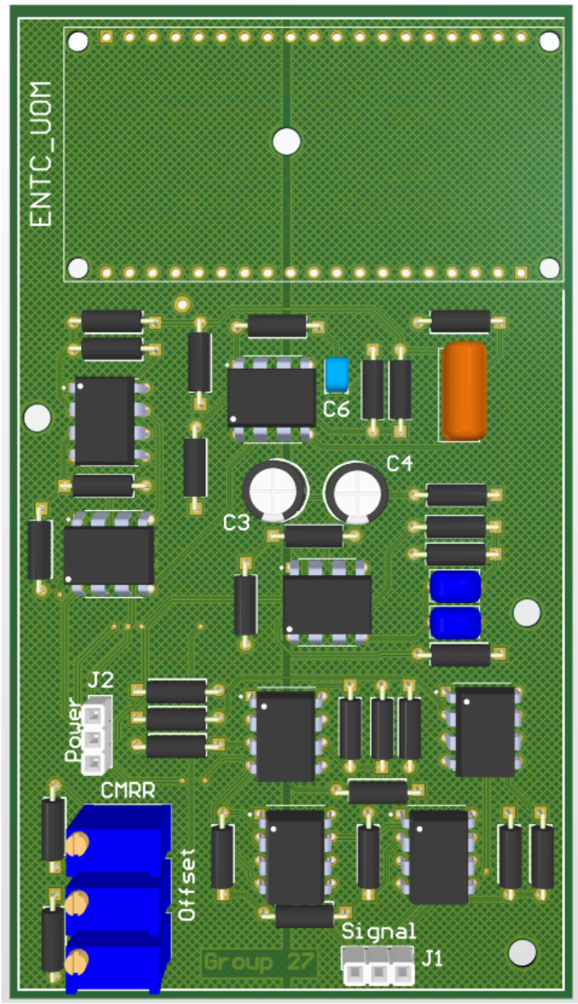


Figure 25: Main PCB 3D view

7.5.2 Power circuit

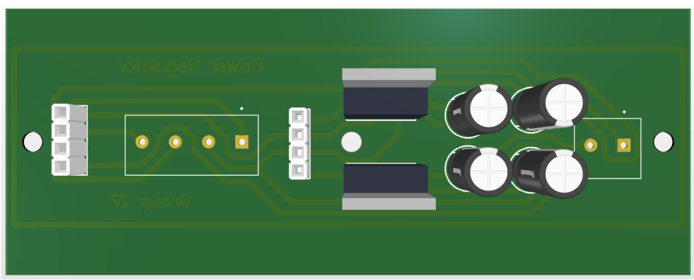


Figure 26: Power regulator PCB 3D view

7.6 Enclosure

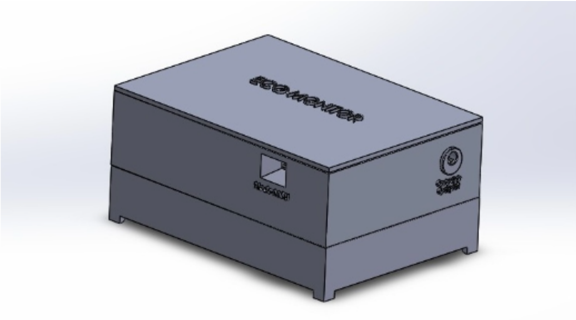


Figure 27: Enclosure design

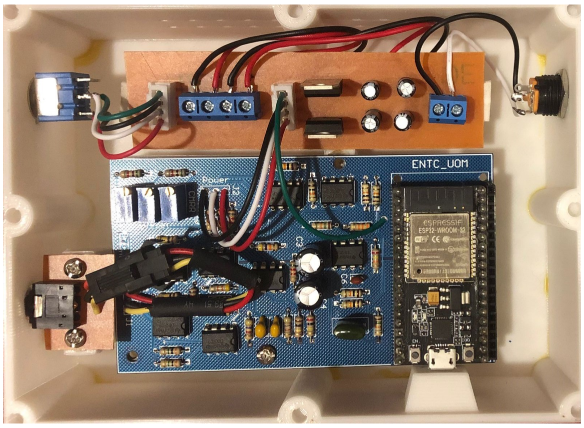


Figure 28: Final assembly

7.7 Signal display Arduino code

Serial_Plotter.ino

```
int signal=0;
void setup() {
  // put your setup code here, to run once:

  Serial.begin(9600);
  pinMode(A0,INPUT);
}

void loop() {
  signal = analogRead(A0);
  Serial.println(signal);
  delay(100);
  // put your main code here, to run repeatedly:

}

```

Figure 29: Arduino serial plotter code for signal displaying