1. Microprocessor (EX551, E4531)

Basics and Architecture

- **2070 Bhadra**: Define bus? Explain different types of bus. Define RTL. Write down the RTL for MOV r1, r2 in 8085 microprocessor. [4+4]
- **2070 Magh**: Differentiate between Hardwired and Microprogrammed Control Unit used in microprocessors? Write the fetch and execution cycle for LXI D,9050H instruction in RTL specifications. Explain each step. [4+4]
- **2071 Magh**: Define instruction cycle and machine cycle. Explain briefly the instruction processing cycle of Von Neumann machine. [4+4]
- **2072 Ashwin**: What is Bus? Explain Bus organization of microprocessor with diagram? Calculate the memory handling capacity of the processor having address bus of 24 lines and data bus of 16 lines. [2+4+2]
- **2072 Magh**: Draw and explain the block diagram of a computer. Explain stored program concept. [4+4]
- **2073 Bhadra**: Explain RTL based on any 8085 instruction. Define Stored program concept. [4+4]
- **2073 Magh**: Differentiate between Microprocessor and Microcontrollers. Explain how the microprocessor is organized in microprocessor based systems. [4+4]
- **2074 Bhadra**: Explain fetch and execution cycle of an instruction of a stored program computer. Illustrate with the help of RTL specification. [5+3]
- **2075 Baisakh**: Compare and contrast between hardwired and microprogrammed CU. [4]
- **2075 Bhadra**: Describe Von Neumann Machine. Differentiate Hardwired control unit and Micro programmed control unit. [4+4]
- **2076 Baisakh**: Explain the different components of microprocessor based system with necessary figure. Differentiate between microprocessor and microcontroller. [5+3]
- **2078 Baishakh**: What are the basic characteristics that differentiate microprocessor? Define stored program concept. Differentiate between Von Neumann and Harvard Architecture. [2+2+4]
- **2078 Poush**: Define stored program concept. Differentiate between Accumulator based processor with register based processor. Write the RTL for instruction LXI H, 20 H in 8085 processor. [4+4]
- **2078 Chaitra**: What is RTL? Write down the RTL code for the instruction LXI H, 3000H. [1+7]
- **2079 Jestha**: Explain stored program concept used in Von-Neumann computer. [4]
- **2080 Ashwin**: Define bus, Write about bus organization. [4] / Explain Von Neumann Architecture with its limitation. [4]
- **2080 Chaitra**: Differentiate between microprocessor and micro controller. Explain fetch and execute cycle using RTL for instruction LXI B, 2050H. [4+4]
- **2081 Ashwin**: Define control unit. List its different types. Compare and contrast between them. [2+1+5]

Models and Registers

- **2070 Bhadra**: In how many ways 8085 instructions can be classified? Explain with examples. What is the purpose of the branching instructions? [6+2]
- **2070 Magh**: Write any three features of 8085 microprocessor. Explain the addressing modes of 8085 with example. [3+5]
- **2071 Bhadra**: Explain briefly the programmer's model of 8085 microprocessor. [3]
- **2071 Magh**: Draw the internal architecture of 8085 microprocessor and explain each part. [8]
- **2072 Ashwin**: Explain the instruction format and data format of 8085 microprocessor Explain different addressing modes of 8085 microprocessor. [4+4]
- **2072 Magh**: What is flag? Discuss about 8085 associated flags. Along with suitable examples show how these flags are affected by arithmetic and logical group of instructions. [1+2+5]
- **2073 Bhadra**: What are the characteristics of 8085 microprocessor? Discuss all the input and output signals that are originated from microprocessor. [2+6]
- **2073 Magh**: What is flag? Discuss about 8085 associated flags. Along with suitable example show how these flags are affected by arithmetic and logical group of instructions. [1+2+5]
- **2074 Bhadra**: What is the use of Program Counter and Stack Pointer registers of 8085 microprocessor? How these registers get affected during CALL, RET, PUSH and POP instructions explain with suitable examples. [4+4]
- **2075 Baisakh**: Draw the programming model of 8085 and explain each unit. [2+4] / Explain the operations and uses of RST instructions in 8085. [4]
- **2075 Bhadra**: Draw the internal architecture of 8086 microprocessor and explain it. [8]
- **2076 Baisakh**: Explain the function of following pin signals of 8085 microprocessor: HOLD, HLDA, READY, RD, WR, IO/M, ALE, INTA [8]
- **2078 Baishakh**: What are the features of 8085 microprocessor? Explain the instruction format and data format of 8085 microprocessor. [4+4]
- **2078 Poush**: What is the use of Program Counter and Stack Pointer registers of 8085 microprocessor? How these registers get affected during CALL, RET, PUSH and POP instructions explain with suitable example. [4+4]
- **2078 Chaitra**: Draw the internal architecture of 8085 microprocessor and explain its each block. [8]
- **2079 Jestha**: Draw the programming model of 8085 microprocessor and explain the following instructions of 8085 with syntax and example: JNZ, POP and CALL. [2+6]
- **2080 Ashwin**: List out and explain the 40 different PIN signals used by 8085 microprocessor with a neat diagram. [8]
- **2080 Chaitra**: Draw programming model of 8085 and explain each term in detail. [8]
- **2081 Ashwin**: How is delay calculated in 8085 microprocessor? Explain with example. How PUSH and POP instruction works in 8085 microprocessor? [5+3]

Assembly Language Programming (ALP) and Instructions

- **2070 Bhadra**: Write an assembly language program for 8085 to exchange the bits D6 and D2 of every byte of a program. Suppose there are 200 bytes in the program starting from memory location 8090H. [8]

- **2070 Magh**: Write an assembly language program in 8085 to divide a byte stored in memory location 9070 H by byte stored in 9071 H and store the remainder and quotient at 9072 H and 9073 H respectively. [8]
- **2071 Bhadra**: Write a program for 8085 to add the upper and lower nibble of ten 8 bit words stored in a table that starts from location 5B20H. Store the Separate results in locations just after the table. [8]
- **2071 Magh**: Write an assembly language program for 8085. Table1 contains 16 no. of 8 bit data, transfer data which have number of 1s greater than 3 from table1 to table2, otherwise store FFH in table2. [8]
- **2072 Ashwin**: Write a program in 8085 to calculate the number of ones in the upper nibble of an array of numbers stored in a table, Store the count of ones in a location just after the table. [8]
- **2072 Magh**: Write a program for 8085 to generate multiplication table of a number stored at 8230H and store the generated table starting at 8231H. For example, if location 8230H has number 05H then store 05H at 8231.H, 0AH at 8232H and so on. [8]
- **2073 Bhadra**: How are the flags of 8085 processor affected during the usage of arithmetic and logic instructions? Explain with examples. Explain the following instructions with example program (i) DAA (ii) SPHL (iii) RAL (iv) PCHL [4+4]
- **2073 Magh**: Write an assembly language program for 8085 to find the square of ten 8-bit numbers which are < 0FH, stored from memory location C050H. Store the result from the end of the source table. [8]
- **2074 Bhadra**: There are two tables holding twenty data whose starting address is 9000H and 9020H respectively. Write a program to add the content of first table with the content of second table having same array index. Store sum and carry into the third and fourth table indexing from 9040H and 9060H respectively. [8]
- **2075 Baisakh**: Write an ALP in 8085 to transfer 20 bytes of data in a table to another table by interchanging D7 and D3 bits of each byte. [8]
- **2075 Bhadra**: Write a program for 8085 to count the numbers for which upper nibble is higher than the lower nibble; and store the count at the end of table having 50 bytes data from C050H. [8]
- **2076 Baisakh**: Explain the operation of following instructions of 8085 with syntax, size, and flag status with examples: STA, SHLD, DCX, RLC, POP, LDAX, DAD, SBB [8] / Write a program in 8085 to find the largest and smallest bytes from the list of 20 bytes stored starting from memory location C050 H. Store the largest byte and smallest byte in C070 H and C071 H respectively. [8]
- **2078 Baishakh**: There are 40 8-bit numbers in a table with address starting form 9090H. Write a program in 8085 to transfer these numbers to another table with address form A010H if lower nibble of a number is greater than higher nibble. Otherwise transfer by setting bit D2 and resetting bit D6. [8]
- **2078 Poush**: A set of 10 numbers are stored in memory location C070 H onward. WAP in 8085 to test whether the number is odd or even. Store the even number in separate list starting from memory location C090H. [8]
- **2078 Chaitra**: An array of bytes is stored starting from memory location C301H. Length of this array is stored in memory location C300H. Write an assembly language program in 8085 to add upper and lower nibble of each byte and store the sum starting from memory location C401H. [8]

- **2079 Jestha**: 15 bytes of data are stored in first array in memory. Write an ALP in 8085 to store number of 1's and number of 0's of each byte in second and third array in memory. [8]
- **2080 Ashwin**: A set of 10 numbers are stored in memory location C070 H onward. WAP in 8085 to test whether the number is odd or even. Store the even number in separate list stating from memory location C090H. [8]
- **2080 Chaitra**: There are 10, 8-bit data stored from memory location 7C000H. Copy data to 7C20H if D6 is 1 & D0 is 0, otherwise copy by flipping bit D6 & D0. [8]
- **2081 Ashwin**: A set of 50, 8-bit numbers are stored in memory location A090H onward. Write a program in 8085 to set D7 bit, reset D5 bit and complement D7 bit if the number is greater than 50H else store FFH in the destination table starting at B090H. [8]

Interfacing and Memory Management

- **2070 Bhadra**: Draw internal block diagram of 8086. Explain Bus Interface Unit. [5+3]
- **2071 Magh**: Draw the address decoding circuit to interface two RAM memory block each of 8 KB at address C000H. [8]
- **2073 Bhadra**: Design an interfacing circuit for following problem: i) 74LS138: 3 to 8 Decoder ii) 2732 (4K*8): EP-ROM address range should begin at 0000H and additional 4K memory space should be available for future explanation iii) 6116(2K*8): CMOS R/W memory. [8]
- **2073 Magh**: With a neat diagram explain the interfacing circuit using a 3 to 8 decoder (74LS138) needed to connect the following memory units to the 8085 microprocessor consecutively starting from memory location A000H: 2Kx8 ROM chip, 2Kx8 RAM chip, 4Kx8 EPROM chip. [8]
- **2074 Bhadra**: Design an address decoding circuit to interface two 8k*8 ROM chips at address starting at 4000H. [5]
- **2075 Bhadra**: Differentiate synchronous bus and asynchronous bus. Design an address decoding circuit to interface 4 KB ROM and 2KB RAM. The starting address is 4000 H. Use suitable decoder. [2+6]
- **2076 Baisakh**: What is programmable peripheral interface (PPI)? Write down the different modes of operation available in PPI. Explain how different modes of PPI can be used. [2+6]
- **2078 Baishakh**: Design an interfacing circuit to interface one 4 KB EPROM and two 2 KB RW memory for 8085 microprocessor. [8]
- **2078 Chaitra**: Design the address decoding interface of an input port and output port for 8085 at FAH and F8H address. Use at least one 74LS 138 decoder. Explain clearly how the microprocessor reads/writes to this input and output devices. [8]
- **2078 Poush**: Design the address decoding interface of an input port and output port for 8085 at 31H and 82 H address. Use block decoder. [8]
- **2079 Jestha**: Design the address decoding circuit or interface for one ROM and three RAMs of 8 KB each with 8085 microprocessor with base address 4000H. [6]
- **2080 Ashwin**: Design an address decoding circuit to interface two 2732 EPROM of 4KB and one 6116 RAM of 2KB with starting address of 2600H using 74LS138 (i.e.) 3 to 8 Decoder. [8]

- **2080 Chaitra**: Design an address decoding circuit to interface one PROM of 4K*8, one EEPROM of 2K*8 and one SRAM of 8K*8 with memory location starting at 3000H. [8]
- **2081 Ashwin**: Explain memory mapped IO and IO mapped IO. Suppose you have two 2 KB RAM chips, draw interfacing diagram showing all the control signal to interface these RAMs to Intel 8085 with starting address at 4000H. [2+6]

Interrupts and Control

- **2070 Bhadra**: How interrupt vector table is used in microprocessors to manage the interrupt? Explain how software and hardware interrupts are used in 8086 microprocessor in detail. [3+5]
- **2070 Magh**: Differentiate Maskable and Non-Maskable interrupt. Write the general sequence to be followed when interrupt occurs. [2+6]
- **2072 Ashwin**: What is interrupt? What is its importance in microprocessor? How interrupts from different peripherals can be handled with single INTR pin in 8086 microprocessor? Explain. [2+3+3]
- **2073 Bhadra**: Differentiate between maskable and non-maskable interrupts. Explain how different interrupt pins of 8085 are used. [2+6]
- **2073 Magh**: Explain the purpose of the EI, DI, SIM and RIM instructions of the 8085 processor while using interrupts. Describe how the 8085 obtains the starting address of the interrupt service routine for each of the hardware interrupts. [8]
- **2074 Bhadra**: What are the software interrupts of 8085? Discuss the different hardware interrupts available in 8086. Write down the steps, sequentially carried out by the systems when an interrupt occurs. [3+3+2]
- **2075 Bhadra**: Differentiate polling vs. interrupt. Explain how interrupt vector table is used to handle interrupts in 8086 microprocessor. [2+6]
- **2076 Baisakh**: What are vectored and non-vectored interrupts? List and explain different interrupts available in 8085 microprocessor. How interrupts are handled by 8085 microprocessor. [2+6]
- **2078 Baishakh**: What do you mean by interrupt? How interrupt is handled in 8085 microprocessor? Explain SIM and RIM instruction in detail. [1+3+4]
- **2078 Chaitra**: Explain the SIM instruction in 8085. How interrupt are handled in 8085 microprocessor? [5+3]
- **2078 Poush**: How is interrupt processing differs from pooling? Write general sequence to be followed when interrupt occurs. [3+5]
- **2080 Ashwin**: Differentiate between maskable and non-maskable interrupt. Explain RIM instruction with its uses. [3+5]
- **2080 Chaitra**: Describe Polled Interrupt and Chained interrupt. Explain Interrupt processing cycle of 8085 microprocessor. [3+5]
- **2081 Ashwin**: How is interrupt handled in 8085 microprocessor? Explain in detail about different hardware interrupts available in 8085 microprocessor. [4+4]

Timing and Cycles

- **2070 Bhadra**: Write the various machine cycle involved in LDA C030 stored at C050. Write the use of following pins of 8085 microprocessor. ALE, IO/M, READY, RD, AD0-AD7. [3+5]
- **2070 Magh**: What do you mean by serial interface? Differentiate between synchronous and asynchronous serial interfacing. Describe how we can use RS-232 standard to transfer data from DTE to DCE and vice versa? [1+3+4]
- **2071 Bhadra**: Draw and explain the bus timing for OUT 42H instruction of 8085 microprocessor. [8]
- **2071 Magh**: Draw timing diagram of instruction LDA 2080H. Calculate the time needed to execute this instruction if the crystal frequency is 6 MHZ. [6+2]
- **2073 Magh**: Draw and explain the timing diagram of LXI D, 2465 H. Calculate the time required to execute this instruction if the crystal frequency is 6MHZ. [6+2]
- **2074 Bhadra**: What do you mean by Machine cycle and T-states? Draw a bus timing diagram for an instruction ANI 55H of 8085 microprocessor. Calculate the time required to execute such instruction, if microprocessor is operating at 2MHz clock frequency. [2+4+5+1]
- **2075 Baisakh**: Explain the execution of Instruction ANI 4BH in 8085 with the help of timing diagram. [5]
- **2075 Bhadra**: What is instruction cycle and machine cycle? Explain the timing diagram instruction LXI B, A050H with necessary diagram. [2+6]
- **2076 Baisakh**: What are different machine operations of 8085 microprocessor? Explain the bus timing cycle of ADI 25H (op code) with timing diagram. [3+5]
- **2078 Baishakh**: Draw the timing diagram of MVI M, 30H and explain it. [3+5]
- **2078 Poush**: Draw the bus timing diagram for STA 3050H which is stored in stored in memory location 8200H. [6]
- **2078 Chaitra**: Draw the timing diagram for the instruction JMP 8080H. Assume the instruction is stored in memory starting at 2000H. [8]
- **2079 Jestha**: Explain the operations of HOLD and HLDA pins of 8085 used in DMA with block diagram showing DMA controller. [5]
- **2080 Ashwin**: Write the bus timing cycle for an instruction LHLD 8040H stored at memory location C020H. [5]
- **2080 Chaitra**: Draw bus timing diagram of instruction OUT 01H which is at location 4000H. Also calculate the time required to execute the instruction if clock frequency is 5 MHz. [6+2]
- **2081 Ashwin**: Explain in brief about different serial data transfer methods. Write RTL and draw timing diagram of instruction MVI M,55H. [3+5]

Miscellaneous (Including Operating Systems and Parallelism)

- **2070 Bhadra**: Write the conditions that may cause deadlock to arise. Explain Flynn's classification. [4+4]
- **2070 Magh**: Write down the difference of RISC and CISC computers. [3]
- **2072 Ashwin**: What is register based and accumulator based architecture? Differentiate between CISC and RISC architecture? [2+6]
- **2073 Bhadra**: What is interprocess communication? How does deadlock occur? How can it be solved? [2+3+3]

- **2073 Magh**: Discuss about Flynn's Classification. What are the key features having with a typical Operating system? [4+4]
- **2074 Bhadra**: What do you mean by accumulator based microprocessor? Compare RISC and CISC architecture. [2+6]
- **2075 Bhadra**: What is pseudo and real parallelism? Explain Flynn's Classification. [4+4]
- **2076 Baisakh**: What are the features of RISC architecture? Differentiate register based and accumulator based architecture. [5+3]
- **2078 Poush**: Discuss about Flynn's Classification. What are the key features having with a typical Operating system? [4+4]
- **2078 Chaitra**: Write notes on: a) RISC and CISC Architectures b) Features of operating systems [2x4]
- **2079 Jestha**: Discuss about Flynn's Classification. What are the key features of a typical operating system? [4+4] / Describe various organizations of multiprocessing system. Explain various features of modern operating system. [4+4]
- **2080 Ashwin**: Discuss about Flynn's Classification. What are the key features having with a typical Operating system? [4+4]
- **2080 Chaitra**: Discuss about Flynn's Classification. Write the differences between RISC and CISC architecture. [4+4]
- **2081 Ashwin**: Define deadlock and explain the necessary conditions responsible for deadlock. Differentiate between real and pseudo parallelism. [5+3]

Short Notes

- **2070 Bhadra**: Write short notes on: a) Hardwired and micro program control unit b) EXE and COM programs [4x2]
- **2070 Magh**: Write short notes on: a) Serial and parallel interface b) Programmable peripheral interface [2x4]
- **2071 Magh**: Write short notes on: a) I/O mapped and memory mapped I/O b) DMA [4x2]
- **2072 Ashwin**: Write short notes on: a) DMA b) INTR and MUL [2x4]
- **2073 Bhadra**: Write short notes on: i) USART ii) RISC [4x2]
- **2073 Magh**: Write short notes on: i) RS232 [4x2]
- **2074 Bhadra**: Write short notes on any two: a) Flags in 8086 Microprocessor b) DMA Controller c) Deadlock and its Remedies [2x4]
- **2075 Baisakh**: Write short notes on any two: a) One pass and two pass assembler b) DMA Controller c) OS and Its features [2x4]
- **2076 Baisakh**: Write short notes on: a) RS 232 Standard b) Programmable Peripheral Interface [4x2]
- **2078 Baishakh**: Write short notes on: a) Flag register in 8086 b) RS 232 c) PPI device 8255 [2x4]
- **2078 Poush**: Write short notes on: a) USART b) EXE and COM Program [2x4]
- **2078 Chaitra**: Write short notes on: a) Flags of 8085 b) EXE and COM programs c) OS and its functions [2x4]
- **2079 Jestha**: Write short notes on: a) 8237 DMA Controller b) 8086 Addressing Mode c) Semaphore [2x4]

- **2080 Ashwin**: Write short notes on: a) IVT of 8086 b) Pseudo Parallelism and Real Parallelism c) Synchronous and Asynchronous Bus [2x4]
- **2080 Chaitra**: Write short notes on: (Any Two) a) IVT of 8086 b) Pseudo Parallelism and Real Parallelism c) Synchronous and Asynchronous Bus [2x4]
- **2081 Ashwin**: Write short notes on: (Any Two) a) Instruction formats in 8085 b) DMA c) Memory Hierarchy [4+4]