Spartan-6 LX9 MicroBoard

Avnet Design Services

www.em.avnet.com/s6microboard

Spartan-6 LX9 MicroBoard Rev C
8/2/2012

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Modified Rev A Boards are Functionally Equivalent to Rev B Boards.

Modified Rev B Boards are Functionally Equivalent to Rev C Boards.

X's are a "No ERC" directive to the Design Rule Checker to ignore rule violations.

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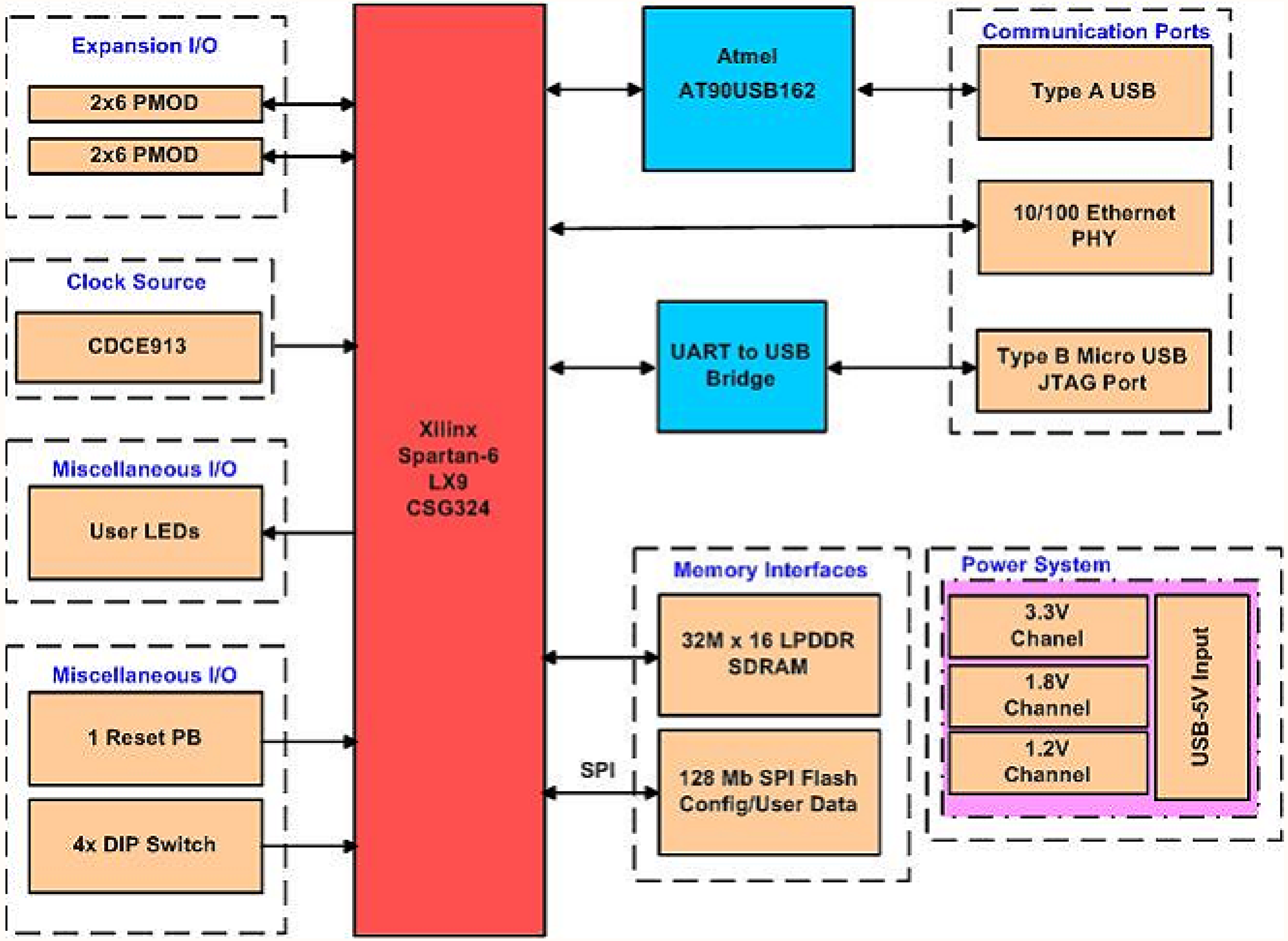
Title: Sheet 1 - Lead Sheet		
Size: B	Document Number: S6-LX9-SCH-C	Rev: C
Date: 8/2/2012	Sheet 1 of 10	



X's are a "No ERC" directive to the Design Rule Checker to ignore rule violations.

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Title: Sheet 2 - Block Diagram
Size: B
Document Number: S6-LX9-SCH-C
Rev: C
Date: 8/2/2012
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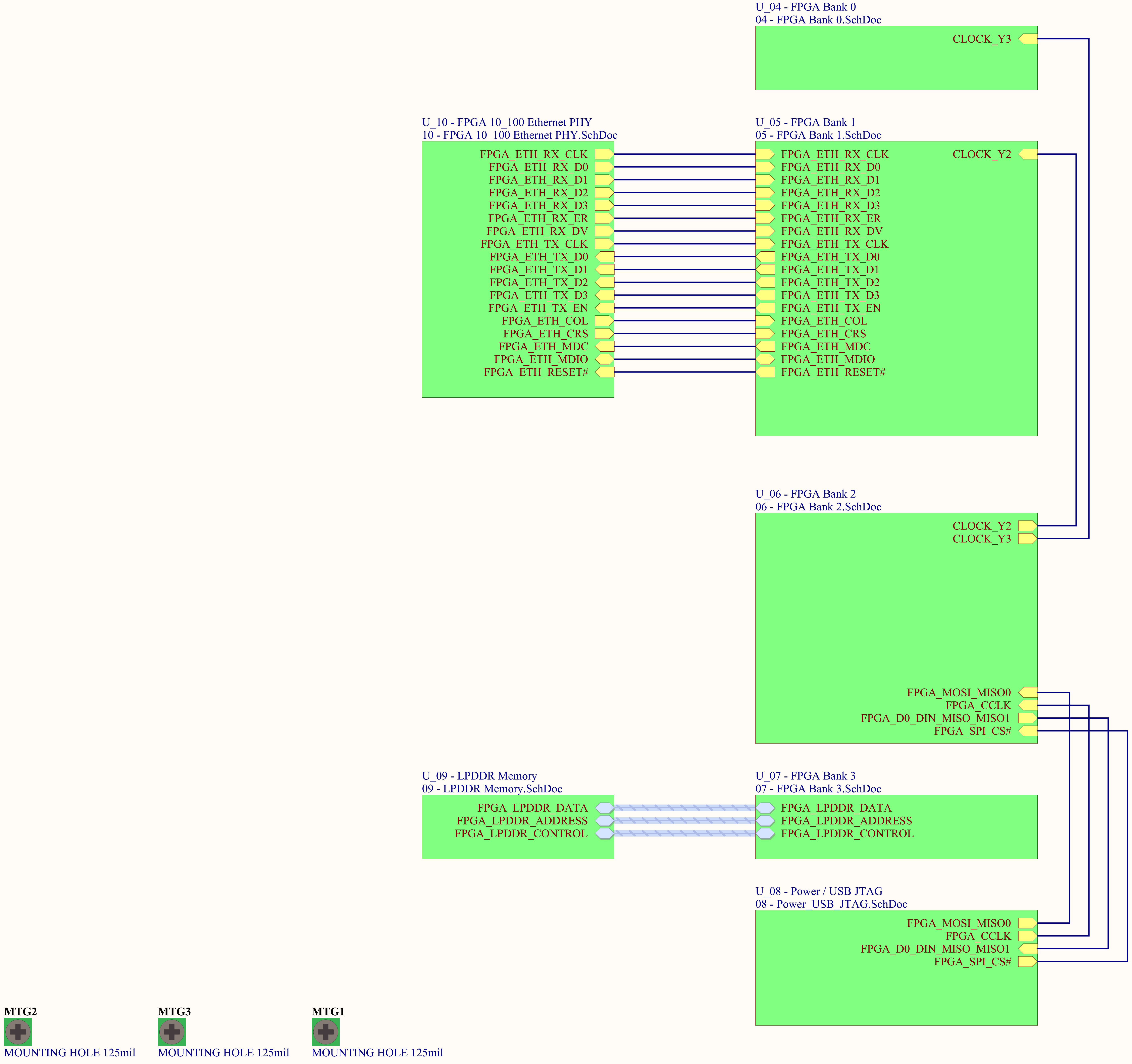

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Title: Sheet 3 - Architecture
Size: C
Document Number: S6-LX9-SCH-C
Rev: C
Date: 8/2/2012
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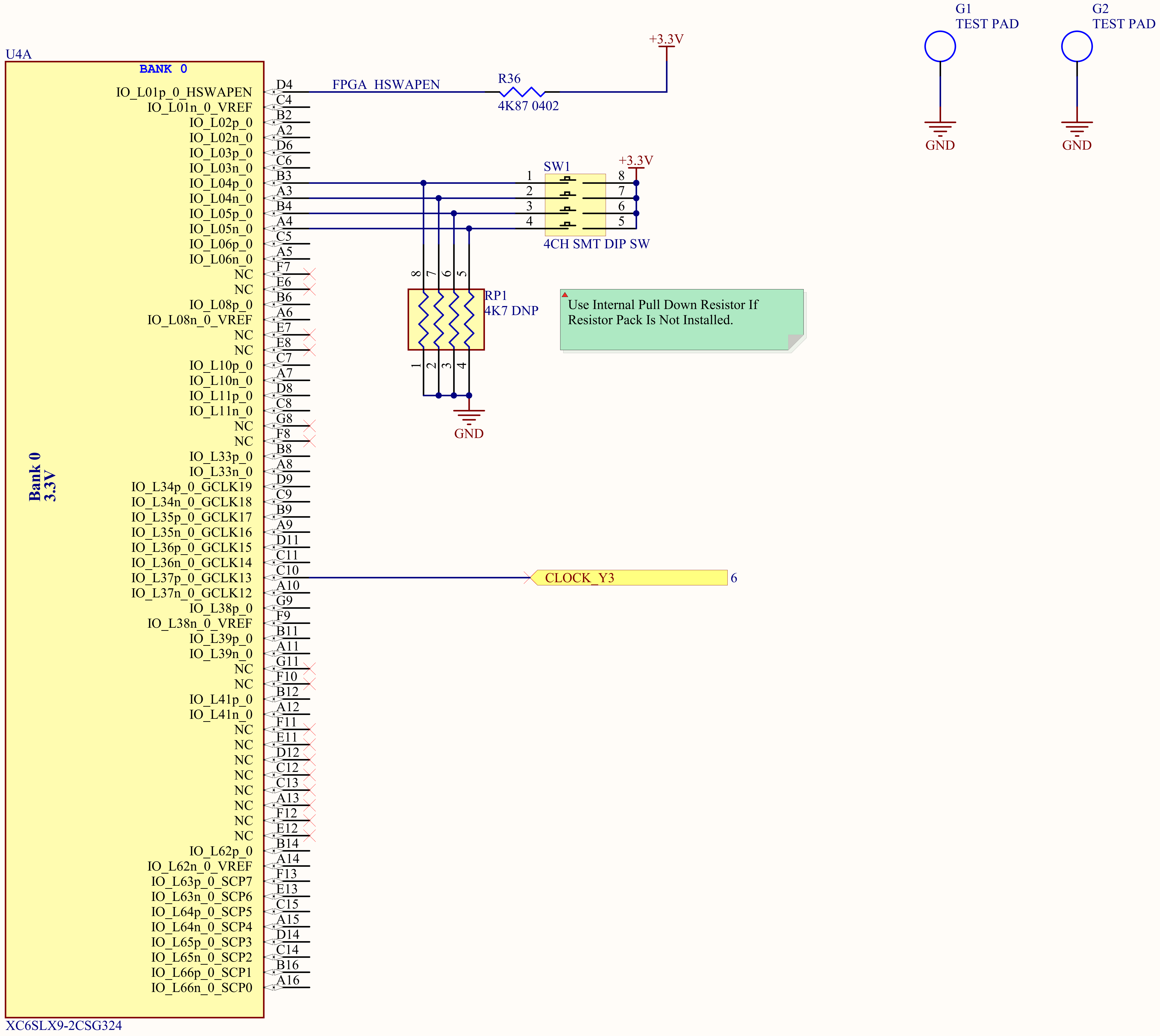

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Title: Sheet 4 - FPGA Bank 0

Size:	Document Number:	Rev:
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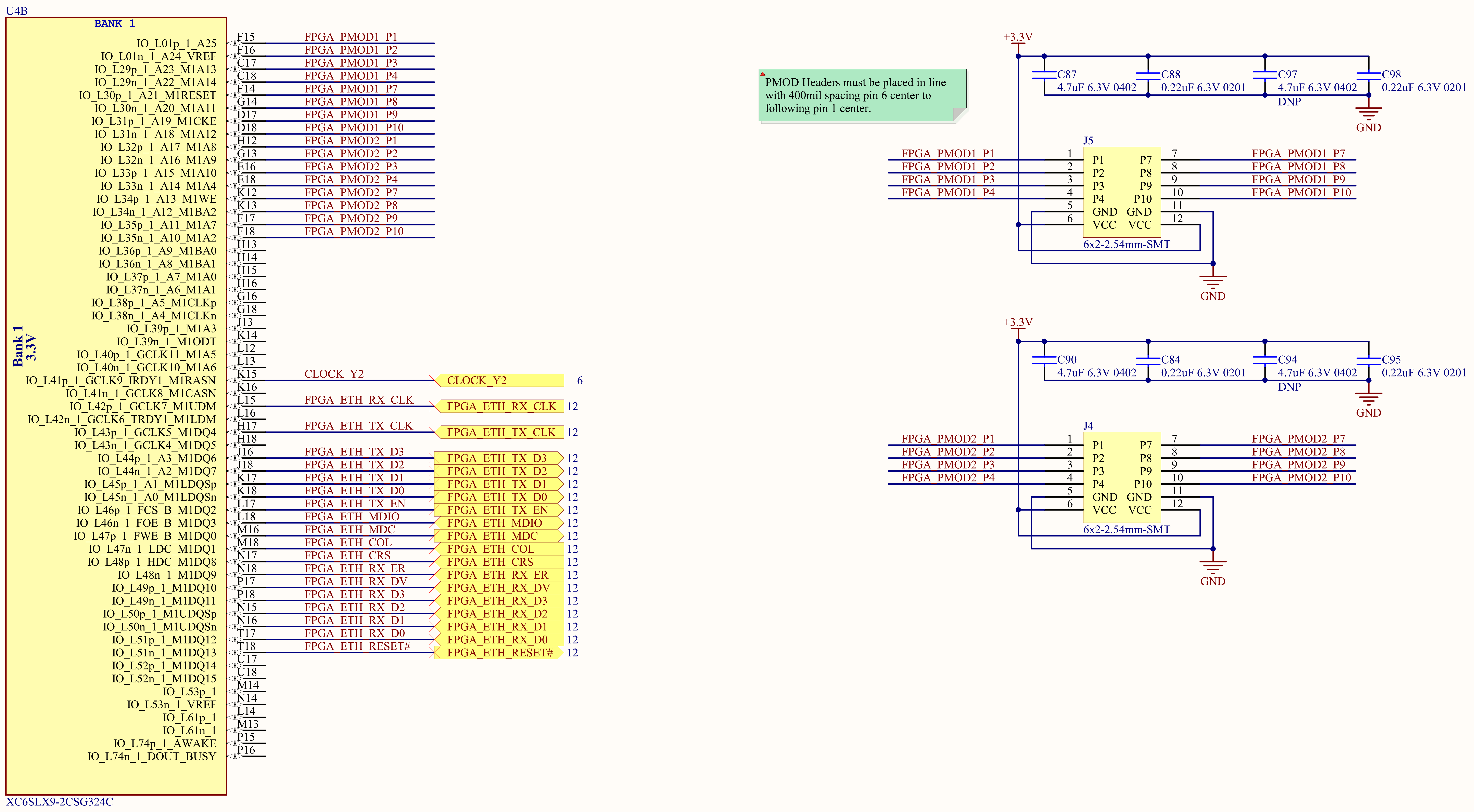

PMOD Headers must be placed in line with 400mil spacing pin 6 center to following pin 1 center.

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Title: Sheet 5 - FPGA Bank 1

Size: B	**Document Number:** S6-LX9-SCH-C	**Rev:** C
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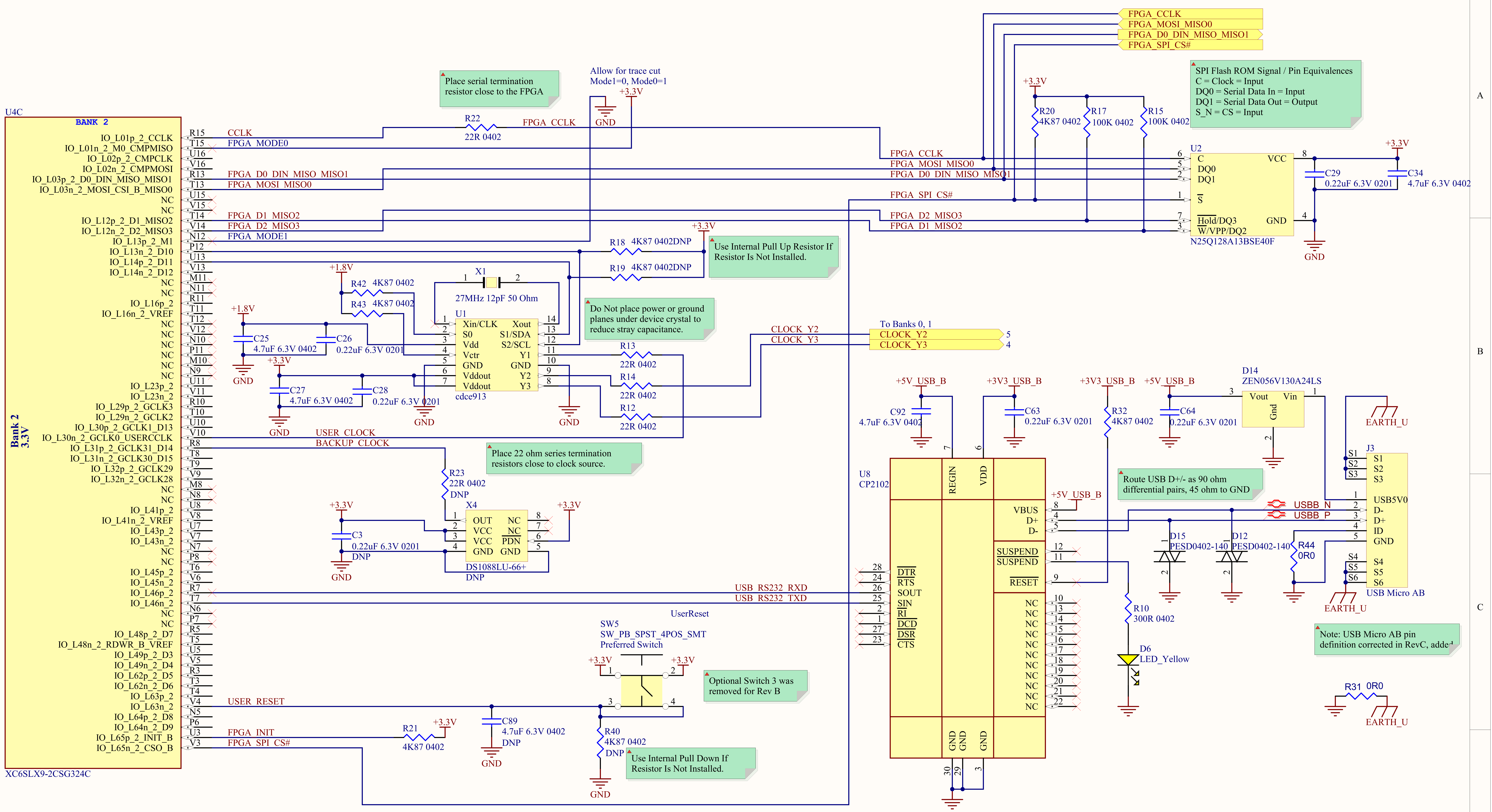

Place serial termination resistor close to the FPGA

Allow for trace cut
Mode1=0, Mode0=1

SPI Flash ROM Signal / Pin Equivalences
C = Clock = Input
DQ0 = Serial Data In = Input
DQ1 = Serial Data Out = Output
S_N = CS = Input

Use Internal Pull Up Resistor If Resistor Is Not Installed.

Do Not place power or ground planes under device crystal to reduce stray capacitance.

Place 22 ohm series termination resistors close to clock source.

Route USB D+/- as 90 ohm differential pairs, 45 ohm to GND

Note: USB Micro AB pin definition corrected in RevC, adde

Optional Switch 3 was removed for Rev B

Use Internal Pull Down If Resistor Is Not Installed.

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Title: Sheet 6 - FPGA Bank 2

Size: B
Document Number: S6-LX9-SCH-C
Rev: C

Date: 8/2/2012
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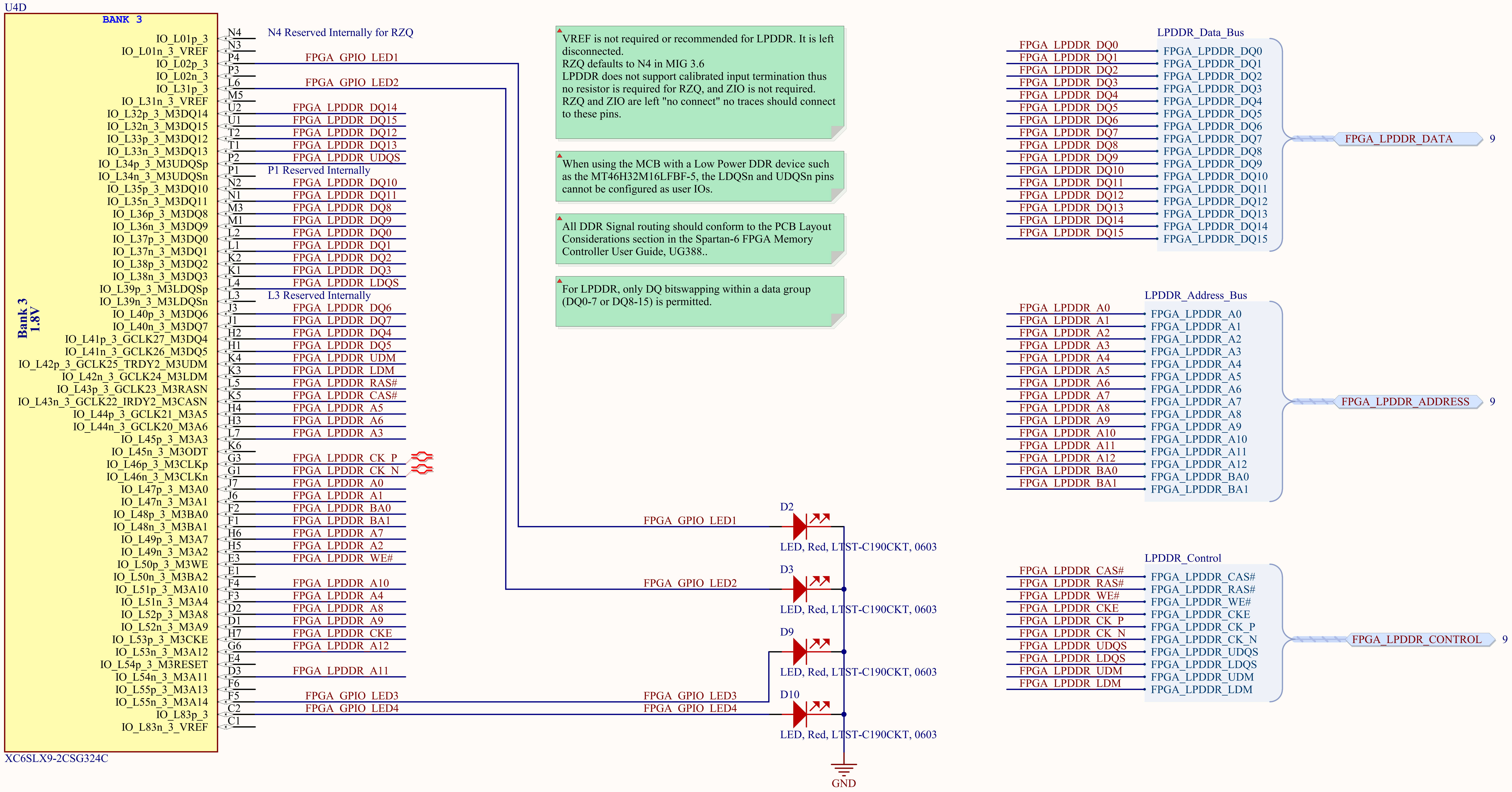

VREF is not required or recommended for LPDDR. It is left disconnected.
RZQ defaults to N4 in MIG 3.6
LPDDR does not support calibrated input termination thus no resistor is required for RZQ, and ZIO is not required.
RZQ and ZIO are left "no connect" no traces should connect to these pins.

When using the MCB with a Low Power DDR device such as the MT46H32M16LFBF-5, the LDQSn and UDQSn pins cannot be configured as user IOs.

All DDR Signal routing should conform to the PCB Layout Considerations section in the Spartan-6 FPGA Memory Controller User Guide, UG388..

For LPDDR, only DQ bitswapping within a data group (DQ0-7 or DQ8-15) is permitted.

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Title: **Sheet 7 - FPGA Bank 3**
Size: B
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Route USB D+/- as 90 ohm differential pairs, 45 ohm to GND

Place 22 ohm series termination resistors close to USB XCVR.

Two 0.22 0201 Ceramic Caps are substituted for each Xilinx recommended 0.47 0402 Ceramic Caps.

Floating Avcc pin 32 was connected to +3V3_USB_A for Rev B

Footprint was fixed for Rev B

Diode is used to prevent any current backflow from a Parallel IV cable connection.

FRAGILE, USE SHUNTS ONLY

Optional Switch 2 was removed for Rev B

Route in a similar scheme to the example in the data sheet.

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Title: Sheet 8 - Power / USB JTAG

Size:	Document Number:	Rev:
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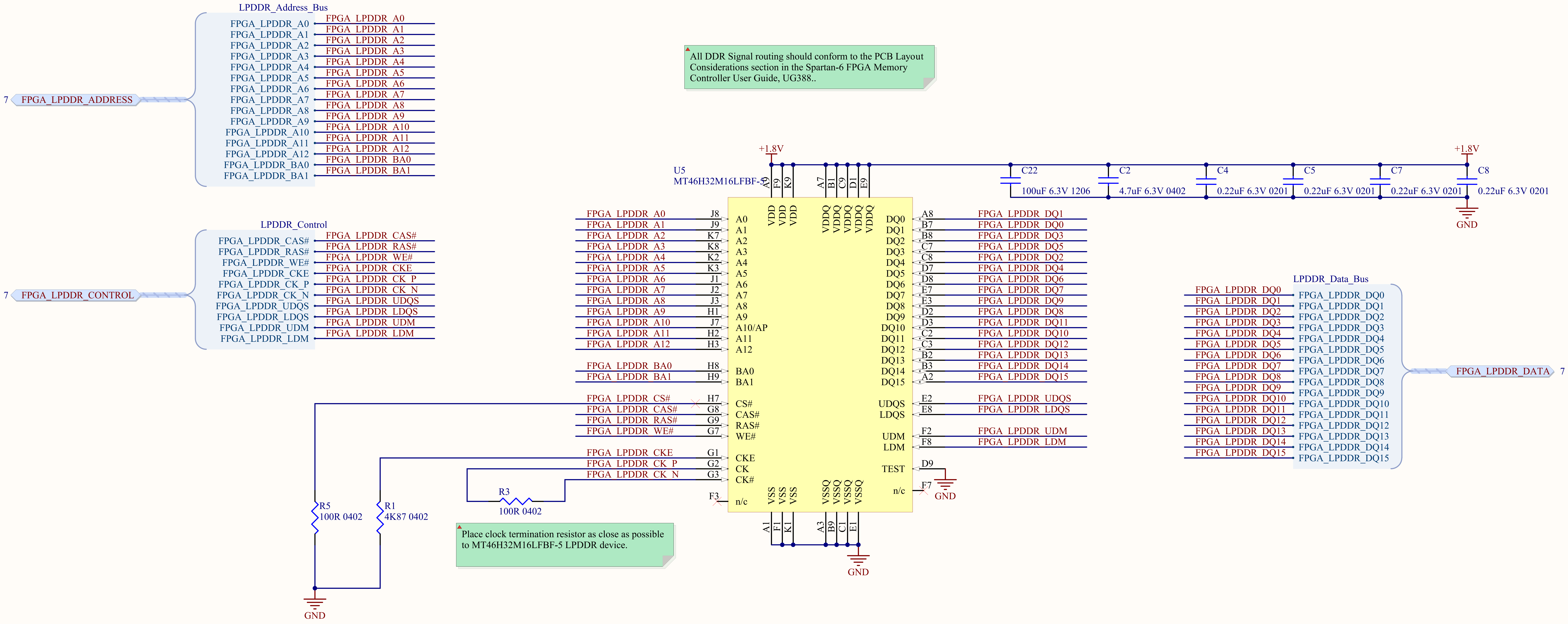

All DDR Signal routing should conform to the PCB Layout Considerations section in the Spartan-6 FPGA Memory Controller User Guide, UG388..

Place clock termination resistor as close as possible to MT46H32M16LFBF-5 LPDDR device.

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Title: **Sheet 9 - LPDDR Memory**

Size: B
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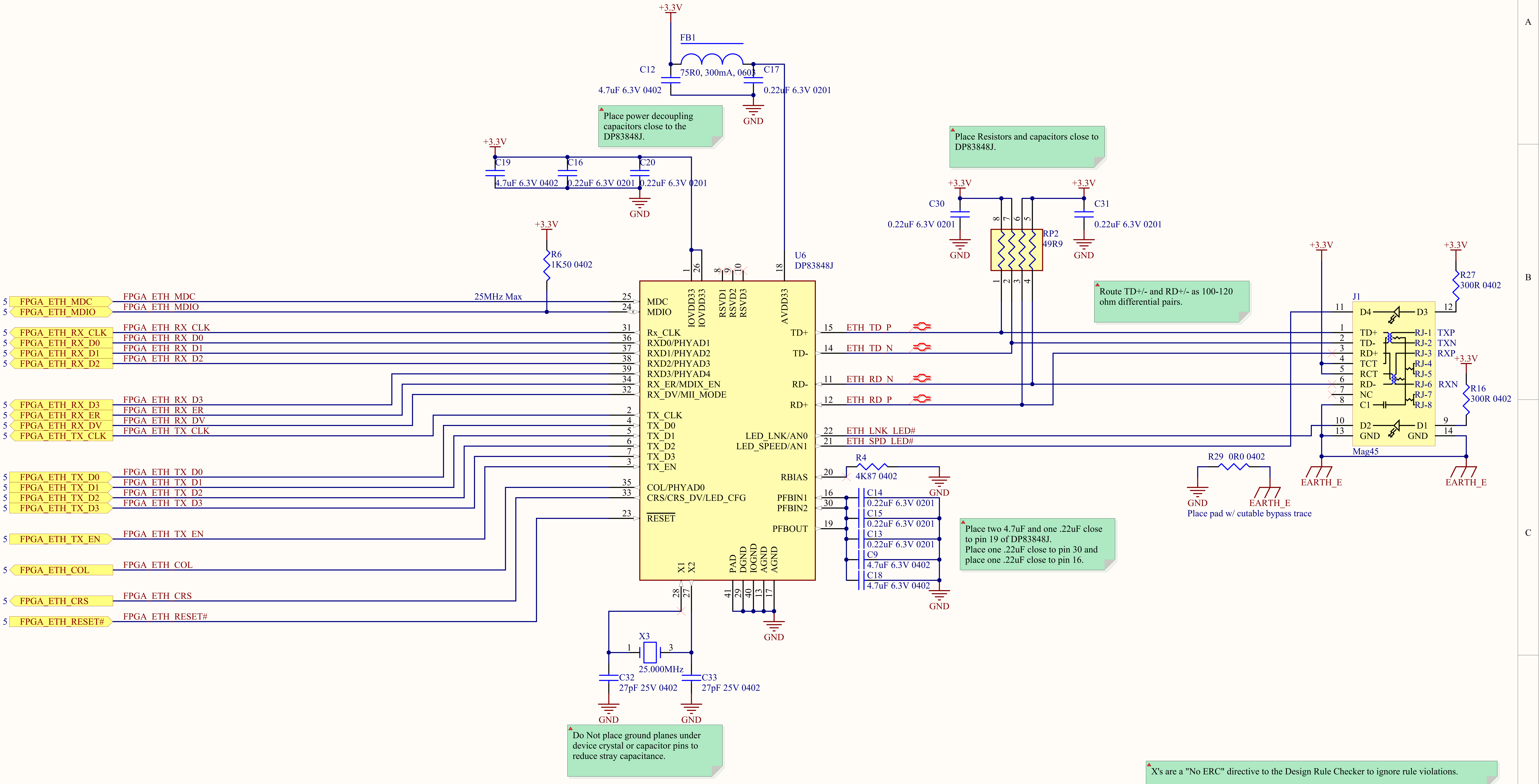

Place power decoupling capacitors close to the DP83848J.

Place Resistors and capacitors close to DP83848J.

Route TD+/- and RD+/- as 100-120 ohm differential pairs.

Place two 4.7uF and one .22uF close to pin 19 of DP83848J.
Place one .22uF close to pin 30 and place one .22uF close to pin 16.

Place pad w/ cutable bypass trace

Do Not place ground planes under device crystal or capacitor pins to reduce stray capacitance.

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Title: Sheet 10 - FPGA 10/100 Ethernet PHY
Size: B
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