Noisy Quantum Computing
116037

Assignment 1

Aviv Azran
201325792

Contents

1 Introduction

building the circuits under specific depth requirements isn't such an easy task since the circuits are being transpiled by IBM code before running on actual devices. There are numerous reasons for that such as the geometry of each device, which dictates the way a certain gate is being implemented.

each device has a specific universal set of gates and thus, a circuit consisting ONLY of the gates present in its set will be (under certain conditions) transpiled as at was designed, while on a different device, it will be transpiled to a version which consists of the device's set of gates.

Another thing which impacts the traspiled circuit is the presence of gate sequences which can be written simply as the identity operator I .

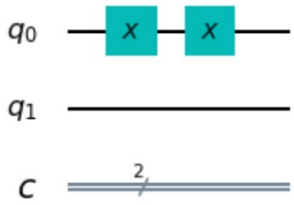
those Sequences appear to be deleted completely in the transpiled version of the circuit.

let's see an example:

1.1 Disappearing gate sequence example

We will take the following simple sequence:

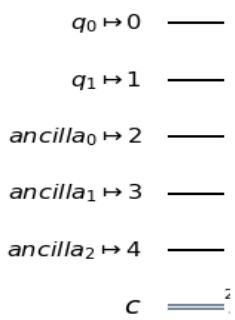
$$XX = I$$



using qiskit command `depth()` allows us to get the depth of the circuit.

```
dagger_example depth is:2'
```

Now we'll have a look at the the transpiled circuit, which can be generated using `transpile(circuit,backend)` where `backend` represents the device used (and thus, the function is bound to return a different circuit for devices constructed differently).



And if we use the `depth()` function again…

```
'dagger_example_transpiled depth is:0'
```

Moreover, the a device's geometry is a crucial attribute to take into consideration when designing a circuit as we will see in the upcoming designs. To conclude, in order the construct a circuit which will enable us to REALLY witness the the effects of noise, dephasing or any other phenomenon arise of physical limitations, we must first achieve a circuit design which will be transpiled into a circuit which still the depth demand. In the upcoming sections we will build circuits based on "weak spots" found in the analysis of the error-geometry diagrams of the devices.

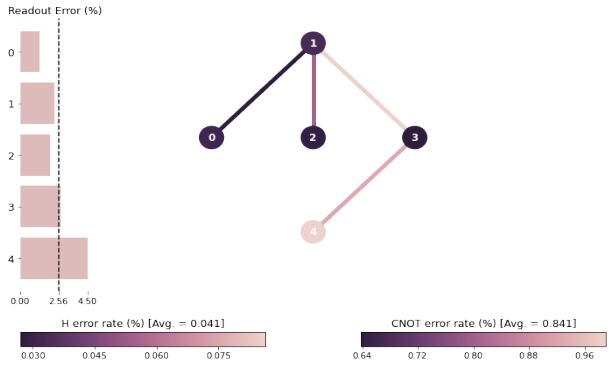
2 Devices and analysis

I've chosen the following devices:

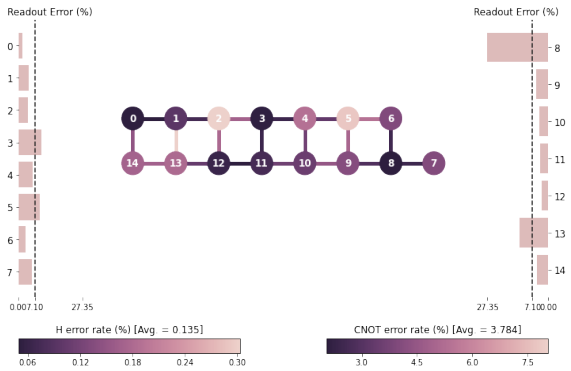
1. ibmq_16_melbourne - (16 qubits)
1. ibmq_ourense - (5 qubits)

Geometry and error rate

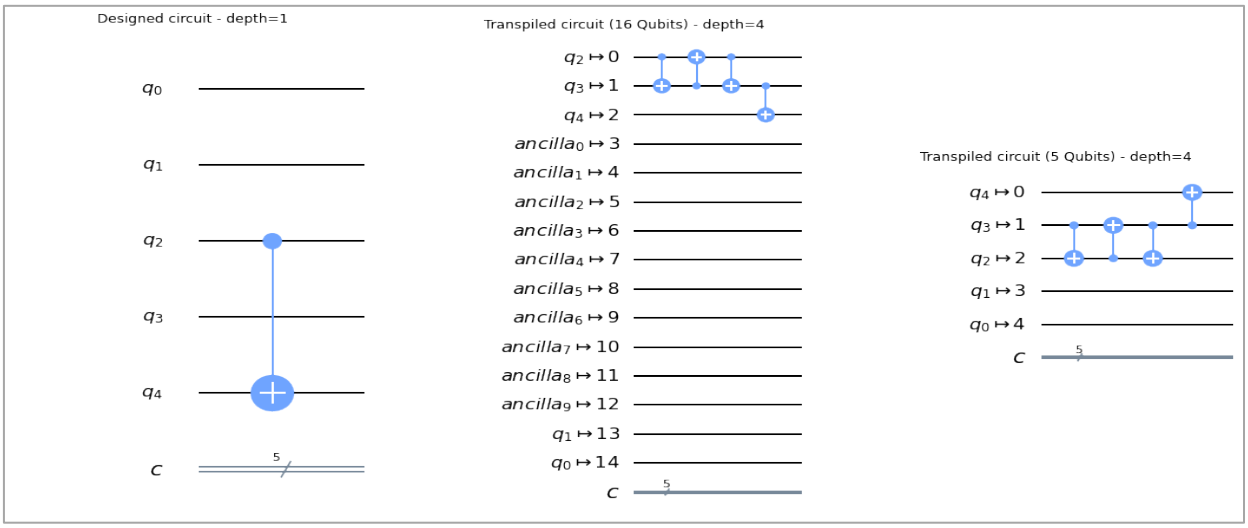
ibmq_ourense Error Map



ibmq_16_melbourne Error Map

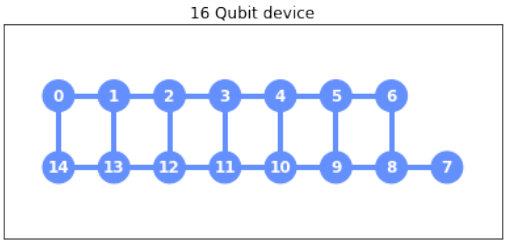


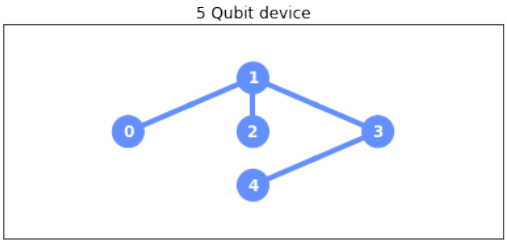
Examining the devices geometry, can see that for both devices, interactions between *q2* and *q4* for example aren't direct. it is achieved by interacting with the qubits that are directly connected with each other. the meaning is that applying CNOT with *q2* and *q4* as control and target can't be implemented directly. let's build a circuit to show this.



3 Circuits

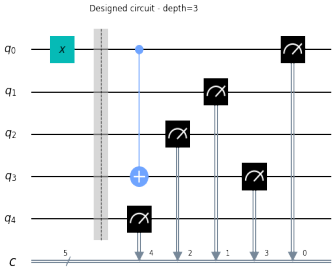
Knowing the above and taking the relatively high error rate of the CNOT gate into account, suggests that we can use the gate we used above to construct a circuit with high sensitivity to errors and noise. Taking the transpilation matter into account, we'll try to overcome the depth difference between different devices by constructing circuits which will be transpiled into circuits with the same depth for both 5 and 16 qubits devices. This is achieved by examining the coupling diagrams of the devices.

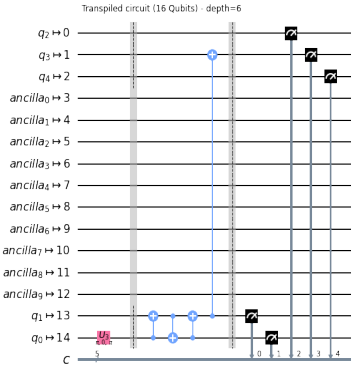


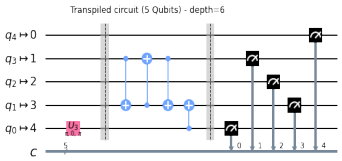


For each of the two circuits we will use qubits featuring the same distance from each other to preserve the depth

3.1 Deep circuit





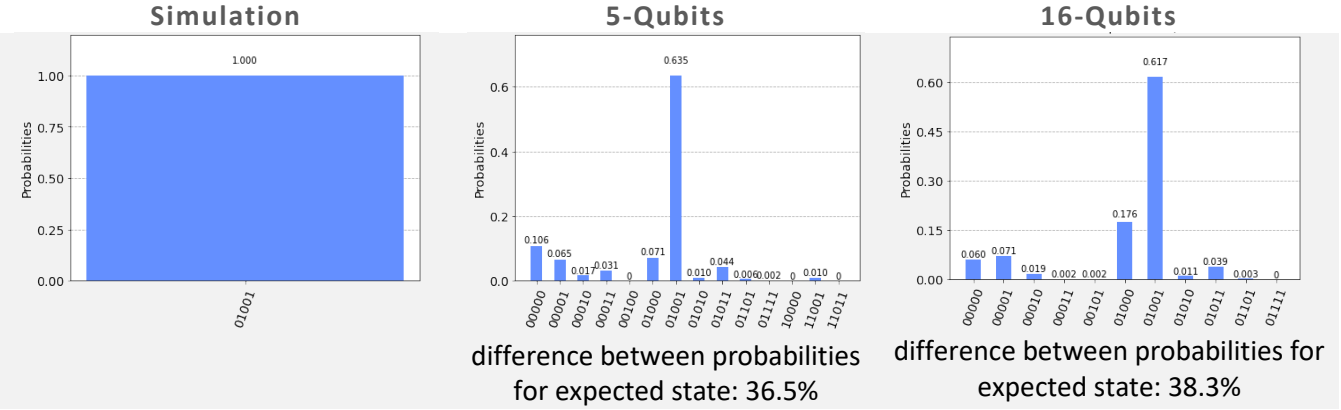


3.1.1 Theoretical calculation

For an initial quantum state $|\psi_0\rangle = |00000...0\rangle$, the state after gate X is $|\psi_0\rangle = |10000...0\rangle$.

After the CNOT gate, $|\psi_0\rangle = |10010...0\rangle$

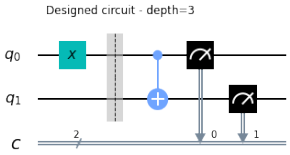
3.1.2 Results

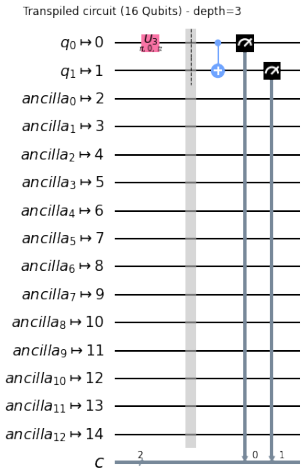


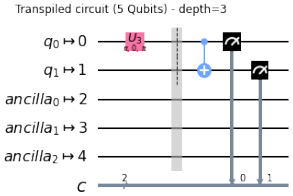
difference between probabilities for expected state: 36.5%

difference between probabilities for expected state: 38.3%

3.2 Shallow circuit





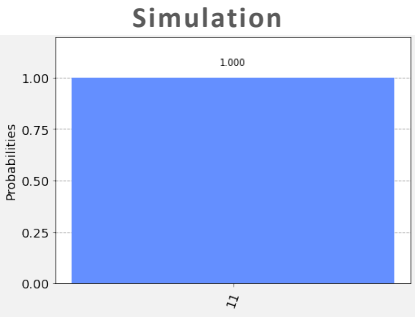


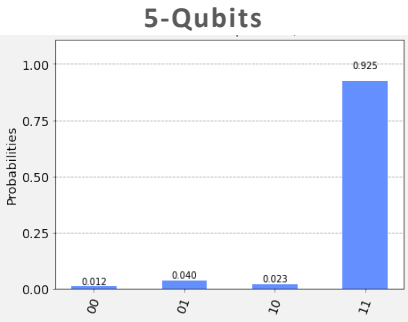
3.2.1 Theoretical calculation

For an initial quantum state $|\psi_0\rangle = |00000...0\rangle$, the state after gate X is $|\psi_0\rangle = |10000...0\rangle$.

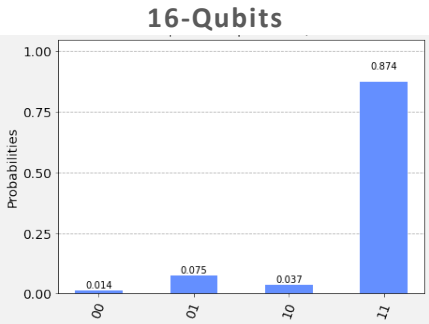
After the CNOT gate, $|\psi_0\rangle = |11000...0\rangle$

3.2.2 Results





difference between probabilities for expected state: 7.5%



difference between probabilities for expected state: 12.6%

4 Conclusion

In this assignment we designed two circuits, each of different depth, and compared their output when running on 3 different platforms: simulator, 5 qubit device and 16 qubit device. We saw that the devices differ of each other in a few aspects such as the qubits coupling, the gates used to implement operations, T1, T2 times (which we haven't discussed about here) and more. By observing the coupling diagrams, we constructed circuits which hold the depth requirements even after the transpilation process, allowing us to bypass the issue of bad correlation between the designed and transpiled circuits. We used CNOT based operations for the circuits, since those feature high error rate with respect to other gates.

We saw that depth difference between the design and the transpilation was 3 for a single use of CNOT. The 5-qubit device produced a high error of 36.5% relative to the simulation, while the 16-qubit device produced 38.3% error

4.1 Deep circuit

We saw that depth difference between the design and the transpilation was 3 for a single use of CNOT. The 5-qubit device produced a high error of 36.5% relative to the simulation, while the 16-qubit device produced 38.3% error.

4.2 Shallow circuit

depth value of 3 achieved across both devices and matched the initial design. for the 5-qubit device we got 7.5% error relative to the simulation. much better than we got for the deep circuit. Yet, for the 16-qubit device we got an error of 12.6% relative to simulation

4.3 Summary

We saw that for both circuits, the 16-qubit device produced results with higher error compared to simulation and 5-qubits device. we can deduce that this is due to the qubits influencing each other, and thus, more qubits mean more influence. In addition, the environmental noise is also to be considered in future analysis.

Note: difference between devices also arise of the different implementation of the same unitary operation on a single qubit, but since we were asked to construct only two circuits with depth demands, I have decided not to address the issue here.