

bq30z50-R1 and bq30z55-R1

Technical Reference



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Preface

Read this First

This manual discusses the modules and peripherals of the bq30z50-R1 and bq30z55-R1 devices, and how each is used to build a complete battery pack gas gauge and protection solution.

Notational Conventions

The following notation is used, if SBS commands and data flash values are mentioned within a text block:

- SBS commands are set in italic; for example, *Voltage*.
- SBS bits and flags are capitalized, set in italic and enclosed with square brackets; for example, [*TCA*].
- Data flash values are set in bold italic; for example, ***CUV Threshold***.
- All data flash bits and flags are capitalized, set in bold italic and enclosed with square brackets, for example, [***NR***].

All SBS commands, data flash values, and flags mentioned in a chapter are listed at the end of each chapter for reference.

The reference format for SBS commands is: SBS:Command Name(Command No.):Manufacturer Access(MA No.)[Flag], for example:

SBS:Voltage(0x09), or SBS:ManufacturerAccess(0x00):Seal Device(0x0020)

The reference format for data flash values is: DF:Class Name:Subclass Name(Subclass ID):Value Name(Offset)[Flag], for example:

DF:1st Level Safety:Voltage(576):CUV Threshold(13), or

DF:ChargeControl:ChargingFaults(482)Charge Fault Cfg(8)[OC].

Introduction

The bq30z50-R1 and bq30z55-R1 device provides a feature-rich gas gauging solution for 2-series cell to 4-series cell battery-pack applications. The device has extended capabilities, including:

- SBS Data Updates Every 250 ms; Values Are Filtered, Not Averaged
- Unseal via Authentication with Keys in IF, Enhanced Security
- Advanced Impedance Track Algorithm v3.75 with Cell Balancing During Rest
- Fast Host-Side Calibration
- Fast Qmax Learning
- Independent Function Enable/Disable: FET, IT, BB, LT, PF, FUSE, LED
- Cell and FET Temperature Configuration Options and up to Five Independently Selectable Sources for Each Option
- Manufacturer Access Commands for Test: Fuse, FET, LED, Toggle
- Extended Lifetimes Tracking
- Black Box Recorder

Calibration

2.1 Overview

The device has integrated routines that support calibration of current, voltage, and temperature readings, accessible after writing 0xF080 to 0xF082 to **ManufacturerAccess()**. When the calibration routines are activated, the **ManufacturerStatus()**[CAL] flag is set, and raw ADC data is available on **ManufacturerData()**.

| ManufacturerAccess() | Description |
|-----------------------------|--|
| 0xF02d | Enable/Disable Calibration mode in ManufacturingStatus() |
| 0xF080 | Disable raw ADC data output on ManufacturerData() |
| 0xF081 | Output raw ADC data of voltage, current, and temperature on ManufacturerData() |
| 0xF082 | Output raw ADC data of voltage, current, and temperature on ManufacturerData() . This mode includes a shunt of the coulomb counter input. |

The **ManufacturerData()** output format is:
ZZYYaaAAabbBBccCCddDDeeEEffFFggGGhhHHiiiJJkkKKllLL,

where:

| Value | Format | Description |
|--------------|---------------|---|
| ZZ | byte | 8-bit counter, increments when raw ADC values are refreshed, typically every 250 ms |
| YY | byte | Output status ManufacturerAccess() = 0xF081: 1 ManufacturerAccess() = 0xF082: 2 |
| AAaa | 2's comp | ManufacturerAccess() = 0xF081: coulomb counter ManufacturerAccess() = 0xF082: internal shorted coulomb counter |
| BBbb | 2's comp | Cell Voltage 1 |
| CCcc | 2's comp | Cell Voltage 2 |
| DDdd | 2's comp | Cell Voltage 3 |
| EEee | 2's comp | Cell Voltage 4 |
| FFff | 2's comp | Internal temperature sensor |
| GGgg | 2's comp | Temperature Sensor 1 |
| HHhh | 2's comp | Temperature Sensor 2 |
| IIii | 2's comp | Temperature Sensor 3 |
| JJjj | 2's comp | Temperature Sensor 4 |
| KKkk | 2's comp | PACK Voltage |
| LLll | 2's comp | BAT Voltage |

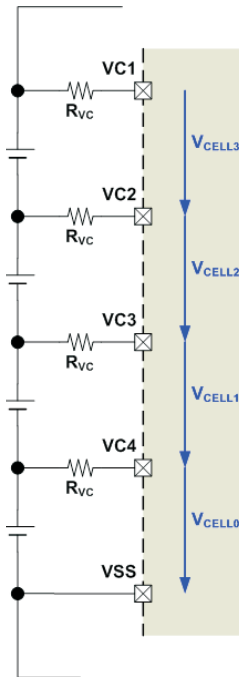
2.2 Combining Calibrations

Calibrations can be combined to shorten calibration time. Calibration times under four seconds are achievable using this method.

Table 2-1. Combining Calibrations

| Time (s) | ZZ in ManufacturerData() | Action |
|----------|--------------------------|--|
| 0 | N | <ul style="list-style-type: none"> Read DF values Apply 0 mA current Apply cell voltages Apply known temperature ManufacturerAccess() = 0xF082 Poll ManufacturerData() for ZZ increment |
| 0.25 | N + 1 | <ul style="list-style-type: none"> Poll ManufacturerData() for ZZ increment |
| 0.5 | N + 2 | <ul style="list-style-type: none"> Store ManufacturerData() block 1 Poll ManufacturerData() for ZZ increment |
| 0.75 | N + 3 | <ul style="list-style-type: none"> Store ManufacturerData() block 2 Poll ManufacturerData() for ZZ increment |
| 1 | N + 4 | <ul style="list-style-type: none"> Store ManufacturerData() block 3 Poll ManufacturerData() for ZZ increment |
| 1.25 | N + 5 | <ul style="list-style-type: none"> Store ManufacturerData() block 4 Apply Pack Voltage ManufacturerAccess() = 0xF081 Poll ManufacturerData() for ZZ increment |
| 1.5 | N + 6 | <ul style="list-style-type: none"> Poll ManufacturerData() for ZZ increment |
| 1.75 | N + 7 | <ul style="list-style-type: none"> Store ManufacturerData() block 5 Poll ManufacturerData() for ZZ increment |
| 2 | N + 8 | <ul style="list-style-type: none"> Store ManufacturerData() block 6 Poll ManufacturerData() for ZZ increment |
| 2.25 | N + 9 | <ul style="list-style-type: none"> Store ManufacturerData() block 7 Poll ManufacturerData() for ZZ increment |
| 2.5 | N + 10 | <ul style="list-style-type: none"> Store ManufacturerData() block 8 Apply calibration current Poll ManufacturerData() for ZZ increment |
| 2.75 | N + 11 | <ul style="list-style-type: none"> Poll ManufacturerData() for ZZ increment |
| 3 | N + 12 | <ul style="list-style-type: none"> Store ManufacturerData() block 9 Poll ManufacturerData() for ZZ increment |
| 3.25 | N + 13 | <ul style="list-style-type: none"> Store ManufacturerData() block 10 Poll ManufacturerData() for ZZ increment |
| 3.5 | N + 14 | <ul style="list-style-type: none"> Store ManufacturerData() block 11 Poll ManufacturerData() for ZZ increment |
| 3.75 | N + 15 | <ul style="list-style-type: none"> Store ManufacturerData() block 12 Calculate CC Offset using blocks 1 to 4 Calculate board Offset using blocks 5 to 8 Calculate current gain using blocks 9 to 12 Calculate Cell Voltage 1–4 using blocks 1 to 4 Calculate Pack Voltage using blocks 5 to 8 Calculate Temperatures using blocks 5 to 8 Write values to data flash |

2.3 Cell Voltage Calibration



1. Apply known voltages in mV to the cell voltage inputs:
 - V_{CELL0} between VC4 pin and VSS pin
 - V_{CELL1} between VC3 pin and VC4 pin
 - V_{CELL2} between VC2 pin and VC3 pin
 - V_{CELL3} between VC1 pin and VC2 pin
2. Send 0xF081 or 0xF082 to **ManufacturerAccess()** to enable raw cell voltage output on **ManufacturerData()**.
3. Poll **ManufacturerData()** until ZZ increments by 2 before reading data.
4. Grab the ADC conversion readings of cell voltages from **ManufacturerData()**:
 - ADC_{CELL0} = AAaa of **ManufacturerData()**, is $ADC_{CELL0} < 0x8000$? If yes, use ADC_{CELL0} ; otherwise, $ADC_{CELL0} = AAaa - 0xFFFF + 0x0001$
 - ADC_{CELL1} = BBbb of **ManufacturerData()**, is $ADC_{CELL1} < 0x8000$? If yes, use ADC_{CELL1} ; otherwise, $ADC_{CELL1} = BBbb - 0xFFFF + 0x0001$
 - ADC_{CELL2} = CCCC of **ManufacturerData()**, is $ADC_{CELL2} < 0x8000$? If yes, use ADC_{CELL2} ; otherwise, $ADC_{CELL2} = CCCC - 0xFFFF + 0x0001$
 - ADC_{CELL3} = DDdd of **ManufacturerData()**, is $ADC_{CELL3} < 0x8000$? If yes, use ADC_{CELL3} ; otherwise, $ADC_{CELL3} = DDdd - 0xFFFF + 0x0001$
5. Average several readings for higher accuracy. Poll **ManufacturerData()** until ZZ increments, which indicates updated values.
6. Calculate gain values:

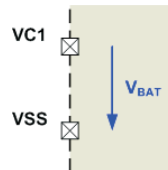
$$Cell\ Scale\ 0 = \frac{V_{CELL0}}{ADC_{CELL0}} * 2^{16}$$

$$Cell\ Scale\ 1 = \frac{V_{CELL0} + V_{CELL1}}{ADC_{CELL0} + ADC_{CELL1}} * 2^{16} \quad Cell\ Scale\ 2 = \frac{V_{CELL0} + V_{CELL1} + V_{CELL2}}{ADC_{CELL0} + ADC_{CELL1} + ADC_{CELL2}} * 2^{16}$$

$$Cell\ Scale\ 3 = \frac{V_{CELL0} + V_{CELL1} + V_{CELL2} + V_{CELL3}}{ADC_{CELL0} + ADC_{CELL1} + ADC_{CELL2} + ADC_{CELL3}} * 2^{16}$$
7. Update the data flash with Cell Scale 0, Cell Scale 1, Cell Scale 2, Cell Scale 3.

8. Re-check the voltage reading. Repeat the steps if the readings are not accurate.

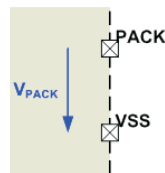
2.4 BAT Voltage Calibration



1. Apply known voltages in mV to the voltage input:
 - V_{BAT} between VC4 pin and VSS pin
2. Enter calibration mode if **ManufacturerStatus()**[CAL] = 0, send 0x002D to **ManufacturerAccess()**
3. Send 0xF081 or 0xF082 to **ManufacturerAccess()** to enable raw cell voltage output on **ManufacturerData()**.
4. Poll **ManufacturerData()** until ZZ increments by 2 before reading data.
5. Grab ADC conversion readings of cell stack voltage from **ManufacturerData()**:
 - $ADC_{BAT} = \text{LLII of } \mathbf{ManufacturerData()}$, is $ADC_{BAT} < 0x8000$? If yes use ADC_{BAT} , otherwise $ADC_{BAT} = \text{LLII} - 0xFFFF - 0x0001$
6. To average several readings for higher accuracy, poll **ManufacturerData()** until ZZ increments, which indicates updated values.
 - $ADC_{BAT} = [ADC_{BAT}(\text{reading } n) + \dots + ADC_{BAT}(\text{reading } 1)]/n$
7. Calculate gain value:

$$BAT \text{ Gain} = \frac{V_{BAT}}{ADC_{BAT}} * 2^{16}$$
8. Update data flash with **BAT Gain**.
9. Re-check the voltage reading, and repeat steps if the readings are not accurate.
10. Exit calibration mode by sending 0x002D to **ManufacturerAccess()** or continue with calibration.

2.5 PACK Voltage Calibration

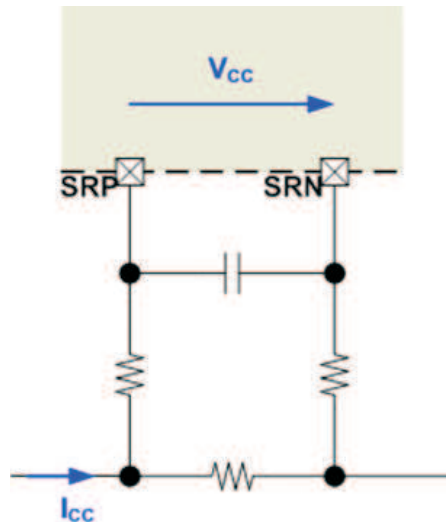


1. Apply known voltages in mV to the voltage input:
 - V_{PACK} between PACK pin and VSS pin
2. Enter calibration mode if **ManufacturerStatus()**[CAL] = 0, send 0x002D to **ManufacturerAccess()**.
3. Send 0xF081 or 0xF082 to **ManufacturerAccess()** to enable raw cell voltage output on **ManufacturerData()**.
4. Poll **ManufacturerData()** until ZZ increments by 2 before reading data.
5. Grab ADC conversion readings of pack voltage from **ManufacturerData()**:
 - $ADC_{PACK} = \text{KKkk of } \mathbf{ManufacturerData()}$, is $ADC_{PACK} < 0x8000$? If yes, use ADC_{PACK} , otherwise $ADC_{PACK} = \text{KKkk} - 0xFFFF - 0x0001$.
6. To average several readings for higher accuracy, poll **ManufacturerData()** until ZZ increments, which indicates updated values.
 - $ADC_{PACK} = [ADC_{PACK}(\text{reading } n) + \dots + ADC_{PACK}(\text{reading } 1)]/n$
7. Calculate gain value:

$$PACK\ Gain = \frac{V_{PACK}}{ADC_{PACK}} * 2^{16}$$

8. Update data flash with **PACK Gain**.
9. Re-check voltage reading; repeat Steps 4 to 6 if readings are not accurate.
10. Exit calibration mode by sending 0x002D to **ManufacturerAccess()** or continue with calibration.

2.6 Current Calibration



2.6.1 Offset Calibration

1. Apply a known current of 0 mA:
 - Make sure no current is flowing through the sense resistor connected between the SRP and SRN pins.
2. Send 0xF082 to **ManufacturerAccess()** to enable raw CC output on **ManufacturerData()** with CC shunt.
3. Read *Coulomb Counter Offset Samples* from data flash.
4. Poll **ManufacturerData()** until ZZ increments by 2 before reading data.
5. Grab the ADC conversion readings of current from **ManufacturerData()**:
 - $ADC_{CC} = AAaa$ of **ManufacturerData()**, is $ADC_{CC} < 0x8000$? If yes, use ADC_{CC} ; otherwise, $ADC_{CC} = AAaa - 0xFFFF - 0x0001$.
6. To average several readings for higher accuracy, poll **ManufacturerData()** until ZZ increments, which indicates updated values.
 - $ADC_{CC} = [ADC_{CC}(\text{reading } n) + \dots + ADC_{CC}(\text{reading } 1)]/n$
7. Calculate offset value:

$$CC_{offset} = ADC_{CC} * (Coulomb\ Counter\ Offset\ Samples)$$
8. Update the data flash with CC Offset.
9. Re-check the current reading. Repeat the steps if the readings are not accurate.

2.6.2 Board Offset Calibration

1. Apply a known current of 0 mA:
 - Make sure no current is flowing through the sense resistor connected between SRP pin and SRN pin.
2. Send 0xF081 to **ManufacturerAccess()** to enable raw CC output on **ManufacturerData()**.
3. Read *Coulomb Counter Offset Samples* from data flash.

4. Poll **ManufacturerData()** until ZZ increments by 2 before reading data.
5. Grab the ADC conversion readings of current from **ManufacturerData()**:
 - $ADC_{CC} = \text{AAaa of } \mathbf{ManufacturerData()}$, is $ADC_{CC} < 0x8000$? If yes, use ADC_{CC} ; otherwise, $ADC_{CC} = \text{AAaa} - 0xFFFF - 0x0001$.
6. To average several readings for higher accuracy, poll **ManufacturerData()** until ZZ increments, which indicates updated values.
 - $ADC_{CC} = [ADC_{CC}(\text{reading } n) + \dots + ADC_{CC}(\text{reading } 1)]/n$
7. Calculate offset value:

$$\text{Board offset} = (ADC_{CC} - CC \text{ Offset} / (\text{Coulomb Counter Offset Samples})) * (\text{Coulomb Counter Offset Samples})$$
8. Update the data flash with *Board Offset*.
9. Re-check the current reading. Repeat the steps if the readings are not accurate.

2.6.3 Gain Calibration

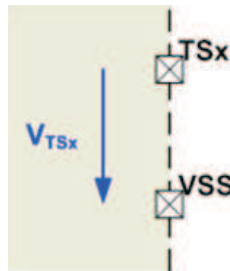
1. Apply a known current in mA to the current input.
 - Make sure current I_{CC} is flowing through the sense resistor connected between SRP pin and SRN pin.
2. Send 0xF081 to **ManufacturerAccess()** to enable raw CC output on **ManufacturerData()**.
3. Read *Coulomb Counter Offset Samples* from data flash.
4. Poll **ManufacturerData()** until ZZ increments by 2 before reading data.
5. Grab the ADC conversion readings of current from **ManufacturerData()**:
 - $ADC_{CC} = \text{AAaa of } \mathbf{ManufacturerData()}$, is $ADC_{CC} < 0x8000$? If yes, use ADC_{CC} ; otherwise, $ADC_{CC} = \text{AAaa} - 0xFFFF - 0x0001$.
6. To average several readings for higher accuracy, poll **ManufacturerData()** until ZZ increments, which indicates updated values.
 - $ADC_{CC} = [ADC_{CC}(\text{reading } n) + \dots + ADC_{CC}(\text{reading } 1)]/n$
7. Calculate gain values:

$$CC \text{ Gain} = \frac{I_{CC}}{(Board \text{ Offset}) + (CC \text{ Offset})}$$

$$ADC_{CC} - \frac{ADC_{CC}}{(\text{Coulomb Counter Offset Samples})}$$

$$Capacity \text{ Gain} = CC \text{ Gain} * 298261.6178$$
8. Update the data flash with CC Gain, *Capacity Gain*.
9. Re-check the current reading. Repeat the steps if the readings are not accurate.

2.7 Temperature Calibration



2.7.1 Internal Temperature Sensor Calibration (Option 1)

1. Apply a known temperature in 0.1°C.
 - Make sure temperature Temp_{TINT} is applied to the device.
2. Enable TINT as the SBS temperature source by setting the Misc Configuration bit 7 to 1.

3. Grab the reported temperature from the SBS temperature.
4. Calculate temperature offset:

$$TINT\ offset = TEMP_{TINT} - TINT + TINT\ offset_{old}$$
5. Update the data flash with the calculated value.
6. Re-check the current reading. Repeat the steps if the readings are not accurate.

2.7.2 Internal Temperature Sensor Calibration (Option 2)

1. Apply a known temperature in 0.1°C.
 - Make sure temperature Temp_{TINT} is applied to the device.
2. Read *Int Coeff 1*, *Int Coeff 2*, *Int Coeff 3*, *Int Coeff 4* from data flash.
3. Send 0xF081 or 0xF082 to **ManufacturerAccess()** to enable raw cell voltage output on **ManufacturerData()**.
4. Poll **ManufacturerData()** until ZZ increments by 2 before reading data.
5. Grab the ADC conversion readings of temperature from **Temperature()**:
 - ADC_{TINT} = FFff of **ManufacturerData()**, is ADC_{INT} < 0x8000? If yes, use ADC_{TINT}; otherwise, ADC_{TINT} = FFff – 0xFFFF – 0x0001.
6. To average several readings for higher accuracy, poll **ManufacturerData()** until ZZ increments, which indicates updated values.
 - ADC_{TINT} = [ADC_{TINT}(reading n) + ... + ADC_{TINT}(reading 1)]/n
7. Calculate temperature offset:

$$A = ADC_{TINT} / 2^{16}$$

$$T_{TINT} = ((INT\ Coeff\ 1) * A^3 + (INT\ Coeff\ 2) * A^2 + (INT\ Coeff\ 3) * A + (INT\ Coeff\ 4)) * 0.1 - 273.15$$

$$Internal\ Temperature\ Offset = TEMP_{TINT} - T_{TINT}$$
8. Update the data flash with the *Internal Temperature Offset*.
9. Re-check the temperature reading. Repeat the steps if the readings are not accurate.

2.7.3 TS1 Calibration (Option 1)

1. Apply a known temperature in 0.1°C.
 - Make sure temperature Temp_{TS1} is applied to the thermistor connected to the TS1 pin.
2. Enable TS1 as the SBS temperature source by setting the Misc Configuration bit 7 to 0.
3. Grab the reported temperature from the SBS temperature.
4. Calculate the temperature offset:

$$TS1\ offset = TEMP_{TS1} - TS1 + TS1\ offset_{old}$$
5. Update the data flash with the calculated value.
6. Re-check the current reading. Repeat the steps if the readings are not accurate.

2.7.4 TS1 Calibration (Option 2)

1. Apply a known temperature in 0.1°C.
 - Make sure temperature Temp_{TS1} is applied to the thermistor connected to the TS1 pin.
2. Read Coeff a1, Coeff a2, Coeff a3, Coeff a4, Coeff b1, Coeff b2, Coeff b3, Coeff b4 from data flash.
3. Send 0xF081 or 0xF082 to **ManufacturerAccess()** to enable raw cell voltage output on **ManufacturerData()**.
4. Poll **ManufacturerData()** until ZZ increments by 2 before reading data.
5. Grab the ADC conversion readings of temperature from **ManufacturerData()**:
 - ADC_{TS1} = GGgg of **ManufacturerData()**, is ADC_{TS1} < 0x8000? If yes, use ADC_{TS1}; otherwise, ADC_{TS1} = GGgg – 0xFFFF – 0x0001.
6. To average several readings for higher accuracy, poll **ManufacturerData()** until ZZ increments, which

indicates updated values.

$$\bullet \quad \text{ADC}_{\text{TS1}} = [\text{ADC}_{\text{TS1}}(\text{reading } n) + \dots + \text{ADC}_{\text{TS1}}(\text{reading } 1)]/n$$

7. Calculate temperature offset:

$$A = \frac{\text{ADC}_{\text{TS1}}}{2^{15}}$$

$$B = \frac{A}{(\text{Coeff } A1) * A^4 + (\text{Coeff } A2) * A^3 + (\text{Coeff } A3) * A^2 + (\text{Coeff } A4) * A + (\text{Coeff } A5)} * 2^{14}$$

$$T_{\text{TS1}} = ((\text{Coeff } B1) * B^3 + (\text{Coeff } B2) * B^2 + (\text{Coeff } B3) * B^1 + (\text{Coeff } B4)) * 0.1 - 273.15$$

$$\text{External1 Temperature Offset} = \text{TEMP}_{\text{TS1}} - T_{\text{TS1}}$$

8. Update the data flash with the calculated *External 1 Temperature Offset*.
9. Re-check the temperature reading. Repeat the steps if the readings are not accurate.

2.7.5 TS2 Calibration (Option 1)

1. Apply a known temperature in 0.1°C.
 - Make sure temperature Temp_{TS2} is applied to the thermistor connected to the TS2 pin.
2. Enable TS2 by setting the Secondary Thermistor to 1.
3. Grab the reported temperature from the extended command 0x7D.
4. Calculate temperature offset:

$$\text{TS2 offset} = \text{TEMP}_{\text{TS2}} - \text{TS2} + \text{TS2 offset}_{\text{old}}$$
5. Update the data flash with the calculated value.
6. Re-check the current reading. Repeat the steps if the readings are not accurate.

2.7.6 TS2 Calibration (Option 2)

1. Apply a known temperature in 0.1°C.
 - Make sure temperature Temp_{TS2} is applied to the thermistor connected to the TS2 pin.
2. Read Coeff a1, Coeff a2, Coeff a3, Coeff a4, Coeff b1, Coeff b2, Coeff b3, Coeff b4 from data flash based on TS2 configuration to cell or FET temperature.
3. Poll **ManufacturerData()** until ZZ increments by 2 before reading data.
4. Grab ADC conversion readings of temperature from **ManufacturerData()**:
 - $\text{ADC}_{\text{TS2}} = \text{HHhh of } \text{ManufacturerData}()$, is $\text{ADC}_{\text{TS2}} < 0x8000$? If yes use ADC_{TS2} , otherwise $\text{ADC}_{\text{TS2}} = -(0xFFFF - \text{HHhh} + 0x0001)$
5. To average several readings for higher accuracy, poll **ManufacturerData()** until ZZ increments, which indicates updated values.
 - $\text{ADC}_{\text{TS2}} = [\text{ADC}_{\text{TS2}}(\text{reading } n) + \dots + \text{ADC}_{\text{TS2}}(\text{reading } 1)]/n$

6. Calculate temperature offset:

$$A = \frac{\text{ADC}_{\text{TS2}}}{2^{15}}$$

$$B = \frac{A}{(\text{Coeff } A1) * A^4 + (\text{Coeff } A2) * A^3 + (\text{Coeff } A3) * A^2 + (\text{Coeff } A4) * A + (\text{Coeff } A5)} * 2^{14}$$

$$T_{\text{TS2}} = ((\text{Coeff } B1) * B^3 + (\text{Coeff } B2) * B^2 + (\text{Coeff } B3) * B^1 + (\text{Coeff } B4)) * 0.1 - 273.15$$

$$\text{External 2 Temperature Offset} = \text{TEMP}_{\text{TS2}} - T_{\text{TS2}}$$

7. Update the data flash with calculated with **External 2 Temperature Offset**.
8. Re-check the temperature reading. Repeat the steps if the readings are not accurate.

2.7.7 TS3 Calibration (Option 1)

1. Apply a known temperature in 0.1°C
 - Make sure temperature Temp_{TS3} is applied to the thermistor connected to the TS3 pin.
2. Enable TS3 by setting the Secondary Thermistor to 1.
3. Grab the reported temperature from the extended command 0x7D.
4. Calculate temperature offset:

$$TS3\ offset = TEMP_{TS3} - TS3 + TS3\ offset_{old}$$
5. Update the data flash with the calculated value.
6. Re-check the current reading. Repeat the steps if the readings are not accurate.

2.7.8 TS3 Calibration (Option 2)

1. Apply a known temperature in 0.1°C
 - Make sure temperature Temp_{TS3} is applied to the thermistor connected to the TS3 pin.
2. Read Coeff a1, Coeff a2, Coeff a3, Coeff a4, Coeff b1, Coeff b2, Coeff b3, Coeff b4 from data flash based on TS3 configuration to cell or FET temperature.
3. Poll **ManufacturerData()** until ZZ increments by 2 before reading data.
4. Grab ADC conversion readings of temperature from **ManufacturerData()**:
 - ADC_{TS3} = Iiii of **ManufacturerData()**, is ADC_{TS3} < 0x8000? If yes use ADC_{TS3}, otherwise ADC_{TS3} = Iiii – 0xFFFF – 0x0001
5. To average several readings for higher accuracy, poll **ManufacturerData()** until ZZ increments that indicates updates values.
 - $ADC_{TS3} = [ADC_{TS3}(\text{reading } n) + \dots + ADC_{TS3}(\text{reading } 1)]/n$
6. Calculate temperature offset:

$$A = \frac{ADC_{TS3}}{2^{15}}$$

$$B = \frac{A}{(CoeffA1)*A^4 + (CoeffA2)*A^3 + (CoeffA3)*A^2 + (CoeffA4)*A + (CoeffA5)} * 2^{14}$$

$$T_{TS3} = ((CoeffB1)*B^3 + (CoeffB2)*B^2 + (CoeffB3)*B^1 + (CoeffB4))*0.1 - 273.15$$

$$External\ 3\ Temperature\ Offset = TEMP_{TS3} - T_{TS3}$$
7. Update the data flash with calculated with **External 3 Temperature Offset**.
8. Re-check the temperature reading. Repeat the steps if the readings are not accurate.

2.7.9 TS4 Calibration (Option 1)

1. Apply a known temperature in 0.1°C
 - Make sure temperature Temp_{TS4} is applied to the thermistor connected to the TS4 pin.
2. Enable TS4 by setting the Secondary Thermistor to 1.
3. Grab the reported temperature from the extended command 0x7D.
4. Calculate temperature offset:

$$TS4\ offset = TEMP_{TS4} - TS4 + TS4\ offset_{old}$$
5. Update the data flash with the calculated value.
6. Re-check the current reading. Repeat the steps if the readings are not accurate.

2.7.10 TS4 Calibration (Option 2)

1. Apply a known temperature in 0.1°C
 - Make sure temperature Temp_{TS4} is applied to the thermistor connected to the TS4 pin.

2. Read **Coeff a1, Coeff a2, Coeff a3, Coeff a4, Coeff b1, Coeff b2, Coeff b3, Coeff b4** from data flash based on TS4 configuration to cell or FET temperature.
3. Poll **ManufacturerData()** until ZZ increments by 2 before reading data.
4. Grab ADC conversion readings of temperature from **ManufacturerData()**:
 - $ADC_{TS4} = JJjj$ of **ManufacturerData()**, is $ADC_{TS4} < 0x8000$? If yes use ADC_{TS4} , otherwise $ADC_{TS4} = JJjj - 0xFFFF - 0x0001$
5. To average several readings for higher accuracy, poll **ManufacturerData()** until ZZ increments that indicates updates values.
 - $ADC_{TS4} = [ADC_{TS4}(\text{reading } n) + \dots + ADC_{TS4}(\text{reading } 1)]/n$
6. Calculate temperature offset:

$$A = \frac{ADC_{TS4}}{2^{15}}$$

$$B = \frac{A}{(CoeffA1)*A^4 + (CoeffA2)*A^3 + (CoeffA3)*A^2 + (CoeffA4)*A + (CoeffA5)} * 2^{14}$$

$$T_{TS4} = ((Coeff B1)*B^3 + (Coeff B2)*B^2 + (Coeff B3)*B^1 + (Coeff B4))*0.1 - 273.15$$

$$External\ 4\ Temperature\ Offset = TEMP_{TS4} - T_{TS4}$$

7. Update the data flash with calculated with **External 4 Temperature Offset**.
8. Re-check the temperature reading. Repeat the steps if the readings are not accurate.

Protections

3.1 Introduction

All of the protection items can be enabled or disabled under Settings/Enabled Protections 0–15 and Settings/Enabled Protections 16–31.

3.2 Cell Undervoltage Protection

The device can detect undervoltage in batteries and protect cells from damage by preventing further discharge.

| Status | Condition | Action |
|----------|---|--|
| Normal | All Cell voltages in Voltages() > Threshold | <ul style="list-style-type: none"> • SafetyAlert()[CUV] = 0 • BatteryStatus()[TDA] = 0 |
| Alert | Any Cell voltages in Voltages() ≤ Threshold | <ul style="list-style-type: none"> • SafetyAlert()[CUV] = 1 • If not charging, BatteryStatus()[TDA] = 1. |
| Trip | Any Cell voltages in Voltages() continuous ≤ Threshold for Delay duration | <ul style="list-style-type: none"> • SafetyAlert()[CUV] = 0 • SafetyStatus()[CUV] = 1 • BatteryStatus()[FD] = 1 • Discharging is not allowed. |
| Recovery | SafetyStatus()[CUV] = 1 AND All Cell voltages in Voltages() > Recovery AND (CUV_RECOV_CHG = 0 OR (CUV_RECOV_CHG = 1 AND Charging Detected)) | <ul style="list-style-type: none"> • SafetyStatus()[CUV] = 0 • BatteryStatus()[FD] = 0 • Discharging is allowed. |

3.3 Cell Undervoltage Compensated Protection

The device can detect undervoltage in batteries and protect cells from damage by preventing further discharge. The protection is compensated by the **Current()** * **CellResistance4..1**.

| Status | Condition | Action |
|----------|--|---|
| Normal | All Cell voltages in Voltages() – Current() * Cell Resistance > Threshold | <ul style="list-style-type: none"> • SafetyAlert()[CUVC] = 0 • BatteryStatus()[TDA] = 0 |
| Alert | Any Cell voltages in Voltages() – Current() * Cell Resistance ≤ Threshold | <ul style="list-style-type: none"> • SafetyAlert()[CUVC] = 1 • If not charging, BatteryStatus()[TDA] = 1. |
| Trip | Any Cell voltages in Voltages() – Current() * Cell Resistance continuous ≤ Threshold for Delay duration | <ul style="list-style-type: none"> • SafetyAlert()[CUVC] = 0 • SafetyStatus()[CUVC] = 1 • BatteryStatus()[FD] = 1 • BatteryStatus()[TDA] = 0 • Discharging is not allowed. |
| Recovery | SafetyStatus()[CUVC] = 1 AND All Cell voltages in Voltages() > Recovery AND (CUV_RECOV_CHG = 0 OR (CUV_RECOV_CHG = 1 AND Charging Detected)) | <ul style="list-style-type: none"> • SafetyStatus()[CUVC] = 0 • BatteryStatus()[FD] = 0 • Discharging is allowed. |

3.4 Cell Overvoltage Protection

The device can detect cell overvoltage in batteries and protect cells from damage by preventing further charging.

| Status | Condition | Action |
|----------|---|---|
| Normal | Temperature() \leq T2 AND all Cell voltages in Voltages() < Threshold Low Temp | SafetyAlert()[COV] = 0 |
| Normal | T2 < Temperature() \leq T3 AND all Cell voltages in Voltages() < Threshold Standard Temp | SafetyAlert()[COV] = 0 |
| Normal | T3 < Temperature() AND all Cell voltages in Voltages() < Threshold High Temp | SafetyAlert()[COV] = 0 |
| Normal | T5 < Temperature() \leq T6 AND all Cell voltages in Voltages() < Threshold Rec Temp | SafetyAlert()[COV] = 0 |
| Alert | Temperature() \leq T2 AND any Cell voltages in Voltages() \geq Threshold Low Temp | SafetyAlert()[COV] = 1 |
| Alert | T2 < Temperature() \leq T3 AND any Cell voltages in Voltages() \geq Threshold Standard Temp | SafetyAlert()[COV] = 1 |
| Alert | T3 < Temperature() AND any Cell voltages in Voltages() \geq Threshold High Temp | SafetyAlert()[COV] = 1 |
| Alert | T5 < Temperature() \leq T6 AND any Cell voltages in Voltages() \geq Threshold Rec Temp | SafetyAlert()[COV] = 1 |
| Trip | Temperature() \leq T2 AND any Cell voltages in Voltages() continuous \geq Threshold Low Temp for Delay duration | <ul style="list-style-type: none"> SafetyAlert()[COV] = 0 SafetyStatus()[COV] = 1 If charging, BatteryStatus()[TCA] = 1 If charging, BatteryStatus()[OCA] = 1 Charging is not allowed. |
| Trip | T2 < Temperature() \leq T3 AND any Cell voltages in Voltages() continuous \geq Threshold Standard Temp for Delay duration | <ul style="list-style-type: none"> SafetyAlert()[COV] = 0 SafetyStatus()[COV] = 1 If charging, BatteryStatus()[TCA] = 1 If charging, BatteryStatus()[OCA] = 1 Charging is not allowed. |
| Trip | T3 < Temperature() AND any Cell voltages in Voltages() continuous \geq Threshold High Temp for Delay duration | <ul style="list-style-type: none"> SafetyAlert()[COV] = 0 SafetyStatus()[COV] = 1 If charging, BatteryStatus()[TCA] = 1 If charging, BatteryStatus()[OCA] = 1 Charging is not allowed. |
| Trip | T5 < Temperature() \leq T6 AND any Cell voltages in Voltages() continuous \geq Threshold Rec Temp for Delay duration | <ul style="list-style-type: none"> SafetyAlert()[COV] = 0 SafetyStatus()[COV] = 1 If charging, BatteryStatus()[TCA] = 1 If charging, BatteryStatus()[OCA] = 1 Charging is not allowed. |
| Recovery | SafetyStatus()[COV] = 1 AND Temperature() \leq T2 AND all Cell voltages in Voltages() < Recovery Low Temp | <ul style="list-style-type: none"> SafetyStatus()[COV] = 0 BatteryStatus()[TCA] = 0 BatteryStatus()[OCA] = 0 Charging is allowed. |
| Recovery | SafetyStatus()[COV] = 1 AND T2 < Temperature() \leq T3 AND all Cell voltages in Voltages() < Recovery Standard Temp | <ul style="list-style-type: none"> SafetyStatus()[COV] = 0 BatteryStatus()[TCA] = 0 BatteryStatus()[OCA] = 0 Charging is allowed. |
| Recovery | SafetyStatus()[COV] = 1 AND T3 < Temperature() AND all Cell voltages in Voltages() < Recovery High Temp | <ul style="list-style-type: none"> SafetyStatus()[COV] = 0 BatteryStatus()[TCA] = 0 BatteryStatus()[OCA] = 0 Charging is allowed. |

| Status | Condition | Action |
|----------|---|---|
| Recovery | SafetyStatus()[COV] = 1 AND T5 < Temperature() ≤ T6 AND all Cell voltages in Voltages() < Recovery Rec Temp | <ul style="list-style-type: none"> • SafetyStatus()[COV] = 0 • BatteryStatus()[TCA] = 0 • BatteryStatus()[OCA] = 0 • Charging is allowed. |

3.5 Overcurrent in Charge Protection

The device has two independent overcurrent in charge protections that can be set to different current and delay thresholds to accommodate different charging behaviors.

| Status | Condition | Action |
|----------|--|--|
| Normal | Current() < OCC1:Threshold | SafetyAlert()[OCC1] = 0 |
| Normal | Current() < OCC2:Threshold | SafetyAlert()[OCC2] = 0 |
| Alert | Current() ≥ OCC1:Threshold | SafetyAlert()[OCC1] = 1 |
| Alert | Current() ≥ OCC2:Threshold | SafetyAlert()[OCC2] = 1 |
| Trip | Current() continuous ≥ OCC1:Threshold for OCC1:Delay duration | <ul style="list-style-type: none"> • SafetyAlert()[OCC1] = 0 • SafetyStatus()[OCC1] = 1 • If charging, BatteryStatus()[TCA] = 1 • Charging is not allowed. • Start recovery delay timer |
| Trip | Current() continuous ≥ OCC2:Threshold for OCC2:Delay duration | <ul style="list-style-type: none"> • SafetyAlert()[OCC2] = 0 • SafetyStatus()[OCC2] = 1 • If charging, BatteryStatus()[TCA] = 1 • Charging is not allowed. • Start recovery delay timer |
| Recovery | [SafetyStatus()[OCC1] = 1 OR SafetyStatus()[OCC2] = 1] AND Current() < OCC:Recovery Threshold AND recovery delay timer running > OCC:Recovery Delay Time | <ul style="list-style-type: none"> • SafetyStatus()[OCC1] = 0 • SafetyStatus()[OCC2] = 0 • BatteryStatus()[TCA] = 0 • Charging is allowed. |

3.6 Overcurrent in Discharge Protection

The device has two independent overcurrent in discharge protections that can be set to different current and delay thresholds to accommodate different load behaviors.

| Status | Condition | Action |
|----------|--|--|
| Normal | Current() > OCD1:Threshold | SafetyAlert()[OCD1] = 0 |
| Normal | Current() > OCD2:Threshold | SafetyAlert()[OCD2] = 0 |
| Alert | Current() ≤ OCD1:Threshold | SafetyAlert()[OCD1] = 1 |
| Alert | Current() ≤ OCD2:Threshold | SafetyAlert()[OCD2] = 1 |
| Trip | Current() continuous ≤ OCD1:Threshold for OCD1:Delay duration | <ul style="list-style-type: none"> • SafetyAlert()[OCD1] = 0 • SafetyStatus()[OCD1] = 1 • Discharging is not allowed. • Start recovery delay timer |
| Trip | Current() continuous ≤ OCD2:Threshold for OCD2:Delay duration | <ul style="list-style-type: none"> • SafetyAlert()[OCD2] = 0 • SafetyStatus()[OCD2] = 1 • Discharging is not allowed. • Start recovery delay timer |
| Recovery | [SafetyStatus()[OCD1] = 1 OR SafetyStatus()[OCD2] = 1] AND Current() > OCD:Recovery Threshold and recovery delay timer running > OCD:Recovery Delay Time | <ul style="list-style-type: none"> • SafetyStatus()[OCD1] = 0 • SafetyStatus()[OCD2] = 0 • Discharging is allowed. |

3.7 Hardware-Based Protection

The device has three main hardware-based protections—OLD, SCC, and SCD—with adjustable current and delay time. The data flash protection Threshold and Delay settings are documented in [Appendix A](#). By setting the [RSNS] bit under Settings:AFE State Control provide an option to divide the Threshold value into half. The Threshold settings are in mV, hence, the actual current that will trigger the protection is based on the RSNS resistor used in the schematic design.

All the hardware-based protections provides a short term Trip/Alert/Recovery protection to account for a current spike as well as a Trip/Alert/Latch protection for true faulty condition. The latch feature also stops the FETs from toggling on and off continuously, preventing damage to the FETs.

In general, when a fault is Detected after the Delay time, both CHG and DSG FETs will be disabled (Trip stage). An internal fault counter will be incremented (Alert stage). Since both FETs are off, the current will drop to 0 mA, after Recovery time, the CHG and DSG FETs will be turned on again (Recovery stage).

If the alert is caused by a current spike, the fault count will be decremented after Counter Dec Delay time. If this is a true faulty condition, the device will enter the Trip stage after Delay time, and repeat the Trip/Alert/Recovery cycle. The internal fault counter is incremented every time the device goes through the Trip/Alert/Recovery cycle. Once the internal fault counter hits the Latch Limit, the protection enters a Latch stage and the fault will only be cleared through the Latch Reset condition.

The Trip/Alert/Recovery/Latch stages are documented in each hardware-based protection sections below.

3.7.1 Overload in Discharge Protection

The device has a hardware-based overload in discharge protection with adjustable current and delay.

| Status | Condition | Action |
|----------------------|--|--|
| Normal | Current() > (Threshold / RSNS) | SafetyAlert()[OLD] = 0, if OLD counter = 0 |
| Trip | Current() continuous \leq (Threshold / RSNS) for Delay duration | <ul style="list-style-type: none"> • SafetyStatus()[OLD] = 1 • CHG FET and DSG FET disabled • Increment OLD counter |
| Alert | OLD counter > 0 | <ul style="list-style-type: none"> • SafetyAlert()[OLD] = 1 • Decrement OLD counter by one after each Counter Dec Delay period |
| Recovery | SafetyStatus()[OLD] = 1 AND SafetyStatus()[OLDL] = 0 AND Recovery duration wait time | <ul style="list-style-type: none"> • SafetyStatus()[OLD] = 0 • CHG FET and DSG FET return to normal |
| Latch | OLD counter \geq Latch Limit | <ul style="list-style-type: none"> • SafetyStatus()[OLD] = 0 • SafetyStatus()[OLDL] = 1 • Reset OLD counter • Disable recovery method • Enable reset method |
| Latch Reset (NR = 0) | SafetyStatus()[OLDL] = 1 AND System Configuration[NR] = 0 AND Low-high-low transition on PRES pin | <ul style="list-style-type: none"> • SafetyStatus()[OLDL] = 0 • CHG FET and DSG FET return to normal • Disable reset method • Enable recovery method |
| Latch Reset (NR = 1) | SafetyStatus()[OLDL] = 1 AND System Configuration[NR] = 1 AND Reset duration wait time | <ul style="list-style-type: none"> • SafetyStatus()[OLDL] = 0 • CHG FET and DSG FET return to normal • Disable reset method • Enable recovery method |

3.7.2 Short Circuit in Charge Protection

The device has a hardware-based short circuit in charge protection with adjustable current and delay.

| Status | Condition | Action |
|----------------------|--|--|
| Normal | Current() < (Threshold[2:0] / RSNS) | SafetyAlert()[SCC] = 0, if SCC counter = 0 |
| Trip | Current() continuous \geq (Threshold[2:0] / RSNS) for Threshold[7:4] duration | <ul style="list-style-type: none"> • SafetyStatus()[SCC] = 1 • If charging, BatteryStatus()[TCA] = 1 • CHG FET and DSG FET disabled • Increment SCC counter |
| Alert | SCC counter > 0 | <ul style="list-style-type: none"> • SafetyAlert()[SCC] = 1 • Decrement SCC counter by one after each Counter Dec Delay period |
| Recovery | SafetyStatus()[SCC] = 1 AND SafetyStatus()[SCCL] = 0 AND Recovery duration wait time | <ul style="list-style-type: none"> • SafetyStatus()[SCC] = 0 • BatteryStatus()[TCA] = 0 • CHG FET and DSG FET return to normal |
| Latch | SCC counter \geq Latch Limit | <ul style="list-style-type: none"> • SafetyStatus()[SCC] = 0 • SafetyStatus()[SCCL] = 1 • Reset SCC counter • Disable recovery method • Enable reset method |
| Latch Reset (NR = 0) | SafetyStatus()[SCCL] = 1 AND System Configuration[NR] = 0 AND Low-high-low transition on PRES pin | <ul style="list-style-type: none"> • SafetyStatus()[SCCL] = 0 • BatteryStatus()[TCA] = 0 • CHG FET and DSG FET return to normal • Disable reset method • Enable recovery method |
| Latch Reset (NR = 1) | SafetyStatus()[SCCL] = 1 AND System Configuration[NR] = 1 AND Reset duration wait time | <ul style="list-style-type: none"> • SafetyStatus()[SCCL] = 0 • BatteryStatus()[TCA] = 0 • CHG FET and DSG FET return to normal • Disable reset method • Enable recovery method |

3.7.3 Short Circuit in Discharge Protection

The device has a hardware-based short circuit in discharge protection with adjustable current and delay.

| Status | Condition | Action |
|----------|--|--|
| Normal | Current() > (Threshold[2:0] / RSNS) | SafetyAlert()[SCD] = 0, if SCD counter = 0 |
| Trip | Current() continuous \leq (Threshold[2:0] / RSNS) for Threshold[7:4] duration | <ul style="list-style-type: none"> • SafetyStatus()[SCD] = 1 • CHG FET and DSG FET disabled • Increment SCD counter |
| Alert | SCD counter > 0 | <ul style="list-style-type: none"> • SafetyAlert()[SCD] = 1 • Decrement SCD counter by one after each Counter Dec Delay period |
| Recovery | SafetyStatus()[SCD] = 1 AND SafetyStatus()[SCDL] = 0 AND Recovery duration wait time | <ul style="list-style-type: none"> • SafetyStatus()[SCD] = 0 • CHG FET and DSG FET return to normal |
| Latch | SCD counter \geq Latch limit | <ul style="list-style-type: none"> • SafetyStatus()[SCD] = 0 • SafetyStatus()[SCDL] = 1 • Reset SCD counter • Disable recovery method • Enable reset method |

| Status | Condition | Action |
|----------------------|---|--|
| Latch Reset (NR = 0) | SafetyStatus() [SCDL] = 1 AND System Configuration[NR] = 0 AND Low-high-low transition on PRES pin | <ul style="list-style-type: none"> • SafetyStatus() [SCDL] = 0 • CHG FET and DSG FET return to normal • Disable reset method • Enable recovery method |
| Latch Reset (NR = 1) | SafetyStatus() [SCCL] = 1 AND System Configuration[NR] = 1 AND Reset duration wait time | <ul style="list-style-type: none"> • SafetyStatus() [SCDL] = 0 • CHG FET and DSG FET return to normal • Disable reset method • Enable recovery method |

3.8 Overtemperature in Charge Protection

The device has an overtemperature protection for cells in charge direction.

| Status | Condition | Action |
|----------|--|---|
| Normal | Cell Temperature in Temperatures() < Threshold AND charging | SafetyAlert() [OTC] = 0 |
| Alert | Cell Temperature in Temperatures() ≥ Threshold AND charging | SafetyAlert() [OTC] = 1 |
| Trip | Cell Temperature in Temperatures() ≥ Threshold AND charging for Delay duration | <ul style="list-style-type: none"> • SafetyAlert() [OTC] = 0 • SafetyStatus() [OTC] = 1 • BatteryStatus() [OTA] = 1 • If charging, BatteryStatus() [TCA] = 1 • Charging Disabled if Temperature Configuration[OTFET] = 1 |
| Recovery | SafetyStatus() [OTC] AND Cell Temperature in Temperatures() < Recovery | <ul style="list-style-type: none"> • SafetyStatus() [OTC] = 0 • BatteryStatus() [OTA] = 0 • BatteryStatus() [TCA] = 0 • Charging is allowed if Temperature Configuration[OTFET] = 1. |

3.9 Overtemperature in Discharge Protection

The device has an overtemperature protection for cells in discharge direction.

| Status | Condition | Action |
|----------|---|---|
| Normal | Cell Temperature in Temperatures() < Threshold AND discharging | SafetyAlert() [OTD] = 0 |
| Alert | Cell Temperature in Temperatures() ≥ Threshold AND discharging | SafetyAlert() [OTD] = 1 |
| Trip | Cell Temperature in Temperatures() ≥ Threshold AND discharging for Delay duration | <ul style="list-style-type: none"> • SafetyAlert() [OTD] = 0 • SafetyStatus() [OTD] = 1 • BatteryStatus() [OTA] = 1 • Discharging Disabled if Temperature Configuration[OTFET] = 1 |
| Recovery | SafetyStatus() [OTD] AND Cell Temperature in Temperatures() < Recovery | <ul style="list-style-type: none"> • SafetyStatus() [OTD] = 0 • BatteryStatus() [OTA] = 0 • Discharging is allowed if Temperature Configuration[OTFET] = 1. |

3.10 Overtemperature FET Protection

The device has an overtemperature protection to limit the FET temperature.

| Status | Condition | Action |
|----------|--|--|
| Normal | FET Temperature in Temperatures() < Threshold | SafetyAlert()[OTF] = 0 |
| Alert | FET Temperature in Temperatures() ≥ Threshold | SafetyAlert()[OTF] = 1 |
| Trip | FET Temperature in Temperatures() ≥ Threshold for Delay duration | <ul style="list-style-type: none"> • SafetyAlert()[OTF] = 0 • SafetyStatus()[OTF] = 1 • BatteryStatus()[OTA] = 1 • CHG FET and DSG FET off if Temperature Configuration[OTFET] =1 |
| Recovery | SafetyStatus()[OTF] AND FET Temperature in Temperatures() < Recovery | <ul style="list-style-type: none"> • SafetyStatus()[OTD] = 0 • BatteryStatus()[OTA] = 0 • CHG FET and DSG FET return to normal |

3.11 SBS Host Watchdog Protection

The device can check for periodic communication over SBS and prevent usage of the battery pack if no valid communication is Detected.

| Status | Condition | Action |
|----------|---|---|
| Trip | No valid SBS transaction for Delay duration | <ul style="list-style-type: none"> • SafetyStatus()[HWD] = 1 • Charging disabled, CHG FET off |
| Recovery | Valid SBS transaction Detected | <ul style="list-style-type: none"> • SafetyStatus()[HWD] = 0 • CHG FET returns to normal, charging is allowed. |

3.12 Pre-Charge Timeout Protection

The device can measure the pre-charge time and stop charging if it exceeds the adjustable period.

| Status | Condition | Action |
|---------------------|---|--|
| Enable | Current() > Charge Threshold AND ChargingStatus()[PV] = 1 | <ul style="list-style-type: none"> • Start PTO timer • SafetyAlert()[PTO] = 1 • SafetyAlert()[PTOS] = 0 |
| Suspend or Recovery | Current() < Suspend Threshold | <ul style="list-style-type: none"> • Stop PTO timer • SafetyAlert()[PTO] = 1 • SafetyAlert()[PTOS] = 1 |
| Trip | PTO time > Delay | <ul style="list-style-type: none"> • Stop PTO timer • SafetyAlert()[PTO] = 0 • SafetyStatus()[PTO] = 1 • If charging, BatteryStatus()[TCA] = 1 • Charging is not allowed. |
| Reset | SafetyStatus()[PTO] = 1 AND System Configuration[NR] = 0 AND (Discharge by an amount of Reset OR low-high-low transition on PRES) | <ul style="list-style-type: none"> • Stop and reset PTO timer • SafetyAlert()[PTO] = 0 • SafetyAlert()[PTOS] = 0 • SafetyStatus()[PTO] = 0 • BatteryStatus()[TCA] = 0 • Charging is allowed. |
| Reset | SafetyStatus()[PTO] = 1 AND System Configuration[NR] = 1 AND (Discharge by an amount of Reset) | <ul style="list-style-type: none"> • Stop and reset PTO timer • SafetyAlert()[PTO] = 0 • SafetyAlert()[PTOS] = 0 • SafetyStatus()[PTO] = 0 • BatteryStatus()[TCA] = 0 • Charging is allowed. |

3.13 Fast Charge Timeout Protection

The device can measure the charge time and stop charging if it exceeds the adjustable period.

| Status | Condition | Action |
|---------------------|---|--|
| Enable | Current() > Charge Threshold AND (ChargingStatus() [LV] = 1 OR ChargingStatus() [MV] = 1 OR ChargingStatus() [HV] = 1) | <ul style="list-style-type: none"> Start CTO timer SafetyAlert()[CTO] = 1 SafetyAlert()[CTOS] = 0 |
| Suspend or Recovery | Current() < Suspend Threshold | <ul style="list-style-type: none"> Stop CTO timer SafetyAlert()[CTO] = 1 SafetyAlert()[CTOS] = 1 |
| Trip | CTO time > Delay | <ul style="list-style-type: none"> Stop CTO timer SafetyAlert()[CTO] = 0 SafetyStatus()[CTO] = 1 If charging, BatteryStatus()[TCA] = 1 Charging is not allowed. |
| Reset | SafetyStatus() [CTO] = 1 AND System Configuration [NR] = 0 AND (Discharge by an amount of Reset OR low-high-low transition on PRES) | <ul style="list-style-type: none"> Stop and reset CTO timer SafetyAlert()[CTO] = 0 SafetyAlert()[CTOS] = 0 SafetyStatus()[CTO] = 0 BatteryStatus()[TCA] = 0 Charging is allowed. |
| Reset | SafetyStatus() [CTO] = 1 AND System Configuration [NR] = 1 AND (Discharge by an amount of Reset) | <ul style="list-style-type: none"> Stop and reset CTO timer SafetyAlert()[CTO] = 0 SafetyAlert()[CTOS] = 0 SafetyStatus()[CTO] = 0 BatteryStatus()[TCA] = 0 Charging is allowed. |

3.14 Overcharge Protection

The device can prevent continuing charging if the pack is charged in excess over **FullChargeCapacity()**.

| Status | Condition | Action |
|----------|---|---|
| Normal | RemainingCapacity() < FullChargeCapacity() | SafetyAlert() [OC] = 0 |
| Alert | RemainingCapacity() ≥ FullChargeCapacity() | SafetyAlert() [OC] = 1 |
| Trip | RemainingCapacity() ≥ FullChargeCapacity() + Threshold | <ul style="list-style-type: none"> SafetyAlert()[OC] = 0 SafetyStatus()[OC] = 1 If charging, BatteryStatus()[TCA] = 1 Charging is not allowed. |
| Recovery | SafetyStatus() [OC] = 1 System Configuration [NR] = 0 AND (Low-high-low transition on PRES pin | <ul style="list-style-type: none"> SafetyStatus()[OC] = 0 BatteryStatus()[TCA] = 0 Charging is allowed. |
| Recovery | SafetyStatus() [OC] = 1 System Configuration [NR] = 1 AND continuous discharge of Recovery OR RemainingStateOfCharge() < RSOC Recovery | <ul style="list-style-type: none"> SafetyStatus()[OC] = 0 BatteryStatus()[TCA] = 0 Charging is allowed. |

3.15 Over-ChargingVoltage() Protection

The device can stop charging if it measures a difference between the requested **ChargingVoltage()** and the delivered voltage from the charger.

| Status | Condition | Action |
|----------|---|---|
| Normal | Voltage() < ChargingVoltage() + CHGV:Threshold | SafetyAlert()[CHGV] = 0 |
| Alert | Voltage() ≥ ChargingVoltage() + CHGV:Threshold | SafetyAlert()[CHGV] = 1 |
| Trip | Voltage() continuous ≥ ChargingVoltage() + CHGV:Threshold for CHGV:Delay period | <ul style="list-style-type: none"> • SafetyAlert()[CHGV] = 0 • SafetyStatus()[CHGV] = 1 • If charging, BatteryStatus()[TCA] = 1 • Charging is not allowed. |
| Recovery | SafetyStatus()[CHGV] = 1 AND Voltage() ≤ ChargingVoltage() + CHGV Recovery | <ul style="list-style-type: none"> • SafetyStatus()[CHGV] = 0 • BatteryStatus()[TCA] = 0 • Charging is allowed. |

3.16 Over-ChargingCurrent() Protection

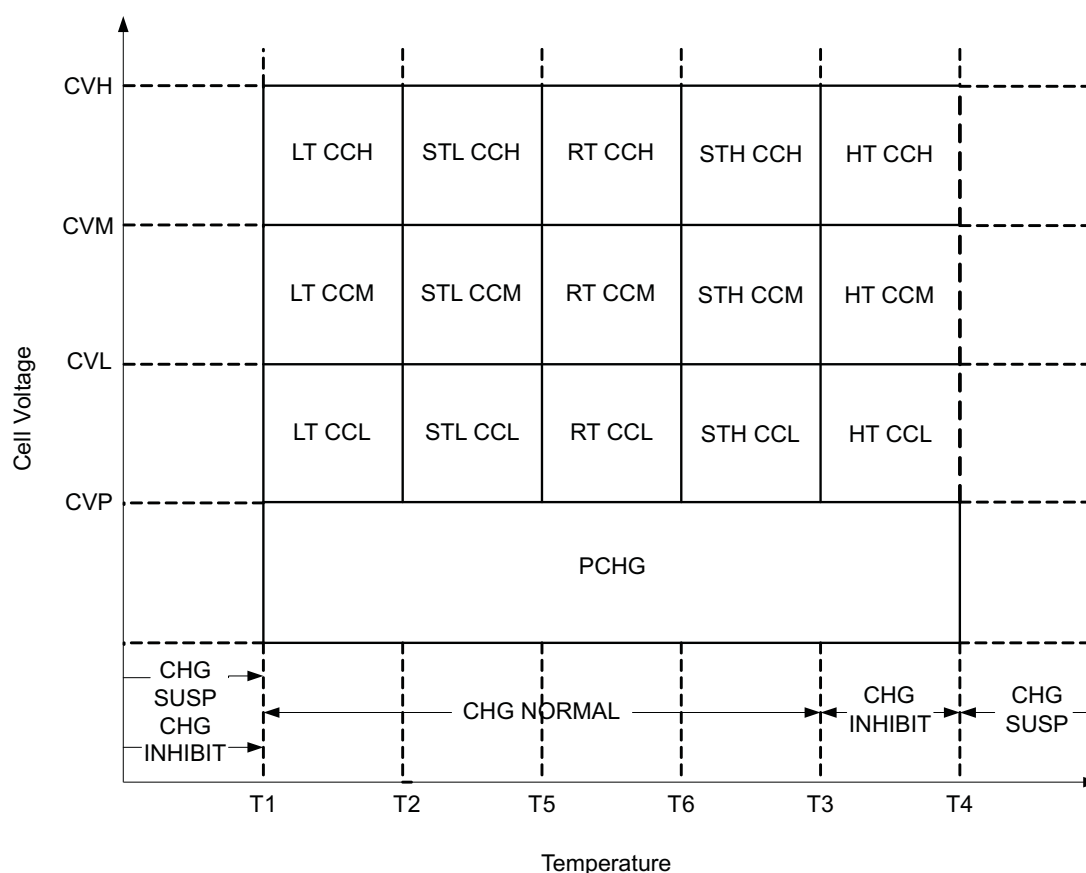
The device can stop charging if it measures a difference between the requested **ChargingCurrent()** and the delivered current from the charger.

| Status | Condition | Action |
|----------|---|---|
| Normal | Current() < ChargingCurrent() + CHGC:Threshold | SafetyAlert()[CHGC] = 0 |
| Alert | Current() ≥ ChargingCurrent() + CHGC:Threshold | SafetyAlert()[CHGC] = 1 |
| Trip | Current() continuous ≥ ChargingCurrent() + CHGC:Threshold for CHGC:Delay period | <ul style="list-style-type: none"> • SafetyAlert()[CHGC] = 0 • SafetyStatus()[CHGC] = 1 • If charging, BatteryStatus()[TCA] = 1 • Charging is not allowed. |
| Recovery | SafetyStatus()[CHGC] = 1 AND Current() ≤ ChargingCurrent() + CHGC Recovery | <ul style="list-style-type: none"> • SafetyStatus()[CHGC] = 0 • BatteryStatus()[TCA] = 0 • Charging is allowed. |

Advanced Charge Algorithm

4.1 Introduction

The device can change value of **ChargingVoltage()** and **ChargingCurrent()** based on **Temperature()** and **Cell Voltage1..4()**. Its flexible charging algorithm is JEITA compatible and can also meet ATL cell charge requirements. The **ChargingStatus()** register shows the state of the charging algorithm.



4.2 Charge Temperature Ranges

The measured temperature is segmented into several temperature ranges. The charging algorithm adjusts **ChargingCurrent()** and **ChargingVoltage()** according to the temperature range. The temperature range need to be set to following:

$$T1 \leq T2 \leq T5 \leq T6 \leq T3 \leq T4$$

| Status | Condition | Action |
|-------------------|----------------------------------|---|
| Under Temp | $\text{Temperature}() < T1$ | $\text{ChargingStatus}()[\text{UT}] = 1$ |
| Low Temp | $T1 < \text{Temperature}() < T2$ | $\text{ChargingStatus}()[\text{LT}] = 1$ |
| Standard Temp Low | $T2 < \text{Temperature}() < T5$ | $\text{ChargingStatus}()[\text{STL}] = 1$ |
| Recommended | $T5 < \text{Temperature}() < T6$ | $\text{ChargingStatus}()[\text{RT}] = 1$ |

| Status | Condition | Action |
|--------------------|--------------------------------|----------------------------------|
| Standard Temp High | T6 < Temperature() < T3 | ChargingStatus()[STH] = 1 |
| High Temp | T3 < Temperature() < T4 | ChargingStatus()[HT] = 1 |
| Over Temp | T4 < Temperature() | ChargingStatus()[OT] = 1 |

4.3 Voltage Range

The measured cell voltage is segmented into several voltage ranges. The charging algorithm adjusts **ChargingCurrent()** according to the temperature range and voltage range. The voltage range need to be set to following:

ChargingVoltage Low ≤ ChargingVoltage Med ≤ ChargingVoltageHigh ≤ x Temp Charging:Voltage

| Status | Condition | Action |
|------------|---|---------------------------------|
| Pre-Charge | Any Cell Voltages in Voltages() < Charging Voltage Low | ChargingStatus()[PV] = 1 |
| Low | Charging Voltage Low < all Cell Voltages in Voltages() OR any Cell Voltages in Voltages() < Charging Voltage Med | ChargingStatus()[LV] = 1 |
| Medium | Charging Voltage Med < all Cell Voltages in Voltages() OR any Cell Voltages in Voltages() < Charging Voltage High | ChargingStatus()[MV] = 1 |
| High | Charging Voltage High < all Cell Voltages in Voltages() | ChargingStatus()[HV] = 1 |

A voltage hysteresis setting is available, and is applied when the voltage decreases.

4.4 Charging Current

The **ChargingCurrent()** value will change depending on charge algorithm.

| ChargingStatus() | | | | | | | | | | Action |
|------------------|----|---------|----|----|----|----|----|----|----|--|
| UT | LT | STL/STH | HT | RT | OT | PV | LV | MV | HV | |
| 1 | 0 | 0 | 0 | 0 | 0 | x | x | x | x | ChargingCurrent() = 0 |
| 0 | x | x | x | x | 0 | 1 | 0 | 0 | 0 | ChargingCurrent() = PCHG:Current |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | ChargingCurrent() = Low Temp Charging:Current Low |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | ChargingCurrent() = Low Temp Charging:Current Med |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | ChargingCurrent() = Low Temp Charging:Current High |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | ChargingCurrent() = Standard Temp Charging:Current Low |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | ChargingCurrent() = Standard Temp Charging:Current Med |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | ChargingCurrent() = Standard Temp Charging:Current High |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | ChargingCurrent() = Standard Temp Charging:Current Low |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | ChargingCurrent() = Standard Temp Charging:Current Med |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | ChargingCurrent() = Standard Temp Charging:Current High |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | ChargingCurrent() = Rec Temp Charging:Current Low |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | ChargingCurrent() = Rec Temp Charging:Current Med |

| ChargingStatus() | | | | | | | | | | Action |
|------------------|----|---------|----|----|----|----|----|----|----|--|
| UT | LT | STL/STH | HT | RT | OT | PV | LV | MV | HV | |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | ChargingCurrent() = Rec Temp Charging:Current High |
| 0 | 0 | 0 | 0 | 0 | 1 | x | x | x | x | ChargingCurrent() = 0 |

4.5 Charging Voltage

The **ChargingVoltage()** will change depending on the charge algorithm.

| ChargingStatus() | | | | | | Action |
|------------------|----|---------|----|----|----|--|
| UT | LT | STL/STH | HT | RT | OT | |
| 1 | 0 | 0 | 0 | 0 | 0 | ChargingVoltage() = 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | ChargingVoltage() = Low Temp Charging:Voltage * Number of cells |
| 0 | 0 | 1 | 0 | 0 | 0 | ChargingVoltage() = Standard Temp Charging:Voltage * Number of cells |
| 0 | 0 | 0 | 1 | 0 | 0 | ChargingVoltage() = High Temp Charging:Voltage * Number of cells |
| 0 | 0 | 0 | 0 | 1 | 0 | ChargingVoltage() = Rec Temp Charging:Voltage * Number of cells |
| 0 | 0 | 0 | 0 | 0 | 1 | ChargingCurrent() = 0 |

A temperature hysteresis setting is available, and is applied when temperature decreases.

4.6 Valid Charge Termination

The charge termination condition has to be met to enable valid charge termination.

| Status | Condition | Action |
|--------------------------|--|--|
| Charging | GaugingStatus()[REST] = 0 AND GaugingStatus()[DSG] = 0 | Charge Algorithm active |
| Valid Charge Termination | (Charging AND AverageCurrent() continuous < Charge Term Taper Current AND Voltage() > ChargingVoltage()/Number of Cells + Charge Term Voltage AND Δcharge > Taper Charge) for two consecutive 40-s periods | <ul style="list-style-type: none"> ChargingStatus()[VCT] sets If SBS Configuration[FCSETVCT], BatteryStatus[FC] = 1 If SBS Configuration[TCASETVCT], BatteryStatus[TCA] = 1 If BatteryStatus[TCA], ChargingStatus[MCHG] = 1 If ChargingStatus[MCHG]: <ul style="list-style-type: none"> If Charging Configuration[CHGFET] = 1, CHG and PCHG FET off AND ChargingCurrent() = 0 If Charging Configuration[CHGFET] = 0, CHG FET active and ChargingCurrent() = MaintenanceCurrent |

4.7 Charge Inhibit

The device can prevent start of charging at high and low temperatures to prevent damage of the cells.

| Status | Condition | Action |
|--------|-------------------------|--|
| Normal | T1 < Temperature() < T3 | <ul style="list-style-type: none"> ChargingStatus()[IN] = 0 ChargingVoltage() = charging algorithm ChargingCurrent() = charging algorithm |
| Trip | Temperature() < T1 | <ul style="list-style-type: none"> ChargingStatus()[IN] = 1 ChargingVoltage() = 0 ChargingCurrent() = 0 No charging is allowed if Charging Configuration[CHGIN] = 1. |

| Status | Condition | Action |
|--------|---|--|
| Trip | Temperature() > T3 while no charging | <ul style="list-style-type: none"> • ChargingStatus()[IN] = 1 • ChargingVoltage() = 0 • ChargingCurrent() = 0 • No charging is allowed if Charging Configuration[CHGIN] = 1. |

4.8 Charge Suspend

The device can stop charging at high and low temperatures to prevent damage of the cells.

| Status | Condition | Action |
|--------|--------------------------------|--|
| Normal | T1 < Temperature() < T4 | <ul style="list-style-type: none"> • ChargingStatus()[SU] = 0 • ChargingVoltage() = charging algorithm • ChargingCurrent() = charging algorithm |
| Trip | Temperature() < T1 | <ul style="list-style-type: none"> • ChargingStatus()[SU] = 1 • ChargingVoltage() = 0 • ChargingCurrent() = 0 • No charging is allowed if Charging Configuration[CHGSU] = 1. |
| Trip | Temperature() > T4 | <ul style="list-style-type: none"> • ChargingStatus()[SU] = 1 • ChargingVoltage() = 0 • ChargingCurrent() = 0 • No charging is allowed if Charging Configuration[CHGSU] = 1. |

4.9 ChargingVoltage() Rate of Change

The device can slope the value changes from one range to another to avoid jumping between different voltage ranges.

NOTE: The host needs to read **ChargingVoltage()** at least once a second during charging to adjust the charger accordingly.

| Status | Condition | Action |
|--------|---------------------------------------|---|
| Trip | ChargingVoltage() Range Change | <ul style="list-style-type: none"> • ChargingStatus()[CVR] = 1 • ChargingVoltage() = OldRange + n * (New Range – Old Range)/Voltage Rate, n = 1.. Voltage Rate for Voltage Rate seconds |

4.10 ChargingCurrent() Rate of Change

The device can slope the value changes from one range to another to avoid jumping between different current ranges.

NOTE: The host needs to read **ChargingCurrent()** at least once a second during charging to adjust the charger accordingly.

| Status | Condition | Action |
|--------|---------------------------------------|---|
| Trip | ChargingCurrent() Range Change | <ul style="list-style-type: none"> • ChargingStatus()[CCR] = 1 • ChargingCurrent() = OldRange + n * (New Range – Old Range)/Current Rate, n = 1.. Current Rate for Current Rate seconds |

4.11 Charging Loss Compensation

The device can modify **ChargingVoltage()** and **ChargingCurrent()** to compensate losses caused by the FETs, the fuse, and the sense resistor by measuring the cell voltages directly and adjusting **ChargingCurrent()** and **ChargingVoltage()** accordingly.

In constant current mode, the device can increase the **ChargingVoltage()** value to compensate the drop losses.

NOTE: The host must read **ChargingVoltage()** and/or **ChargingCurrent()** at least once a second during charging to adjust the charger accordingly.

| Status | Condition | Action |
|--------|---|---|
| Normal | Current() > CCC Current Threshold AND Sum(Cell Voltages in Voltages()) = Charging algorithm voltage | <ul style="list-style-type: none"> • ChargingStatus()[CCC] = 0 • ChargingVoltage() = Charge Algorithm |
| Active | Current() > CCC Current Threshold AND Sum(Cell Voltages in Voltages()) < Charging algorithm voltage | <ul style="list-style-type: none"> • ChargingStatus()[CCC] = 1 • ChargingVoltage() = Charge Algorithm + [PackVoltage() – Sum(Cell Voltages in Voltages())] |
| Limit | [PackVoltage() – Sum(Cell Voltages in Voltages())] > CCC Voltage Threshold | ChargingVoltage() = Charge Algorithm + CCC Voltage |

Permanent Fail

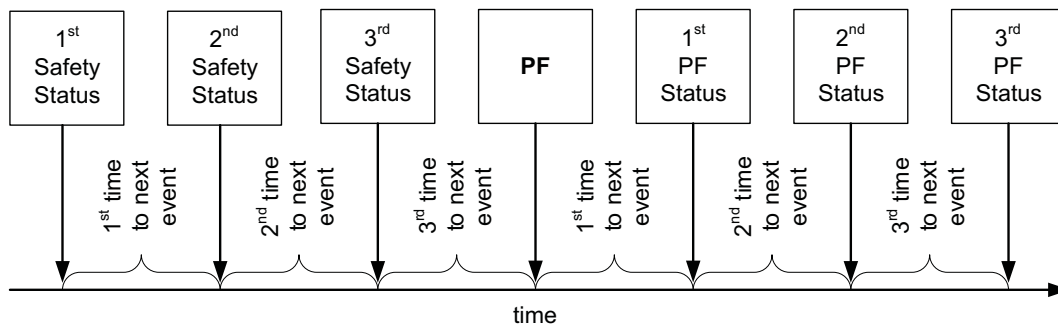
5.1 Introduction

The device can permanently disable the use of the battery pack in case of a severe failure. The following actions in sequence are taken in permanent fail (PF) mode when the **Settings:Manufacturing Status[PF_EN]** bit is enabled. An individual PF event can be enabled and disabled with **Settings:Enabled PF0–15** and **Settings:Enabled PF16–31** even after [PF_EN] bit is enabled.

1. Precharge, charge, and discharge FETs are turned off.
2. The following SBS data is changed: If charging, **BatteryStatus()[TCA]** = 1, if not charging, **BatteryStatus()[TDA]** = 1, **ChargingCurrent()** = 0, **ChargingVoltage()** = 0.
3. A backup of the internal AFE hardware registers are written to data flash: STATUS, STATE_CONTROL, OUTPUT_STATUS, FUNCTION_CONTROL, CELL_SEL, OCDV, OCDD, SCD1, SCD2
4. The black box data of the last three **SafetyStatus()** changes leading up to PF with time difference is written into data flash.
5. The cause of the permanent fail is logged into **PFAAlert** and **PFStatus**.
6. The following SBS values are preserved in data flash for failure analysis:
 - **SafetyAlert()**
 - **SafetyStatus()**
 - **PFAAlert()**
 - **PFStatus()**
 - **OperationStatus()**
 - **ChargingStatus()**
 - **GaugingStatus()**
 - **Voltages()**
 - **Temperatures()**
 - **DOD()**
7. Data flash writing is disabled, except subsequent **PFStatus** flags.
8. Subsequent PFs are appended to **PFAAlert** and **PFStatus** in PF Status class. PF Status is also logged separately to the Black Box Recorder 1st, 2nd, and 3rd PF Status.
9. The FUSE pin is driven high if configured for specific failures.

5.2 Black Box Recorder

The black box recorder maintains the last three updates of **SafetyStatus()** in memory. In case of permanent failure, this information is written to data flash together with the first three updates of **PFStatus()** after the PF event.



NOTE: This information is useful in failure analysis, and can provide a full recording of the events and conditions leading up to the permanent failure.

If there were less than three safety events before PF, then some information will be left blank.

5.3 Cell Undervoltage Permanent Fail

The device can permanently disable the battery in case of severe low level of cell voltage.

| Status | Condition | Action |
|--------|--|---|
| Normal | All Cell voltages in Voltages() > Threshold | <ul style="list-style-type: none"> • PFAAlert() [CUV] = 0 • BatteryStatus() [TDA] = 0 |
| Alert | Any Cell voltages in Voltages() ≤ Threshold | <ul style="list-style-type: none"> • PFAAlert() [CUV] = 1 • If not charging, BatteryStatus() [TDA] = 1. |
| Trip | Any Cell voltages in Voltages() continuous ≤ Threshold for Delay duration AND Enabled PF 0–15 [CUV] = 1 | <ul style="list-style-type: none"> • PFAAlert() [CUV] = 0 • PFStatus() [CUV] = 1 • BatteryStatus() [FD] = 1 • If not charging, BatteryStatus() [TDA] = 1. |

5.4 Cell Overvoltage Permanent Fail

The device can permanently disable the battery in case of severe cell overvoltage.

| Status | Condition | Action |
|--------|--|---|
| Normal | All Cell voltages in Voltages() < Threshold | PFAAlert() [COV] = 0 |
| Alert | Any Cell voltages in Voltages() ≥ Threshold | PFAAlert() [COV] = 1 |
| Trip | Any Cell voltages in Voltages() continuous ≥ Threshold for Delay duration AND Enabled PF 0–15 [COV] = 1 | <ul style="list-style-type: none"> • PFAAlert() [COV] = 0 • PFStatus() [COV] = 1 • If charging, BatteryStatus() [OCA] = 1 |

5.5 Copper Deposition Permanent Fail

The device can permanently disable the battery in case of severe low level of cell voltage. The copper deposition check checks cell voltages upon wake up from shutdown mode while keeping the charge and precharge FETs off until the check is complete.

| Status | Condition | Action |
|--------|--|---|
| Normal | All Cell voltages in Voltages() > Threshold | <ul style="list-style-type: none"> • PFAAlert() [CUDEP] = 0 • BatteryStatus() [TDA] = 0 |
| Alert | Any Cell voltages in Voltages() ≤ Threshold | <ul style="list-style-type: none"> • PFAAlert() [CUDEP] = 1 • If not charging, BatteryStatus() [TDA] = 1. |
| Trip | Any Cell voltages in Voltages() continuous ≤ Threshold for Delay duration AND Enabled PF 0–15 [CUDEP] = 1 | <ul style="list-style-type: none"> • PFAAlert() [CUDEP] = 0 • PFStatus() [CUDEP] = 1 • BatteryStatus() [FD] = 1 • If not charging, BatteryStatus() [TDA] = 1. |

5.6 Overtemperature Cell Permanent Fail

The device can permanently disable the battery pack in case of severe overtemperature of the cells.

| Status | Condition | Action |
|--------|--|--|
| Normal | Cell Temperature in Temperatures() < Threshold | PFAAlert() [OTCE] = 0 |
| Alert | Cell Temperature in Temperatures() ≥ Threshold | PFAAlert() [OTCE] = 1 |
| Trip | Cell Temperature in Temperatures() continuous ≥ Threshold for Delay duration AND Enabled PF 0–15 [OTCE] = 1 | <ul style="list-style-type: none"> • PFAAlert() [OTCE] = 0 • PFStatus() [OTCE] = 1 • BatteryStatus() [OTA] = 1 |

5.7 Overtemperature FET Permanent Fail

The device can permanently disable the battery pack in case of severe overtemperature on the power FET.

| Status | Condition | Action |
|--------|--|--|
| Normal | FET Temperature in Temperatures() < Threshold | PFAAlert() [OTF] = 0 |
| Alert | FET Temperature in Temperatures() ≥ Threshold | PFAAlert() [OTF] = 1 |
| Trip | FET Temperature in Temperatures() continuous ≥ Threshold for Delay duration AND Enabled PF 0–15 [OTF] = 1 | <ul style="list-style-type: none"> • PFAAlert() [OTF] = 0 • PFStatus() [OTF] = 1 • BatteryStatus() [OTA] = 1 |

5.8 QMax Imbalance Permanent Fail

The device can permanently disable the battery pack in case the capacity of one of the cells is much lower than the others.

| Status | Condition | Action |
|--------|---|--|
| Normal | $\Delta(QMax\ Cell\ 0..3) < \text{Threshold}$ | PFAAlert() [QIM] = 0 |
| Alert | $\Delta(QMax\ Cell\ 0..3) \geq \text{Threshold}$ | PFAAlert() [QIM] = 1 |
| Trip | $\Delta(QMax\ Cell\ 0..3)$ continuous ≥ Threshold for Delay duration AND Enabled PF 0–15 [QIM] = 1 | <ul style="list-style-type: none"> • PFAAlert() [QIM] = 0 • PFStatus() [QIM] = 1 |

5.9 Cell Balancing Permanent Fail

The device can permanently disable the battery pack in case one of the cells in stack is cell balanced much more than the others.

| Status | Condition | Action |
|--------|--|--|
| Normal | $\Delta(\text{Time Cell } 0..3) < \text{Delta Threshold}$ | PFA Alert()[CB] = 0 |
| Alert | $\Delta(\text{Time Cell } 0..3) \geq \text{Delta Threshold}$ | PFA Alert()[CB] = 1 |
| Trip | $\Delta(\text{Time Cell } 0..3)$ continuous $\geq \text{Delta Threshold}$ for Delay duration AND Enabled PF 0–15[CB] = 1 | <ul style="list-style-type: none"> • PFAAlert()[CB] = 0 • PFStatus()[CB] = 1 |
| Trip | Max (Time Cell 0..3) \geq Max Threshold AND Enabled PF 0–15[CB] = 1 | <ul style="list-style-type: none"> • PFAAlert()[CB] = 0 • PFStatus()[CB] = 1 |

5.10 Capacity Degradation Permanent Fail

The device can permanently disable the battery pack in case the capacity of the cell stack is degraded below a threshold.

| Status | Condition | Action |
|--------|--|--|
| Normal | $\text{All}(Q_{\text{Max}1..4}) > \text{Threshold}$ | PFA Alert()[CD] = 0 |
| Alert | $\text{Any}(Q_{\text{Max}1..4}) \leq \text{Threshold}$ | PFA Alert()[CD] = 1 |
| Trip | $\text{Any}(Q_{\text{Max}1..4})$ continuous $\leq \text{Threshold}$ for Delay cycles AND Enabled PF 0–15[CD] = 1 | <ul style="list-style-type: none"> • PFAAlert()[CD] = 0 • PFStatus()[CD] = 1 |

5.11 Impedance Permanent Fail

The device can permanently disable the battery pack in case the impedance of one of the cells is much higher than the others.

NOTE: **Reference Grid** is configurable from 0 (resistance at fully charged cell) to 14 (resistance at fully discharged cell). The **Design Resistance** will be automatically calculated and updated during learning cycle and is part of the golden image).

| Status | Condition | Action |
|--------|--|--|
| Normal | $\Delta(\text{Cell}0..3 \text{ R}_a \text{ at Reference Grid}) < (\text{Delta Threshold} * \text{Design Resistance})$ | PFA Alert()[IMP] = 0 |
| Alert | $\Delta(\text{Cell}0..3 \text{ R}_a \text{ at Reference Grid}) \geq (\text{Delta Threshold} * \text{Design Resistance})$ | PFA Alert()[IMP] = 1 |
| Trip | $\Delta(\text{Cell}0..3 \text{ R}_a \text{ at Reference Grid}) \geq (\text{Delta Threshold} * \text{Design Resistance})$ for Ra Update Counts AND Enabled PF 0–15[IMP] = 1 | <ul style="list-style-type: none"> • PFAAlert()[IMP] = 0 • PFStatus()[IMP] = 1 |
| Trip | $\Delta(\text{Cell}0..3 \text{ R}_a \text{ at Reference Grid}) \geq (\text{Max Threshold} * \text{Design Resistance})$ AND Enabled PF 0–15[IMP] = 1 | <ul style="list-style-type: none"> • PFAAlert()[IMP] = 0 • PFStatus()[IMP] = 1 |

5.12 Voltage Imbalance at Rest Permanent Fail

The device can permanently disable the battery pack in case of voltage difference between the cells in a stack while at rest.

| Status | Condition | Action |
|--------|--|------------------------------|
| Normal | <ul style="list-style-type: none"> • All Cell voltages in Voltages() < Check Voltage • Current() > Check Current • $\Delta(\text{Cell voltages in Voltages}()) < \text{Delta Threshold}$ | PFA Alert()[VIMR] = 0 |
| Alert | Any Cell voltages in Voltages() \geq Check Voltage AND Current () continuous < Check Current for Duration AND $\Delta(\text{Cell voltages in Voltages}()) \geq \text{Delta Threshold}$ | PFA Alert()[VIMR] = 1 |

| Status | Condition | Action |
|--------|--|--|
| Trip | [Any Cell voltages in Voltages() \geq Check Voltage AND Current() continuous $<$ Check Current for Duration AND Δ (Cell voltages in Voltages()) \geq Delta Threshold] for Delay duration AND Enabled PF 0–15[VIMR] = 1 | <ul style="list-style-type: none"> • PFAAlert()[VIMR] = 0 • PFStatus()[VIMR] = 1 |

5.13 Voltage Imbalance Active Permanent Fail

The device can permanently disable the battery pack in case of voltage difference between the cells in a stack while active.

| Status | Condition | Action |
|--------|---|--|
| Normal | <ul style="list-style-type: none"> • All Cell voltages in Voltages() $<$ Check Voltage • Current() $<$ Check Current • Δ(Cell voltages in Voltages()) $<$ Delta Threshold | PFAAlert()[VIMA] = 0 |
| Alert | Any Cell voltages in Voltages() \geq Check Voltage AND Current() continuous $>$ Check Current for Duration AND Δ (Cell voltages in Voltages()) \geq Delta Threshold | PFAAlert()[VIMA] = 1 |
| Trip | [Any Cell voltages in Voltages() \geq Check Voltage AND Current() continuous $>$ Check Current for Duration AND Δ (Cell voltages in Voltages()) continuous \geq Delta Threshold] for Delay duration AND Enabled PF 0–15[VIMA] = 1 | <ul style="list-style-type: none"> • PFAAlert()[VIMA] = 0 • PFStatus()[VIMA] = 1 |

5.14 Charge FET Permanent Fail

The device can permanently disable the battery pack in case the charge FET is not working properly.

| Status | Condition | Action |
|--------|--|--|
| Normal | CHG FET off AND Current() $<$ OFF Threshold | PFAAlert()[CFETF] = 0 |
| Alert | CHG FET off AND Current() \geq OFF Threshold | PFAAlert()[CFETF] = 1 |
| Trip | CHG FET off AND Current() continuously \geq OFF Threshold for Delay duration AND Enabled PF 16–32[CFETF] = 1 | <ul style="list-style-type: none"> • PFAAlert()[CFETF] = 0 • PFStatus()[CFETF] = 1 |

5.15 Discharge FET Permanent Fail

The device can permanently disable the battery pack in case the discharge FET is not working properly.

| Status | Condition | Action |
|--------|---|--|
| Normal | DSG FET off AND Current() $>$ OFF Threshold | PFAAlert()[DFET] = 0 |
| Alert | DSG FET off AND Current() \leq OFF Threshold | PFAAlert()[DFET] = 1 |
| Trip | DSG FET off AND Current() continuously \leq OFF Threshold for Delay duration AND Enabled PF 16–32[DFET] = 1 | <ul style="list-style-type: none"> • PFAAlert()[DFET] = 0 • PFStatus()[DFET] = 1 |

5.16 Thermistor Permanent Fail

The device can permanently disable the battery pack when it detects an open (internally pulled up) or short (grounded) failure in the thermistor circuit. When a fault is Detected, the **PFAALER()[TH]** bit will be set to 1. If the fault is still present after the Permanent Fail:ADC Delay time, the **PFAALER()[TH]** bit will be cleared and **PFStatus()[TH]** will be set to 1.

5.17 Chemical Fuse Permanent Fail

The device can detect a non-working fuse. The device cannot disable the battery pack permanently but can record this event for analysis.

| Status | Condition | Action |
|--------|--|--|
| Normal | FUSE pin = high AND Current() < Threshold | PFAAlert()[FUSE] = 0 |
| Alert | FUSE pin = high AND Current() ≥ Threshold | PFAAlert()[FUSE] = 1 |
| Trip | FUSE pin = high AND Current() continuous ≥ Threshold for Delay duration AND Enabled PF 16–32[FUSE] = 1 | <ul style="list-style-type: none"> • PFAAlert()[FUSE] = 0 • PFStatus()[FUSE] = 1 |

5.18 AFE Register Permanent Fail

The device compares the AFE hardware register periodically with a RAM backup. If the comparison fails too many times, the device disables the pack permanently.

| Status | Condition | Action |
|--------|--|--|
| Normal | AFE register fail counter = 0 | <ul style="list-style-type: none"> • PFAAlert()[AFER] = 0 • Compare AFE register and RAM backup every Compare Period |
| Alert | AFE register fail counter > 0 | <ul style="list-style-type: none"> • PFAAlert()[AFER] = 1 • Decrement AFE register fail counter by one after each Delay Period • Compare AFE register and RAM backup every Compare Period |
| Trip | AFE register fail counter ≥ Threshold AND Enabled PF 16–32[AFER] = 1 | <ul style="list-style-type: none"> • PFAAlert()[AFER] = 0 • PFStatus()[AFER] = 1 |

5.19 AFE Communication Permanent Fail

The device monitors the internal communication to the AFE hardware. If the read or write fails exceed a limit within a timeframe, the device disables the pack permanently.

| Status | Condition | Action |
|--------|--|--|
| Normal | AFE read/write fail counter = 0 | PFAAlert()[AFEC] = 0 |
| Alert | AFE read/write fail counter > 0 | <ul style="list-style-type: none"> • PFAAlert()[AFEC] = 1 • Decrement AFE read/write fail counter by one after each Delay period |
| Trip | Read and Write Fail counter ≥ Threshold AND Enabled PF 16–32[AFEC] = 1 | <ul style="list-style-type: none"> • PFAAlert()[AFEC] = 0 • PFStatus()[AFEC] = 1 |

5.20 Second Level Protection Permanent Fail

The device can detect external trigger of the chemical fuse by an external protection circuit such as a 2nd-level protector by monitoring the FUSE pin state.

If the device detects FUSE pin high state, the CHG and DSG FET are turned off.

| Status | Condition | Action |
|--------|--|--|
| Normal | Reset AFE and FUSE pin = low AND no FUSE trigger by firmware | <ul style="list-style-type: none"> • PFAAlert()[2LVL] = 0 • Reset internal PF 2LVL counter |
| Alert | FUSE pin = high AND no FUSE trigger by firmware | <ul style="list-style-type: none"> • PFAAlert()[2LVL] = 1 • Increment internal PF 2LVL counter • Wait for PF 2LVL Delay time • Reset AFE |
| Trip | Internal PF 2LVL counter > Threshold AND Enabled PF 16–32[2LVL] = 1 | <ul style="list-style-type: none"> • PFAAlert()[2LVL] = 0 • PFStatus()[2LVL] = 1 |

5.21 PTC Permanent Fail

The device can detect overtemperature using a positive temperature coefficient (PTC) resistor connected to PTC pin. This protection also works in shutdown mode.

If the device detects PTC pin high state, the CHG and DSG FET are turned off. Pack is disabled permanently. State can only be reset by fully power cycle the device.

If PTC permanent fail is not used, the PTC pin should be connected to VSS with a 10-kΩ resistor.

| Status | Condition | Action |
|--------|---|---|
| Normal | Reset AFE and PTC pin = low AND no FUSE trigger by firmware | PFStatus()[PTC] = 0 |
| Trip | PTC pin = high | <ul style="list-style-type: none"> • PFStatus()[PTC] = 1 • FUSE = high |

5.22 Instruction Flash Checksum Permanent Fail

The device can permanently disable the battery in case it detects a difference between the stored IF checksum and the calculated IF checksum right after device reset.

| Status | Condition | Action |
|--------|--|--|
| Normal | Stored and calculated IF checksum match | PFAAlert()[IFC] = 0 |
| Trip | Stored and calculated IF checksum after reset don't match AND Enabled PF 16–32[IFC] = 1 | <ul style="list-style-type: none"> • PFAAlert()[IFC] = 0 • PFStatus()[IFC] = 1 |

5.23 Open Cell Voltage Connection Permanent Fail

The device can permanently disable the battery in case it detects a difference between the BAT pin voltage and the sum of the individual cell voltages.

| Status | Condition | Action |
|--------|---|--|
| Normal | Sum(Cell voltages in Voltages())—BAT voltage in Voltages()) < Threshold | PFAAlert()[OCECO] = 0 |
| Alert | Sum(Cell voltages in Voltages())—BAT voltage in Voltages()) ≥ Threshold | PFAAlert()[OCECO] = 1 |
| Trip | Sum(Cell voltages in Voltages())—BAT voltage in Voltages()) continuous ≥ Threshold for Delay Period AND Enabled PF 16–32[OCECO] = 1 | <ul style="list-style-type: none"> • PFAAlert()[OCECO] = 0 • PFStatus()[OCECO] = 1 |

5.24 Data Flash Permanent Fail

The device can permanently disable the battery in case a data flash write fails.

| Status | Condition | Action |
|--------|--|---|
| Normal | Data flash write ok | PFAAlert()[DFW] = 0 |
| Trip | Data flash write not successful AND Enabled PF 16–32[DFW] = 1 | <ul style="list-style-type: none"> • PFAAlert()[DFW] = 0 • PFFStatus()[DFW] = 1 |

Power Modes

To enhance battery life, the bq30z50-R1 and bq30z55-R1 supports different power modes to save power and minimize power consumption during operation.

6.1 Normal Mode

In Normal mode, the device takes voltage, current, and temperature readings every 250 ms, performs protection and gauging calculations, and updates SBS data. Between these periods of activity, the device is in a reduced power state.

6.2 Sleep Mode

6.2.1 Device Sleep

When the sleep conditions are met, the device goes to Sleep mode with periodic wake-ups to reduce power consumption. The device returns to Normal mode if SBS communication and current is detected.

| Status | Condition | Action |
|----------|--|---|
| Enable | System Configuration[SLEEP] = 1 | OperationStatus()[SLEEP] = 1 |
| Activate | System Configuration[NR] = 0 AND OperationStatus()[PRES] = 0 AND Current() < Sleep:Sleep Current AND SMBus clock and data lines low for 5 s. | <ul style="list-style-type: none"> Turn off CHG FET, DSG FET, PCHG FET Device goes to sleep Device wakes up every Sleep Voltage Time period to measure voltage and temperature Device wakes up every Sleep Current Time period to measure current |
| Activate | System Configuration[NR] = 1 AND Current() < Sleep:Sleep Current AND SMBus clock and data lines low for 5 s. | <ul style="list-style-type: none"> Turn off CHG FET, PHCG FET if System Configuration[SLEEPCHG] = 0 Device goes to sleep Device wakes up every Sleep Voltage Time period to measure voltage and temperature Device wakes up every Sleep Current Time period to measure current |
| Exit | System Configuration[NR] = 0 AND OperationStatus()[PRES] = 1 | Return to Normal mode |
| Exit | Current() > Sleep:Sleep Current | Return to Normal mode |
| Exit | SMBus clock and data lines high | Return to Normal mode |
| Exit | Wake comparator trips | Return to Normal mode |
| Exit | SafetyAlert() flag or PFAAlert() flag set | Return to Normal mode |

6.2.1.1 Wake Function

The device can exit Sleep mode, if enabled, by the presence of a voltage across SRP and SRN. The level of the current signal needed is programmed in *Power:Wake Current Reg.*

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Low Byte | RSVD | RSVD | RSVD | RSVD | RSVD | IWAKE | RSNS1 | RSNS0 |

Reserved (Bits 7–3): Reserved, do not use.

IWAKE (Bit 2):

0 = 0.5A (or if RSNS0=RSNS1=0 then this function is disabled)

1 = 1.0A (or if RSNS0=RSNS1=0 then this function is disabled)

| RSNS1 | RSNS0 | Resistance |
|-------|-------|--------------------|
| 0 | 0 | Disabled (default) |
| 0 | 1 | 2.5 mΩ |
| 1 | 0 | 5 mΩ |
| 1 | 1 | 10 mΩ |

6.2.2 ManufacturerAccess Sleep

The device can be sent to sleep with **ManufacturerAccess()** if the sleep conditions are met. This function is used to test sleep exit conditions.

6.3 Ship Mode

In Ship mode, the device enters a low power mode with no voltage, current, and temperature measurements.

6.3.1 Ship Hibernate Mode

In Ship Hibernate mode, the device enters a low-power mode with no voltage, current, and temperature measurements, the FETs are turned off, and the MCU is in a halt state. The device will return to Normal mode on SBS communication detection. The device can be configured to ship hibernate with discharge FET on through Settings: System Configuration[SHIPDSG]. The device can be sent to this mode with **ManufacturerAccess()** Ship command.

6.3.2 Ship Shutdown Mode

In Ship Shutdown mode, the device shuts down to minimize power consumption, and the FETs are turned off. The device will return to Normal mode when voltage at PACK pin > VSTARTUP. The device can be sent to this mode with the **ManufacturerAccess()** **Shutdown** command. Charger voltage must not be present for the device to enter Ship Shutdown mode.

6.4 Shutdown Mode

6.4.1 Voltage Based Shutdown

The device can be configured to shutdown at a programmable stack voltage threshold to minimize power consumption and avoid draining the battery. This function also works in Permanent Failure mode to prevent polymer cell swelling.

| Status | Condition | Action |
|----------|---|---|
| Enable | Min(Cell Voltage in Voltages()) < Shutdown Voltage | OperationStatus()[SDV]= 1 |
| Activate | Min(Cell Voltage in Voltages()) continuous < Shutdown Voltage for Shutdown Time | The device disables everything and turns off. |
| Exit | Voltage at PACK pin > VSTARTUP | <ul style="list-style-type: none"> OperationStatus()[SDV]= 0 Return to Normal mode |

Gauging

7.1 Impedance Track

The device features the most advanced Impedance Track gauging algorithm v3.75, and is capable of supporting a maximum battery pack capacity of 32 Ah. The algorithm estimates run time and capacity.

The Impedance Track algorithm v3.75 features the following:

- Cell balancing during relax (CBR)
- Ability to learn Qmax without a rest period following the end of discharge (FAST_QMax)
- Compatible with LiFePO4 chemistries (LFP_RELAX)
- Greatly improved low temperature accuracy
- Greatly improved RSOC convergence to 0% at EDV (RSOC_CONV)
- Detailed status information via SBS for convenient debug and evaluation (no GG logging necessary)
 - DOD0
 - Qpassed
 - Grid numbers
 - Ra calculations
 - Balance timers
- Option to apply low pass filter smoothing to RemCap and FCC (SMOOTH)
- Option to prevent RSOC jumps during discharge (RSOC_HOLD)

7.2 Gas Gauge Mode

| Status | Condition | Action |
|-----------|---|---|
| Charge | Current() > Chg Current Threshold | <ul style="list-style-type: none"> • GaugingStatus()[DSG] = 0 • GaugingStatus()[REST] = 0 |
| Relax | GaugingStatus()[DSG] = 0–1 transition AND Current() < Quit Current Threshold for Chg Relax Time | <ul style="list-style-type: none"> • GaugingStatus()[DSG] = 1 • GaugingStatus()[REST] = 1, if: • DOD0 updated and • OCV updated and • QMax updated |
| Relax | GaugingStatus()[DSG] = 1–0 transition AND Current() < Quit Current Threshold for Dsg Relax Time | <ul style="list-style-type: none"> • GaugingStatus()[DSG] = 1 • GaugingStatus()[REST] = 1, if: • DOD0 updated and • OCV updated and • QMax updated |
| Discharge | Current() < (–) Dsg Current Threshold | <ul style="list-style-type: none"> • GaugingStatus()[DSG] = 1 • GaugingStatus()[REST] = 0 • RA update |

LED Display

The device has a LED display that can show various status information.

| Status | Condition | Action |
|----------|---|---|
| Activate | High—low transition of DISP pin | <ul style="list-style-type: none"> LED Display shows state of charge for LED Support:LED Hold Time LED Display shows each active PF code for 2x LED Hold Time if Settings:LED Configuration[LEDPF1][LEDPF0] = 0,1 |
| Activate | Settings:LED Configuration[LEDR] = 1 AND device reset | <ul style="list-style-type: none"> LED Display shows state of charge for LEDSupport:LED Hold Time LED Display shows each active PF code for 2x LED Hold Time if Settings:LED Configuration[LEDPF1][LEDPF0] = 0,1 |
| Activate | Settings:LED Configuration[LEDRCA] = 1 AND BatteryStatus[RCA] 0 to 1 transition | LED Display flashes with LED Flash Rate |
| Activate | Settings:LED Configuration[LEDCHG] = 1 AND Current() > 0 | <ul style="list-style-type: none"> LED Display shows state of charge for LEDSupport:LED Hold Time LED Display shows each active PF code for 2x LED Hold Time if Settings:LED Configuration[LEDPF1][LEDPF0] = 0,1 |
| Activate | ManufacturerStatus()=0x002C | <ul style="list-style-type: none"> LED Display shows state of charge for LED Support:LED Hold Time LED Display shows each active PF code for 2x LED Hold Time if Settings:LED Configuration[LEDPF1][LEDPF0] = 0,1 |
| Toggle | ManufacturerStatus()=0x002B | Toggle LED on or off |
| Disabled | SafetyStatus()[CUV] = 1 | LED Display Disabled |

8.1 LED Display State of Charge

The state of charge can display **RelativeStateOfCharge()** or **(AbsoluteStateOfCharge() / DesignCapacity())**, selectable with Settings:LED Configuration[LEDMODE]. All data flash settings are available through LED Support:LED Config subclass.

| | State of Charge | |
|-------------|----------------------|----------------------|
| | Current() > 0 | Current() <= 0 |
| Flash Alert | 0% – CHG Flash Alarm | 0% – DSG Flash Alarm |
| LED1 | CHG Thresh 1 – 100% | DSG Thresh 1 – 100% |
| LED2 | CHG Thresh 2 – 100% | DSG Thresh 2 – 100% |
| LED3 | CHG Thresh 3 – 100% | DSG Thresh 3 – 100% |
| LED4 | CHG Thresh 4 – 100% | DSG Thresh 4 – 100% |
| LED5 | CHG Thresh 5 – 100% | DSG Thresh 5 – 100% |

8.2 LED Display PF Codes

Each active PF code is shown for 2x **LED Hold Time** with lowest priority to highest priority.

| PF Flag | Priority | LED3 | LED2 | LED1 |
|----------|----------|------------------|------------------|------------------|
| No PF | 0 | LED Blink Period | off | off |
| CUV | 0 | LED Blink Period | on | off |
| COV | 1 | LED Blink Period | LED Flash Period | off |
| CUDEP | 2 | Fast Blink | off | on |
| OTCE | 3 | LED Blink Period | LED Flash Period | on |
| OTF | 4 | LED Blink Period | On | LED Flash Period |
| QIM | 5 | LED Blink Period | LED Flash Period | LED Flash Period |
| CB | 6 | LED Blink Period | off | LED Blink Period |
| IMP | 7 | LED Blink Period | on | LED Blink Period |
| CD | 8 | LED Flash Period | LED Blink Period | off |
| VIMR | 9 | off | LED Blink Period | off |
| VIMA | 10 | on | LED Blink Period | off |
| CFETF | 11 | LED Flash Period | LED Blink Period | LED Flash Period |
| DFETF | 12 | off | LED Blink Period | LED Flash Period |
| THERM | 13 | on | LED Blink Period | LED Flash Period |
| FUSE | 14 | LED Flash Period | LED Blink Period | LED Blink Period |
| AFE_P | 15 | off | LED Blink Period | LED Blink Period |
| AFE_C | 16 | on | off | LED Blink Period |
| 2LVL | 17 | LED Flash Period | off | LED Blink Period |
| Reserved | 18 | off | off | LED Blink Period |
| Reserved | 19 | on | on | LED Blink Period |
| OCECO | 20 | LED Flash Period | on | LED Blink Period |
| DFW | 21 | off | on | LED Blink Period |

Lifetime Data Collection

The device has extensive capabilities logging events over life of battery useful for analysis. The data is collected in RAM and only written DF under following conditions to avoid wear out of flash:

- Every 10 hours if RAM content is different from flash
- In permanent fail, before data flash updates are disabled
- A reset counter increments
- Before scheduled shutdown
- Before low voltage shutdown

The lifetime data stops collecting under following conditions:

- After permanent fail
- Lifetime Data collection is disabled

Total firmware Runtime starts when lifetime data is enabled.

- Voltage
 - Max/Min Cell Voltage Each Cell
 - Max Delta Voltage
- Current
 - Max Charge/Discharge Current
 - Max Average Discharge Current
 - Max Average Discharge Power
- Safety Events (12 most common are tracked)
 - Number of Safety Events
 - Cycle Count at Last Safety Event(s)
- Charging Events
 - Number of Valid Charge Terminations
 - Cycle Count at Last Charge Termination
- Gauging Events
 - Number of QMax updates
 - Cycle Count at Last QMax update
 - Number of RA updates
 - Cycle Count at Last RA update
- Power Events: Number of Resets
- Cell Balancing
 - Cell Balancing Time each Cell
- Temperature
 - Max/Min Cell Temp
 - Delta Cell Temp
 - Max/Min Int Temp Sensor
 - Max FET Temp
- Time

- Total runtime
- Time spent different temperature ranges

Device Security

10.1 Description

The device uses SHA-1 one way has function for device authentication by host system. Unseal or Full Access mode is also protected using SHA-1 authentication.

10.2 SHA-1 Description

The SHA-1 is known as a one-way hash function, meaning there is no known mathematical method of computing the input given only the output. The specification of the SHA-1, as defined by FIPS 180–2, states that the input consists of 512 bit blocks with a total input length less than 264 bits. Inputs which do not conform to integer multiples of 512 bit blocks are padded before any block is input to the hash function. The SHA-1 algorithm outputs 160 bits, commonly referred to as the digest.

(As of April 23, 2004 the latest revision is FIPS 180–2). SHA-1 or secure hash algorithm is used to compute a condensed representation of a message or data also known as hash. For messages $< 2^{64}$ the SHA-1 produces an 160-bit output called digest.

The device generates an SHA-1 input block of 288 bits (total input = 160 bit message + 128 bit key). To complete the 512 bit block size requirement of the SHA-1, the device pads the key and message with a 1, followed by 159 0's, followed by the 64 bit value for 288 (000...00100100000), which conforms to the pad requirements specified by FIPS 180–2.

Detailed information about the SHA-1 algorithm can be found:

1. <http://www.itl.nist.gov/fipspubs/fip180-1.htm>
2. <http://csrc.nist.gov/publications/fips>
3. www.faqs.org/rfcs/rfc3174.html

10.3 HMAC Description

The SHA-1 engine is used to calculate a modified HMAC value. Using a public message and a secret key, the HMAC output is considered to be a secure fingerprint that authenticates the device used to generate the HMAC.

To compute the HMAC let H designate the SHA-1 hash function, M designate the message transmitted to the device, and KD designate the unique 128 bit unseal/full access/authentication key of the device. HMAC(M) is defined as:

$H[KD || H(KD || M)]$, where || symbolizes an append operation

The message, M, is appended to the unseal/full access/authentication key, KD, and padded to become the input to the SHA-1 hash. The output of this first calculation is then appended to the unseal/full access/authentication key, KD, padded again, and cycled through the SHA-1 hash a second time. The output is the HMAC digest value.

10.4 Authentication

1. Generate 160-bit message M using a random number generator that meets approved random number generators described in FIPS PUB 140–2
2. Generate SHA-1 input block B1 of 512 bytes (total input = 128-bit authentication key KD + 160 bit message M + 1 + 159 0s + 100100000)
3. Generate SHA-1 hash HMAC1 using B1.

4. Generate SHA-1 input block B2 of 512 bytes (total input =128-bit authentication key KD + 160 bit hash HMAC1 + 1 + 159 0s + 100100000)
5. Generate SHA-1 hash HMAC2 using B2.
6. With no active **ManufacturerInput()** data waiting, write 160-bit message M to **ManufacturerInput()** in the format 0xAABBCCDDEEFFGGHHIIJJKLLMMNNOOPPQQRRSSTT, where AA is LSB
7. Wait 250 ms, then read ManufacturerInput() for HMAC3.
8. Compare host HMAC2 with device HMAC3, it matches, both host and device have the same key KD and device is authenticated.

10.5 Unseal/Full Access

1. Send Unseal (0x0031) or Full Access (0x0032) command to **ManufacturerAccess()**.
2. Read 160-bit message M from **ManufacturerInput()** in the format 0xAABBCCDDEEFFGGHHIIJJKLLMMNNOOPPQQRRSSTT, where AA is LSB
3. Generate SHA-1 input block B1 of 512 bytes (total input =128-bit unseal/full access key KD + 160 bit message M + 1 + 159 0s + 100100000)
4. Generate SHA-1 hash HMAC1 using B1.
5. Generate SHA-1 input block B2 of 512 bytes (total input =128-bit unseal/full access key KD + 160 bit hash HMAC1 + 1 + 159 0s + 100100000)
6. Generate SHA-1 hash HMAC2 using B2.
7. Write 160-bit hash HMAC2 to **ManufacturerInput()** in the format 0xAABBCCDDEEFFGGHHIIJJKLLMMNNOOPPQQRRSSTT, where AA is LSB
8. Device compares hash HMAC2 with internal calculated hash HMAC3. If it matches, device allows unsealed/full access mode indicated with the **OperationStatus()**[SEC1],[SEC0] flags.

SBS Commands

11.1 0x00 ManufacturerAccess()

The **ManufacturerAccess()** command has several functions depending on the data written to this command.

11.1.1 0x0000 ManufacturerData

This command returns **ManufacturerData()** information.

| Status | Condition | Action |
|----------|---------------------------------------|---|
| Activate | 0x0000 to ManufacturerAccess() | Output ManufacturerData() on ManufacturerData() |

11.1.2 0x0001 Device Type

The device can be checked for the IC part number.

| Status | Condition | Action |
|--------|---------------------------------------|---|
| Enable | 0x0001 to ManufacturerAccess() | <ul style="list-style-type: none"> Returns the IC part number on subsequent read on ManufacturerData() in the following format: aaAA, where: aaAA: device type |

11.1.3 0x0002 Firmware Version

The device can be checked for the firmware version of the IC.

| Status | Condition | Action |
|--------|--|--|
| Enable | 0x0002 to ManufacturerAccess() | <ul style="list-style-type: none"> Returns the firmware revision on ManufacturerData() in the following format: ddDDvvVVbbBBttzzZZRREE, where: ddDD: Device Number vvVV: Version bbBB: build number tt: Firmware type zzZZ: Impedance Track Version RR: reserved EE: reserved |
| Enable | Write following sequence within 4 seconds; also works in sealed mode: <ol style="list-style-type: none"> Block write to 0x22 with block size 62 Block write to 0x20 with block size 62 Block write to 0x22 with block size 62 | <ul style="list-style-type: none"> Returns the firmware revision on ManufacturerData() in the following format: ddDDvvVVbbBBttzzZZRREE, where: ddDD: Device Number vvVV: Version bbBB: build number tt: Firmware type zzZZ: Impedance Track Version RR: reserved EE: reserved |

11.1.4 0x0003 Hardware Version

The device can be checked for the hardware version of the IC.

| Status | Condition | Action |
|--------|---------------------------------------|---|
| Enable | 0x0003 to ManufacturerAccess() | Returns the hardware revision on subsequent read on ManufacturerData() |

11.1.5 0x0004 Instruction Flash Checksum

The device can return the instruction flash checksum.

| Status | Condition | Action |
|--------|---------------------------------------|---|
| Enable | 0x0004 to ManufacturerAccess() | Returns the IF checksum on subsequent read on ManufacturerData() after a wait time of 250 ms |

11.1.6 0x0005 Data Flash Checksum

The device can return the data flash checksum.

| Status | Condition | Action |
|--------|---------------------------------------|--|
| Enable | 0x0005 to ManufacturerAccess() | Returns the DF checksum on subsequent read on ManufacturerData() after a wait time of 250 ms. Only static DF items are included in the checksum. No items modified by the device or items that are different device to device are included. |

11.1.7 0x0006 Chemical ID

This command returns the chemical ID of the OCV tables used in the gauging algorithm.

| Status | Condition | Action |
|--------|---------------------------------------|---|
| Enable | 0x0006 to ManufacturerAccess() | Returns the chemical ID on subsequent read on ManufacturerData() |

11.1.8 0x0010 Shutdown Mode

The device can be sent to shutdown mode before shipping to reduce power consumption to a minimum. The device will wake up when a voltage is applied to PACK.

| Status | Condition | Action |
|--------|---|---|
| Normal | OperationStatus() [SH] = 0 | |
| Enable | 0x0010 to ManufacturerAccess; when sealed, two times in a row | OperationStatus() [SD] = 1 |
| Trip | [NR] = 1 AND Current() = 0 AND Voltage on PACK = 0 | FETs are turned off after Power:Shutdown time. Device will enter shutdown mode after another passage of Power:Shutdown time. (i.e. 2x of the Shutdown time after the command is set and 1x of the Shutdown time after the FETs are off) |
| Trip | Delay after command is sent > Power:Shutdown Time | No charging or discharging is allowed; device is shutdown. |

11.1.9 0x0011 Sleep Mode

The device can be send to sleep with **ManufacturerAccess()** if the sleep conditions are met.

| Status | Condition | Action |
|----------|--|--|
| Enable | 0x0011 to ManufacturerAccess() | OperationStatus() [SLEEPM] = 1 |
| Activate | Settings:System Configuration[NR] = 0 AND OperationStatus() [PRES] = 0 AND Current() < Power:Sleep Current | <ul style="list-style-type: none"> Turn off CHG FET, DSG FET, PCHG FET Device goes to sleep Device wakes up every Power:Sleep Voltage Time period to measure voltage and temperature Device wakes up every Power:Sleep Current Time period to measure current |
| Activate | Settings:System Configuration:System[NR] = 1 AND Current() < Power:Sleep Current | <ul style="list-style-type: none"> Turn off DSG FET, PCHG FET Turn off CHG FET if Settings:System Configuration[SLEEPCHG] = 0 Device goes to sleep Device wakes up every Power:Sleep Voltage Time period to measure voltage and temperature Device wakes up every Power:Sleep Current Time period to measure current |
| Exit | Settings:System Configuration[NR] = 0 AND OperationStatus() [PRES] = 1 | <ul style="list-style-type: none"> OperationStatus()[SLEEPM] = 0 Return to Normal mode |
| Exit | Current() > Power:Sleep Current | <ul style="list-style-type: none"> OperationStatus()[SLEEPM] = 0 Return to Normal mode |
| Exit | Wake Comparator trips | <ul style="list-style-type: none"> OperationStatus()[SLEEPM] = 0 Return to Normal mode |
| Exit | SafetyAlert() flag or PFAAlert() flag set | <ul style="list-style-type: none"> OperationStatus()[SLEEPM] = 0 Return to Normal mode |

11.1.10 0x0012 Device Reset

This command resets the device.

| Status | Condition | Action |
|--------|---------------------------------------|------------------|
| Enable | 0x0012 to ManufacturerAccess() | Reset the device |

11.1.11 0x001d Fuse Toggle

This command activate/deactivate FUSE pin for ease of manufacturing testing.

| Status | Condition | Action |
|---------|---|---|
| Disable | OperationStatus() [FUSE] = 1 AND 0x001d to ManufacturerAccess() | <ul style="list-style-type: none"> OperationStatus()[FUSE] = 0 FUSE pin drive low |
| Enable | OperationStatus() [FUSE] = 0 AND 0x001d to ManufacturerAccess() | <ul style="list-style-type: none"> OperationStatus()[FUSE] = 1 FUSE pin drive high |

11.1.12 0x001e PRE-CHG FET

This command turns on/off Pre-CHG FET drive function to ease testing during manufacturing.

| Status | Condition | Action |
|---------|--|--|
| Disable | ManufacturingStatus() [FET][PCHG] = 0,1 AND 0x001e to ManufacturerAccess() | <ul style="list-style-type: none"> ManufacturingStatus()[FET][PCHG] = 0,0 precharge function defined with PCHG1,PCHG0 turns off |
| Enable | ManufacturingStatus() [FET][PCHG] = 0,0 AND 0x001e to ManufacturerAccess() | <ul style="list-style-type: none"> ManufacturingStatus()[FET][PCHG] = 0,1 precharge function defined with PCHG1,PCHG0 turns on |

11.1.13 0x001f CHG FET

This command turns on/off CHG FET drive function to ease testing during manufacturing.

| Status | Condition | Action |
|---------|--|--|
| Disable | ManufacturingStatus() [FET][CHG] = 0,1 AND 0x001f to ManufacturerAccess() | <ul style="list-style-type: none"> • ManufacturingStatus() [FET][CHG] = 0,0 • CHG FET turns off |
| Enable | ManufacturingStatus() [FET][CHG] = 0,0 AND 0x001f to ManufacturerAccess() | <ul style="list-style-type: none"> • ManufacturingStatus() [FET][CHG] = 0,1 • CHG FET turns on |

11.1.14 0x0020 DSG FET

This command turns on/off DSG FET drive function to ease testing during manufacturing.

| Status | Condition | Action |
|---------|--|--|
| Disable | ManufacturingStatus() [FET][DSG] = 0,1 AND 0x0020 to ManufacturerAccess() | <ul style="list-style-type: none"> • ManufacturingStatus() [FET][DSG] = 0,0 • DSG FET turns off |
| Enable | ManufacturingStatus() [FET][DSG] = 0,0 AND 0x0020 to ManufacturerAccess() | <ul style="list-style-type: none"> • ManufacturingStatus() [FET][DSG] = 0,1 • DSG FET turns on |

11.1.15 0x0021 Gauging

This command enables or disable the gauging function to ease testing during manufacturing.

| Status | Condition | Action |
|---------|---|---|
| Disable | ManufacturingStatus() [Gauge] = 1 AND 0x0021 to ManufacturerAccess() | <ul style="list-style-type: none"> • ManufacturingStatus() [Gauge] = 0 • disable gauging feature |
| Enable | ManufacturingStatus() [Gauge] = 0 AND 0x0021 to ManufacturerAccess() | <ul style="list-style-type: none"> • ManufacturingStatus() [Gauge] = 1 • Enable gauging feature |

11.1.16 ManufacturerAccess() 0x0022 FET Control

This command enables/disables control of the CHG, DSG, and PCHG FET by the firmware.

| Status | Condition | Action |
|---------|---|--|
| Disable | ManufacturingStatus() [FET] = 1 AND 0x0022 to ManufacturerAccess() | <ul style="list-style-type: none"> • ManufacturingStatus() [FET] = 0 • CHG, DSG and PCHG FET are disabled and remain OFF |
| Enable | ManufacturingStatus() [FET] = 0 AND 0x0022 to ManufacturerAccess() | <ul style="list-style-type: none"> • ManufacturingStatus() [FET] = 1 • CHG, DSG and PCHG FET are controlled by the firmware |

11.1.17 ManufacturerAccess() 0x0023 Lifetime Data Collection

This command enables/disables Lifetime data collection for ease of manufacturing.

| Status | Condition | Action |
|---------|--|--|
| Disable | ManufacturingStatus() [LF] = 1 AND 0x0023 to ManufacturerAccess() | <ul style="list-style-type: none"> • ManufacturingStatus() [LF] = 0 • Lifetime Data collection feature disabled |
| Enable | ManufacturingStatus() [LF] = 0 AND 0x0023 to ManufacturerAccess() | <ul style="list-style-type: none"> • ManufacturingStatus() [LF] = 1 • Lifetime Data collection feature enabled |

11.1.18 ManufacturerAccess() 0x0024 Permanent Failure

This command enables/disables Permanent Failure for ease of manufacturing.

| Status | Condition | Action |
|---------|---|--|
| Disable | ManufacturingStatus()[PF] = 1 AND 0x0024 to ManufacturerAccess() | <ul style="list-style-type: none"> • ManufacturingStatus()[PF] = 0 • Permanent Failure feature disabled |
| Enable | ManufacturingStatus()[PF] = 0 AND 0x0024 to ManufacturerAccess() | <ul style="list-style-type: none"> • ManufacturingStatus()[PF] = 1 • Permanent Failure feature enabled |

11.1.19 ManufacturerAccess() 0x0025 Black Box Recorder

This command enables/disables Black box recorder function for ease of manufacturing.

| Status | Condition | Action |
|---------|--|--|
| Disable | ManufacturingStatus()[BBR] = 1 AND 0x0025 to ManufacturerAccess() | <ul style="list-style-type: none"> • ManufacturingStatus()[BBR] = 0 • Black Box Recorder feature disabled |
| Enable | ManufacturingStatus()[BBR] = 0 AND 0x0025 to ManufacturerAccess() | <ul style="list-style-type: none"> • ManufacturingStatus()[BBR] = 1 • Black Box Recorder feature enabled |

11.1.20 ManufacturerAccess() 0x0026 Fuse

This command enables/disables firmware fuse toggle function for ease of manufacturing.

| Status | Condition | Action |
|---------|---|--|
| Disable | ManufacturingStatus()[FUSE] = 1 AND 0x0026 to ManufacturerAccess() | <ul style="list-style-type: none"> • ManufacturingStatus()[FUSE] = 0 • FUSE pin action disabled |
| Enable | ManufacturingStatus()[FUSE] = 0 AND 0x0026 to ManufacturerAccess() | <ul style="list-style-type: none"> • ManufacturingStatus()[FUSE] = 1 • FUSE pin action enabled |

11.1.21 ManufacturerAccess() 0x0027 LED Enable

This command enables/disables LED Display function for ease of manufacturing.

| Status | Condition | Action |
|---------|---|---|
| Disable | ManufacturingStatus() [LED] = 1 AND 0x0027 to ManufacturerAccess() | <ul style="list-style-type: none"> • ManufacturingStatus() [LED] = 0 • LED Display action disabled |
| Enable | ManufacturingStatus() [LED] = 0 AND 0x0027 to ManufacturerAccess() | <ul style="list-style-type: none"> • ManufacturingStatus() [LED] = 1 • LED Display action enabled |

11.1.22 ManufacturerAccess() 0x0028 Lifetime Data Reset

This command resets Lifetime data in data flash for ease of manufacturing.

| Status | Condition | Action |
|--------|---------------------------------------|---------------------------|
| Reset | 0x0028 to ManufacturerAccess() | Clear Lifetime Data in DF |

11.1.23 ManufacturerAccess() 0x0029 Permanent Fail Data Reset

This command resets PF data in data flash for ease of manufacturing.

| Status | Condition | Action |
|--------|---------------------------------------|---------------------|
| Reset | 0x0029 to ManufacturerAccess() | Clear PF Data in DF |

11.1.24 ManufacturerAccess() 0x002a Black Box Recorder Reset

This command resets the black box recorder data in data flash for ease of manufacturing.

| Status | Condition | Action |
|--------|---------------------------------------|-------------------------------------|
| Reset | 0x002a to ManufacturerAccess() | Clear Black Box Recorder data in DF |

11.1.25 ManufacturerAccess() 0x002b LED Toggle

This command activate/deactivate configured LEDs for ease of manufacturing testing.

| Status | Condition | Action |
|---------|---|--|
| Disable | OperationStatus() [LED] = 1 AND 0x002b to ManufacturerAccess() | <ul style="list-style-type: none"> • OperationStatus() [LED] = 0 • LED disabled |
| Enable | OperationStatus() [LED] = 0 AND 0x002b to ManufacturerAccess() | <ul style="list-style-type: none"> • OperationStatus() [LED] = 1 • LED enabled |

11.1.26 ManufacturerAccess() 0x002c LED Display On

This command simulates low-high-low detection on the /DISP pin for ease of manufacturing testing.

| Status | Condition | Action |
|----------|---------------------------------------|--|
| Activate | 0x002c to ManufacturerAccess() | Simulates low-high-low detection on the $\overline{\text{DISP}}$ pin |

11.1.27 ManufacturerAccess() 0x002D CAL Mode

This command enables output of the raw ADC and CC data on **ManufacturerData()**.

| Status | Condition | Action |
|---------|---|---|
| Disable | ManufacturingStatus() [CAL] = 1 AND 0x002D to ManufacturerAccess() | <ul style="list-style-type: none"> ManufacturingStatus() [CAL] = 0 disable output of ADC and CC raw data on ManufacturingData() |
| Enable | ManufacturingStatus() [CAL] = 0 AND 0x002D to ManufacturerAccess() | <ul style="list-style-type: none"> ManufacturingStatus() [CAL] = 1 Enable output of ADC and CC raw data on ManufacturingData(), controllable with 0xF081 and 0xF082 on ManufacturerAccess() |

11.1.28 ManufacturerAccess() 0x0030 Seal Device

This command seals the device for the field, disabling certain SBS commands and access to DF.

| Status | Condition | Action |
|--------|---|--|
| Sealed | OperationStatus() [SEC1, SEC0] = 0,1 or 1,0 AND 0x0030 to ManufacturerAccess() | <ul style="list-style-type: none"> OperationStatus() [SEC1, SEC0] = 1,1 Certain SBS Commands not available, see SBS table for details |

11.1.29 ManufacturerAccess() 0x0031 UnSeal Device

This command unseals the device after valid SHA-1 authentication.

| Status | Condition | Action |
|----------|--|--|
| Initiate | OperationStatus() [SEC1, SEC0] = 1,1 AND 0x0031 to ManufacturerAccess() | <ul style="list-style-type: none"> OperationStatus() [AUTH] = 1 160-bit random number message available at ManufacturerInput() in the format 0xAABBCCDDEEFFGGHHIIJJKLLMMNNOOPPQQRRSSTTT, where AA is LSB |
| Unseal | Correct 160-bit HMAC digest computed with random number + Unseal Key written to ManufacturerInput() in the format 0xAABBCCDDEEFFGGHHIIJJKLLMMNNOOPP, where AA is LSB | <ul style="list-style-type: none"> OperationStatus() [SEC1, SEC0] = 0,1 OperationStatus() [AUTH] = 0 device unsealed after 250 ms, for available SBS commands in unseal mode see SBS table. |
| Invalid | incorrect 160-bit hash written to ManufacturerInput() | <ul style="list-style-type: none"> wait time 250 ms OperationStatus() [SEC1, SEC0] = 0,0 OperationStatus() [AUTH] = 0 |

11.1.30 ManufacturerAccess() 0x0032 Full Access Device

This command enable Full Access to the device after valid SHA-1 authentication.

| Status | Condition | Action |
|-------------|---|--|
| Initiate | OperationStatus() [SEC1, SEC0] = 1,1 or 1,0 AND 0x0032 to ManufacturerAccess() | <ul style="list-style-type: none"> OperationStatus() [AUTH] = 1 160-bit random number message available at ManufacturerInput() in the format 0xAABBCCDDEEFFGGHHIIJJKLLMMNNOOPPQQRRSSTTT, where AA is LSB |
| Full Access | Correct 160-bit HMAC digest computed with random number + Full Access Key written to ManufacturerInput() in the format 0xAABBCCDDEEFFGGHHIIJJKLLMMNNOOPP, where AA is LSB | <ul style="list-style-type: none"> OperationStatus() [SEC1, SEC0] = 1,1 OperationStatus() [AUTH] = 0 device enables full access after 250 ms, for available SBS commands in full access mode see SBS table. |
| Invalid | Incorrect 160-bit hash written to ManufacturerInput() | <ul style="list-style-type: none"> wait time 250 ms OperationStatus() [SEC1, SEC0] = 0,0 OperationStatus() [AUTH] = 0 |

11.1.31 ManufacturerAccess() 0x0033 ROM Mode

This command enables the ROM mode for IF update.

| Status | Condition | Action |
|----------|--|---|
| ROM Mode | OperationStatus() [SEC1,SEC0] = 1,0 AND 0x0033 to ManufacturerAccess() | Device goes to ROM mode ready for update, use 0x08 to ManufacturerAccess() to return |

11.1.32 ManufacturerAccess() 0x0034 Ship Mode

In ship mode the device enters a low power mode with no voltage, current and temperature measurements, FETs turned off and MCU in a halt state. The device will return to Normal mode on SBS communication detection.

| Status | Condition | Action |
|----------|---|---|
| Enable | 0x0034 to ManufacturerAccess() | OperationStatus() [SHIPM] = 1 |
| Activate | Current() < Power: Sleep Current AND No SBS communication for power: Ship Mode Com Delay | <ul style="list-style-type: none"> • Turn off CHG FET, PCHG FET • Turn off DSG FET, if Settings:System Configuration[SHIPDSG]=0 • No Voltage, Temperature or Current Measurements • No Gauging • MCU in halt state HFO turned off. |
| Exit | SBS communication to device | <ul style="list-style-type: none"> • OperationStatus()[SHIPM] = 0 • Return to Normal mode |

11.1.33 ManufacturerAccess() 0x0035 Unseal Key

This command enters a new Unseal key into the device.

| Status | Condition | Action |
|-----------|---|---|
| initiate | OperationStatus() [SEC1,SEC0] = 1,0 AND 0x0035 to ManufacturerAccess() | <ul style="list-style-type: none"> • OperationStatus()[AUTH] = 1 • 160-bit random number message available at ManufacturerInput() in the format 0xAABBCCDDEEFFGGHHIIJJKKLLMMNN OOPP QRRSSTTT, where AA is LSB |
| Enter Key | Correct 128-bit Key written to ManufacturerInput() in the format 0xAABBCCDDEEFFGGHHIIJJKKLLMMNN OOPP, where AA is LSB | <ul style="list-style-type: none"> • Wait time 250 ms • OperationStatus()[AUTH] = 0 • device returns 160-bit digest at ManufacturerInput() in the format 0xAABBCCDDEEFFGGHHIIJJKKLLMMNN OOPP QRRSSTTT, where AA is LSB. Digest was calculated using the random number + key. compare with own calculations check validity of key. |

11.1.34 ManufacturerAccess() 0x0036 Full Access Key

This command enters a new Full Access key into the device.

| Status | Condition | Action |
|----------|--|--|
| initiate | OperationStatus() [SEC1,SEC0] = 1,0 AND 0x0036 to ManufacturerAccess() | <ul style="list-style-type: none"> • OperationStatus()[AUTH] = 1 • 160-bit random number available at ManufacturerInput() |

| Status | Condition | Action |
|-----------|--|--|
| Enter Key | Correct 128-bit Key written to ManufacturerInput() in the format 0xAABBCCDDEEFFGGHHIIJJKLLMMNNO OPP, where AA is LSB | <ul style="list-style-type: none"> Wait time 250 ms OperationStatus()[AUTH] = 0 device returns 160-bit digest at ManufacturerInput() in the format 0xAABBCCDDEEFFGGHHIIJJKLLMMNNOOPP QRRRSSTTT, where AA is LSB. Digest was calculated using the random number + key. compare with own calculations check validity of key. |

11.1.35 ManufacturerAccess() 0x0037 Authentication Key

This command enters a new authentication key into the device.

| Status | Condition | Action |
|-----------|--|---|
| Initiate | OperationStatus() [SEC1,SEC0] = 1,0 AND 0x0037 to ManufacturerAccess() | <ul style="list-style-type: none"> OperationStatus()[AUTH] = 1 160-bit random number available at ManufacturerInput() |
| Enter Key | Correct 128-bit Key written to ManufacturerInput() in the format 0xAABBCCDDEEFFGGHHIIJJKLLMMNNO OPP, where AA is LSB | <ul style="list-style-type: none"> Wait time 250 ms OperationStatus()[AUTH] = 0 device returns 160-bit HMAC digest at ManufacturerInput() in the format 0xAABBCCDDEEFFGGHHIIJJKLLMMNNOOPP QRRRSSTTT, where AA is LSB. The HMAC digest was calculated using the random number + key. Compare with own calculations check validity of key. |

11.1.36 ManufacturerAccess() 0x0050 SafetyAlert

This command returns the SafetyAlert() flags on **ManufacturerData()**.

| Status | Condition | Action |
|----------|---------------------------------------|---|
| Activate | 0x0050 to ManufacturerAccess() | Output SafetyAlert() flags on ManufacturerData() |

11.1.37 ManufacturerAccess() 0x0051 SafetyStatus

This command returns the SafetyStatus() flags on **ManufacturerData()**.

| Status | Condition | Action |
|----------|---------------------------------------|--|
| Activate | 0x0051 to ManufacturerAccess() | Output SafetyStatus() flags on ManufacturerData() |

11.1.38 ManufacturerAccess() 0x0052 PFAAlert

This command returns the PFAAlert() flags on **ManufacturerData()**.

| Status | Condition | Action |
|----------|---------------------------------------|--|
| Activate | 0x0052 to ManufacturerAccess() | Output PFAAlert() flags on ManufacturerData() |

11.1.39 ManufacturerAccess() 0x0053 PFStatus

This command returns the PFStatus() flags on **ManufacturerData()**.

| Status | Condition | Action |
|----------|---------------------------------------|--|
| Activate | 0x0053 to ManufacturerAccess() | Output PFStatus() flags on ManufacturerData() |

11.1.40 **ManufacturerAccess() 0x0054 OperationStatus**

This command returns the **OperationStatus()** flags on **ManufacturerData()**.

| Status | Condition | Action |
|----------|---------------------------------------|--|
| Activate | 0x0054 to ManufacturerAccess() | Output OperationStatus() flags on ManufacturerData() |

11.1.41 **ManufacturerAccess() 0x0055 ChargingStatus**

This command returns the **ChargingStatus()** flags on **ManufacturerData()**.

| Status | Condition | Action |
|----------|---------------------------------------|---|
| Activate | 0x0055 to ManufacturerAccess() | Output ChargingStatus() flags on ManufacturerData() |

11.1.42 **ManufacturerAccess() 0x0056 GaugingStatus**

This command returns the **GaugingStatus()** flags on **ManufacturerData()**.

| Status | Condition | Action |
|----------|---------------------------------------|--|
| Activate | 0x0056 to ManufacturerAccess() | Output GaugingStatus() flags on ManufacturerData() |

11.1.43 **ManufacturerAccess() 0x0057 ManufacturingStatus**

This command returns the **ManufacturingStatus()** flags on **ManufacturerData()**.

| Status | Condition | Action |
|----------|---------------------------------------|--|
| Activate | 0x0057 to ManufacturerAccess() | Output ManufacturingStatus() flags on ManufacturerData() |

11.1.44 **ManufacturerAccess() 0x0058 AFE Register**

This command returns the **AFERegister()** values on **ManufacturerData()**.

| Status | Condition | Action |
|----------|---------------------------------------|---|
| Activate | 0x0058 to ManufacturerAccess() | Output AFERegister() values on ManufacturerData() |

11.1.45 **ManufacturerAccess() 0x0060 Lifetime Data Block 1**

This command returns the Lifetime data on **ManufacturerData()**.

| Status | Condition | Action |
|----------|---------------------------------------|--|
| Activate | 0x0060 to ManufacturerAccess() | Output 32 bytes of lifetime data values on ManufacturerData() |

11.1.46 ManufacturerAccess() 0x0061 Lifetime Data Block 2

This command returns the Lifetime data on **ManufacturerData()**.

| Status | Condition | Action |
|----------|---------------------------------------|--|
| Activate | 0x0061 to ManufacturerAccess() | Output 27 bytes of lifetime data values on ManufacturerData() |

11.1.47 ManufacturerAccess() 0x0062 Lifetime Data Block 3

This command returns the Lifetime data on **ManufacturerData()**.

| Status | Condition | Action |
|----------|---------------------------------------|--|
| Activate | 0x0062 to ManufacturerAccess() | Output 12 bytes of lifetime data values on ManufacturerData() |

11.1.48 ManufacturerAccess() 0x0070 ManufacturerInfo

This command returns ManufacturerInfo on **ManufacturerData()**.

| Status | Condition | Action |
|----------|---------------------------------------|--|
| Activate | 0x0070 to ManufacturerAccess() | Output 32 bytes of ManufacturerInfo on ManufacturerData() |

11.1.49 ManufacturerAccess() 0x0071 Voltages

This command returns the CellVoltage, PackVoltage, and BatVoltage on **ManufacturerData()**.

| Status | Condition | Action |
|----------|---------------------------------------|---|
| Activate | 0x0071 to ManufacturerAccess() | Output 12 bytes of voltage data values on ManufacturerData() |

11.1.50 ManufacturerAccess() 0x0072 Temperatures

This command returns the internal temp sensor, TS1, TS2, TS3, TS4, CellTemp and FETTemp on **ManufacturerData()**.

| Status | Condition | Action |
|----------|---------------------------------------|---|
| Activate | 0x0072 to ManufacturerAccess() | Output 14 bytes of temperature data values on ManufacturerData() |

11.1.51 ManufacturerAccess() 0x0073 ITSTATUS1

This command instructs the device to return Impedance Track related gauging information on **ManufacturerData()**.

| Status | Condition | Action |
|----------|---------------------------------------|--|
| Activate | 0x0073 to ManufacturerAccess() | Output 30 bytes of IT data values on ManufacturerData() |

11.1.52 ManufacturerAccess() 0x0074 ITSTATUS2

This command instructs the device to return Impedance Track related gauging information on **ManufacturerData()**.

| Status | Condition | Action |
|----------|---------------------------------------|--|
| Activate | 0x0074 to ManufacturerAccess() | Output 10 bytes of IT data values on ManufacturerData() |

11.1.53 ManufacturerAccess() 0xF080 Exit Calibration Output Mode

This command returns the data acquisition to Normal mode.

| Status | Condition | Action |
|----------|---|---|
| Activate | ManufacturerData() [CAL] = 1 AND 0xF080 to ManufacturerAccess() | Stop output of ADC or CC data on ManufacturerData() and return to normal data acquisition mode |

11.1.54 ManufacturerAccess() 0xF081 Output CC and ADC for Calibration

This command let the device output the raw values of Coulomb counter, CellVoltage1, CellVoltage2, CellVoltage3, CellVoltage4, TS1, TS2, TS3, TS4, Tint, PACK, and BAT as block on **ManufacturerData()** with updates every 250 ms for calibration purposes.

The format of each value 2's complement, MSB first.

| Status | Condition | Action |
|---------|--|---|
| Disable | ManufacturingStatus() [CAL] = 1 AND 0xF080 to ManufacturerAccess() | <ul style="list-style-type: none"> • ManufacturingStatus()[CAL] = 0 • Stop output of ADC and CC data on ManufacturerData() and return to normal data acquisition mode |
| Enable | 0xF081 to ManufacturerAccess() | <ul style="list-style-type: none"> • ManufacturingStatus()[CAL] = 1 • outputs the raw CC and AD values on ManufacturerData() in the format of ZZZYaaAAabbBBccCCddDDeeEEffFGggGGhhHHiiIjjJkKKIILL, where: <ul style="list-style-type: none"> – ZZ: rolling 8-bit counter, increments when values are refreshed – YY: status, 1 when MAC() = 0xF081, 2 when MAC()=0xF082 – AAaa: Coulomb counter – BBaa: CellVoltage1 – CCaa: CellVoltage2 – DDaa: CellVoltage3 – EEee: CellVoltage4 – FFff: Tint – GGgg: TS1 – HHhh: TS2 – Iiii: TS3 – JJJj: TS4 – KKKk: PackVoltage – LLLl: BatVoltage |

11.1.55 ManufacturerAccess() 0xF082 Output shorted Cc AND ADC Offset for Calibration

This command let the device output the raw CC value on **ManufacturerData()**.

The format of each value 2's complement, MSB first.

| Status | Condition | Action |
|---------|---|--|
| Disable | ManufacturingStatus() [CAL] = 1 AND 0xF080 to ManufacturerAccess() | <ul style="list-style-type: none"> • ManufacturingStatus() [CAL] = 0 • Stop output of ADC and CC data on ManufacturerData() and return to normal data acquisition mode |
| Enable | 0xF082 to ManufacturerAccess() | <ul style="list-style-type: none"> • ManufacturingStatus() [CAL] = 1 • outputs the raw CC and AD values on ManufacturerData() in the format of ZZYyaaAAAbbBBccCCddDDeeEEffFFggGGhhHHiiiJJkkKKIILL, where: • ZZ: rolling 8-bit counter, increments when values are refreshed • YY: status, 1 when MAC() = 0xF081, 2 when MAC()=0xF082 • AAaa: Coulomb counter • BBaa: CellVoltage1 • CCaa: CellVoltage2 • DDaa: CellVoltage3 • EEee: CellVoltage4 • FFff: Tint • GGgg: TS1 • HHhh: TS2 • Iiii: TS3 • JJjj: TS4 • KKKk: PackVoltage • LLll: BatVoltage |

11.1.56 ManufacturerAccess() 0x01yy DF Access Row Address

This command sets the DF row with address yy on **ManufacturerInfo()** for immediate read/write on **ManufacturingInfo()**.

| Status | Condition | Action |
|----------|---------------------------------------|--|
| Activate | 0x01yy to ManufacturerAccess() | Prepare DF 32-byte row with address yy on ManufacturerInfo() for block read or write. |

11.2 0x01 RemainingCapacityAlarm()

This read/write word function sets a low capacity alarm threshold.

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|---------|--------------------------|--------|----|----|----------|------|-----|-------|--------|---------------------------------|
| | | SE | US | FA | | | | | | |
| 0x01 | RemainingCapacityAlarm() | R/W | | | Word | U2 | 0 | 65535 | mAh | BatteryMode() [CAPM] = 0 |
| | | | | | | | | | 10 mWh | BatteryMode() [CAPM] = 1 |

11.3 0x02 RemainingTimeAlarm()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|---------|----------------------|--------|----|----|----------|------|-----|-------|------|------|
| | | SE | US | FA | | | | | | |
| 0x02 | RemainingTimeAlarm() | R/W | | | Word | U2 | 0 | 65535 | min | |

11.4 0x03 BatteryMode()

| SBS Cmd | Name | Access | | | Proto- col | Type | Min | Max | Note |
|------------|---------------|--------|----|----|---------------|------|--------|--------|---|
| | | SE | US | FA | | | | | |
| 0x03 | BatteryMode() | R/W | | | Word | H2 | 0x0000 | 0xFFFF | Bit 0: ICC—Internal Charge Controller (R) 0 = Function not supported Bit 1: PBC—Primary Battery Support (R) 1 = Primary or Secondary Battery Support Bit 2: Reserved Bit 3: Reserved Bit 4: Reserved Bit 5: Reserved Bit 6: Reserved Bit 7: CF—Condition Flag 0 = Battery OK 1 = Conditioning cycle requested Bit 8: CCE—Charge Controller Enabled (R/W) 0 = Internal charge controller disabled |
| 0x03 | BatteryMode() | R/W | | | Word | H2 | 0x0000 | 0xFFFF | Bit 9: PB—Primary Battery (R/W) 0 = Battery operating in its secondary role (default) 1 = Battery operating in its primary role Bit 10: Reserved Bit 11: Reserved Bit 12: Reserved Bit 13: AM—Alarm Mode (R/W) 0 = Enable Alarm Warning broadcasts to host and smart battery charger 1 = Disable Alarm Warning broadcasts to host and smart battery charger Bit 14: CHGM—Charger Mode (R/W) 0 = Enable ChargingVoltage() and ChargingCurrent() broadcasts to host and smart battery charger 1 = Disable ChargingVoltage() and ChargingCurrent() broadcasts to host and smart battery charger Bit 15: CAPM—Capacity Mode (R/W) 0 = Report in mA or mAh (default) 1 = Report in 10 mW or 10 mWh |

11.5 0x04 AtRate()

This read/write word function sets the value used in calculating **AtRateTimeToFull()** and **AtRateTimeToEmpty()**.

| SBS Cmd | Name | Access | | | Proto- col | Type | Min | Max | Unit | Note |
|------------|----------|--------|----|----|---------------|------|--------|-------|-------|---------------------------------|
| | | SE | US | FA | | | | | | |
| 0x04 | AtRate() | R/W | | | Word | I2 | –32768 | 32767 | mA | BatteryMode() [CAPM] = 0 |
| | | | | | | | | | 10 mW | BatteryMode() [CAPM] = 1 |

11.6 0x05 AtRateToFull()

This word read function returns the remaining time to fully charge the battery stack.

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|------------|----------------|--------|----|----|----------|------|-----|-------|------|-----------------------------------|
| | | SE | US | FA | | | | | | |
| 0x05 | AtRateToFull() | R | | | Word | U2 | 0 | 65534 | min | 65535 indicates not being charged |

11.7 0x06 AtRateToEmpty()

This word read function returns the remaining time to fully discharge the battery stack.

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|------------|-----------------|--------|----|----|----------|------|-----|-------|------|-----------------------------------|
| | | SE | US | FA | | | | | | |
| 0x06 | AtRateToEmpty() | R | | | Word | U2 | 0 | 65534 | min | 65535 indicates not being charged |

11.8 0x07 AtRateOK()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|------------|------------|--------|----|----|----------|------|-----|-----|------|------------|
| | | SE | US | FA | | | | | | |
| 0x07 | AtRateOK() | R | | | Word | | | | | 0 = not ok |

11.9 0x08 Temperature()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|------------|---------------|--------|----|----|----------|------|-----|-------|-------|------|
| | | SE | US | FA | | | | | | |
| 0x08 | Temperature() | R | | | Word | U2 | 0 | 65535 | 0.1°K | |

11.10 0x09 Voltage()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|------------|-----------|--------|----|----|----------|------|-----|-------|------|------|
| | | SE | US | FA | | | | | | |
| 0x09 | Voltage() | R | | | Word | U2 | 0 | 65535 | mV | |

11.11 0x0A Current()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|------------|-----------|--------|----|----|----------|------|--------|-------|------|------|
| | | SE | US | FA | | | | | | |
| 0x0A | Current() | R | | | Word | I2 | –32767 | 32768 | mA | |

11.12 0x0B AverageCurrent()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|------------|-----------|--------|----|----|----------|------|--------|-------|------|------|
| | | SE | US | FA | | | | | | |
| 0x0B | Current() | R | | | Word | I2 | –32767 | 32768 | mA | |

11.13 0x0C MaxError()

This read word function returns an unsigned integer value of the expected margin of error, in %, in the state-of-charge calculation with a range of 1 to 100%.

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|---------|------------|--------|----|----|----------|------|-----|-----|------|------|
| | | SE | US | FA | | | | | | |
| 0x0C | MaxError() | R | | | Word | U2 | 0 | 100 | % | |

| Status | Condition | Action |
|--------|---|--------------------------------------|
| | Full device reset | MaxError() = 100% |
| | RA-table only updated | MaxError() = 5% |
| | QMax only updated | MaxError() = 3% |
| | RA-table and QMax updated | MaxError() = 1% |
| | Each CycleCount() increment after last valid Qmax update | MaxError() increment by 0.05% |
| | Configuration:Max Error Time Cycle Equivalent period passed since last valid QMax update | MaxError() increment by 0.05% |

11.14 0x0D RelativeStateOfCharge()

This read word function returns the predicted remaining battery capacity as a percentage of **FullChargeCapacity()**.

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|---------|-------------------------|--------|----|----|----------|------|-----|-----|------|------|
| | | SE | US | FA | | | | | | |
| 0x0D | RelativeStateOfCharge() | R | | | Word | U2 | 0 | 100 | % | |

11.15 0x0E AbsoluteStateOfCharge()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|---------|-------------------------|--------|----|----|----------|------|-----|-----|------|------|
| | | SE | US | FA | | | | | | |
| 0x0E | AbsoluteStateOfCharge() | R | | | Word | U2 | 0 | 100 | % | |

11.16 0x0F RemainingCapacity()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|---------|---------------------|--------|----|-----|----------|------|-----|-------|--------|---------------------------------|
| | | SE | US | FA | | | | | | |
| 0x0F | RemainingCapacity() | R | R | R/W | Word | U2 | 0 | 65535 | mAh | BatteryMode() [CAPM] = 0 |
| | | | | | | | | | 10 mWh | BatteryMode() [CAPM] = 1 |

11.17 0x10 FullChargeCapacity()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|---------|----------------------|--------|----|-----|----------|------|-----|-------|--------|---------------------------------|
| | | SE | US | FA | | | | | | |
| 0x10 | FullChargeCapacity() | R | R | R/W | Word | U2 | 0 | 65535 | mAh | BatteryMode() [CAPM] = 0 |
| | | | | | | | | | 10 mWh | BatteryMode() [CAPM] = 1 |

11.18 0x11 RunTimeToEmpty()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|------------|------------------|--------|----|----|----------|------|-----|-------|------|------------------------------|
| | | SE | US | FA | | | | | | |
| 0x11 | RunTimeToEmpty() | R | R | R | Word | U2 | 0 | 65534 | min | 65535 = Not being discharged |

11.19 0x12 AverageTimeToEmpty()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|------------|----------------------|--------|----|----|----------|------|-----|-------|------|------------------------------|
| | | SE | US | FA | | | | | | |
| 0x12 | AverageTimeToEmpty() | R | R | R | Word | U2 | 0 | 65534 | min | 65535 = Not being discharged |

11.20 0x13 AverageTimeToFull()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|------------|---------------------|--------|----|----|----------|------|-----|-------|------|------------------------------|
| | | SE | US | FA | | | | | | |
| 0x13 | AverageTimeToFull() | R | R | R | Word | U2 | 0 | 65534 | min | 65535 = Not being discharged |

11.21 0x14 ChargingCurrent()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|------------|-------------------|--------|----|----|----------|------|-----|-------|------|---------------------------------|
| | | SE | US | FA | | | | | | |
| 0x14 | ChargingCurrent() | R | R | R | Word | U2 | 0 | 65534 | mA | 65535 = request maximum current |

11.22 0x15 ChargingVoltage()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|------------|-------------------|--------|----|----|----------|------|-----|-------|------|---------------------------------|
| | | SE | US | FA | | | | | | |
| 0x15 | ChargingVoltage() | R | R | R | Word | U2 | 0 | 65534 | mV | 65535 = request maximum voltage |

11.23 0x16 BatteryStatus()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Note |
|------------|-----------------|--------|----|----|----------|------|-----|-----|---|
| | | SE | US | FA | | | | | |
| 0x16 | BatteryStatus() | R | R | R | Word | H2 | | | Bit 3:0: EC3,EC2,EC1,EC0 Error Code 0x0 = OK 0x1 = Busy 0x2 = Reserved Command 0x3 = Unsupported Command 0x4 = AccessDenied 0x5 = Overflow/Underflow 0x6 = BadSize 0x7 = UnknownError Bit 4: FD—Fully Discharged 0 = Battery ok 1 = Battery fully depleted Bit 5: FC—Fully Charged 0 = Battery not fully charged 01 = Battery fully charged Bit 6: DSG—Discharging 0 = Battery is charging 1 = Battery is discharging Bit 7: INIT—Initialization 0 = Inactive 1 = Active Bit 8: RTA—Remaining Time Alarm 0 = Inactive 1 = Active |
| 0x16 | BatteryStatus() | R | R | R | Word | H2 | | | Bit 9: RCA—Remaining Capacity Alarm 0 = Inactive 1 = Active Bit 10: Reserved Undefined Bit 11: TDA—Terminate Discharge Alarm 0 = Inactive 1 = Active Bit 12: OTA—Overtemperature Alarm 0 = Inactive 1 = Active Bit 13: Reserved Undefined Bit 14: TCA—Terminate Charge Alarm 0 = Inactive 1 = Active Bit 15: OCA—Over Charged Alarm 0 = Inactive 1 = Active |

11.24 0x17 CycleCount()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|------------|--------------|--------|----|----|----------|------|-----|-------|--------|------------------------------|
| | | SE | US | FA | | | | | | |
| 0x17 | CycleCount() | R | R | R | Word | U2 | 0 | 65534 | cycles | 65535 = 65535 or more cycles |

11.25 0x18 DesignCapacity()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|------------|------------------|--------|----|----|----------|------|-----|-------|--------|-------------------------|
| | | SE | US | FA | | | | | | |
| 0x18 | DesignCapacity() | R | R | R | Word | U2 | 0 | 65535 | mAh | BatteryMode()[CAPM] = 0 |
| | | | | | | | | | 10 mWh | BatteryMode()[CAPM] = 1 |

11.26 0x19 DesignVoltage()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|------------|-----------------|--------|----|----|----------|------|-----|-------|------|------|
| | | SE | US | FA | | | | | | |
| 0x19 | DesignVoltage() | R | R | R | Word | U2 | 0 | 65535 | mV | |

11.27 0x1A SpecificationInfo()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Note |
|------------|---------------------|--------|----|----|----------|------|--------|--------|---|
| | | SE | US | FA | | | | | |
| 0x1A | SpecificationInfo() | R | R | R | Word | H2 | 0x0000 | 0xFFFF | Bit 0,1,2,3: Revision Revision 0,0,0,1 = Version 1.0 and 1.1 (default) Bit 4,5,6,7: Version Version 0,0,0,1 = Version 1.0 0,0,1,1 = Version 1.1 0,0,1,1 = Version 1.1 with optional PEC support Bit 8,9,10,11: VScale Voltage Scale Factor 0,0,0,0 = reported voltages scaled by 10E0 0,0,0,1 = reported voltages scaled by 10E1 0,0,1,0 = reported voltages scaled by 10E2 0,0,1,1 = reported voltages scaled by 10E3 Bit 12,13,14,15: Current 0,0,0,0 = reported currents and capacities scaled by 10E0 except ChargingVoltage() and ChargingCurrent() 0,0,0,1 = reported currents and capacities scaled by 10E1 except ChargingVoltage() and ChargingCurrent() 0,0,1,0 = reported currents and capacities scaled by 10E2 except ChargingVoltage() and ChargingCurrent() 0,0,1,1 = reported currents and capacities scaled by 10E3 except ChargingVoltage() and ChargingCurrent() |

11.28 0x1B ManufacturerDate()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Note |
|------------|--------------------|--------|----|----|----------|------|-----|-----|--|
| | | SE | US | FA | | | | | |
| 0x1B | ManufacturerDate() | R | R | R | Word | | | | ManufacturerDate() value in the following format: Day + Month*32 + (Year-1980)*256 |

11.29 0x1C SerialNumber()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|------------|----------------|--------|----|----|----------|------|-----|-----|------|------|
| | | SE | US | FA | | | | | | |
| 0x1C | SerialNumber() | R | R | R | Word | | | | | |

11.30 0x20 ManufacturerName()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|------------|--------------------|--------|----|----|----------|------|-----|-----|------|------|
| | | SE | US | FA | | | | | | |
| 0x20 | ManufacturerName() | R | R | R | Block | S21 | | | | |

11.31 0x21 DeviceName()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|------------|--------------|--------|----|----|----------|------|-----|-----|------|------|
| | | SE | US | FA | | | | | | |
| 0x21 | DeviceName() | R | R | R | Block | S21 | | | | |

11.32 0x22 DeviceChemistry()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|------------|-------------------|--------|----|----|----------|------|-----|-----|------|------|
| | | SE | US | FA | | | | | | |
| 0x22 | DeviceChemistry() | R | R | R | Block | S4 | | | | |

11.33 0x23 ManufacturerData()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|------------|--------------------|--------|----|----|----------|------|-----|-----|------|------|
| | | SE | US | FA | | | | | | |
| 0x23 | ManufacturerData() | R | R | R | Block | | | | | |

11.34 0x2F Authentication() AND ManufacturerInput()

This read/write block function provides SHA-1 authentication in default mode. It is also used to enable data flash read/writes and provide authentication input for sealed, unsealed, full access mode.

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Unit | Note |
|------------|---------------------|--------|-----|-----|----------|------|-----|-----|------|------|
| | | SE | US | FA | | | | | | |
| 0x2F | ManufacturerInput() | R/W | R/W | R/W | Block | | | | | |

| Status | Condition | Action |
|------------------|---|--|
| Authentication | No active ManufacturerInput() data waiting AND write 160-bit challenge to ManufacturerInput() in the format 0xAABBCCDDEEFFGGHHIIJJKLLMMNNO OPPQRRSSTT, where AA is LSB. | <ul style="list-style-type: none"> • OperationStatus()[AUTH] = 1 • Wait 250 ms • OperationStatus()[AUTH] = 0 • Device returns 160-bit digest at ManufacturerInput() in the format 0xAABBCCDDEEFFGGHHIIJJKLLMMNNOOPP QRRSSTTT, where AA is LSB, using the challenge + authentication key. Compare with own calculations to confirm validity of key. |
| ManufacturerInfo | Valid word sent to ManufacturerAccess() | Output block based on ManufacturerAccess() input for one time readout. Note: 0xF081 and 0xF082 on ManufacturerAccess() will be available for multi-read out until cleared with 0xF080. |

11.35 0x3C–0x3F Cell Voltages()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Default | Unit | Note |
|------------|----------------|--------|----|----|----------|------|-----|-------|---------|------|------|
| | | SE | US | FA | | | | | | | |
| 0x3c | Cell 3 voltage | R | R | R | Word | I2 | 0 | 32767 | | mV | |
| 0x3d | Cell 2 voltage | R | R | R | Word | I2 | 0 | 32767 | | mV | |

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Default | Unit | Note |
|---------|----------------|--------|---|---|----------|------|-----|-------|---------|------|------|
| 0x3e | Cell 1 voltage | R | R | R | Word | I2 | 0 | 32767 | | mV | |
| 0x3f | Cell 0 voltage | R | R | R | Word | I2 | 0 | 32767 | | mV | |

11.36 0x50 SafetyAlert()

| SBS Cmd | Name | Access | | | Proto- col | Type | Min | Max | Note |
|------------|---------------|--------|----|----|---------------|------|-----|-----|---|
| | | SE | US | FA | | | | | |
| 0x50 | SafetyAlert() | N/A | R | R | Block | | | | Bit 0: CUV—Cell Undervoltage 0 = Inactive 1 = Detected Bit 1: COV—Cell Overvoltage 0 = Inactive 1 = Detected Bit 2: OCC1—Overcurrent in Charge 1st Tier 0 = Inactive 1 = Detected Bit 3: OCC2—Overcurrent in Charge 2nd Tier 0 = Inactive 1 = Detected Bit 4: OCD1—Overcurrent in Discharge 1st Tier 0 = Inactive 1 = Detected Bit 5: OCD2—Overcurrent in Discharge 2nd Tier 0 = Inactive 1 = Detected Bit 6: OLD—Overload in discharge 0 = Inactive 1 = Detected Bit 7: Reserved Bit 8: SCC—Short circuit in charge 0 = Inactive 1 = Detected Bit 9: Reserved Bit 10: SCD—Short circuit in discharge 0 = Inactive 1 = Detected Bit 11: Reserved Bit 12: OTC—Overtemperature in charge 0 = Inactive 1 = Detected Bit 13: OTD—Overtemperature in discharge 0 = Inactive 1 = Detected Bit 14: CUV—I*R compensated CUV 0 = Inactive 1 = Detected Bit 15: Reserved |

| SBS Cmd | Name | Access | | | Proto- col | Type | Min | Max | Note |
|------------|---------------|--------|----|----|---------------|------|-----|-----|---|
| | | SE | US | FA | | | | | |
| 0x50 | SafetyAlert() | N/A | R | R | Block | | | | Bit 16: OTF—FET overtemperature 0 = Inactive 1 = Detected Bit 17: HWD—SBS Host watchdog timeout 0 = Inactive 1 = Detected Bit 18: PTO—Pre-charging timeout 0 = Inactive 1 = Detected Bit 19: PTOS—Pre-charging timeout suspend 0 = Inactive 1 = Detected Bit 20: CTO—Charging timeout 0 = Inactive 1 = Detected Bit 21: CTOS—Charging timeout suspend 0 = Inactive 1 = Detected Bit 22: OC—Overcharge 0 = Inactive 1 = Detected Bit 23: CHGC—Charging Current higher than requested 0 = Inactive 1 = Detected Bit 24: CHGV—Charging Voltage higher than requested 0 = Inactive 1 = Detected Bit 25: Reserved Bit 26: Reserved Bit 27: Reserved Bit 28: Reserved Bit 29: Reserved Bit 30: Reserved Bit 31: Reserved |

11.37 0x51 SafetyStatus()

| SBS Cmd | Name | Access | | | Proto- col | Type | Min | Max | Note |
|------------|----------------|--------|----|----|---------------|------|-----|-----|---|
| | | SE | US | FA | | | | | |
| 0x51 | SafetyStatus() | N/A | R | R | Block | | | | Bit 0: CUV—Cell UnderVoltage 0 = Inactive 1 = Detected Bit 1: COV—Cell Overvoltage 0 = Inactive 1 = Detected Bit 2: OCC1—Overcurrent in Charge 1st Tier 0 = Inactive 1 = Detected Bit 3: OCC2—Overcurrent in Charge 2nd Tier 0 = Inactive 1 = Detected Bit 4: OCD1—Overcurrent in Discharge 1st Tier 0 = Inactive 1 = Detected Bit 5: OCD2—Overcurrent in Discharge 2nd Tier 0 = Inactive 1 = Detected Bit 6: OLD—Overload in discharge 0 = Inactive 1 = Detected Bit 7: OLDL—Overload in discharge latch 0 = Inactive 1 = Detected Bit 8: SCC—Short circuit in charge 0 = Inactive 1 = Detected Bit 9: SCCL—Short circuit in charge latch 0 = Inactive 1 = Detected Bit 10: SCD—Short circuit in discharge 0 = Inactive 1 = Detected Bit 11: SCDL—Short circuit in discharge latch 0 = Inactive 1 = Detected |

| SBS Cmd | Name | Access | | | Proto- col | Type | Min | Max | Note |
|------------|----------------|--------|----|----|---------------|------|-----|-----|--|
| | | SE | US | FA | | | | | |
| 0x51 | SafetyStatus() | N/A | R | R | Block | | | | Bit 12: OTC—Overtemperature in charge 0 = Inactive 1 = Detected Bit 13: OTD—Overtemperature in discharge 0 = Inactive 1 = Detected Bit 14: CUVC—I*R compensated CUV 0 = Inactive 1 = Detected Bit 15: Reserved Bit 16: OTF—FET overtemperature 0 = Inactive 1 = Detected Bit 17: HWD—SBS Host watchdog timeout 0 = Inactive 1 = Detected Bit 18: PTO—Pre-charging timeout 0 = Inactive 1 = Detected Bit 19: Reserved Bit 20: CTO—Charging timeout 0 = Inactive 1 = Detected Bit 21: Reserved Bit 22: OC—Overcharge 0 = Inactive 1 = Detected Bit 23: CHGC—Charging Current higher than requested 0 = Inactive 1 = Detected Bit 24: CHGV—Charging Voltage higher than requested 0 = Inactive 1 = Detected Bit 25: Reserved Bit 26: Reserved Bit 27: Reserved Bit 28: Reserved Bit 29: Reserved Bit 30: Reserved Bit 31: Reserved |

11.38 0x52 PFAAlert()

| SBS Cmd | Name | Access | | | Proto- col | Type | Min | Max | Note |
|------------|------------|--------|----|----|---------------|------|-----|-----|---|
| | | SE | US | FA | | | | | |
| 0x52 | PFAAlert() | N/A | R | R | Block | | | | Bit 0: CUV—Cell undervoltage 0 = Inactive 1 = Detected Bit 1: COV—Cell overvoltage 0 = Inactive 1 = Detected Bit 2: CUDEP—Copper deposition 0 = Inactive 1 = Detected Bit 3: Reserved Bit 4: OTCE—Overtemperature 0 = Inactive 1 = Detected Bit 5: Reserved Bit 6: OTF—Overtemperature FET 0 = Inactive 1 = Detected Bit 7: QIM—QMax Imbalance 0 = Inactive 1 = Detected Bit 8: CB—Cell balancing 0 = Inactive 1 = Detected Bit 9: IMP—Cell impedance 0 = Inactive 1 = Detected Bit 10: CD—Capacity Deterioration 0 = Inactive 1 = Detected Bit 11: VIMR—Voltage imbalance at Rest 0 = Inactive 1 = Detected Bit 12: VIMA—Voltage imbalance at Rest 0 = Inactive 1 = Detected Bit 13: Reserved Bit 14: Reserved Bit 15: Reserved |

| SBS Cmd | Name | Access | | | Proto- col | Type | Min | Max | Note |
|------------|------------|--------|----|----|---------------|------|-----|-----|--|
| | | SE | US | FA | | | | | |
| 0x52 | PFAAlert() | N/A | R | R | Block | | | | Bit 16: CFETF—Charge FET 0 = Inactive 1 = Detected Bit 17: DFET—Discharge FET 0 = Inactive 1 = Detected Bit 18: TH—Thermistor 0 = Inactive 1 = Detected Bit 19: FUSE—Fuse 0 = Inactive 1 = Detected Bit 20: AFER—AFE Register 0 = n/a 1 = Detected Bit 21: AFEC—AFE Communication 0 = Inactive 1 = Detected Bit 22: 2LVL—FUSE input indicating fuse trigger by external 2nd level protection 0 = Inactive 1 = Detected Bit 23: Reserved Bit 24: Reserved Bit 25: OCECO—Open VCx 0 = n/a 1 = Detected Bit 26: Reserved Bit 27: Reserved Bit 28: Reserved Bit 29: Reserved Bit 30: Reserved Bit 31: Reserved |

11.39 0x53 PFStatus()

| SBS Cmd | Name | Access | | | Proto- col | Type | Min | Max | Note |
|------------|------------|--------|----|----|---------------|------|-----|-----|--|
| | | SE | US | FA | | | | | |
| 0x53 | PFStatus() | N/A | R | R | Block | | | | Bit 0: CUV—Cell undervoltage 0 = Inactive 1 = Active Bit 1: COV—Cell overvoltage 0 = Inactive 1 = Active Bit 2: Reserved Bit 3: Reserved Bit 4: OTCE—Overtemperature 0 = Inactive 1 = Active Bit 5: Reserved Bit 6: OTF—Overtemperature FET 0 = Inactive 1 = Active Bit 7: QIM—QMax Imbalance 0 = Inactive 1 = Active Bit 8: CB—Cell balancing 0 = Inactive 1 = Active Bit 9: IMP—Cell impedance 0 = Inactive 1 = Active Bit 10: CD—Capacity Deterioration 0 = Inactive 1 = Active Bit 11: VIMR—Voltage imbalance at Rest 0 = Inactive 1 = Active Bit 12: VIMA—Voltage imbalance at Rest 0 = Inactive 1 = Active Bit 13: Reserved Bit 14: Reserved Bit 15: Reserved |

| SBS Cmd | Name | Access | | | Proto- col | Type | Min | Max | Note |
|------------|------------|--------|----|----|---------------|------|-----|-----|--|
| | | SE | US | FA | | | | | |
| 0x53 | PFStatus() | N/A | R | R | Block | | | | Bit 16: CFETF—Charge FET 0 = Inactive 1 = Active Bit 17: DFET—Discharge FET 0 = Inactive 1 = Active Bit 18: TH—Thermistor 0 = Inactive 1 = Active Bit 19: FUSE—Fuse 0 = Inactive 1 = Active Bit 20: AFER—AFE Register 0 = n/a 1 = Active Bit 21: AFEC—AFE Communication 0 = Inactive 1 = Active Bit 22: 2LVL FUSE input indicating fuse trigger by external 2nd level protection 0 = Inactive 1 = Active Bit 23: PTC—PTC by AFE 0 = Inactive 1 = Active Bit 24: IFC—Instruction Flash Checksum 0 = n/a 1 = IF checksum failure Bit 25: OCECO—Open VCx 0 = n/a 1 = Active Bit 26: DFW—DF write failure 0 = n/a 1 = Active Bit 27: Reserved Bit 28: Reserved Bit 29: Reserved Bit 30: Reserved Bit 31: Reserved |

11.40 0x54 OperationStatus()

| SBS Cmd | Name | Access | | | Proto- col | Type | Min | Max | Note |
|------------|-------------------|--------|----|----|---------------|------|-----|-----|---|
| | | SE | US | FA | | | | | |
| 0x54 | OperationStatus() | N/A | R | R | Block | | | | Bit 0: PRES — PRES input state 0 = PRES pin high 1 = PRES pin low Detected Bit 1: DSG—DSG FET Status 0 = Disabled 1 = Enabled Bit 2: CHG—CHG FET Status 0 = Disabled 1 = Enabled Bit 3: PCHG—PCHG FET Status 0 = Disabled 1 = Enabled Bit 4: GPOD—GPOD FET Status 0 = Disabled 1 = Enabled Bit 5: FUSE—FUSE input 0 = FUSE pin low 1 = FUSE pin high Detected Bit 6: CB—Cell Balancing 0 = Inactive 1 = Active Bit 7: LED—LED Enable 0 = Inactive 1 = Active Bit 9:8: SEC1,SEC0—Security Mode0 0 = Reserved 1, 0 = Full Access 0, 1 = Unsealed 1,1 = Sealed |
| 0x54 | OperationStatus() | N/A | R | R | Block | | | | Bit 10: CAL—Cal Raw ADC/CC output active 0 = Inactive 1 = Active Bit 11: SS—SafetyStatus 0 = Inactive 1 = Active Bit 12: PF—Permanent Failure 0 = Inactive 1 = Active Bit 13: XDSG—Discharging Disabled 0 = Inactive 1 = Active Bit 14: XCHG—Charging Disabled 0 = Inactive 1 = Active Bit 15: SLEEP—Sleep condition met 0 = Disabled 1 = Enabled Bit 16: SDM—Shutdown activated by ManufacturerAccess() 0 = Inactive 1 = Active Bit 17: SHIPM—Ship mode activated with ManufacturerAccess() 0 = Inactive 1 = Active Bit 18: AUTH—Authentication ongoing 0 = Inactive 1 = Active |

| SBS Cmd | Name | Access | | | Proto- col | Type | Min | Max | Note |
|------------|-------------------|--------|----|----|---------------|------|-----|-----|--|
| | | SE | US | FA | | | | | |
| 0x54 | OperationStatus() | N/A | R | R | Block | | | | Bit 19: AWD—AFE Watchdog failure 0 = Inactive 1 = Active Bit 20: FVS—Fast Voltage Sampling 0 = Inactive 1 = Active Bit 21: CALO—Raw ADC/CC offset output 0 = Inactive 1 = Active Bit 22: SDV—Shutdown activated by voltage 0 = Inactive 1 = Active Bit 23: SLEEPM—Sleep mode active by ManufacturerAccess() 0 = Inactive 1 = Active Bit 24: INIT—Initialization after full reset, cleared when SBS data calculated and available 0 = Inactive 1 = Active Bit 25: SMBLCAL—CC auto offset calibration ongoing after SBS line goes low 0 = Inactive 1 = Active Bit 26: SLEEPQMax—QMax update in Sleep mode 0 = Inactive 1 = Active Bit 27: SLEEP—Checking current in Sleep mode 0 = Inactive 1 = Active Bit 28: XLSBS Fast Mode 0 = Inactive 1 = Active Bit 29: Reserved Bit 30: Reserved Bit 31: Reserved |

11.41 0x55 ChargingStatus()

| SBS Cmd | Name | Access | | | Proto- col | Type | Min | Max | Note |
|------------|-----------------------|--------|----|----|---------------|------|-----|-----|---|
| | | SE | US | FA | | | | | |
| 0x55 | ChargingSta- tus() | | R | R | Block | | | | Bit 0: UT—Under Temperature Range 0 = Inactive 1 = Active Bit 1: LT—Low Temperature Range 0 = Inactive 1 = Active Bit 2: STL—Standard Temperature Low Range 0 = Inactive 1 = Active Bit 3: RT—Recommended Temperature Range 0 = Inactive 1 = Active Bit 4: ST—Standard Temperature High Range 0 = Inactive 1 = Active Bit 5: HT—High Temperature Range 0 = Inactive 1 = Active Bit 6: OT—Over Temperature Range 0 = Inactive 1 = Active Bit 7: PV—Precharge Voltage Range 0 = Inactive 1 = Active Bit 8: LV—Low Voltage Range 0 = Inactive 1 = Active Bit 9: MV—Mid Voltage Range 0 = Inactive 1 = Active Bit 10: HV—High Voltage Range 0 = Inactive 1 = Active Bit 11: IN—Charge Inhibit 0 = Inactive 1 = Active Bit 12: SU—Charge Suspend 0 = Inactive 1 = Active Bit 13: CCR—ChargingCurrent() Rate 0 = Inactive 1 = Active Bit 14: CVR— ChargingVoltage() Rate 0 = Inactive 1 = Active Bit 15: CCC—ChargingCurrent() Compensation 0 = Inactive 1 = Active |

11.42 0x56 GaugingStatus()

| SBS Cmd | Name | Access | | | Proto- col | Type | Min | Max | Note |
|------------|-----------------|--------|----|----|---------------|------|-----|-----|---|
| | | SE | US | FA | | | | | |
| 0x56 | GaugingStatus() | | R | R | Block | | | | Bit 0: RESTDOD0, OCV and QMax Updated 0 = Not updated 1 = Updated Bit 1: DSG—Discharge Detected 0 = Charging 1 = Discharging Bit 2: RU—Resistance update 0 = Disabled 1 = Enabled Bit 3: VOK Cell Voltage OK for QMax update 0 = Inactive 1 = Active Bit 4: QEN—QMax updates 0 = Disabled 1 = Enabled Bit 5: FD—Fully Discharged Detected by gauge algorithm 0 = Disabled 1 = Enabled Bit 6: FC—Fully Charged Detected by gauge algorithm 0 = Disabled 1 = Enabled Bit 7: NSFM—Negative scale factor mode 0 = Disabled 1 = Enabled Bit 8: VDQ—Discharge qualified for learning 0 = Disabled 1 = Enabled Bit 9: QMax—QMax updated. This flag toggles every time QMax is updated. Bit 10: RX—Resistance update. This flag toggles every time Resistance is updated. Bit 11: LDMD—Load Mode 0 = Constant current mode 1 = Constant power mode Bit 12: OCVFR—OCV in flat region 0 = OCV outside flat region 1 = OCV in flat region Bit 13: TDA—Terminate Discharge Alarm set by gauging algorithm 0 = Disabled 1 = Enabled Bit 14: TCA—Terminate Charge Alarm set by gauging algorithm 0 = Disabled 1 = Enabled Bit 15: LPF Relax—LiPh Relax Mode, only active with Chem ID 0x400 0 = Disabled 1 = Enabled |

11.43 0x57 ManufacturingStatus()

The enable bits FET_EN, LF_EN, PF_EN, BBR_ENFUSE_EN, and LED_EN can be set in the golden image if packmaker does not want to send the individual enable commands. The only function that can not be enabled by setting DF Setting Manufacturing Status is IT Enable. The IT Enable cmd is needed to take DOD0 value for fast Qmax, etc.

| SBS Cmd | Name | Access | | | Proto- col | Type | Min | Max | Default | Note |
|------------|---------------------------|--------|----|----|---------------|------|-----|-----|---------|---|
| | | SE | US | FA | | | | | | |
| 0x57 | Manufacturin gStatus() | | R | R | Block | | | | 0x8000 | Bit 0: PCHG—PCHG Function, only available with FET = 0 0 = Disabled 1 = Enabled Bit 1: CHG—CHG FET, only available with FET = 0 0 = Disabled 1 = Enabled Bit 2: DSG—DSG FET, only available with FET = 0 0 = Disabled 1 = Enabled Bit 3: GAUGE—Gauging 0 = Disabled 1 = Enabled (default) Bit 4: FET—FET action 0 = Disabled 1 = Enabled (default) Bit 5: LF—Lifetime data collection 0 = Disabled 1 = Enabled (default) Bit 6: PF—Permanent Fail 0 = Disabled 1 = Enabled (default) Bit 7: BBR—Black box recorder 0 = Disabled 1 = Enabled (default) Bit 8: FUSE—FUSE action 0 = Disabled 1 = Enabled (default) Bit 9: LED—LED Display 0 = Disabled 1 = Enabled (default) Bit 10: Reserved Bit 11: Reserved Bit 12: Reserved Bit 13: Reserved Bit 14: Reserved Bit 15: CAL ADC or CC output on ManufacturerData() 0 = Disabled 1 = Enabled (default) |

11.44 0x58 AFERegisters()

| SBS Cmd | Name | Access | | | Proto- col | Type | Min | Max | Note |
|------------|----------------|--------|----|----|---------------|------|-----|-----|---|
| | | SE | US | FA | | | | | |
| 0x58 | AFERegisters() | | R | R | Block | | | | Output AFE register values on ManufacturerData() in the following format: AABBCDDDEEFFGGHHIIJJKK where: <ul style="list-style-type: none"> • AA: STATUS register • BB: STATE_CONTROL register • CC: OUTPUT_CONTROL register • DD: OUTPUT_STATUS register • EE: FUNCTION_CONTROL register • FF: CELL_SEL register • GG: OCDV register • HH: OCDD register • II: SCC register • JJ: SCD1 register • KK: SCD2 register |

11.45 0x60 Lifetime Data Block 1

| SBS Cmd | Name | Access | | | Proto- col | Type | Min | Max | Note |
|------------|-----------------------------|--------|----|----|---------------|------|-----|-----|--|
| | | SE | US | FA | | | | | |
| 0x60 | Lifetime Data Block 1 | | R | R | Block | | | | <p>Output lifetimes values on ManufacturerData() in the following format: AABBCCDDEEFFGGHHIIJJKLLMMN NOOPPQQRRSSTTUUVVWWXXVVZZ 112233445566 where:</p> <ul style="list-style-type: none"> • in the following format: • AA: Max Cell Voltage 1 • BB: Max Cell Voltage 2 • CC: Max Cell Voltage 3 • DD: Max Cell Voltage 4 • EE: Min Cell Voltage 1 • FF: Min Cell Voltage 2 • GG: Min Cell Voltage 3 • HH: Min Cell Voltage 4 • II: Max Delta Cell Voltage • JJ: Max Charge Current • KK: Max Discharge Current • LL: Max Average Discharge Current • MM: Max Average Discharge Power • NN: No of COV Events • OO: Last COV Event • PP: No of CUV Events • QQ: Last CUV Event • RR: No of OCD1 Events • SS: Last OCD1 Event • TT: No of OCD2 Events • UU: Last OCD2 Event • VV: No of OCC1 Events • WW: Last OCC1 Event • XX: No of OCC2 Events • YY: Last OCC2 Event • ZZ: No of OLD Events • 11: Last OLD Event • 22: No of SCD Events • 33: Last SCD Event • 44: No of SCC Events • 55: Last SCC Event • 66: No of OTC Events |

11.46 0x61 Lifetime Data Block 2

| SBS Cmd | Name | Access | | | Proto- col | Type | Min | Max | Default | Note |
|------------|-----------------------------|--------|----|----|---------------|------|-----|-----|---------|---|
| | | SE | US | FA | | | | | | |
| 0x61 | Lifetime Data Block 2 | | R | R | Block | | | | | Output lifetimes values on ManufacturerData() in the following format: • AABBCDDDEFFGGHHIIJJKKL LMMNNOOPPQQRRSSTTUUVV WWXXVVZZ11 where: • AA: Last OTC Event • BB: No of OTD Events • CC: Last OTD Event • DD: No of OTF Events • EE: Last OTF Event • FF: No Valid Charge Terminations • GG: Last Valid Charge Termination • HH: No of QMax Updates • II: Last QMax Update • JJ: No of RA Updates • KK: Last RA Update • LL: No of RA Disables • MM: Last RA Disable • NN: No of Shutdowns • OO: No of Partial Resets • PP: No of Full Resets • QQ: No of WDT Resets • RR: CB Time Cell 1 • SS: CB Time Cell 2 • TT: CB Time Cell 3 • UU: CB Time Cell 4 • VV: Max Temp Cell • WW: Min Temp Cell • XX: Max Delta Cell Temp • YY: Max Temp Int Sensor • ZZ: Min Temp Int Sensor • 11: Max Temp FET |

11.47 0x62 Lifetime Data Block 3

| SBS Cmd | Name | Access | | | Proto- col | Type | Min | Max | Default | Note |
|------------|-----------------------------|--------|----|----|---------------|------|-----|-----|---------|---|
| | | SE | US | FA | | | | | | |
| 0x62 | Lifetime Data Block 3 | | R | R | Block | | | | | Output lifetimes values on ManufacturerData() • in the following format: aaAAbbBBccCCddDDeeEEffFFg gGGhhHH where: • AAaa: Total firmware Run Time • BBbb: Time Spent in UT • CCcc: Time Spent in LT • DDdd: Time Spent in STL *EEee: Time Spent in RT • FFff: Time Spent in STH • GGgg: Time Spent in HT • HHhh: Time Spent in OT |

11.48 0x70 ManufacturerInfo()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Note |
|------------|--------------------|--------|-----|-----|----------|------|-----|-----|---|
| | | SE | US | FA | | | | | |
| 0x70 | ManufacturerInfo() | R | R/W | R/W | Block | | | | Instruct the device to return 32 bytes of ManufacturerInfo() . Output 32 bytes of ManufacturerInfo on ManufacturerData() in the following format: AABBCCDDEEFFGGHHIIJJKLLMMNN OOPPQQRRSSTTUUVVWWXXVZZ112 233445566 |

11.49 0x71 Voltages()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Note |
|------------|------------|--------|----|----|----------|------|-----|-----|---|
| | | SE | US | FA | | | | | |
| 0x71 | Voltages() | n/a | R | R | Block | | | | Output 12 bytes of voltage data values on ManufacturerData() in the following format: aaAAbbBBccCCddDDeeEEffFF where: <ul style="list-style-type: none"> • AAaa: Cell Voltage 0 • BBbb: Cell Voltage 1 • CCcc: Cell Voltage 2 • DDdd: Cell Voltage 3 • EEee: BAT Voltage • FFff: PACK Voltage |

11.50 0x72 Temperatures()

| SBS Cmd | Name | Access | | | Protocol | Type | Min | Max | Note |
|------------|----------------|--------|----|----|----------|------|-----|-----|--|
| | | SE | US | FA | | | | | |
| 0x72 | Temperatures() | n/a | R | R | Block | | | | <ul style="list-style-type: none"> • Output 14 bytes of temperature data values on ManufacturerData() in the following format: aaAAbbBBccCCddDDeeEEffFF where: • AAaa: Int Temperature • BBbb: TS1 Temperature • CCcc: TS2 Temperature • DDdd: TS3 Temperature • EEee: TS4 Temperature • FFff: Cell Temperature • GGgg: FET Temperature |

11.51 0x73 ITStatus1()

This read block function returns gauging algorithm related parameters.

| SBS Cmd | Name | Access | | | Proto- col | Type | Min | Max | Note |
|------------|-------------|--------|----|----|---------------|------|-----|-----|--|
| | | SE | US | FA | | | | | |
| 0x73 | ITStatus1() | n/a | R | R | Block | | | | Output 30 bytes of IT data values on ManufacturerData() in the following format: aaAAbbBBccCCddDDeeEEffFFGGggH HhhIiijJjjkkKKllLmmMMnnNNooOO where: <ul style="list-style-type: none"> • AAaa: DOD0 Cell 0 • BBbb: DOD0 Cell 1 • CCcc: DOD0 Cell 2 • DDdd: DOD0 Cell 3 • EEee: Passed Charge since last DOD0 Update • FFff: QMax Cell 0 • GGgg: QMax Cell 1 • HHhh: QMax Cell 2 • Iiii: QMax Cell 3 • JJJjKKkk: State Time • LLlI: DOD EOC Cell 0 • MMmm: DOD EOC Cell 1 • NNnn: DOD EOC Cell 2 • OOoo: DOD EOC Cell 3 |

| Attribute | Description | Format |
|------------------|---|--------|
| DOD0_0 | Depth of discharge cell 0 | I2 |
| DOD0_1 | Depth of discharge cell 1 | I2 |
| DOD0_2 | Depth of discharge cell 2 | I2 |
| DOD0_3 | Depth of discharge cell 3 | I2 |
| ChargeDOD0Update | Passed charge since last DOD0 update | I2 |
| QMax0 | Qmax of cell 0 | I2 |
| QMax1 | Qmax of cell 1 | I2 |
| QMax2 | Qmax of cell 2 | I2 |
| QMax3 | Qmax of cell 3 | I2 |
| StateTime | Time past since last state change (DSG,CHG,RST) | U4 |
| DODEOC0 | Depth of discharge cell at End of Charge cell 0 | U2 |
| DODEOC1 | Depth of discharge cell at End of Charge cell 1 | U2 |
| DODEOC2 | Depth of discharge cell at End of Charge cell 2 | U2 |
| DODEOC3 | Depth of discharge cell at End of Charge cell 3 | U2 |

11.52 0x74 ITStatus2()

This read block function returns gauging algorithm related parameters.

| SBS Cmd | Name | Access | | | Proto- col | Type | Min | Max | Note |
|------------|-------------|--------|----|----|---------------|------|-----|-----|--|
| | | SE | US | FA | | | | | |
| 0x74 | ITStatus2() | | R | R | Block | | | | Output 30 bytes of IT data values on ManufacturerData() in the following format: AABBCCDDEEFFggGGhhHHiiiJJkkKKILL mmMMnnNNooOPppPPqqQRRr where: <ul style="list-style-type: none"> • AA: Pack Grid point • BB: Learned Status • CC: Grid Cell 0 • DD: Grid Cell 1 • EE: Grid Cell 2 • FF: Grid Cell 3 • GGgg: CompRes Cell 0 • HHhh: CompRes Cell 1 • Iiii: CompRes Cell 2 • JJjj: CompRes Cell 3 • Kkkk: CB Time Cell 0 • LLLl: CB Time Cell 1 • MMmm: CB Time Cell 2 • NNnn: CB Time Cell 3 • OOOo: RaScale0 • PPpp: RaScale1 • QQqq: RaScale2 • RRRr: RaScale3 |

| Attribute | Description | Format |
|-----------|--|---|
| PackGrid | Active pack grid point (minimum of CellGrid0 to CellGrid3) | U1 |
| LStatus | Learned status of resistance table | Bit 1,0: CF—QMax status 0,0 = Battery OK 0,1 = QMax is first updated in learning cycle 1,0 = QMax and resistance table updated in learning cycle Bit 2: ITEN—IT enable 0 = IT disabled 1 = IT Enabled Bit 3: ITEN—QMax update in Field 0 = QMax never updated in field 1 = Qmax updated in filed |
| CellGrid0 | Active grid point cell 0 | U1 |
| CellGrid1 | Active grid point cell 1 | U1 |
| CellGrid2 | Active grid point cell 2 | U1 |
| CellGrid3 | Active grid point cell 3 | U1 |
| CompRes0 | Last calculated temperature compensated resistance cell 0 | U2 |
| CompRes1 | Last calculated temperature compensated resistance cell 1 | U2 |
| CompRes2 | Last calculated temperature compensated resistance cell 2 | U2 |
| CompRes3 | Last calculated temperature compensated resistance cell 3 | U2 |
| CBTime0 | Calculated cell balancing time cell 0 | U2 |
| CBTime1 | Calculated cell balancing time cell 1 | U2 |
| CBTime2 | Calculated cell balancing time cell 2 | U2 |
| CBTime3 | Calculated cell balancing time cell 3 | U2 |
| RaScale0 | Ra Table scaling factor cell 0 | U2 |
| RaScale1 | Ra Table scaling factor cell 1 | U2 |

| Attribute | Description | Format |
|-----------|--------------------------------|--------|
| RaScale2 | Ra Table scaling factor cell 2 | U2 |
| RaScale3 | Ra Table scaling factor cell 3 | U2 |

Data Flash Values and Device Configuration

12.1 Data Formats

12.1.1 Unsigned Integer

Unsigned integers are stored without changes as 1-byte, 2-byte or 4-byte values.

12.1.2 Integer

Integer values are stored in 2's-complement format in 1-byte, 2-byte, or 4-byte values.

12.1.3 Floating Point

Floating point are stored using 4 byte format, where the MSB is the exponent, byte 3 to 0 the mantissa in unsigned integer format, with the MSB in byte 3 as sign bit.

Where:

Exp: Exponent

Mantissa: 23 bit mantissa with 24 bit as sign bit.

The floating point value is represented as:

12.1.4 Hex

Bit register definitions are stored in unsigned integer format.

12.1.5 String

String values are stored with length byte first, followed by a number of data bytes defined with the length byte.

12.2 Protections

12.2.1 CUV—Cell Undervoltage

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|-----------|------|-----|-------|---------|------|--------------------------------------|
| Protections | CUV | Threshold | I2 | 0 | 32767 | 2800 | mV | Cell undervoltage trip threshold |
| Protections | CUV | Delay | U1 | 0 | 255 | 2 | s | Cell undervoltage trip delay |
| Protections | CUV | Recovery | I2 | 0 | 32767 | 3000 | mV | Cell undervoltage recovery threshold |

12.2.2 CUV—Cell Undervoltage Compensated

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|-----------|------|-----|-------|---------|------|--|
| Protections | CUVC | Threshold | I2 | 0 | 32767 | 2900 | mV | Cell undervoltage compensated trip threshold |
| Protections | CUVC | Delay | U1 | 0 | 255 | 2 | s | Cell undervoltage compensated trip delay |
| Protections | CUVC | Recovery | I2 | 0 | 32767 | 3000 | mV | Cell undervoltage compensated recovery threshold |

12.2.3 COV—Cell Overvoltage

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|-------------------------|------|-----|-------|---------|------|---|
| Protections | COV | Threshold Low Temp | I2 | 0 | 32767 | 4250 | mV | Cell overvoltage low temperature range trip threshold |
| Protections | COV | Threshold Standard Temp | I2 | 0 | 32767 | 4250 | mV | Cell overvoltage standard temperature range trip threshold |
| Protections | COV | Threshold High Temp | I2 | 0 | 32767 | 4250 | mV | Cell overvoltage high temperature range trip threshold |
| Protections | COV | Threshold Rec Temp | I2 | 0 | 32767 | 4250 | mV | Cell overvoltage recommended temperature range trip threshold |
| Protections | COV | Delay | U1 | 0 | 255 | 2 | s | Cell overvoltage trip delay |
| Protections | COV | Recovery Low Temp | I2 | 0 | 32767 | 4150 | mV | Cell overvoltage low temperature range recovery threshold |
| Protections | COV | Recovery Standard Temp | I2 | 0 | 32767 | 4150 | mV | Cell overvoltage standard temperature recovery range threshold |
| Protections | COV | Recovery High Temp | I2 | 0 | 32767 | 4150 | mV | Cell overvoltage high temperature range recovery threshold |
| Protections | COV | Recovery Rec Temp | I2 | 0 | 32767 | 4150 | mV | Cell overvoltage recommended temperature range recovery threshold |

12.2.4 OCC1—Overcurrent In Charge 1

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|-----------|------|--------|-------|---------|------|--|
| Protections | OCC1 | Threshold | I2 | –32768 | 32767 | 6000 | mA | Overcurrent in Charge 1 trip threshold |
| Protections | OCC1 | Delay | U1 | 0 | 255 | 6 | s | Overcurrent in Charge 1 trip delay |

12.2.5 OCC2—Overcurrent In Charge 2

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|-----------|------|--------|-------|---------|------|--|
| Protections | OCC2 | Threshold | I2 | –32768 | 32767 | 8000 | mA | Overcurrent in Charge 2 trip threshold |
| Protections | OCC2 | Delay | U1 | 0 | 255 | 3 | s | Overcurrent in Charge 2 trip delay |

12.2.6 OCC Overcurrent In Charge Recovery

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|--------------------|------|--------|-------|---------|------|--|
| Protections | OCC | Recovery Threshold | I2 | –32768 | 32767 | –50 | mA | Overcurrent in Charge 1 and 2 recovery threshold |
| Protections | OCC | Recovery Delay | U1 | 0 | 255 | 5 | s | Overcurrent in Charge 1 and 2 recovery delay |

12.2.7 OCD1—Overcurrent In Discharge 1

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|-----------|------|--------|-------|---------|------|---|
| Protections | OCD1 | Threshold | I2 | –32768 | 32767 | –6000 | mA | Overcurrent in Discharge 1 trip threshold |
| Protections | OCD1 | Delay | U1 | 0 | 255 | 6 | s | Overcurrent in Discharge 1 trip delay |

12.2.8 OCD2—Overcurrent In Discharge 2

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|-----------|------|--------|-------|---------|------|---|
| Protections | OCD2 | Threshold | I2 | –32768 | 32767 | –8000 | mA | Overcurrent in Discharge 2 trip threshold |
| Protections | OCD2 | Delay | U1 | 0 | 255 | 3 | s | Overcurrent in Discharge 2 trip delay |

12.2.9 OCD—Overcurrent In Discharge Recovery

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|----------------|------|--------|-------|---------|------|---|
| Protections | OCD | Recovery | I2 | –32768 | 32767 | 50 | mA | Overcurrent in Discharge 1 and 2 recovery threshold |
| Protections | OCD | Recovery Delay | U1 | 0 | 255 | 5 | s | Overcurrent in Discharge 1 and 2 recovery delay |

12.2.10 OLD—Overload in Discharge

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|-------------------|------|------|------|---------|--------|--|
| Protections | OLD | Threshold | H1 | 0x00 | 0x0F | 0x09 | 10 mV | Bit 3:0: Overload Trip Threshold between SRP and SRN Threshold can be set from 50 mV to 200 mV with 10 mV step. If Settings:AFE State Control[RSNS] = 1, threshold value will be divided in half. See Appendix A for details. |
| Protections | OLD | Delay | H1 | 0x00 | 0x0F | 0x0F | 2 ms | Bit 3:0: Overload Trip Delay Delay can be set from 1 ms to 31 s with 2-ms steps. See Appendix A for details. |
| Protections | OLD | Latch Limit | U1 | 0 | 255 | 0 | counts | Overload latch counter trip threshold |
| Protections | OLD | Counter Dec Delay | U1 | 0 | 255 | 10 | s | Overload latch counter decrement delay |
| Protections | OLD | Recovery | U1 | 0 | 255 | 5 | s | Overload recovery time |
| Protections | OLD | Reset | U1 | 0 | 255 | 15 | s | Overload latch reset time |

12.2.11 SCC—Short Circuit In Charge

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|-------------------|------|------|------|---------|------|--|
| Protections | SCC | Threshold | H1 | 0x00 | 0xFF | 0x77 | | Bit 2:0: Short Circuit in Charge Threshold—Threshold can be set from 100 mV to 300 mV in 50-mV steps. If Settings:AFE State Control[RSNS] = 1, Threshold value will be divided in half. Bit 3: Reserved Bit 7:4: Short Circuit in Charge Delay Time—Delay can be set from 0 μ s to 915 μ s in 61- μ s steps. See Appendix A for details. |
| Protections | SCC | Latch Limit | U1 | 0 | 255 | 0 | | Short Circuit in Charge Latch counter trip threshold |
| Protections | SCC | Counter Dec Delay | U1 | 0 | 255 | 10 | s | Short Circuit in Charge counter decrement delay |
| Protections | SCC | Recovery | U1 | 0 | 255 | 5 | s | Short Circuit in Charge recovery time |
| Protections | SCC | Reset | U1 | 0 | 255 | 15 | s | Short Circuit in Charge latch reset time |

12.2.12 SCD1—Short Circuit In Discharge 1

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|-----------|------|------|------|---------|------|---|
| Protections | SDC1 | Threshold | H1 | 0x00 | 0xFF | 0x77 | | Bit 2:0: Short Circuit in Discharge1 Threshold—Threshold can be set from 100 mV to 300 mV in 50 mV step. If Settings:AFE State Control[RSNS] = 1, Threshold value will be divided in half. Bit 3: Reserved Bit 7:4: Short Circuit in Discharge1 Delay Time—Delay can be set from 0 μ s to 915 μ s in 61- μ s step. If Settings:AFE State Control[SCDDx2] = 1, Delay Time value will be doubled. See Appendix A for details. |

12.2.13 SCD2—Short Circuit in Discharge 2

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|-----------|------|------|------|---------|------|---|
| Protections | SCD2 | Threshold | H1 | 0x00 | 0xFF | 0xE7 | | Bit 2:0: Short Circuit in Discharge2 Threshold—Threshold can be set from 100 mV to 300 mV in 50mV step. If Settings:AFE State Control[RSNS] = 1, Threshold value will be divided in half. Bit 3: Reserved Bit 7:4: Short Circuit in Discharge2 Delay Time—Delay can be set from 0 μ s to 458 μ s in 30 μ s step. If Settings:AFE State Control[SCDDx2] = 1, Delay Time value will be doubled. See Appendix A for details. |

12.2.14 SCD—Short Circuit in Discharge

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|-------------------|------|-----|-----|---------|------|---|
| Protections | SCD | Latch Limit | U1 | 0 | 255 | 0 | | Short Circuit in Discharge Latch counter trip threshold |
| Protections | SCD | Counter Dec Delay | U1 | 0 | 255 | 10 | s | Short Circuit in Discharge counter decrement delay |
| Protections | SCD | Recovery | U1 | 0 | 255 | 5 | s | Short Circuit in Discharge recovery time |
| Protections | SCD | Reset | U1 | 0 | 255 | 15 | s | Short Circuit in Discharge latch reset time |

12.2.15 OTC—Over Temperature in Charge

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|-----------|------|------|------|---------|-------|--|
| Protections | OTC | Threshold | I2 | –400 | 1500 | 550 | 0.1°C | Over Temperature in Charge trip threshold |
| Protections | OTC | Delay | U1 | 0 | 255 | 2 | s | Over Temperature in Charge Cell trip delay |
| Protections | OTC | Recovery | I2 | –400 | 1500 | 500 | 0.1°C | Over Temperature in Charge Cell recovery threshold |

12.2.16 OTD—Over Temperature in Discharge

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|-----------|------|------|------|---------|-------|--|
| Protections | OTD | Threshold | I2 | –400 | 1500 | 600 | 0.1°C | Over Temperature in Discharge trip threshold |
| Protections | OTD | Delay | U1 | 0 | 255 | 2 | s | Over Temperature in Discharge trip delay |
| Protections | OTD | Recovery | I2 | –400 | 1500 | 550 | 0.1°C | Over Temperature in Discharge recovery threshold |

12.2.17 OTF—Over Temperature FET

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|-----------|------|------|------|---------|-------|---|
| Protections | OTF | Threshold | I2 | –400 | 1500 | 800 | 0.1°C | Over Temperature FET trip threshold |
| Protections | OTF | Delay | U1 | 0 | 255 | 2 | s | Over Temperature FET trip delay |
| Protections | OTF | Recovery | I2 | –400 | 1500 | 650 | 0.1°C | Over Temperature FET recovery threshold |

12.2.18 HWD—Host Watchdog

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|-------|------|-----|-----|---------|------|------------------------------|
| Protections | HWD | Delay | U1 | 0 | 255 | 10 | s | SBS Host watchdog trip delay |

12.2.19 PTO—Pre Charge Mode Time Out

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|-------------------|------|--------|-------|---------|------|--------------------------------------|
| Protections | PTO | Charge Threshold | I2 | –32768 | 32767 | 2000 | mA | Pre-Charge Timeout Current Threshold |
| Protections | PTO | Suspend Threshold | I2 | –32768 | 32767 | 1800 | mA | Pre-Charge Timeout Suspend Threshold |
| Protections | PTO | Delay | U2 | 0 | 65535 | 1800 | s | Pre-Charge Timeout trip delay |
| Protections | PTO | Reset | I2 | –32768 | 32767 | 2 | mA | Pre-Charge Timeout Reset Threshold |

12.2.20 CTO—Fast Charge Mode Time Out

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|-------------------|------|--------|-------|---------|------|---------------------------------------|
| Protections | PTO | Charge Threshold | I2 | –32768 | 32767 | 2500 | mA | Fast-Charge Timeout Current Threshold |
| Protections | PTO | Suspend Threshold | I2 | –32768 | 32767 | 2000 | mA | Fast-Charge Timeout Suspend Threshold |
| Protections | PTO | Delay | U2 | 0 | 65535 | 54000 | s | Fast-Charge Timeout trip delay |
| Protections | PTO | Reset | I2 | –32768 | 32767 | 2 | mA | Fast-Charge Timeout Reset Threshold |

12.2.21 OC—Over Charge

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|---------------|------|--------|-------|---------|------|--|
| Protections | OC | Threshold | I2 | –32768 | 32767 | 300 | mAh | Overcharge trip threshold |
| Protections | OC | Recovery | I2 | –32768 | 32767 | 2 | mAh | Overcharge recovery threshold |
| Protections | OC | RSOC Recovery | U1 | 0 | 100 | 90 | % | Overcharge RemainingStateOfCharge() recovery threshold |

12.2.22 CHGV—Charging Voltage

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|-----------|------|--------|-------|---------|------|---|
| Protections | CHGV | Threshold | I2 | –32768 | 32767 | 500 | mV | ChargingVoltage() delta trip threshold |
| Protections | CHGV | Delay | U1 | 0 | 255 | 30 | s | ChargingVoltage() delta trip delay |
| Protections | CHGV | Recovery | I2 | –32768 | 32767 | –500 | mV | ChargingVoltage() delta recovery threshold |

12.2.23 CHGC—ChargingCurrent

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|-----------|------|--------|-------|---------|------|--|
| Protections | CHGC | Threshold | I2 | –32768 | 32767 | 500 | mA | ChargingCurrent() delta trip threshold |
| Protections | CHGC | Delay | U1 | 0 | 255 | 2 | s | ChargingCurrent() delta trip delay |
| Protections | CHGC | Recovery | I2 | –32768 | 32767 | 100 | mA | ChargingCurrent() delta recovery threshold |

12.3 Permanent Fail

12.3.1 CUV—Cell Undervoltage

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------|----------|-----------|------|-----|-------|---------|------|----------------------------------|
| Permanent Fail | CUV | Threshold | I2 | 0 | 32767 | 2500 | mV | Cell Undervoltage trip threshold |
| Permanent Fail | CUV | Delay | U1 | 0 | 255 | 2 | s | Cell Undervoltage trip delay |

12.3.2 COV—Cell Overvoltage

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------|----------|-----------|------|-----|-------|---------|------|---------------------------------|
| Permanent Fail | COV | Threshold | I2 | 0 | 32767 | 4400 | mV | Cell Overvoltage trip threshold |
| Permanent Fail | COV | Delay | U1 | 0 | 255 | 2 | s | Cell Overvoltage trip delay |

12.3.3 CUDEP—Copper Deposition

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------|----------|-----------|------|-----|-------|---------|------|----------------------------------|
| Permanent Fail | CUDEP | Threshold | I2 | 0 | 32767 | 2500 | mV | Copper Deposition trip threshold |
| Permanent Fail | CUDEP | Delay | U1 | 0 | 255 | 2 | s | Copper Deposition trip delay |

12.3.4 OTCE—Over Temperature Cell

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------|----------|-----------|------|------|------|---------|-------|--------------------------------------|
| Permanent Fail | OTCE | Threshold | I2 | –400 | 1500 | 650 | 0.1°C | Over Temperature Cell trip threshold |
| Permanent Fail | OTCE | Delay | U1 | 0 | 255 | 2 | s | Over Temperature Cell trip delay |

12.3.5 OTF—Over Temperature FET

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------|----------|-----------|------|------|------|---------|-------|-------------------------------------|
| Permanent Fail | OTF | Threshold | I2 | –400 | 1500 | 1000 | 0.1°C | Over Temperature FET trip threshold |
| Permanent Fail | OTF | Delay | U1 | 0 | 255 | 2 | s | Over Temperature FET trip delay |

12.3.6 QIM—QMax Imbalance

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------|----------|-----------|------|-----|-------|---------|---------|-------------------------------|
| Permanent Fail | QIM | Threshold | I2 | 0 | 32767 | 500 | mAh | QMax Imbalance trip threshold |
| Permanent Fail | QIM | Delay | U1 | 0 | 255 | 2 | updates | QMax Imbalance trip delay |

12.3.7 CB—Cell Balance

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------|----------|-----------------|------|-----|-------|---------|--------|--|
| Permanent Fail | CB | Max Threshold | I2 | 0 | 32767 | 120 | 2h | Cell Balance max trip threshold |
| Permanent Fail | CB | Delta Threshold | U1 | 0 | 32767 | 20 | 2h | Cell Balance cell delta trip threshold |
| Permanent Fail | CB | Delay | U1 | 0 | 255 | 2 | cycles | Cell Balance trip delay |

12.3.8 VIMR—Voltage Imbalance at Rest

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------|----------|-----------------|------|-----|-------|---------|------|--|
| Permanent Fail | VIMR | Check Voltage | I2 | 0 | 5000 | 3600 | mV | Voltage Imbalance at Rest Check Voltage |
| Permanent Fail | VIMR | Check Current | I2 | 0 | 32767 | 10 | mA | Voltage Imbalance at Rest Check Current |
| Permanent Fail | VIMR | Delta Threshold | I2 | 0 | 5000 | 200 | mV | Voltage Imbalance at Rest trip threshold |
| Permanent Fail | VIMR | Delay | U1 | 0 | 255 | 2 | s | Voltage Imbalance at Rest Check trip delay |
| Permanent Fail | VIMR | Duration | U2 | 0 | 65535 | 100 | s | Voltage Imbalance at Rest Check Duration |

12.3.9 VIMA—Voltage Imbalance Active

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------|----------|-----------------|------|-----|-------|---------|------|---|
| Permanent Fail | VIMA | Check Voltage | I2 | 0 | 5000 | 3600 | mV | Voltage Imbalance active Check Voltage |
| Permanent Fail | VIMA | Check Current | I2 | 0 | 32767 | 10 | mA | Voltage Imbalance active Check Current |
| Permanent Fail | VIMA | Delta Threshold | I2 | 0 | 5000 | 300 | mV | Voltage Imbalance active trip threshold |
| Permanent Fail | VIMA | Delay | U1 | 0 | 255 | 2 | s | Voltage Imbalance active Check trip delay |

12.3.10 IMP—Impedance Imbalance

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------|----------|-----------------|------|-----|-------|---------|------------|-------------------------------------|
| Permanent Fail | IMP | Delta Threshold | U1 | 0 | 32767 | 400 | % | Impedance Imbalance delta threshold |
| Permanent Fail | IMP | Max Threshold | I2 | 0 | 32767 | 300 | % | Impedance Imbalance max threshold |
| Permanent Fail | IMP | Delay | U1 | 0 | 255 | 2 | RA updates | Impedance Imbalance trip delay |

12.3.11 CD—Capacity Degradation

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------|----------|-----------|------|-----|-------|---------|--------|---------------------------------|
| Permanent Fail | CD | Threshold | I2 | 0 | 32767 | 4200 | mAh | Capacity Degradation threshold |
| Permanent Fail | CD | Delay | U1 | 0 | 255 | 2 | cycles | Capacity Degradation trip delay |

12.3.12 CFETF—CHG FET Failure

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------|----------|---------------|------|-----|-----|---------|------|------------------------------------|
| Permanent Fail | CFETF | OFF Threshold | I2 | 0 | 500 | 5 | mA | CHG FET OFF current trip threshold |
| Permanent Fail | CFETF | Delay | U1 | 0 | 255 | 2 | s | CHG FET OFF trip delay |

12.3.13 DFET—DFET Failure

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------|----------|---------------|------|------|-----|---------|------|------------------------------------|
| Permanent Fail | DFET | OFF Threshold | I2 | –500 | 0 | –5 | mA | DSG FET OFF current trip threshold |
| Permanent Fail | DFET | Delay | U1 | 0 | 255 | 2 | s | DSG FET OFF trip delay |

12.3.14 TH—NTC Thermistor Failure

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------|----------|--------------------|------|-----|-------|---------|------------|--|
| Permanent Fail | TH | ADC High Threshold | U2 | 0 | 65535 | 32752 | A/D counts | Thermistor open fail raw ADC trip threshold |
| Permanent Fail | TH | ADC Low Threshold | U2 | 0 | 65535 | 15 | A/D counts | Thermistor short fail raw ADC trip threshold |
| Permanent Fail | TH | ADC Delay | U1 | 0 | 255 | 10 | s | Thermistor fail trip delay |

12.3.15 FUSE—FUSE Failure

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------|----------|-----------|------|-----|-----|---------|------|-------------------------------------|
| Permanent Fail | FUSE | Threshold | I2 | 0 | 255 | 5 | mA | FUSE activation fail trip threshold |
| Permanent Fail | FUSE | Delay | U1 | 0 | 255 | 2 | s | FUSE activation fail trip delay |

12.3.16 AFER—AFE Register

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------|----------|----------------|------|-----|-----|---------|--------|---|
| Permanent Fail | AFER | Threshold | U1 | 0 | 255 | 100 | counts | AFE Register comparison fail trip threshold |
| Permanent Fail | AFER | Delay Period | U1 | 0 | 255 | 2 | s | AFE Register comparison fail trip delay |
| Permanent Fail | AFER | Compare Period | U1 | 0 | 255 | 3 | s | AFE Register comparison compare period |

12.3.17 AFEC—AFE Communication

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------|----------|--------------|------|-----|-----|---------|--------|---------------------------------------|
| Permanent Fail | AFEC | Threshold | U1 | 0 | 255 | 100 | counts | AFE Communication fail trip threshold |
| Permanent Fail | AFEC | Delay Period | U1 | 0 | 255 | 5 | s | AFE Communication fail trip delay |

12.3.18 2LVL—2nd Level OV

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------|----------|-----------|------|-----|-----|---------|------|--|
| Permanent Fail | 2LVL | Threshold | U1 | 0 | 255 | 2 | s | 2nd Level Protector trip detection delay |

12.3.19 OCECO—Open Cell Connection

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------|----------|--------------|------|-----|-------|---------|------|---|
| Permanent Fail | OCECO | Threshold | U2 | 0 | 32767 | 5000 | mV | Open Cell Tab Connection trip threshold |
| Permanent Fail | OCECO | Delay Period | U1 | 0 | 255 | 2 | s | Open Cell Tab Connection trip delay |

12.4 Advanced Charge Algorithm

12.4.1 Temperature Ranges

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------------------|--------------------|------|------|------|-----|---------|------|--|
| Advanced Charge Algorithms | Temperature Ranges | T1 | I1 | –128 | 127 | 0 | | T1 low temperature range lower limit |
| Advanced Charge Algorithms | Temperature Ranges | T2 | I1 | –128 | 127 | 12 | | T2 low temperature range to standard temperature range |

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------------------|--------------------|------------|------|------|-----|---------|------|--|
| Advanced Charge Algorithms | Temperature Ranges | T5 | I1 | -128 | 127 | 30 | | T5 recommended temperature range lower limit |
| Advanced Charge Algorithms | Temperature Ranges | T6 | I1 | -128 | 127 | 55 | | T6 recommended temperature range upper limit |
| Advanced Charge Algorithms | Temperature Ranges | T3 | I1 | -128 | 127 | 20 | | T3 standard temperature range to high temperature range |
| Advanced Charge Algorithms | Temperature Ranges | T4 | I1 | -128 | 127 | 25 | | T4 high temperature range upper limit |
| Advanced Charge Algorithms | Temperature Ranges | Hysteresis | I1 | -128 | 127 | 0 | | Temperature Hysteresis, applied when temperature is decreasing |

12.4.2 Low Temp Charging

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------------------|-------------------|--------------|------|-----|-------|---------|------|--|
| Advanced Charge Algorithms | Low Temp Charging | Voltage | I2 | 0 | 32767 | 3000 | mV | Low temperature range ChargingVoltage() |
| Advanced Charge Algorithms | Low Temp Charging | Current Low | I2 | 0 | 32767 | 132 | mA | Low temperature range low voltage range ChargingCurrent() |
| Advanced Charge Algorithms | Low Temp Charging | Current Med | I2 | 0 | 32767 | 352 | mA | Low temperature range medium voltage range ChargingCurrent() |
| Advanced Charge Algorithms | Low Temp Charging | Current High | I2 | 0 | 32767 | 264 | mA | Low temperature range high voltage range ChargingCurrent() |

12.4.3 Standard Temp Charging

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------------------|------------------------|--------------|------|-----|-------|---------|------|---|
| Advanced Charge Algorithms | Standard Temp Charging | Voltage | I2 | 0 | 32767 | 4200 | mV | Standard temperature range ChargingVoltage() |
| Advanced Charge Algorithms | Standard Temp Charging | Current Low | I2 | 0 | 32767 | 1980 | mA | Standard temperature range low voltage range ChargingCurrent() |
| Advanced Charge Algorithms | Standard Temp Charging | Current Med | I2 | 0 | 32767 | 4004 | mA | Standard temperature range medium voltage range ChargingCurrent() |
| Advanced Charge Algorithms | Standard Temp Charging | Current High | I2 | 0 | 32767 | 2992 | mA | Standard temperature range high voltage range ChargingCurrent() |

12.4.4 High Temp Charging

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------------------|--------------------|-------------|------|-----|-------|---------|------|--|
| Advanced Charge Algorithms | High Temp Charging | Voltage | I2 | 0 | 32767 | 4000 | mV | High temperature range ChargingVoltage() |
| Advanced Charge Algorithms | High Temp Charging | Current Low | I2 | 0 | 32767 | 1012 | mA | High temperature range low voltage range ChargingCurrent() |

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------------------|--------------------|--------------|------|-----|-------|---------|------|---|
| Advanced Charge Algorithms | High Temp Charging | Current Med | I2 | 0 | 32767 | 1980 | mA | High temperature range medium voltage range ChargingCurrent() |
| Advanced Charge Algorithms | High Temp Charging | Current High | I2 | 0 | 32767 | 1496 | mA | High temperature range high voltage range ChargingCurrent() |

12.4.5 REC Temp Charging

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------------------|-------------------|--------------|------|-----|-------|---------|------|--|
| Advanced Charge Algorithms | Rec Temp Charging | Voltage | I2 | 0 | 32767 | 4100 | mV | Recommended temperature range ChargingVoltage() |
| Advanced Charge Algorithms | Rec Temp Charging | Current Low | I2 | 0 | 32767 | 2508 | mA | Recommended temperature range low voltage range ChargingCurrent() |
| Advanced Charge Algorithms | Rec Temp Charging | Current Med | I2 | 0 | 32767 | 4488 | mA | Recommended temperature range medium voltage range ChargingCurrent() |
| Advanced Charge Algorithms | Rec Temp Charging | Current High | I2 | 0 | 32767 | 3520 | mA | Recommended temperature range high voltage range ChargingCurrent() |

12.4.6 PCHG

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------------------|----------|---------|------|-----|-------|---------|------|------------------------------|
| Advanced Charge Algorithms | PCHG | Current | I2 | 0 | 32767 | 88 | mA | Pre-Charge ChargingCurrent() |

12.4.7 MCHG

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------------------|----------|---------|------|-----|-------|---------|------|-------------------------------|
| Advanced Charge Algorithms | MCHG | Current | I2 | 0 | 32767 | 44 | mA | Maintenance ChargingCurrent() |

12.4.8 Voltage Range

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------------------|---------------|-----------------------|------|-----|-------|---------|------|--|
| Advanced Charge Algorithms | Voltage Range | Charging Voltage Low | I2 | 0 | 32767 | 2500 | mV | Pre-Charge Voltage range to Charging Voltage Low range |
| Advanced Charge Algorithms | Voltage Range | Charging Voltage Med | I2 | 0 | 32767 | 3600 | mV | Charging Voltage Low range to Charging Voltage Med range |
| Advanced Charge Algorithms | Voltage Range | Charging Voltage High | I2 | 0 | 32767 | 4000 | mV | Charging Voltage Med to Charging Voltage High range |
| Advanced Charge Algorithms | Voltage Range | Hysteresis | U1 | 0 | 255 | 0 | mV | Charging Voltage Hysteresis applied when voltage is decreasing |

12.4.9 Termination Config

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------------------|--------------------|---------------------------|------|-----|-------|---------|------|--|
| Advanced Charge Algorithms | Termination Config | Charge Term Taper Current | I2 | 0 | 32767 | 250 | mA | Valid Charge Termination taper current qualifier threshold |
| Advanced Charge Algorithms | Termination Config | Charge Term Voltage | I2 | 0 | 32767 | 75 | mV | Valid Charge Termination delta voltage qualifier, max cell based |

12.4.10 Cell Balancing Config

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------------------|-----------------------|-------------------------------|------|-----|------------|---------|-------|--|
| Advanced Charge Algorithms | Cell Balancing Config | Balance Time per mAh cell 0 | U2 | 0 | 65535 | 367 | s/mAh | Required balance time per mAh, calculated based on external resistor value at VCx pins using following formula: $3600 \text{ mA*s} / (\text{VCELL} / (\text{RVCX} + \text{RCB}) * \text{DUTY}) / 1000$ where: VCELL = average cell voltage (3.7 V) RVCX = resistor value in series to VCx input (100 Ω) RCB = cell balancing FET RDSON (150 Ω) DUTY = cell balancing duty cycle (66%) |
| Advanced Charge Algorithms | Cell Balancing Config | Balance Time per mAh cell 1–3 | U2 | 0 | 65535 | 514 | s/mAh | Required balance time per mAh, calculated based on external resistor value at VCx pins using following formula: $3600 \text{ mA*s} / (\text{VCELL} / (2 * \text{RVCX} + \text{RCB}) * \text{DUTY}) / 1000$ where: VCELL = average cell voltage (3.7 V) RVCX = resistor value in series to VCx input (100 Ω) RCB = cell balancing FET RDSON (150 Ω) DUTY = cell balancing duty cycle (66%) |
| Advanced Charge Algorithms | Cell Balancing Config | Min Start Balance Delta | U1 | 0 | 255 | 3 | mV | Minimum cell voltage delta to start cell balancing. This condition is checked in relaxation state and so it only applies if cell balancing at reset is enabled. |
| Advanced Charge Algorithms | Cell Balancing Config | Relax Balance Interval | U4 | 0 | 4294967295 | 18000 | s | Minimum relax time after cell balancing stopped to enable balancing again. This parameter applies to cell balancing at reset only. |
| Advanced Charge Algorithms | Cell Balancing Config | Min RSOC for Balancing | U1 | 0 | 100 | 80 | % | Minimum RelativeStateOfCharge() threshold for cell balancing. This condition is checked during relaxation and so it only applies if cell balancing at reset is enabled. |

12.4.11 Charging Rate of Change

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------------------|-------------------------|--------------|------|-----|-----|---------|---------|--|
| Advanced Charge Algorithms | Charging Rate of Change | Current Rate | U1 | 1 | 255 | 1 | steps/s | Number of steps to add between any 2 ChargingCurrent() settings |
| Advanced Charge Algorithms | Charging Rate of Change | Voltage Rate | U1 | 1 | 255 | 1 | steps/s | Number of steps to add between any 2 ChargingVoltage() settings |

12.4.12 Charge Loss Compensation

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|----------------------------|--------------------------|-----------------------|------|-----|-------|---------|------|--|
| Advanced Charge Algorithms | Charge Loss Compensation | CCC Current Threshold | I2 | 0 | 32767 | 3520 | mA | Constant Current Charge mode ChargingCurrent() threshold to activate Charge Loss Compensation |
| Advanced Charge Algorithms | Charge Loss Compensation | CCC Voltage Threshold | I2 | 0 | 255 | 4200 | mV | Constant Current Charge mode max ChargingVoltage() increase limit |

12.5 System Data

12.5.1 Manufacturer Data

| Class | Subclass | Name | Type | Min | Max | Unit | Description |
|-------------|-------------------|------------------|------|-----|-------|------|---|
| System Data | Manufacturer Data | ManufacturerInfo | S33 | | | | ManufacturerInfo() value |
| System Data | Manufacturer Data | DF Checksum | U2 | 0 | 65535 | | Holding place for DF checksum, not modified or read by device, for reference only |

12.6 SBS Configuration

12.6.1 Data

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------------|----------|-------------------------|------|-----|-------|---------|--------|---|
| SBS Configuration | Data | Remaining Ah Cap. Alarm | I2 | 0 | 32767 | 300 | mAh | RemainingCapacityAlarm() value in mAh |
| SBS Configuration | Data | Remaining Wh Cap. Alarm | I2 | 0 | 32767 | 432 | 10 mWh | RemainingCapacityAlarm() value in 10 mWh |
| SBS Configuration | Data | Remaining Time Alarm | U2 | 0 | 65535 | 10 | min | RemainingTimeAlarm() value |

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------------|----------|---------------------------|------|--------|--------|---------|--------|--|
| SBS Configuration | Data | Initial Battery Mode | H2 | 0x0000 | 0xFFFF | 0x81 | | BatteryMode() value Bit 0: ICC Internal_Charge_Controller 0 = Function not supported Bit 1: PBC Primary_Battery_Support 1 = Primary or Secondary Battery Support Bit 2: Reserved Bit 3: Reserved Bit 4: Reserved Bit 5: Reserved Bit 6: Reserved Bit 7: CF—Condition_Flag 0 = Battery OK 1 = Conditioning cycle requested Bit 8: CCE—Charge_Controller_Enabled (R/W) 0 = Internal charge controller disabled Bit 9: PB—Primary_Battery (R/W) 0 = Battery operating in its secondary role (default) 1 = Battery operating in its primary role Bit 10: Reserved Bit 11: Reserved Bit 12: Reserved Bit 13: AM—Alarm Mode (R/W) 0 = Enable Alarm Warning broadcasts to host and smart battery charger 1 = Disable Alarm Warning broadcasts to host and smart battery charger Bit 14: CHGM—Charger_Mode (R/W) 0 = Enable ChargingVoltage() and ChargingCurrent() broadcasts to host and smart battery charger 1 = Disable ChargingVoltage() and ChargingCurrent() broadcasts to host and smart battery charger Bit 15: CAPM—Capacity_Mode (R/W) 0 = Report in mA or mAh (default) 1 = Report in 10 mW or 10 mWh |
| SBS Configuration | Data | Design Voltage | I2 | 0 | 32767 | 14400 | mV | DesignVoltage() value |
| SBS Configuration | Data | Specification Information | H2 | 0x0000 | 0xFFFF | 0x31 | | SpecificationInfo() value in the following format: Bit 0,1,2,3: Revision Revision 0,0,0,1 = Version 1.0 and 1.1 (default) Bit 4,5,6,7: Version Version 0,0,0,1 = Version 1.0 0,0,1,1 = Version 1.1 0,0,1,1 = Version 1.1 with optional PEC support Bit 8,9,10,11: VScale Voltage Scale Factor 0,0,0,0 = reported voltages scaled by 10E0 0,0,0,1 = reported voltages scaled by 10E1 0,0,1,0 = reported voltages scaled by 10E2 0,0,1,1 = reported voltages scaled by 10E3 Bit 12,13,14,15: IPScale Voltage Scale Factor 0,0,0,0 = reported currents and capacities scaled by 10E0 except ChargingVoltage() and ChargingCurrent() 0,0,0,1 = reported currents and capacities scaled by 10E1 except ChargingVoltage() and ChargingCurrent() 0,0,1,0 = reported currents and capacities scaled by 10E2 except ChargingVoltage() and ChargingCurrent() 0,0,1,1 = reported currents and capacities scaled by 10E3 except ChargingVoltage() and ChargingCurrent() |
| SBS Configuration | Data | Manufacturer Date | U2 | 0 | 65535 | | | ManufacturerDate() value in the following format: Day + Month*32 + (Year–1980)*256 |
| SBS Configuration | Data | Serial Number | H2 | 0x0000 | 0xFFFF | | | SerialNumber() value |
| SBS Configuration | Data | Cycle Count | U2 | 0 | 65535 | | cycles | CycleCount() value |
| SBS Configuration | Data | Cycle Count Percentage | U1 | 0 | 255 | 90 | % | Accumulated discharge of FullChargeCapacity() * (Cycle Count Percentage) to increment CycleCount() |
| SBS Configuration | Data | Max Error Limit | U1 | 0 | 100 | 100 | % | MaxError() threshold to set BatteryMode()[CF] |
| SBS Configuration | Data | Design Capacity | I2 | 0 | 32767 | 4400 | mAh | DesignCapacity() value in mAh |
| SBS Configuration | Data | Design Capacity | I2 | 0 | 32767 | 6336 | 10 mWh | DesignCapacity() value in 10 mWh |
| SBS Configuration | Data | Manufacturer Name | S21 | | | | | ManufacturerName() value |

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------------|----------|------------------|------|-----|-----|---------|------|--------------------------------|
| SBS Configuration | Data | Device Name | S21 | | | | | DeviceName() value |
| SBS Configuration | Data | Device Chemistry | S5 | | | | | DeviceChemistry() value |

12.6.2 FD

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------------|----------|-------------------------|------|-----|------|---------|------|--|
| SBS Configuration | FD | Set Voltage Threshold | I2 | 0 | 5000 | 3000 | mV | BatteryStatus()[FD] cell voltage set threshold |
| SBS Configuration | FD | Clear Voltage Threshold | I2 | 0 | 5000 | 3100 | mV | BatteryStatus()[FD] cell voltage clear threshold |
| SBS Configuration | FD | Set RSOC % Threshold | U1 | 0 | 100 | 0 | % | BatteryStatus()[FD]RemainingStateOfCharge() set threshold |
| SBS Configuration | FD | Clear RSOC % Threshold | U1 | 0 | 100 | 5 | % | BatteryStatus()[FD]RemainingStateOfCharge() clear threshold |

12.6.3 FC

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------------|----------|-------------------------|------|-----|------|---------|------|---|
| SBS Configuration | FC | Set Voltage Threshold | I2 | 0 | 5000 | 4200 | mV | BatteryStatus()[FC] cell voltage set threshold |
| SBS Configuration | FC | Clear Voltage Threshold | I2 | 0 | 5000 | 4100 | mV | BatteryStatus()[FC] cell voltage clear threshold |
| SBS Configuration | FC | Set RSOC % Threshold | U1 | 0 | 100 | 100 | % | BatteryStatus()[FC]RemainingStateOfCharge() set threshold |
| SBS Configuration | FC | Clear RSOC % Threshold | U1 | 0 | 100 | 95 | % | BatteryStatus()[FC] RemainingStateOfCharge() clear threshold |

12.6.4 TDA

Per the Smart Battery Data Specification 1.1, TDA is only active while discharging.

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------------|----------|-------------------------|------|-----|------|---------|------|--|
| SBS Configuration | TDA | Set Voltage Threshold | I2 | 0 | 5000 | 3200 | mV | BatteryStatus()[TDA] cell voltage set threshold |
| SBS Configuration | TDA | Clear Voltage Threshold | I2 | 0 | 5000 | 3300 | mV | BatteryStatus()[TDA] cell voltage clear threshold |
| SBS Configuration | TDA | Set RSOC % Threshold | U1 | 0 | 100 | 10 | % | BatteryStatus()[TDA] RemainingStateOfCharge() set threshold |
| SBS Configuration | TDA | Clear RSOC % Threshold | U1 | 0 | 100 | 15 | % | BatteryStatus()[TDA] RemainingStateOfCharge() clear threshold |

12.6.5 TCA

Per the Smart Battery Data Specification 1.1, TCA is only active while charging.

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------------|----------|-------------------------|------|-----|------|---------|------|--|
| SBS Configuration | TCA | Set Voltage Threshold | I2 | 0 | 5000 | 4200 | mV | BatteryStatus()[TCA] cell voltage set threshold |
| SBS Configuration | TCA | Clear Voltage Threshold | I2 | 0 | 5000 | 4100 | mV | BatteryStatus()[TCA] cell voltage clear threshold |
| SBS Configuration | TCA | Set RSOC % Threshold | U1 | 0 | 100 | 100 | % | BatteryStatus()[TCA] RemainingStateOfCharge() set threshold |
| SBS Configuration | TCA | Clear RSOC % Threshold | U1 | 0 | 100 | 95 | % | BatteryStatus()[TCA] RemainingStateOfCharge() clear threshold |

12.6.6 Max Error

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------------|-----------|-----------------------|------|-----|-----|---------|-------|--|
| SBS Configuration | Max Error | Time Cycle Equivalent | U1 | 0 | 255 | 12 | 2h | After valid QMax update, each passed time period of Time Cycle Equivalent will increment of MaxError() by Cycle Delta. Time Cycle Equivalent is provided for packs which may not get frequent Qmax updates like stand-by batteries. Time Cycle Equivalent increments Max Error by 0.05% for every Time Cycle Equivalent time period following the last Qmax update. |
| SBS Configuration | Max Error | Cycle Delta | U1 | 0 | 255 | 5 | 0.01% | Each increment of CycleCount() after valid QMax update will increment of MaxError() by Cycle Delta |

12.7 Lifetimes

12.7.1 Voltage

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-----------|----------|------------------------|------|-----|-----|---------|-------|---|
| Lifetimes | Voltage | Max Voltage Cell 0 | U1 | 0 | 255 | 0 | 20 mV | Maximum reported cell voltage 0 |
| Lifetimes | Voltage | Max Voltage Cell 1 | U1 | 0 | 255 | 0 | 20 mV | Maximum reported cell voltage 1 |
| Lifetimes | Voltage | Max Voltage Cell 2 | U1 | 0 | 255 | 0 | 20 mV | Maximum reported cell voltage 2 |
| Lifetimes | Voltage | Max Voltage Cell 3 | U1 | 0 | 255 | 0 | 20 mV | Maximum reported cell voltage 3 |
| Lifetimes | Voltage | Min Voltage Cell 0 | U1 | 0 | 255 | 255 | 20 mV | Minimum reported cell voltage 0 |
| Lifetimes | Voltage | Min Voltage Cell 1 | U1 | 0 | 255 | 255 | 20 mV | Minimum reported cell voltage 1 |
| Lifetimes | Voltage | Min Voltage Cell 2 | U1 | 0 | 255 | 255 | 20 mV | Minimum reported cell voltage 2 |
| Lifetimes | Voltage | Min Voltage Cell 3 | U1 | 0 | 255 | 255 | 20 mV | Minimum reported cell voltage 3 |
| Lifetimes | Voltage | Max Delta Cell Voltage | U1 | 0 | 255 | 0 | 20 mV | Maximum reported delta between cell voltages 0 to 3 |

12.7.2 Current

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-----------|----------|---------------------|------|-----|-----|---------|--------|---|
| Lifetimes | Current | Max Chg Current | U1 | 0 | 255 | 0 | 200 mA | Maximum reported Current() in charge direction |
| Lifetimes | Current | Max Dsg Current | U1 | 0 | 255 | 0 | 200 mA | Maximum reported Current() in discharge direction |
| Lifetimes | Current | Max Avg Dsg Current | U1 | 0 | 255 | 0 | 200 mA | Maximum reported AverageCurrent() in discharge direction |
| Lifetimes | Current | Max Avg Dsg Power | U1 | 0 | 255 | 0 | W | Maximum reported Power in discharge direction |

12.7.3 Safety Events

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-----------|---------------|-------------------|------|-----|-----|---------|----------|--|
| Lifetimes | Safety Events | No of COV Events | U1 | 0 | 255 | 0 | 8 events | Total number of SafetyStatus()[COV] events |
| Lifetimes | Safety Events | Last COV Event | U1 | 0 | 255 | 0 | 4 cycles | Last SafetyStatus()[COV] event in CycleCount() cycles |
| Lifetimes | Safety Events | No of CUV Events | U1 | 0 | 255 | 0 | 8 events | Total number of SafetyStatus()[CUV] events |
| Lifetimes | Safety Events | Last CUV Event | U1 | 0 | 255 | 0 | 4 cycles | Last SafetyStatus()[CUV] event in CycleCount() cycles |
| Lifetimes | Safety Events | No of OCD1 Events | U1 | 0 | 255 | 0 | 8 events | Total number of SafetyStatus()[OCD1] events |
| Lifetimes | Safety Events | Last OCD1 Event | U1 | 0 | 255 | 0 | 4 cycles | Last SafetyStatus()[OCD1] event in CycleCount() cycles |
| Lifetimes | Safety Events | No of OCD2 Events | U1 | 0 | 255 | 0 | 8 events | Total number of SafetyStatus()[OCD2] events |
| Lifetimes | Safety Events | Last OCD2 Event | U1 | 0 | 255 | 0 | 4 cycles | Last SafetyStatus()[OCD2] event in CycleCount() cycles |
| Lifetimes | Safety Events | No of OCC1 Events | U1 | 0 | 255 | 0 | 8 events | Total number of SafetyStatus()[OCC1] events |
| Lifetimes | Safety Events | Last OCC1 Event | U1 | 0 | 255 | 0 | 4 cycles | Last SafetyStatus()[OCC1] event in CycleCount() cycles |
| Lifetimes | Safety Events | No of OCC2 Events | U1 | 0 | 255 | 0 | 8 events | Total number of SafetyStatus()[OCC2] events |
| Lifetimes | Safety Events | Last OCC2 Event | U1 | 0 | 255 | 0 | 4 cycles | Last SafetyStatus()[OCC2] event in CycleCount() cycles |
| Lifetimes | Safety Events | No of OLD Events | U1 | 0 | 255 | 0 | 8 events | Total number of SafetyStatus()[OLD] events |
| Lifetimes | Safety Events | Last OLD Event | U1 | 0 | 255 | 0 | 4 cycles | Last SafetyStatus()[OLD] event in CycleCount() cycles |
| Lifetimes | Safety Events | No of SCD Events | U1 | 0 | 255 | 0 | 8 events | Total number of SafetyStatus()[SCD] events |
| Lifetimes | Safety Events | Last SCD Event | U1 | 0 | 255 | 0 | 4 cycles | Last SafetyStatus()[SCD] event in CycleCount() cycles |
| Lifetimes | Safety Events | No of SCC Events | U1 | 0 | 255 | 0 | 8 events | Total number of SafetyStatus()[SCC] events |
| Lifetimes | Safety Events | Last SCC Event | U1 | 0 | 255 | 0 | 4 cycles | Last SafetyStatus()[SCC] event in CycleCount() cycles |
| Lifetimes | Safety Events | No of OTC Events | U1 | 0 | 255 | 0 | 8 events | Total number of SafetyStatus()[OTC] events |
| Lifetimes | Safety Events | Last OTC Event | U1 | 0 | 255 | 0 | 4 cycles | Last SafetyStatus()[OTC] event in CycleCount() cycles |
| Lifetimes | Safety Events | No of OTD Events | U1 | 0 | 255 | 0 | 8 events | Total number of SafetyStatus()[OTD] events |
| Lifetimes | Safety Events | Last OTD Event | U1 | 0 | 255 | 0 | 4 cycles | Last SafetyStatus()[OTD] event in CycleCount() cycles |
| Lifetimes | Safety Events | No of OTF Events | U1 | 0 | 255 | 0 | 8 events | Total number of SafetyStatus()[OTF] events |
| Lifetimes | Safety Events | Last OTF Event | U1 | 0 | 255 | 0 | 4 cycles | Last SafetyStatus()[OTF] event in CycleCount() cycles |

12.7.4 Charging Events

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-----------|---------------|---------------------------------|------|-----|-----|---------|----------|---|
| Lifetimes | Safety Events | No of Valid Charge Terminations | U1 | 0 | 255 | 0 | 8 events | Total number of valid charge termination events |
| Lifetimes | Safety Events | Last Valid Charge Termination | U1 | 0 | 255 | 0 | 4 cycles | Last valid charge termination in CycleCount() cycles |

12.7.5 Gauging Events

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-----------|----------------|--------------------|------|-----|-----|---------|----------|--|
| Lifetimes | Gauging Events | No of QMax Updates | U1 | 0 | 255 | 0 | 8 events | Total number of GaugingStatus()[QMax] toggles |
| Lifetimes | Gauging Events | Last QMax Update | U1 | 0 | 255 | 0 | 4 cycles | Last GaugingStatus()[QMax] toggle in CycleCount() cycles |
| Lifetimes | Gauging Events | No of RA Updates | U1 | 0 | 255 | 0 | 8 events | Total number of GaugingStatus()[RX] toggles |
| Lifetimes | Gauging Events | Last RA Update | U1 | 0 | 255 | 0 | 4 cycles | Last GaugingStatus()[RX] toggle in CycleCount() cycles |
| Lifetimes | Gauging Events | No of RA Disable | U1 | 0 | 255 | 0 | 8 events | Total number of GaugingStatus()[RU] = 1 events |
| Lifetimes | Gauging Events | Last RA Disable | U1 | 0 | 255 | 0 | 4 cycles | Last GaugingStatus()[RU] = 1 events in CycleCount() cycles |

12.7.6 Power Events

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-----------|--------------|-----------------|------|-----|-----|---------|--------|---------------------------------|
| Lifetimes | Power Events | No of Shutdowns | U1 | 0 | 255 | 0 | events | Total number of Shutdown events |

12.7.7 Cell Balancing

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-----------|----------------|----------------|------|-----|-----|---------|------|---|
| Lifetimes | Cell Balancing | CB Time Cell 0 | U1 | 0 | 255 | 0 | 2h | Total performed cell balancing bypass time cell 0 |
| Lifetimes | Cell Balancing | CB Time Cell 1 | U1 | 0 | 255 | 0 | 2h | Total performed cell balancing bypass time cell 1 |
| Lifetimes | Cell Balancing | CB Time Cell 2 | U1 | 0 | 255 | 0 | 2h | Total performed cell balancing bypass time cell 2 |
| Lifetimes | Cell Balancing | CB Time Cell 3 | U1 | 0 | 255 | 0 | 2h | Total performed cell balancing bypass time cell 3 |

12.7.8 Temperature

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-----------|-------------|---------------------|------|------|-----|---------|------|--|
| Lifetimes | Temperature | Max Temp Cell | I1 | -128 | 127 | -128 | °C | Maximum reported cell temperature |
| Lifetimes | Temperature | Min Temp Cell | I1 | -128 | 127 | 127 | °C | Minimum reported cell temperature |
| Lifetimes | Temperature | Max Delta Temp Cell | I1 | -128 | 127 | 0 | °C | Maximum reported temperature delta for TSx inputs configured as cell temperature |

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-----------|-------------|---------------------|------|------|-----|---------|------|--|
| Lifetimes | Temperature | Max Temp Int Sensor | I1 | –128 | 127 | –128 | °C | Maximum reported internal temperature sensor temperature |
| Lifetimes | Temperature | Min Temp Int Sensor | I1 | –128 | 127 | 127 | °C | Minimum reported internal temperature sensor temperature |
| Lifetimes | Temperature | Max Temp FET | I1 | –128 | 127 | –128 | °C | Maximum reported FET temperature |

12.7.9 Time

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-----------|----------|------------------------|------|-----|-------|---------|------|--|
| Lifetimes | Time | Total firmware Runtime | U2 | 0 | 65535 | 0 | 2 h | Total firmware runtime between resets |
| Lifetimes | Time | Time Spent in UT | U2 | 0 | 65535 | 0 | 2 h | Total firmware runtime spent below T1 |
| Lifetimes | Time | Time Spent in LT | U2 | 0 | 65535 | 0 | 2 h | Total firmware runtime spent between T1 and T2 |
| Lifetimes | Time | Time Spent in STL | U2 | 0 | 65535 | 0 | 2 h | Total firmware runtime spent between T2 and T5 |
| Lifetimes | Time | Time Spent in RT | U2 | 0 | 65535 | 0 | 2 h | Total firmware runtime spent between T5 and T6 |
| Lifetimes | Time | Time Spent in STH | U2 | 0 | 65535 | 0 | 2h | Total firmware runtime spent between T6 and T3 |
| Lifetimes | Time | Time Spent in HT | U2 | 0 | 65535 | 0 | 2 h | Total firmware runtime spent between T3 and T4 |
| Lifetimes | Time | Time Spent in OT | U2 | 0 | 65535 | 0 | 2 h | Total firmware runtime spent above T6 |

12.8 Settings

12.8.1 Fuse

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|----------|----------|---------------------------|------|--------|--------|---------|---|
| Settings | Fuse | Permanent Fail Fuse 0–15 | H2 | 0x0000 | 0xFFFF | 0 | Bit 0: CUV—Cell undervoltage fuse activation 0 = Disabled 1 = Enabled (default) Bit 1: COV—Cell overvoltage fuse activation 0 = Disabled 1 = Enabled (default) Bit 2: Reserved Bit 3: Reserved Bit 4: PF_OTCE—Overtemperature fuse activation 0 = Disabled 1 = Enabled (default) Bit 5: Reserved Bit 6: OTF—Overtemperature FET fuse activation 0 = Disabled 1 = Enabled (default) Bit 7: QIM—QMax Imbalance fuse activation 0 = Disabled 1 = Enabled (default) Bit 8: CB—Cell balancing fuse activation 0 = Disabled 1 = Enabled (default) Bit 9: IMP—Cell impedance fuse activation 0 = Disabled 1 = Enabled (default) Bit 10: CD—Capacity Deterioration fuse activation 0 = Disabled 1 = Enabled (default) Bit 11: VIMR—Voltage imbalance at Rest fuse activation 0 = Disabled 1 = Enabled (default) Bit 12: VIMA—Voltage imbalance at Rest fuse activation 0 = Disabled 1 = Enabled (default) Bit 13: Reserved Bit 14: Reserved Bit 15: Reserved |
| Settings | Fuse | Permanent Fail Fuse 16–32 | H2 | 0x0000 | 0xFFFF | 0 | Bit 0: CFETF—Charge FET 0 = Disabled 1 = Enabled (default) Bit 1: DFETF—Discharge FET 0 = Disabled 1 = Enabled (default) Bit 2: THERM—Thermistor 0 = Disabled 1 = Enabled (default) Bit 3: Reserved Bit 4: AFE_PAFF Register 0 = n/a 1 = Enabled (default) Bit 5: AFE_CAFE Communication 0 = Disabled 1 = Enabled (default) Bit 6: 2LVL—FUSE input indicating fuse trigger by external 2nd level protection 0 = Disabled 1 = Enabled (default) Bit 7: Reserved Bit 8: Reserved Bit 9: OCECO—Open VCx 0 = n/a 1 = Enabled (default) Bit 10: DFW—DF wear out 0 = n/a 1 = Enabled (default) Bit 11: Reserved Bit 12: Reserved Bit 13: Reserved Bit 14: Reserved Bit 15: Reserved |
| Settings | Fuse | Min Fuse Blow Voltage | I2 | 0 | 32767 | 8000 | Minimum voltage required to attempt fuse blow, pack based, FET failures bypass this requirement to blow the fuse |

12.8.2 Manufacturing

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|----------|---------------|----------------------|------|--------|--------|---------|--|
| Settings | Manufacturing | Manufacturing Status | H2 | 0x0000 | 0xFFFF | 0x8000 | Bit 0: PCHG_EN—PCHG Function, only available with FET = 0 0 = Disabled 1 = Enabled Bit 1: CHG_EN—CHG FET, only available with FET = 0 0 = Disabled 1 = Enabled Bit 2: DSG_ENDSG FET, only available with FET = 0 0 = Disabled 1 = Enabled Bit 3: GAUGE_EN—Gauging 0 = Disabled 1 = Enabled (default) Bit 4: FET_EN—FET action 0 = Disabled 1 = Enabled (default) Bit 5: LF_EN—Lifetime data collection 0 = Disabled 1 = Enabled (default) Bit 6: PF_EN—Permanent Fail 0 = Disabled 1 = Enabled (default) Bit 7: BBR_EN—Black box recorder 0 = Disabled 1 = Enabled (default) Bit 8: FUSE_EN—FUSE action 0 = Disabled 1 = Enabled (default) Bit 9: LED_EN—LED Display 0 = Disabled 1 = Enabled (default) Bit 10: Reserved Bit 11: Reserved Bit 12: Reserved Bit 13: Reserved Bit 14: Reserved Bit 15: CAL_EN—ADC or CC output on ManufacturerData() 0 = Disabled 1 = Enabled (default) |

12.8.3 Protection

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|----------|------------|------------------------------|------|--------|--------|---------|---|
| Settings | Protection | Enabled Protections 0–15 | H2 | 0x0000 | 0xFFFF | 0xFFFF | Bit 0: CUV—Cell Undervoltage 0 = Disabled 1 = Enabled (default) Bit 1: COV—Cell Overvoltage 0 = Disabled 1 = Enabled (default) Bit 2: OCC1—Overcurrent in Charge 1st Tier 0 = Disabled 1 = Enabled (default) Bit 3: OCC2—Overcurrent in Charge 2nd Tier 0 = Disabled 1 = Enabled (default) Bit 4: OCD1—Overcurrent in Discharge 1st Tier 0 = Disabled 1 = Enabled (default) Bit 5: OCD2—Overcurrent in Discharge 2nd Tier 0 = Disabled 1 = Enabled (default) Bit 6: AOLD—Overload in Discharge 0 = Disabled 1 = Enabled (default) Bit 7: AOLDL—Overload in Discharge latch 0 = Disabled 1 = Enabled (default) Bit 8: ASCC—Short circuit in charge 0 = Disabled 1 = Enabled (default) Bit 9: ASCCL—Short circuit in charge latch 0 = Disabled 1 = Enabled (default) Bit 10: ASCD—Short circuit in discharge 0 = Disabled 1 = Enabled (default) Bit 11: ASCDL—Short circuit in discharge latch 0 = Disabled 1 = Enabled (default) Bit 12: OTC—Overtemperature in charge 0 = Disabled 1 = Enabled (default) Bit 13: OTD—Overtemperature in discharge 0 = Disabled 1 = Enabled (default) Bit 14: CUVC—I ² R compensated CUV 0 = Disabled 1 = Enabled (default) Bit 15: Reserved |
| Settings | Fuse | Enabled Protections 16–32 | H2 | 0x0000 | 0xFFFF | 0xFFFF | Bit 0: OTF—FET overtemperature 0 = Disabled 1 = Enabled (default) Bit 1: HWDF—SBS Host watchdog timeout 0 = Disabled 1 = Enabled (default) Bit 2: PTO—Pre-charging timeout 0 = Disabled 1 = Enabled (default) Bit 3: PTOS—Pre-charging timeout suspend 0 = Disabled 1 = Enabled (default) Bit 4: CTO—Charging timeout 0 = Disabled 1 = Enabled (default) Bit 5: CTOS—Charging timeout suspend 0 = Disabled 1 = Enabled (default) Bit 6: OC—Overcharge 0 = Disabled 1 = Enabled (default) Bit 7: CHGC—ChargingCurrent() higher than requested 0 = Disabled 1 = Enabled (default) Bit 8: CHGV—ChargingVoltage() higher than requested 0 = Disabled 1 = Enabled (default) Bit 9: Reserved Bit 10: Reserved Bit 11: Reserved Bit 12: Reserved Bit 13: Reserved Bit 14: Reserved Bit 15: Reserved |

12.8.4 Permanent Failure

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|----------|-------------------|------------------|------|--------|--------|---------|---|
| Settings | Permanent Failure | Enabled PF 0–15 | H2 | 0x0000 | 0xFFFF | 0xFFFF | Bit 0: CUV—Cell undervoltage 0 = Disabled 1 = Enabled (default) Bit 1: COV—Cell overvoltage 0 = Disabled 1 = Enabled (default) Bit 2: CUDEP—Copper Deposition 0 = Disabled 1 = Enabled (default) Bit 3: Reserved Bit 4: PF_OTCE—Overtemperature 0 = Disabled 1 = Enabled (default) Bit 5: Reserved Bit 6: OTF—Overtemperature FET 0 = Disabled 1 = Enabled (default) Bit 7: QIM—QMax Imbalance 0 = Disabled 1 = Enabled (default) Bit 8: CB—Cell balancing 0 = Disabled 1 = Enabled (default) Bit 9: IMP—Cell impedance 0 = Disabled 1 = Enabled (default) Bit 10: CD—Capacity Degradation 0 = Disabled 1 = Enabled (default) Bit 11: VIMR—Voltage imbalance at Rest 0 = Disabled 1 = Enabled (default) Bit 12: VIMA—Voltage imbalance at Rest 0 = Disabled 1 = Enabled (default) Bit 13: Reserved Bit 14: Reserved Bit 15: Reserved |
| Settings | Permanent Failure | Enabled PF 16–32 | H2 | 0x0000 | 0xFFFF | 0xFFFF | Bit 0: CFETF—Charge FET 0 = Disabled 1 = Enabled (default) Bit 1: DFET—Discharge FET 0 = Disabled 1 = Enabled (default) Bit 2: TH—Thermistor 0 = Disabled 1 = Enabled (default) Bit 3: FUSE—Fuse 0 = Disabled 1 = Enabled (default) Bit 4: AFER—AFE Register 0 = n/a 1 = Enabled (default) Bit 5: AFEC—AFE Communication 0 = Disabled 1 = Enabled (default) Bit 6: 2LVL—FUSE input indicating fuse trigger by external 2nd level protection 0 = Disabled 1 = Enabled (default) Bit 7: Reserved Bit 8: Reserved Bit 9: OCECO—Open VCx 0 = n/a 1 = Enabled (default) Bit 10: DFW—DF wearout 0 = n/a 1 = Enabled (default) Bit 11: Reserved Bit 12: Reserved Bit 13: Reserved Bit 14: Reserved Bit 15: Reserved |

12.8.5 Configuration

12.8.5.1 Protection Configuration

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|----------|---------------|--------------------------|------|------|------|---------|--|
| Settings | Configuration | Protection Configuration | H1 | 0x00 | 0xFF | 0x01 | Bit 0: Reserved Bit 1: CUV_RECOV_CHG require charge current to recover CUV and CUV 0 = disable 1 = enable Bit 2: Reserved Bit 3: Reserved Bit 4: Reserved Bit 5: Reserved Bit 6: Reserved Bit 7: Reserved |

12.8.5.2 Temperature Configuration

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|----------|---------------|---------------------------|------|--------|--------|---------|---|
| Settings | Configuration | Temperature Configuration | H2 | 0x0000 | 0xFFFF | 0x0087 | Bit 0: Internal TS enable—Internal 0 = Disable internal TS (default) 1 = Enable internal TS Bit 1: TS1 enable—TS1 0 = Disable TS1 1 = Enable TS1 (default) Bit 2: TS2 enable—TS2 0 = Disable TS2 1 = Enable TS2 (default) Bit 3: TS3 enable—TS3 0 = Disable TS3 (default) 1 = Enable TS3 Bit 4: TS4 enable—TS4 0 = Disable TS4 (default) 1 = Enable TS4 Bit 5: Internal TS Mode—Cell temp or FET temp 0 = Cell temp (default) 1 = FET temp Bit 6: TS1 Mode—Cell temp or FET temp 0 = Cell temp (default) 1 = FET temp Bit 7: TS2 Mode—Cell temp or FET temp 0 = Cell temp 1 = FET temp (default) Bit 8: TS3 Mode—Cell temp or FET temp 0 = Cell temp (default) 1 = FET temp Bit 9: TS4 Mode—Cell temp or FET temp 0 = Cell temp (default) 1 = FET temp Bit 10: CTEMP—Cell Temperature protection source 0 = MAX (default) 1 = Average Bit 11: FTEMP—FET Temperature protection source 0 = Max (default) 1 = Average Bit 12: OTFET—Overtemperature FET action 0 = FET action (default) 1 = FET action disabled Bit 13: Reserved Bit 14: Reserved Bit 15: Reserved |

12.8.5.3 LED Configuration

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|----------|---------------|-------------------|------|--------|--------|---------|--|
| Settings | Configuration | LED Configuration | H2 | 0x0000 | 0xFFFF | 0x00D0 | Bit 0: LEDR—LED display activation at device reset 0 = LED display not activated (default) 1 = LED display activated Bit 1: LEDRCA—Flashing of LED display when [RCA] is set 0 = LED display does not flash (default) 1 = LED display does flash Bit 2: LEDCHG—LED display during charging 0 = LED display not active (default) 1 = LED display active Bit 3: LEDMODE—LED display capacity selector 0 = Display RSOC (default) 1 = Display ASOC/DC Bit 5,4: LEDPF1, LEDPF0—LED Display PF Error Code 0,0 = PF Error code not available 0,1 = PF Error code shown after SOC if DISP is held low for LED Hold Time (default) 1,0 = PF Error code not available 1,1 = PF Error code shown after SOC Bit 7,6: LEDC1, LEDC0—LED Sink Current 0,0 = no limit 0,1 = 3 mA 1,0 = 4 mA 1,1 = 5 mA (default) Bit 8: Reserved Bit 9: Reserved Bit 10: Reserved Bit 11: Reserved Bit 12: Reserved Bit 13: Reserved Bit 14: Reserved Bit 15: Reserved |

12.8.5.4 Charging Configuration

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|----------|---------------|------------------------|------|------|------|---------|---|
| Settings | Configuration | Charging Configuration | H | 0x00 | 0xFF | 0 | Bit 1, 0: PCHG1, PCHG0 Precharge method 0, 0 = internal Precharge FET (not a valid option for bq30z55-R1) 0, 1 = CHG FET (default) 1, 0 = GPOD pin 1, 1 = Precharge disabled Bit 2: CRATE—ChargeCurrent rate 0 = ChargeCurrent() %C calculation based on DesignCapacity() (default) 1 = ChargeCurrent() %C calculation based on FullChargeCapacity() Bit 3: CHGSU—FET action in charge suspend mode 0 = FET active (default) 1 = Charging and Precharging disabled, FETs off Bit 4: CHGIN—FET action in charge inhibit mode 0 = FET active (default) 1 = Charging and Precharging disabled, FETs off Bit 5: CHGFET—FET action on terminate charge alarm (TCA) 0 = FET active (default) 1 = Charging and Precharging disabled, FET off Bit 6: CCC—Constant Current Mode Loss Compensation 0 = Disabled (default) 1 = ChargingVoltage() and ChargingCurrent() values are compensated for voltage drop Bit 7: Reserved |

12.8.5.5 System Configuration

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|----------|---------------|----------------------|------|--------|--------|---------|--|
| Settings | Configuration | System Configuration | H2 | 0x0000 | 0xFFFF | 0x0032 | Bit 1,0: CC1, CC0 Cell Count 0,0 = Reserved 0,1 = 2 cell 1,0 = 3 cell 1,1 = 4 cell (default) Bit 2: NR Use PRES in system detection. 0 = Use PRES, removable mode (default). 1 = Non-removable mode Bit 3: SLEEPCHG—CHG FET enabled during sleep 0 = CHG FET off during sleep (default) 1 = CHG FET remains on during sleep Bit 4: SLEEP—Sleep mode 0 = Disable Sleep mode 1 = Enable Sleep mode (default) Bit 5: CB—Cell balancing 0 = Disabled cell balancing 1 = Enable cell balancing (default) Bit 6: CBM—Cell balancing method 0 = Internal cell balancing (default) 1 = External cell balancing Bit 7: CBR—Cell balancing at rest 0 = Disable cell balancing at rest (default) 1 = Enable cell balancing at rest Bit 8: SHIPDSG—DSG FET enabled during ship mode 0 = Disable DSG FET at ship mode(default) 1 = Enable DSG FET at ship mode Bit 9: Reserved Bit 10: Reserved Bit 11: Reserved Bit 12: Reserved Bit 13: Reserved Bit 14: Reserved Bit 15: Reserved |

12.8.5.6 Gauging Configuration

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|----------|---------------|-----------------------|------|------|------|---------|--|
| Settings | Configuration | Gauging Configuration | H2 | 0x00 | 0xFF | 0x1FDA | <p>Bit 0: CCT—Cycle count threshold 0 = use CC % of DesignCapacity() (default) 1 = use CC % of FullChargeCapacity()</p> <p>Bit 1: CSYNC Sync RemainingCapacity() with FullChargeCapacity() at valid charge termination 0 = RemainingCapacity() is not synchronized 1 = RemainingCapacity() is synchronized (default)</p> <p>Bit 2: RSOC—RelativeStateOfCharge() and RemainingCapacity() behavior at end of charge 0 = actual value shown (default) 1 = held at 99% until valid charge termination. On entering valid charge termination update to 100%</p> <p>Bit 3: RESCAP—Reserve capacity calculation method 0 = light load 1 = use Load Select (default)</p> <p>Bit 4: LOCK0—Keep RemainingCapacity() and RelativeStateOfCharge() jumping back during relaxation after 0 and FD are reached during discharge. 0 = Disabled (default) 1 = Enabled</p> <p>Bit 5: SMOOTH—Run RemainingCapacity() through a low-pass filter to smooth out jumps at grid point updates, charge termination, and self-discharge adjustments made in relax mode. Smoothing is bypassed at the end of discharge when EDV is reached. Run FullCapacity() through a low-pass filter to smooth out jumps at charge termination and adjustments made in relax mode. Sample settings and associated low-pass filter time constants are in Table C-1. This smoothing feature uses the following formula updated every 1 second. $xfilter_k = \alpha * xfilter_k + (1 - \alpha) * xadc_k$ where: $xfilter_k$: the new filtered value $xfilter_k$: the previously calculated filter value $xadc_k$: the actual sample value α: filter constant As such, some lag may be observed between charge/discharge current and RemainingCapacity() changes. The SMOOTH function introduces some delays in IT simulation. It could mask out the ReservedCapacity setting if the capacity setting value is too small. If ReservedCapacity is desired, the user should consider using lower filter time, or increase the ReservedCapacity setting as compensation. The additional amount to compensate can be calculated as follows: $\text{Additional ReservedCap(mAH)} = \text{AverageLoadCurrent(mA)} * \text{SmoothFilterSetting(sec)/3600}$ 0 = Disabled (default) 1 = Enabled</p> <p>Bit 6: OCVFR—OCV look up disabled in flat region during charge until charged above flat region. Enabled again after Min Relax Time after Charge 0 = Disabled 1 = Enabled (default)</p> <p>Bit 7: DOD0EW—DOD0 error weighting, calculates new DOD0 values from the newly read value and the previous value using their respective errors. DOD0 readings have an associated error based on elapsed time since reading, conditions at time of reading (reset, charge termination, etc), temperature, amount of relaxation at time of reading, etc. The feature provides more accurate DOD0 points. It was introduced in the bq20z45 device. 0 = Disabled 1 = Enabled (default)</p> |
| Settings | Configuration | Gauging Configuration | H2 | 0x00 | 0xFF | 0x1FDA | <p>Bit 8: LFP_RELAX, LiFePO4 chemistry has a unique slow relaxation near full charge. Detailed, in-house test data suggests that the relaxation after a full charge takes a few days to settle. The slow decaying voltage causes RSOC to continue to drop every 5 hours. Depending on the full charge taper current, the fully settled voltage could be close to or even below FlatVoltMax in some cases. For chemID 4xx (LiFePO4) series, the condition to exit the long relax mode is: the pack had previously charged to full or near full state, and then either a significant long relaxation or a non-trivial discharge has happened, such that when in relaxation, the $OCV < FlatVoltMax$. With the above, Qmax update is disabled because dod will not be taken as long as it is in LFP_relax mode. By the time the gas gauge exits the LFP_relax mode, the OCV is already in the flat zone. So Qmax update takes an alternative approach: Once full charge occurs (FC bit set), dod0=Dod_at_EOC is automatically assigned and valid for Qmax update; VOK is set if there is no Qmax update, or if Qmax is updated, VOK is cleared. The dod error as a result of this action is zero or negligible because in the LiFePO4 table, OCV voltage corresponding to dod=0 is much lower. If LFP_RELAX is set, the firmware automatically enables the feature upon detecting that the chemistry is 4xx series. If clear, the feature is disabled. Lithium Iron Phosphate Relax 0 = Disabled (default) 1 = Enabled</p> |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|----------|---------------|-----------------------|------|------|------|---------|---|
| Settings | Configuration | Gauging Configuration | H2 | 0x00 | 0xFF | 0x1FDA | <p>Bit 9: RSOC_CONV, addresses the convergence of RemCap to 0 at low temperatures and very high rates which may not be satisfactory because of the high granularity of resistance grids. If termination voltage is reached in DOD region with 10% grid interval or at the moment where voltage / SOC dependency is flat, error can be large. Fast resistance scaling will apply a scale factor to resistance in RemCap simulations leading up to 0. This scale factor is computed from actively measured resistance during the discharge. This measured resistance is an active number and may not be used for an Ra update.</p> <p>RSOC, fast resistance scaling</p> <p>0 = Disabled</p> <p>1 = Enabled (default)</p> <p>Bit 10: FAST_QMax_LRN, Fast Qmax learning: eliminates previously required relaxation periods, to use enable IT with perfectly relaxed cells ~50% RSOC (37% minimum), discharge to empty, Qmax will be learned when discharge stops.</p> <p>Fast QMax learning, during discharge when update status is 6. Update status will change to 11 if fast learning is successful.</p> <p>0 = Disabled</p> <p>1 = Enabled (default)</p> <p>Bit 11: Reserved</p> <p>Bit 12: RSOC_HOLD, prevents RSOC rise during discharge. RSOC will be held until calculated value falls below actual state.</p> <p>0 = Disabled (default)</p> <p>1 = Enabled</p> <p>Bit 13: CUV_TERM, CUV discharge termination: Remaining Capacity and Full Capacity calculations to accommodate reaching 0% RSOC before reaching CUV. This is helpful when the cells are out of balance.</p> <p>0 = Disabled</p> <p>1 = Enabled (default)</p> <p>Bit 14: Reserved</p> <p>Bit 15: Reserved</p> |

12.8.5.7 SBS Configuration

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|----------|---------------|-------------------------|------|--------|--------|---------|---|
| Settings | Configuration | SBS Configuration | H1 | 0x00 | 0xFF | 0x20 | Bit 0: BCAST—Enable alert and charging broadcast from device to host 0 = Disabled (default) 1 = Enabled Bit 1: CPE—PEC on charger broadcast 0 = Disabled (default) 1 = Enabled Bit 2: HPE—PEC on host communication 0 = Disabled (default) 1 = Enabled Bit 3: XL Enable 400 kHz com mode 0 = Normal SBS bus speed (default) 1 = 400 kHz bus speed Bit 5,4: BLT1, BLT0—Bus low timeout 0,0 = no SBS bus low timeout 0,1 = 1-s SBS bus low timeout 1,0 = 2-s SBS bus low timeout (default) 1,1 = 3-s SBS bus low timeout Bit 6: Reserved Bit 7: Reserved |
| Settings | Configuration | SBS Data Config 0–15 | H2 | 0x0000 | 0xFFFF | 0x0CAF | Bit 0: TDASETV—Enable TDA flag set by cell voltage threshold 0 = Disabled 1 = Enabled (default) Bit 1: TDACLEARV—Enable TDA flag clear by cell voltage threshold 0 = Disabled 1 = Enabled (default) Bit 2: TDASETRSOC—Enable TDA flag set by RSOC threshold 0 = Disabled 1 = Enabled (default) Bit 3: TDACLEARRSOC—Enable TDA flag clear by RSOC threshold 0 = Disabled 1 = Enabled (default) Bit 4: TCASETV—Enable TCA flag set by cell voltage threshold 0 = Disabled 1 = Enabled (default) Bit 5: TCACLEARV—Enable TCA flag clear by cell voltage threshold 0 = Disabled 1 = Enabled (default) Bit 6: TCASETRSOC—Enable TCA flag set by RSOC threshold 0 = Disabled 1 = Enabled (default) Bit 7: TCACLEARRSOC—Enable TCA flag clear by RSOC threshold 0 = Disabled 1 = Enabled (default) Bit 8: TCACLEARCT—Enable TCA flag clear valid charge termination 0 = Disabled 1 = Enabled (default) Bit 9: FCCLEARCT—Enable FC flag clear by valid charge termination 0 = Disabled 1 = Enabled (default) Bit 10: FCSETVCT enable FC flag set on valid charge termination 0 = Disabled 1 = Enabled (default) Bit 11: TCASETVCT enable TCA flag set on valid charge termination 0 = Disabled 1 = Enabled (default) Bit 12: Reserved Bit 13: Reserved Bit 14: Reserved Bit 15: Reserved |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-------|----------|--------------------------|------|------|------|---------|--|
| | | SBS Data Config 16–32 | H1 | 0x00 | 0xFF | 0xFF | Bit 0: FDSETV—Enable FD flag set by cell voltage threshold 0 = Disabled 1 = Enabled (default) Bit 1: FDCLEARV—Enable FD flag clear by cell voltage threshold 0 = Disabled 1 = Enabled (default) Bit 2: FDSETRSOC—Enable FD flag set by RSOC threshold 0 = Disabled 1 = Enabled (default) Bit 3: FDCLEARRSOC—Enable FD flag clear by RSOC threshold 0 = Disabled 1 = Enabled (default) Bit 4: FCSETV—Enable FC flag set by cell voltage threshold 0 = Disabled 1 = Enabled (default) Bit 5: FCCLEARV—Enable FC flag clear by cell voltage threshold 0 = Disabled 1 = Enabled (default) Bit 6: FCSETRSOC—Enable FC flag set by RSOC threshold 0 = Disabled 1 = Enabled (default) Bit 7: FCCLEARRSOC—Enable FC flag clear by RSOC threshold 0 = Disabled 1 = Enabled (default) |

12.8.5.8 SBS Data Configuration

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|----------|---------------|--------------------------|------|--------|--------|---------|---|
| Settings | Configuration | SBS Data Config 0–15 | H2 | 0x0000 | 0xFFFF | 0x0CAF | Bit 0: TDASET—Enable TDA flag set by cell voltage threshold 0 = Disabled 1 = Enabled (default) Bit 1: TDACLEARV—Enable TDA flag clear by cell voltage threshold 0 = Disabled 1 = Enabled (default) Bit 2: TDASETRSOC—Enable TDA flag set by RSOC threshold 0 = Disabled 1 = Enabled (default) Bit 3: TDACLEARRSOC—Enable TDA flag clear by RSOC threshold 0 = Disabled 1 = Enabled (default) Bit 4: TCASET—Enable TCA flag set by cell voltage threshold 0 = Disabled 1 = Enabled (default) Bit 5: TCACLEARV—Enable TCA flag clear by cell voltage threshold 0 = Disabled 1 = Enabled (default) Bit 6: TCASETRSOC—Enable TCA flag set by RSOC threshold 0 = Disabled 1 = Enabled (default) Bit 7: TCACLEARRSOC—Enable TCA flag clear by RSOC threshold 0 = Disabled 1 = Enabled (default) Bit 8: TCACLEARCT—Enable TCA flag clear valid charge termination 0 = Disabled 1 = Enabled (default) Bit 9: FCCLEARCT—Enable FC flag clear by valid charge termination 0 = Disabled 1 = Enabled (default) Bit 10: FCSETVCT—Enable FC flag set on valid charge termination 0 = Disabled 1 = Enabled (default) Bit 11: TCASETVCT—Enable TCA flag set on valid charge termination 0 = Disabled 1 = Enabled (default) Bit 12: Reserved Bit 13: Reserved Bit 14: Reserved Bit 15: Reserved |
| | | SBS Data Config 16–32 | H1 | 0x00 | 0xFF | 0xFF | Bit 0: FDSETV—Enable FD flag set by cell voltage threshold 0 = Disabled 1 = Enabled (default) Bit 1: FDCLEARV—Enable FD flag clear by cell voltage threshold 0 = Disabled 1 = Enabled (default) Bit 2: FDSETRSOC—Enable FD flag set by RSOC threshold 0 = Disabled 1 = Enabled (default) Bit 3: FDCLEARRSOC—Enable FD flag clear by RSOC threshold 0 = Disabled 1 = Enabled (default) Bit 4: FCSETV—Enable FC flag set by cell voltage threshold 0 = Disabled 1 = Enabled (default) Bit 5: FCCLEARV—Enable FC flag clear by cell voltage threshold 0 = Disabled 1 = Enabled (default) Bit 6: FCSETRSOC—Enable FC flag set by RSOC threshold 0 = Disabled 1 = Enabled (default) Bit 7: FCCLEARRSOC—Enable FC flag clear by RSOC threshold 0 = Disabled 1 = Enabled (default) |

12.8.6 AFE

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|---------------|----------|-------------------|------|------|------|---------|--|
| Configuration | AFE | AFE State Control | H1 | 0x00 | 0xFF | 0 | AFE state after device start up Bit 0: Reserved Bit 1: Reserved Bit 2: Reserved Bit 3: Reserved Bit 4: RSNS Divide OLD, SCC, SDC1 and SCD2 voltage thresholds by 2 0 = Disabled (default) 1 = Enabled Bit 5: SCDDx2 Double SCD1 and SCD2 delay thresholds 0 = Disabled (default) 1 = Enabled Bit 6: Reserved Bit 7: Reserved |

12.9 Power

12.9.1 Power

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------|----------|----------------------|------|-----|-------|---------|------|--|
| Power | Power | Valid Update Voltage | I2 | 0 | 32767 | 7500 | mV | Min stack voltage threshold for Flash update, pack based |

12.9.2 Shutdown

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------|----------|---------------------------|------|-----|-------|---------|------|---|
| Power | Shutdown | Shutdown Voltage | I2 | 0 | 32767 | 1750 | mV | Cell based shutdown voltage trip threshold |
| Power | Shutdown | Shutdown Time | U2 | 0 | 255 | 10 | s | Cell based shutdown voltage trip delay |
| Power | Shutdown | Charger Present Threshold | I2 | 0 | 32767 | 3000 | mV | Pack pin charger present detect threshold, pack based |

12.9.3 Sleep

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------|----------|---------------|------|-----|-------|---------|------|--|
| Power | Sleep | Sleep Current | I2 | 0 | 32767 | 10 | mA | Current() threshold to enter Sleep mode |
| Power | Sleep | Voltage Time | U1 | 0 | 255 | 5 | s | Voltage sampling period in Sleep mode |
| Power | Sleep | Current Time | U1 | 0 | 255 | 20 | s | Current sampling period in Sleep mode |

12.9.4 Ship

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------|----------|---------|------|------|-----|---------|------|---|
| Power | Ship | Delay | I2 | 0 | 255 | 5 | s | Ship mode entry delay |
| Power | Ship | Current | I2 | –250 | 250 | 10 | mA | Current() threshold to enter ship mode |

12.10 Gas Gauging

12.10.1 Current Thresholds

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|--------------------|-----------------------|------|--------|-------|---------|------|---|
| Gas Gauging | Current Thresholds | Dsg Current Threshold | I2 | –32768 | 32767 | 100 | mA | Discharge mode Current() threshold |
| Gas Gauging | Current Thresholds | Chg Current Threshold | I2 | –32768 | 32767 | 50 | mA | Charge mode Current() threshold |
| Gas Gauging | Current Thresholds | Quit Current | I2 | 0 | 32767 | 10 | mA | Current() threshold to enter rest mode |

12.10.2 State

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|---------------------------|------|------|-------|---------|------|--|
| Gas Gauging | State | QMax Cell 0 | I2 | 0 | 32767 | 4400 | mAh | QMax Cell 0 |
| Gas Gauging | State | QMax Cell 1 | I2 | 0 | 32767 | 4400 | mAh | QMax Cell 1 |
| Gas Gauging | State | QMax Cell 2 | I2 | 0 | 32767 | 4400 | mAh | QMax Cell 2 |
| Gas Gauging | State | QMax Cell 3 | I2 | 0 | 32767 | 4400 | mAh | QMax Cell 3 |
| Gas Gauging | State | QMax Pack | I2 | 0 | 32767 | 4400 | mAh | QMax of the whole stack |
| Gas Gauging | State | Update Status | H1 | 0x00 | 0xFF | 0 | | Bit 1:0: Update1, Update0 Update Status 0,0 = Impedance Track gauging and lifetime updating is disabled 0,1 = Ra table updated 1,0 = QMax and Ra table have been updated Bit 2: Enable—Impedance Track gauging and lifetime updating enable 0 = Disabled 1 = Enabled Bit 3: is_QMax_Field_Updated QMax updated with FC and qualified OCV in charge and discharge 0 = Disabled 1 = Enabled (default) Bit 4: Reserved Bit 5: Reserved Bit 6: Reserved Bit 7: Reserved |
| Gas Gauging | State | Cell 0 Chg Voltage at EoC | I2 | 0 | 32767 | 4200 | mV | Cell 0 voltage value at end of charge |
| Gas Gauging | State | Cell 1 Chg Voltage at EoC | I2 | 0 | 32767 | 4200 | mV | Cell 1 voltage value at end of charge |

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|---------------------------|------|--------|-------|---------|-------|---|
| Gas Gauging | State | Cell 2 Chg Voltage at EoC | I2 | 0 | 32767 | 4200 | mV | Cell 2 voltage value at end of charge |
| Gas Gauging | State | Cell 3 Chg Voltage at EoC | I2 | 0 | 32767 | 4200 | mV | Cell 3 voltage value at end of charge |
| Gas Gauging | State | Current at EoC | I2 | −32768 | 32767 | 250 | mA | Current at end of charge |
| Gas Gauging | State | Avg I Last Run | I2 | −32768 | 32767 | −2000 | mA | Average current last discharge cycle |
| Gas Gauging | State | Avg P Last Run | I2 | −32768 | 32767 | −3022 | 10 mW | Average power last discharge cycle |
| Gas Gauging | State | Delta Voltage | I2 | −32768 | 32767 | 0 | mV | Voltage() delta between normal and short load spikes to optimize run time calculation |
| Gas Gauging | State | Max I Last Run | I2 | −32768 | 32767 | −2000 | mA | Max current last discharge cycle |
| Gas Gauging | State | Max P Last Run | I2 | −32768 | 32767 | −3022 | 10 mW | Max power last discharge cycle |

12.11 IT Config

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|--------------|------|-----|-----|---------|------------------------|--|
| Gas Gauging | IT Cfg | Load Select | U1 | 0 | 255 | 7 | | Defines Load compensation mode used by gauging algorithm:IF Load Mode = 0:0 = Avg I Last Run 1 = Present average discharge current 2 = Current 3 = AverageCurrent 4 = DesignCapacity/5 5 = AtRate (mA) 6 = User-Rate-mA 7 = Max Avg I Last RunIF Load Mode = 1:0 = Avg P Last Run 1 = Present average discharge power 2 = Current x Voltage 3 = AverageCurrent x Average Voltage 4 = DesignEnergy/5 5 = AtRate (10 mW) 6 = User-Rate-mW 7 = Max Avg P Last Run |
| Gas Gauging | IT Cfg | Load Mode | U1 | 0 | 255 | 0 | | Defines unit used by gauging algorithm:0 = Constant Current1 = Constant Power |
| Gas Gauging | IT Cfg | Ra Filter | U2 | 0 | 999 | 500 | 0.1% | Filter value used in Ra Updates, specifies what percentage or Ra update is from new value (100%—setting) vs. old value (setting). The recommended setting is 80% if RSOC_CONV feature is enabled. Otherwise, the setting should be 50% as default. |
| Gas Gauging | IT Cfg | Ra Max Delta | U1 | 0 | 255 | 15 | % of Design Resistance | Maximum value of allowed Ra change |

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|-----------------------------|------|--------|-------|---------|-------|--|
| Gas Gauging | IT Cfg | Design Resistance | | | | | | Averaged cell resistance at Reference Grid point. Automatically updated when Update Status is set to 0x6 by the gauge. To automatically update again set Update Status to 0x4 or manually set when Update Status is set to 0x6. |
| Gas Gauging | IT Cfg | Reference Grid | UI | 0 | 15 | 4 | | Reference grid point used by Design Resistance. The default setting should be used if RSOC_CONV feature is enabled. Otherwise, grid point 11 should be used to ensure resistance updates fast enough at the grid where discharge termination occurs. |
| Gas Gauging | IT Cfg | Resistance Parameter Filter | U2 | 1 | 65534 | 65142 | — | This is one of the filters used for resistance update. Reducing this filter setting can improve low temperature performance at high rates. The default setting is 41-s time constant. It is recommended to keep this filter within the range of 4 s (i.e. DF setting = 61680) up to the default 41 s (i.e. DF setting = 65142). Examining the Term Voltage Delta setting and Fast Scale Start SOC should be done prior to twisting this parameter when trying to improve the RSOC performance. The following is the formula to convert the DF setting into actual filter time constant: Filter time constant = $[0.25/(1 - (DF_Value / 65536))] - 0.25$ |
| Gas Gauging | IT Cfg | Term Voltage | I2 | 0 | 32767 | 9000 | mV | Min stack voltage to be used for capacity calculation |
| Gas Gauging | IT Cfg | Term Voltage Delta | I2 | 0 | 32767 | 300 | mV | Controls when the RSOC_CONV feature becomes active. The recommended setting is 3.3 –Term Voltage / Number Cells. The default setting is 300 mV, which is assuming a typical 3V termination voltage per cell. If a different termination voltage is used, this parameter should be adjusted accordingly. |
| Gas Gauging | IT Cfg | User-Rate-mA | I2 | –32768 | 32768 | 0 | mA | Discharge rate used for capacity calculation selected by Load Select |
| Gas Gauging | IT Cfg | User-Rate-mW | I2 | –32768 | 32768 | 0 | 10 mW | Discharge rate used for capacity calculation selected by Load Select |
| Gas Gauging | IT Cfg | Reserve Cap-mAh | I2 | 0 | 32768 | 0 | mAh | Capacity reserved available when gauging algorithm reports 0% RemainingStateOfCharge() |
| Gas Gauging | IT Cfg | Reserve Cap-mWh | I2 | 0 | 32768 | 0 | 10 mW | Capacity reserved available when gauging algorithm reports 0% RemainingStateOfCharge() |

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|----------|-------------------------|------|-----|-------|---------|------|---|
| Gas Gauging | IT Cfg | Max IR Correct | I2 | 0 | 32767 | 400 | mV | Maximum allowable I*R voltage delta for correction |
| Gas Gauging | IT Cfg | RemCap Smoothing Filter | U1 | 0 | 255 | 250 | | RemainingCapacity() smoothing filter value. Sample settings and associated low-pass filter time constants are in Table C-1 |
| Gas Gauging | IT Cfg | Fast Scale Start SOC | U1 | 0 | 100 | 10 | % | Control the start of RSOC_CONV feature based on RSOC %. Rising this setting can improve RSOC drop at the end of discharge. However, the RSOC % chosen for this setting must keep after the sharp drop of the discharge curve (the keen of the discharge curve). |

12.12 LED Config

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|------------|------------------|------|-----|-------|---------|-------------|---|
| LED Support | LED Config | LED Flash Period | U2 | 0 | 65535 | 2048 | 122 μ s | LED Flashing period for alarm display |
| LED Support | LED Config | LED Blink Period | U2 | 0 | 65535 | 4096 | 122 μ s | LED Blinking period for state-of-charge display |
| LED Support | LED Config | LED Delay | U2 | 0 | 65535 | 400 | 122 μ s | Delay time from LED to LED for state-of-charge display |
| LED Support | LED Config | LED Hold Time | U2 | 0 | 255 | 16 | 0.25 s | LED display active time |
| LED Support | LED Config | CHG Flash Alarm | I1 | 0 | 100 | 10 | % | RelativeStateOfCharge() alarm threshold during charging |
| LED Support | LED Config | CHG Thresh 1 | I1 | 0 | 100 | 0 | % | RelativeStateOfCharge() threshold for LED1 during charging |
| LED Support | LED Config | CHG Thresh 2 | I1 | 0 | 100 | 20 | % | RelativeStateOfCharge() threshold for LED2 during charging |
| LED Support | LED Config | CHG Thresh 3 | I1 | 0 | 100 | 40 | % | RelativeStateOfCharge() threshold for LED3 during charging |
| LED Support | LED Config | CHG Thresh 4 | I1 | 0 | 100 | 60 | % | RelativeStateOfCharge() threshold for LED4 during charging |
| LED Support | LED Config | CHG Thresh 5 | I1 | 0 | 100 | 80 | % | RelativeStateOfCharge() threshold for LED5 during charging |
| LED Support | LED Config | DSG Flash Alarm | I1 | 0 | 100 | 10 | % | RelativeStateOfCharge() alarm threshold during discharging |
| LED Support | LED Config | DSG Thresh 1 | I1 | 0 | 100 | 0 | % | RelativeStateOfCharge() threshold for LED1 during discharging |
| LED Support | LED Config | DSG Thresh 2 | I1 | 0 | 100 | 20 | % | RelativeStateOfCharge() threshold for LED2 during discharging |
| LED Support | LED Config | DSG Thresh 3 | I1 | 0 | 100 | 40 | % | RelativeStateOfCharge() threshold for LED3 during discharging |
| LED Support | LED Config | DSG Thresh 4 | I1 | 0 | 100 | 60 | % | RelativeStateOfCharge() threshold for LED4 during discharging |

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|------------|-----------------|------|-----|-----|---------|------|---|
| LED Support | LED Config | DSG Thresh 5 | I1 | 0 | 100 | 80 | % | RelativeStateOfCharge() threshold for LED5 during discharging |

12.13 RA Table

12.13.1 R_a0

| Class | Subclass | Name | Type | Min | Max | Unit | Description |
|----------|----------|-----------------|------|--------|--------|----------------------|---|
| RA Table | R_a0 | Cell 0 R_A Flag | H2 | 0x0000 | 0xFFFF | | High Byte: 0x00: Cell Impedance and QMax updated 0x05: Relaxation mode and QMax update in progress 0x55: Discharge mode and cell updated 0xFF: cell impedance never updated Low-Byte: 0x00: Table not used and QMax updated 0x55: Table being used 0xFF: Table never used, no QMax or cell impedance update . |
| RA Table | R_a0 | Cell 0 R_A 0 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 0 resistance at grid point 0 |
| RA Table | R_a0 | Cell 0 R_A 1 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 0 resistance at grid point 1 |
| RA Table | R_a0 | Cell 0 R_A 2 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 0 resistance at grid point 2 |
| RA Table | R_a0 | Cell 0 R_A 3 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 0 resistance at grid point 3 |
| RA Table | R_a0 | Cell 0 R_A 4 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 0 resistance at grid point 4 |
| RA Table | R_a0 | Cell 0 R_A 5 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 0 resistance at grid point 5 |
| RA Table | R_a0 | Cell 0 R_A 6 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 0 resistance at grid point 6 |
| RA Table | R_a0 | Cell 0 R_A 7 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 0 resistance at grid point 7 |
| RA Table | R_a0 | Cell 0 R_A 8 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 0 resistance at grid point 8 |
| RA Table | R_a0 | Cell 0 R_A 9 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 0 resistance at grid point 9 |
| RA Table | R_a0 | Cell 0 R_A 10 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 0 resistance at grid point 10 |
| RA Table | R_a0 | Cell 0 R_A 11 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 0 resistance at grid point 11 |
| RA Table | R_a0 | Cell 0 R_A 12 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 0 resistance at grid point 12 |
| RA Table | R_a0 | Cell 0 R_A 13 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 0 resistance at grid point 13 |
| RA Table | R_a0 | Cell 0 R_A 14 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 0 resistance at grid point 14 |

12.13.2 R_a1

| Class | Subclass | Name | Type | Min | Max | Unit | Description |
|----------|----------|--------------------|------|--------|--------|----------------------|---|
| RA Table | R_a1 | Cell 1 R_A Flag | H2 | 0x0000 | 0xFFFF | | High-Byte: 0x00: Cell Impedance and QMax updated 0x05: Relaxation mode and QMax update in progress 0x55: Discharge mode and cell updated 0xFF: cell impedance never updated Low-Byte: 0x00: Table not used and QMax updated 0x55: Table being used 0xFF: Table never used, no QMax or cell impedance update |
| RA Table | R_a1 | Cell 1 R_A 0 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 1 resistance at grid point 0 |

| Class | Subclass | Name | Type | Min | Max | Unit | Description |
|----------|----------|---------------|------|--------|-------|----------------------|------------------------------------|
| RA Table | R_a1 | Cell 1 R_A 1 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 1 |
| RA Table | R_a1 | Cell 1 R_A 2 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 2 |
| RA Table | R_a1 | Cell 1 R_A 3 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 3 |
| RA Table | R_a1 | Cell 1 R_A 4 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 4 |
| RA Table | R_a1 | Cell 1 R_A 5 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 5 |
| RA Table | R_a1 | Cell 1 R_A 6 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 6 |
| RA Table | R_a1 | Cell 1 R_A 7 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 7 |
| RA Table | R_a1 | Cell 1 R_A 8 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 8 |
| RA Table | R_a1 | Cell 1 R_A 9 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 9 |
| RA Table | R_a1 | Cell 1 R_A 10 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 10 |
| RA Table | R_a1 | Cell 1 R_A 11 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 11 |
| RA Table | R_a1 | Cell 1 R_A 12 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 12 |
| RA Table | R_a1 | Cell 1 R_A 13 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 13 |
| RA Table | R_a1 | Cell 1 R_A 14 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 14 |

12.13.3 R_a2

| Class | Subclass | Name | Type | Min | Max | Unit | Description |
|----------|----------|-----------------|------|--------|--------|----------------------|---|
| RA Table | R_a2 | Cell 2 R_A Flag | H2 | 0x0000 | 0xFFFF | | High-Byte: 0x00: Cell Impedance and QMax updated 0x05: Relaxation mode and QMax update in progress 0x55: Discharge mode and cell updated 0xFF: cell impedance never updated Low-Byte: 0x00: Table not used and QMax updated 0x55: Table being used 0xFF: Table never used, no QMax or cell impedance update |
| RA Table | R_a2 | Cell 2 R_A 0 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 2 resistance at grid point 0 |
| RA Table | R_a2 | Cell 2 R_A 1 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 2 resistance at grid point 1 |
| RA Table | R_a2 | Cell 2 R_A 2 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 2 resistance at grid point 2 |
| RA Table | R_a2 | Cell 2 R_A 3 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 2 resistance at grid point 3 |
| RA Table | R_a2 | Cell 2 R_A 4 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 2 resistance at grid point 4 |
| RA Table | R_a2 | Cell 2 R_A 5 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 2 resistance at grid point 5 |
| RA Table | R_a2 | Cell 2 R_A 6 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 2 resistance at grid point 6 |
| RA Table | R_a2 | Cell 2 R_A 7 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 2 resistance at grid point 7 |
| RA Table | R_a2 | Cell 2 R_A 8 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 2 resistance at grid point 8 |
| RA Table | R_a2 | Cell 2 R_A 9 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 2 resistance at grid point 9 |
| RA Table | R_a2 | Cell 2 R_A 10 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 2 resistance at grid point 10 |
| RA Table | R_a2 | Cell 2 R_A 11 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 2 resistance at grid point 11 |
| RA Table | R_a2 | Cell 2 R_A 12 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 2 resistance at grid point 12 |

| Class | Subclass | Name | Type | Min | Max | Unit | Description |
|----------|----------|---------------|------|--------|-------|----------------------|------------------------------------|
| RA Table | R_a2 | Cell 2 R_A 13 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 2 resistance at grid point 13 |
| RA Table | R_a2 | Cell 2 R_A 14 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 2 resistance at grid point 14 |

12.13.4 R_a3

| Class | Subclass | Name | Type | Min | Max | Unit | Description |
|----------|----------|-----------------|------|--------|--------|----------------------|---|
| RA Table | R_a3 | Cell 3 R_A Flag | H2 | 0x0000 | 0xFFFF | | High-Byte: 0x00: Cell Impedance and QMax updated 0x05: Relaxation mode and QMax update in progress 0x55: Discharge mode and cell updated 0xFF: cell impedance never updated Low-Byte: 0x00: Table not used and QMax updated 0x55: Table being used 0xFF: Table never used, no QMax or cell impedance update |
| RA Table | R_a3 | Cell 3 R_A 0 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 3 resistance at grid point 0 |
| RA Table | R_a3 | Cell 3 R_A 1 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 3 resistance at grid point 1 |
| RA Table | R_a3 | Cell 3 R_A 2 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 3 resistance at grid point 2 |
| RA Table | R_a3 | Cell 3 R_A 3 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 3 resistance at grid point 3 |
| RA Table | R_a3 | Cell 3 R_A 4 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 3 resistance at grid point 4 |
| RA Table | R_a3 | Cell 3 R_A 5 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 3 resistance at grid point 5 |
| RA Table | R_a3 | Cell 3 R_A 6 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 3 resistance at grid point 6 |
| RA Table | R_a3 | Cell 3 R_A 7 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 3 resistance at grid point 7 |
| RA Table | R_a3 | Cell 3 R_A 8 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 3 resistance at grid point 8 |
| RA Table | R_a3 | Cell 3 R_A 9 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 3 resistance at grid point 9 |
| RA Table | R_a3 | Cell 3 R_A 10 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 3 resistance at grid point 10 |
| RA Table | R_a3 | Cell 3 R_A 11 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 3 resistance at grid point 11 |
| RA Table | R_a3 | Cell 3 R_A 12 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 3 resistance at grid point 12 |
| RA Table | R_a3 | Cell 3 R_A 13 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 3 resistance at grid point 13 |
| RA Table | R_a3 | Cell 3 R_A 14 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 3 resistance at grid point 14 |

12.13.5 R_a0x

| Class | Subclass | Name | Type | Min | Max | Unit | Description |
|----------|----------|------------------|------|--------|--------|--------------------|---|
| RA Table | R_a0x | xCell 0 R_A Flag | H2 | 0x0000 | 0xFFFF | | High-Byte: 0x00: Cell Impedance and QMax updated 0x05: Relaxation mode and QMax update in progress 0x55: Discharge mode and cell updated 0xFF: cell impedance never updated Low-Byte: 0x00: Table not used and QMax updated 0x55: Table being used 0xFF: Table never used, no QMax or cell impedance update |
| RA Table | R_a0x | xCell 0 R_A 0 | I2 | −32768 | 32768 | 2 ^{−10} Ω | Cell 0 resistance at grid point 0 |
| RA Table | R_a0x | xCell 0 R_A 1 | I2 | −32768 | 32768 | 2 ^{−10} Ω | Cell 0 resistance at grid point 1 |
| RA Table | R_a0x | xCell 0 R_A 2 | I2 | −32768 | 32768 | 2 ^{−10} Ω | Cell 0 resistance at grid point 2 |
| RA Table | R_a0x | xCell 0 R_A 3 | I2 | −32768 | 32768 | 2 ^{−10} Ω | Cell 0 resistance at grid point 3 |
| RA Table | R_a0x | xCell 0 R_A 4 | I2 | −32768 | 32768 | 2 ^{−10} Ω | Cell 0 resistance at grid point 4 |
| RA Table | R_a0x | xCell 0 R_A 5 | I2 | −32768 | 32768 | 2 ^{−10} Ω | Cell 0 resistance at grid point 5 |
| RA Table | R_a0x | xCell 0 R_A 6 | I2 | −32768 | 32768 | 2 ^{−10} Ω | Cell 0 resistance at grid point 6 |
| RA Table | R_a0x | xCell 0 R_A 7 | I2 | −32768 | 32768 | 2 ^{−10} Ω | Cell 0 resistance at grid point 7 |
| RA Table | R_a0x | xCell 0 R_A 8 | I2 | −32768 | 32768 | 2 ^{−10} Ω | Cell 0 resistance at grid point 8 |
| RA Table | R_a0x | xCell 0 R_A 9 | I2 | −32768 | 32768 | 2 ^{−10} Ω | Cell 0 resistance at grid point 9 |
| RA Table | R_a0x | xCell 0 R_A 10 | I2 | −32768 | 32768 | 2 ^{−10} Ω | Cell 0 resistance at grid point 10 |
| RA Table | R_a0x | xCell 0 R_A 11 | I2 | −32768 | 32768 | 2 ^{−10} Ω | Cell 0 resistance at grid point 11 |
| RA Table | R_a0x | xCell 0 R_A 12 | I2 | −32768 | 32768 | 2 ^{−10} Ω | Cell 0 resistance at grid point 12 |
| RA Table | R_a0x | xCell 0 R_A 13 | I2 | −32768 | 32768 | 2 ^{−10} Ω | Cell 0 resistance at grid point 13 |
| RA Table | R_a0x | xCell 0 R_A 14 | I2 | −32768 | 32768 | 2 ^{−10} Ω | Cell 0 resistance at grid point 14 |

12.13.6 R_a1x

| Class | Subclass | Name | Type | Min | Max | Unit | Description |
|----------|----------|------------------|------|--------|--------|----------------------|---|
| RA Table | R_a1x | xCell 1 R_A Flag | H2 | 0x0000 | 0xFFFF | | High-Byte: 0x00: Cell Impedance and QMax updated 0x05: Relaxation mode and QMax update in progress 0x55: Discharge mode and Cell updated 0xFF: cell impedance never updated Low-Byte: 0x00: Table not used and QMax updated 0x55: Table being used 0xFF: Table never used, no QMax or cell impedance update |
| RA Table | R_a1x | xCell 1 R_A 0 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 0 |
| RA Table | R_a1x | xCell 1 R_A 1 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 1 |
| RA Table | R_a1x | xCell 1 R_A 2 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 2 |
| RA Table | R_a1x | xCell 1 R_A 3 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 3 |
| RA Table | R_a1x | xCell 1 R_A 4 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 4 |
| RA Table | R_a1x | xCell 1 R_A 5 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 5 |
| RA Table | R_a1x | xCell 1 R_A 6 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 6 |
| RA Table | R_a1x | xCell 1 R_A 7 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 7 |
| RA Table | R_a1x | xCell 1 R_A 8 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 8 |
| RA Table | R_a1x | xCell 1 R_A 9 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 9 |
| RA Table | R_a1x | xCell 1 R_A 10 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 10 |
| RA Table | R_a1x | xCell 1 R_A 11 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 11 |
| RA Table | R_a1x | xCell 1 R_A 12 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 12 |
| RA Table | R_a1x | xCell 1 R_A 13 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 13 |
| RA Table | R_a1x | xCell 1 R_A 14 | I2 | –32768 | 32768 | 2 [^] –10 Ω | Cell 1 resistance at grid point 14 |

12.13.7 R_a2x

| Class | Subclass | Name | Type | Min | Max | Unit | Description |
|----------|----------|------------------|------|--------|--------|----------------------|---|
| RA Table | R_a2x | xCell 2 R_A Flag | H2 | 0x0000 | 0xFFFF | | High-Byte: 0x00: Cell Impedance and QMax updated 0x05: Relaxation mode and QMax update in progress 0x55: Discharge mode and cell updated 0xFF: cell impedance never updated Low-Byte: 0x00: Table not used and QMax updated 0x55: Table being used 0xFF: Table never used, no QMax or cell impedance update |
| RA Table | R_a2x | xCell 2 R_A 0 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 2 resistance at grid point 0 |
| RA Table | R_a2x | xCell 2 R_A 1 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 2 resistance at grid point 1 |
| RA Table | R_a2x | xCell 2 R_A 2 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 2 resistance at grid point 2 |
| RA Table | R_a2x | xCell 2 R_A 3 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 2 resistance at grid point 3 |
| RA Table | R_a2x | xCell 2 R_A 4 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 2 resistance at grid point 4 |
| RA Table | R_a2x | xCell 2 R_A 5 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 2 resistance at grid point 5 |
| RA Table | R_a2x | xCell 2 R_A 6 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 2 resistance at grid point 6 |
| RA Table | R_a2x | xCell 2 R_A 7 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 2 resistance at grid point 7 |
| RA Table | R_a2x | xCell 2 R_A 8 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 2 resistance at grid point 8 |
| RA Table | R_a2x | xCell 2 R_A 9 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 2 resistance at grid point 9 |
| RA Table | R_a2x | xCell 2 R_A 10 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 2 resistance at grid point 10 |
| RA Table | R_a2x | xCell 2 R_A 11 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 2 resistance at grid point 11 |
| RA Table | R_a2x | xCell 2 R_A 12 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 2 resistance at grid point 12 |
| RA Table | R_a2x | xCell 2 R_A 13 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 2 resistance at grid point 13 |
| RA Table | R_a2x | xCell 2 R_A 14 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 2 resistance at grid point 14 |

12.13.8 R_a3x

| Class | Subclass | Name | Type | Min | Max | Unit | Description |
|----------|----------|------------------|------|--------|--------|----------------------|---|
| RA Table | R_a3x | xCell 3 R_A Flag | H2 | 0x0000 | 0xFFFF | | High-Byte: 0x00: Cell Impedance and QMax updated 0x05: Relaxation mode and QMax update in progress 0x55: Discharge mode and cell updated 0xFF: cell impedance never updated Low-Byte: 0x00: Table not used and QMax updated 0x55: Table being used 0xFF: Table never used, no QMax or cell impedance update |
| RA Table | R_a3x | xCell 3 R_A 0 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 3 resistance at grid point 0 |
| RA Table | R_a3x | xCell 3 R_A 1 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 3 resistance at grid point 1 |
| RA Table | R_a3x | xCell 3 R_A 2 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 3 resistance at grid point 2 |
| RA Table | R_a3x | xCell 3 R_A 3 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 3 resistance at grid point 3 |
| RA Table | R_a3x | xCell 3 R_A 4 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 3 resistance at grid point 4 |
| RA Table | R_a3x | xCell 3 R_A 5 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 3 resistance at grid point 5 |
| RA Table | R_a3x | xCell 3 R_A 6 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 3 resistance at grid point 6 |
| RA Table | R_a3x | xCell 3 R_A 7 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 3 resistance at grid point 7 |
| RA Table | R_a3x | xCell 3 R_A 8 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 3 resistance at grid point 8 |
| RA Table | R_a3x | xCell 3 R_A 9 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 3 resistance at grid point 9 |
| RA Table | R_a3x | xCell 3 R_A 10 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 3 resistance at grid point 10 |
| RA Table | R_a3x | xCell 3 R_A 11 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 3 resistance at grid point 11 |
| RA Table | R_a3x | xCell 3 R_A 12 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 3 resistance at grid point 12 |
| RA Table | R_a3x | xCell 3 R_A 13 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 3 resistance at grid point 13 |
| RA Table | R_a3x | xCell 3 R_A 14 | I2 | −32768 | 32768 | 2 [^] −10 Ω | Cell 3 resistance at grid point 14 |

12.14 PF Status

12.14.1 Device Status Data

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|--------------------|-------------------|------|--------|--------|---------|--|
| PF Status | Device Status Data | Safety Alert 0–15 | H2 | 0x0000 | 0xFFFF | 0 | SafetyAlert() bit 0 to bit 15 Bit 0: CUV—Cell Undervoltage 0 = Inactive 1 = Detected Bit 1: COV—Cell Overvoltage 0 = Inactive 1 = Detected Bit 2: OCC1—Overcurrent in Charge 1st Tier 0 = Inactive 1 = Detected Bit 3: OCC2—Overcurrent in Charge 2nd Tier 0 = Inactive 1 = Detected Bit 4: OCD1—Overcurrent in Discharge 1st Tier 0 = Inactive 1 = Detected Bit 5: OCD2—Overcurrent in Discharge 2nd Tier 0 = Inactive 1 = Detected Bit 6: OLD—Overload in discharge 0 = Inactive 1 = Detected Bit 7: OLDL—Overload in discharge latch 0 = Inactive 1 = Detected Bit 8: SCC—Short circuit in charge 0 = Inactive 1 = Detected Bit 9: SCCL—Short circuit in charge latch 0 = Inactive 1 = Detected Bit 10: SCD—Short circuit in discharge 0 = Inactive 1 = Detected Bit 11: SCDL—Short circuit in discharge latch 0 = Inactive 1 = Detected Bit 12: OTC—Overtemperature in charge 0 = Inactive 1 = Detected Bit 13: OTD—Overtemperature in discharge 0 = Inactive 1 = Detected Bit 14: CUVC—I*R compensated CUV 0 = Inactive 1 = Detected Bit 15: Reserved |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|--------------------|--------------------|------|--------|--------|---------|--|
| PF Status | Device Status Data | Safety Status 0–15 | H2 | 0x0000 | 0xFFFF | 0 | SafetyStatus() bit 0 to bit 15 Bit 0: CUV—Cell Undervoltage 0 = Inactive 1 = Detected Bit 1: COV—Cell Overvoltage 0 = Inactive 1 = Detected Bit 2: OCC1—Overcurrent in Charge 1st Tier 0 = Inactive 1 = Detected Bit 3: OCC2—Overcurrent in Charge 2nd Tier 0 = Inactive 1 = Detected Bit 4: OCD1—Overcurrent in Discharge 1st Tier 0 = Inactive 1 = Detected Bit 5: OCD2—Overcurrent in Discharge 2nd Tier 0 = Inactive 1 = Detected Bit 6: OLD—Overload in discharge 0 = Inactive 1 = Detected Bit 7: OLDL—Overload in discharge latch 0 = Inactive 1 = Detected Bit 8: SCC—Short circuit in charge 0 = Inactive 1 = Detected Bit 9: SCCL—Short circuit in charge latch 0 = Inactive 1 = Detected Bit 10: SCD—Short circuit in discharge 0 = Inactive 1 = Detected Bit 11: SCDL—Short circuit in discharge latch 0 = Inactive 1 = Detected Bit 12: OTC—Overtemperature in charge 0 = Inactive 1 = Detected Bit 13: OTD—Overtemperature in discharge 0 = Inactive 1 = Detected Bit 14: CUV— I^*R compensated CUV 0 = Inactive 1 = Detected Bit 15: Reserved |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|--------------------|---------------|------|--------|--------|---------|---|
| PF Status | Device Status Data | PF Alert 0–15 | H2 | 0x0000 | 0xFFFF | 0 | PFAAlert() bit 0 to bit 15 Bit 0: CUV—Cell undervoltage 0 = Inactive 1 = Detected Bit 1: COV—Cell overvoltage 0 = Inactive 1 = Detected Bit 2: CUDEP—Copper Deposition 0 = Inactive 1 = Detected Bit 3: Reserved Bit 4: OTCE—Overtemperature 0 = Inactive 1 = Detected Bit 5: Reserved Bit 6: OTF—Overtemperature FET 0 = Inactive 1 = Detected Bit 7: QIM—QMax Imbalance 0 = Inactive 1 = Detected Bit 8: CB—Cell balancing 0 = Inactive 1 = Detected Bit 9: IMP—Cell impedance 0 = Inactive 1 = Detected Bit 10: CD—Capacity Deterioration 0 = Inactive 1 = Detected Bit 11: VIMR—Voltage imbalance at Rest 0 = Inactive 1 = Detected Bit 12: VIMA—Voltage imbalance at Rest 0 = Inactive 1 = Detected Bit 13: Reserved Bit 14: Reserved Bit 15: Reserved |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|--------------------|----------------|------|--------|--------|---------|--|
| PF Status | Device Status Data | PF Status 0–15 | H2 | 0x0000 | 0xFFFF | 0 | PFStatus() bit 0 to bit 15 Bit 0: CUV—Cell undervoltage 0 = Inactive 1 = Active Bit 1: COV—Cell overvoltage 0 = Inactive 1 = Active Bit 2: Reserved Bit 3: Reserved Bit 4: OTCE—Overtemperature 0 = Inactive 1 = Active Bit 5: Reserved Bit 6: OTF—Overtemperature FET 0 = Inactive 1 = Active Bit 7: QIM—QMax Imbalance 0 = Inactive 1 = Active Bit 8: CB—Cell balancing 0 = Inactive 1 = Active Bit 9: IMP—Cell impedance 0 = Inactive 1 = Active Bit 10: CD—Capacity Deterioration 0 = Inactive 1 = Active Bit 11: VIMR—Voltage imbalance at Rest 0 = Inactive 1 = Active Bit 12: VIMA—Voltage imbalance at Rest 0 = Inactive 1 = Active Bit 13: Reserved Bit 14: Reserved Bit 15: Reserved |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|--------------------|--------------------|------|--------|--------|---------|---|
| PF Status | Device Status Data | Safety Alert 16–31 | H2 | 0x0000 | 0xFFFF | 0 | SafetyAlert() bit 16 to bit 31 Bit 16: OTF—FET overtemperature 0 = Inactive 1 = Detected Bit 17: HWD—SBS Host watchdog timeout 0 = Inactive 1 = Detected Bit 18: PTO—Pre-charging timeout 0 = Inactive 1 = Detected Bit 19: PTOS—Pre-charging timeout suspend 0 = Inactive 1 = Detected Bit 20: CTO—Charging timeout 0 = Inactive 1 = Detected Bit 21: CTOS—Charging timeout suspend 0 = Inactive 1 = Detected Bit 22: OC—Overcharge 0 = Inactive 1 = Detected Bit 23: CHGC—Charging Current higher than requested 0 = Inactive 1 = Detected Bit 24: CHGV—Charging Voltage higher than requested 0 = Inactive 1 = Detected Bit 25: Reserved Bit 26: Reserved Bit 27: Reserved Bit 28: Reserved Bit 29: Reserved Bit 30: Reserved Bit 31: Reserved |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|--------------------|---------------------|------|--------|--------|---------|--|
| PF Status | Device Status Data | Safety Status 16–31 | H2 | 0x0000 | 0xFFFF | 0 | SafetyStatus() bit 16 to bit 31 Bit 16: OTF—FET overtemperature 0 = Inactive 1 = Detected Bit 17: HWD—SBS Host watchdog timeout 0 = Inactive 1 = Detected Bit 18: PTO—Pre-charging timeout 0 = Inactive 1 = Detected Bit 19: PTOS—Pre-charging timeout suspend 0 = Inactive 1 = Detected Bit 20: CTO—Charging timeout 0 = Inactive 1 = Detected Bit 21: CTOS—Charging timeout suspend 0 = Inactive 1 = Detected Bit 22: OC—Overcharge 0 = Inactive 1 = Detected Bit 23: CHGC—Charging Current higher than requested 0 = Inactive 1 = Detected Bit 24: CHGV—Charging Voltage higher than requested 0 = Inactive 1 = Detected Bit 25: Reserved Bit 26: Reserved Bit 27: Reserved Bit 28: Reserved Bit 29: Reserved Bit 30: Reserved Bit 31: Reserved |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|--------------------|----------------|------|--------|--------|---------|--|
| PF Status | Device Status Data | PF Alert 16–31 | H2 | 0x0000 | 0xFFFF | 0 | PFAAlert() bit 16 to bit 31 Bit 16: CFETF—Charge FET 0 = Inactive 1 = Detected Bit 17: DFET—Discharge FET 0 = Inactive 1 = Detected Bit 18: TH—Thermistor 0 = Inactive 1 = Detected Bit 19: FUSE—Fuse 0 = Inactive 1 = Detected Bit 20: AFER—AFE Register 0 = n/a 1 = Detected Bit 21: AFEC—AFE Communication 0 = Inactive 1 = Detected Bit 22: 2LVL—FUSE input indicating fuse trigger by external 2nd level protection 0 = Inactive 1 = Detected Bit 23: Reserved Bit 24: Reserved Bit 25: OCECO—Open VCx 0 = n/a 1 = Detected Bit 26: Reserved Bit 27: Reserved Bit 28: Reserved Bit 29: Reserved Bit 30: Reserved Bit 31: Reserved |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|--------------------|-----------------|------|--------|--------|---------|---|
| PF Status | Device Status Data | PF Status 16–31 | H2 | 0x0000 | 0xFFFF | 0 | PFStatus() bit 16 to bit 31 Bit 16: CFETF—Charge FET 0 = Inactive 1 = Active Bit 17: DFET—Discharge FET 0 = Inactive 1 = Active Bit 18: TH—Thermistor 0 = Inactive 1 = Active Bit 19: FUSE—Fuse 0 = Inactive 1 = Active Bit 20: AFER—AFE Register 0 = n/a 1 = Active Bit 21: AFEC—AFE Communication 0 = Inactive 1 = Active Bit 22: 2LVL—FUSE input indicating fuse trigger by external 2nd level protection 0 = Inactive 1 = Active Bit 23: PTC—PTC by AFE 0 = Inactive 1 = Active Bit 24: IFC—Instruction Flash Checksum 0 = n/a 1 = IF checksum failure Bit 25: OCECO—Open VCx 0 = n/a 1 = Active Bit 26: DFW—DF wearout 0 = n/a 1 = Active Bit 27: Reserved Bit 28: Reserved Bit 29: Reserved Bit 30: Reserved Bit 31: Reserved |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|--------------------|-----------------|------|--------|--------|---------|---|
| PF Status | Device Status Data | PF Status 16–31 | H2 | 0x0000 | 0xFFFF | 0 | Bit 16: SDM—Shutdown activated by ManufacturerAccess() 0 = Inactive 1 = Active Bit 17: SHIPM—Ship Mode activated with ManufacturerAccess() 0 = Inactive 1 = Active Bit 18: AUTH—Authentication ongoing 0 = Inactive 1 = Active Bit 19: AWD—AFE Watchdog failure 0 = Inactive 1 = Active Bit 20: FVS—Fast Voltage Sampling 0 = Inactive 1 = Active Bit 21: CALO—Raw ADC/CC offset output 0 = Inactive 1 = Active Bit 22: SDV—Shutdown activated by voltage 0 = Inactive 1 = Active Bit 23: SLEEPM—Sleep mode active by ManufacturerAccess() 0 = Inactive 1 = Active Bit 24: INIT Initialization after full reset, cleared when SBS data calculated and available 0 = Inactive 1 = Active Bit 25: SMBLCAL—CC auto offset calibration ongoing after SBS line goes low 0 = Inactive 1 = Active Bit 26: SLEEPQMax—QMax update in Sleep mode 0 = Inactive 1 = Active Bit 27: SLEEPCC—Checking current in Sleep mode 0 = Inactive 1 = Active Bit 28: GPOD—GPOD pin status 0 = Inactive (high) 1 = Active (low) Bit 29: Reserved Bit 30: Reserved Bit 31: Reserved |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|--------------------|-----------------------|------|--------|--------|---------|---|
| PF Status | Device Status Data | Operation Status 0–15 | H2 | 0x0000 | 0xFFFF | 0 | OperationStatus() bit 0 to bit 15 Bit 0: PRES —PRES input state 0 = PRES pin high 1 = PRES pin low Detected Bit 1: DSG—DSG FET Status 0 = Disabled 1 = Enabled Bit 2: CHG—CHG FET Status 0 = Disabled 1 = Enabled Bit 3: PCHG—PCHG FET Status 0 = Disabled 1 = Enabled Bit 4: GPOD—PPOD FET Status 0 = Disabled 1 = Enabled Bit 5: FUSE—FUSE input 0 = FUSE pin low 1 = FUSE pin high Detected Bit 6: CB—Cell Balancing 0 = Inactive 1 = Active Bit 7: LED—LED Display 0 = Inactive 1 = Active Bit 8:9: SEC0,SEC1—Security Mode 0,0 = Reserved 0,1 = Unsealed 1,0 = Full Access 1,1 = Sealed Bit 10: CALCal Raw ADC/CC output active 0 = Inactive 1 = Active Bit 11: SS—SafetyStatus 0 = Inactive 1 = Active Bit 12: PF—Permanent Failure 0 = Inactive 1 = Active Bit 13: XD SG—Discharging Disabled 0 = Inactive 1 = Active Bit 14: XCHG—Charging Disabled 0 = Inactive 1 = Active Bit 15: SLEEP—Sleep condition met 0 = Disabled 1 = Enabled |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|--------------------|------------------------|------|--------|--------|---------|---|
| PF Status | Device Status Data | Operation Status 16–31 | H2 | 0x0000 | 0xFFFF | 0 | OperationStatus() bit 16 to bit 31 Bit 16: SDM—Shutdown activated by ManufacturerAccess() 0 = Inactive 1 = Active Bit 17: SHIPM—Ship Mode activated with ManufacturerAccess() 0 = Inactive 1 = Active Bit 18: AUTH—Authentication ongoing 0 = Inactive 1 = Active Bit 19: AWD—AFE Watchdog failure 0 = Inactive 1 = Active Bit 20: FVS—Fast Voltage Sampling 0 = Inactive 1 = Active Bit 21: CALO—Raw ADC/CC offset output 0 = Inactive 1 = Active Bit 22: SDV—Shutdown activated by voltage 0 = Inactive 1 = Active Bit 23: SLEEPM—Sleep mode active by ManufacturerAccess() 0 = Inactive 1 = Active Bit 24: INIT—Initialization after full reset, cleared when SBS data calculated and available 0 = Inactive 1 = Active Bit 25: SMBL—CALCC auto offset calibration ongoing after SBS line goes low 0 = Inactive 1 = Active Bit 26: SLEEPQMax—QMax update in Sleep mode 0 = Inactive 1 = Active Bit 27: SLEEPCC—Checking current in Sleep mode 0 = Inactive 1 = Active Bit 28: XLSBS Fast Mode 0 = Inactive 1 = Active Bit 29: Reserved Bit 30: Reserved Bit 31: Reserved |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|--------------------|-----------------------|------|--------|--------|---------|---|
| PF Status | Device Status Data | Charging Status 0–15 | H2 | 0x0000 | 0xFFFF | 0 | ChargingStatus() bit 0 to bit 15 Bit 0: UT—Under Temperature Range 0 = Inactive 1 = Active Bit 1: LT—Low Temperature Range 0 = Inactive 1 = Active Bit 2: ST—Standard Temperature Range 0 = Inactive 1 = Active Bit 3: HT—High Temperature Range 0 = Inactive 1 = Active Bit 4: RT—Recommended Temperature Range 0 = Inactive 1 = Active Bit 5: OT—Over Temperature Range 0 = Inactive 1 = Active Bit 6: PV—Precharge Voltage Range 0 = Inactive 1 = Active Bit 7: LV—Low Voltage Range 0 = Inactive 1 = Active Bit 8: MV—Medium Voltage Range 0 = Inactive 1 = Active Bit 9: HV—High Voltage Range 0 = Inactive 1 = Active Bit 10: IN—Charge Inhibit 0 = Inactive 1 = Active Bit 11: SU—Charge Suspend 0 = Inactive 1 = Active Bit 12: CCR— ChargingVoltage() Rate 0 = Inactive 1 = Active Bit 13: CVR—ChargingCurrent() Rate 0 = Inactive 1 = Active Bit 14: CCC—ChargingCurrent() Compensation 0 = Inactive 1 = Active Bit 15: Reserved |
| PF Status | Device Status Data | Charging Status 16–23 | H2 | 0x0000 | 0xFFFF | 0 | ChargingStatus() bit 16 to bit 31 Bit 16: VCT—Valid Charge Termination. This flag toggles every time valid charge termination is Detected. Bit 17: Reserved Bit 18: Reserved Bit 19: Reserved Bit 20: Reserved Bit 21: Reserved Bit 22: Reserved Bit 23: Reserved Bit 24: Reserved |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|--------------------|--------------------|----------------|--------|--------|---------|--|
| PF Status | Device Status Data | Gauging Status | H2 | 0x0000 | 0xFFFF | 0 | GaugingStatus() bit 0 to bit 15 Bit 0: REST—Device at rest 0 = Inactive 1 = Active Bit 1: DSG—Discharge Detected 0 = Charging 1 = Discharging Bit 2: RU—Resistance update 0 = Disabled 1 = Enabled Bit 3: VOK—Cell Voltage OK for QMax update 0 = Inactive 1 = Active Bit 4: QEN—QMax updates 0 = Disabled 1 = Enabled Bit 5: FD—Fully Discharged Detected by gauge algorithm 0 = Disabled 1 = Enabled Bit 6: FC—Fully Charged Detected by gauge algorithm 0 = Disabled 1 = Enabled |
| | PF Status | Device Status Data | Gauging Status | H2 | 0x0000 | 0xFFFF | Bit 7: NSFM—Negative scale factor mode 0 = Disabled 1 = Enabled Bit 8: VDQ—Discharge qualified for learning 0 = Disabled 1 = Enabled Bit 9: QMax—QMax updated. This flag toggles every time QMax is updated. Bit 10: RX—Resistance update This flag toggles every time Resistance is updated Bit 11: LDMD—Load Mode 0 = Constant current mode 1 = Constant power mode Bit 12: OCVFR—OCV in flat region 0 = OCV outside flat region 1 = OCV in flat region Bit 13: TDA—Terminate Discharge Alarm set by gauging algorithm 0 = Disabled 1 = Enabled Bit 14: TCA—Terminate Charge Alarm set by gauging algorithm 0 = Disabled 1 = Enabled Bit 15: LPH Relax—LiPh Relax Mode, only active with Chem ID 0x400 0 = Disabled 1 = Enabled |

12.14.2 Device Voltage Data

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-----------|---------------------|----------------|------|-----|-------|---------|------|----------------|
| PF Status | Device Voltage Data | Cell Voltage 0 | I2 | 0 | 32767 | 0 | mV | Cell 0 voltage |
| PF Status | Device Voltage Data | Cell Voltage 1 | I2 | 0 | 32767 | 0 | mV | Cell 1 voltage |

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-----------|---------------------|--------------------|------|-----|-------|---------|------|--------------------|
| PF Status | Device Voltage Data | Cell Voltage 2 | I2 | 0 | 32767 | 0 | mV | Cell 2 voltage |
| PF Status | Device Voltage Data | Cell Voltage 3 | I2 | 0 | 32767 | 0 | mV | Cell 3 voltage |
| PF Status | Device Voltage Data | Bat Direct Voltage | I2 | 0 | 32767 | 0 | mV | Cell stack voltage |
| PF Status | Device Voltage Data | Pack Voltage | I2 | 0 | 32767 | 0 | mV | Pack pin voltage |

12.14.3 Device Current Data

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-----------|---------------------|---------|------|--------|-------|---------|------|-------------|
| PF Status | Device Current Data | Current | I2 | −32768 | 32767 | 0 | mV | Current() |

12.14.4 Device Temperature Data

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-----------|-------------------------|------------------------|------|-----|------|---------|-------|---|
| PF Status | Device Temperature Data | Internal Temperature | I2 | 0 | 9999 | 0 | 0.1°K | Internal temperature sensor temperature |
| PF Status | Device Temperature Data | External 1 Temperature | I2 | 0 | 9999 | 0 | 0.1°K | External TS1 temperature |
| PF Status | Device Temperature Data | External 2 Temperature | I2 | 0 | 9999 | 0 | 0.1°K | External TS2 temperature |
| PF Status | Device Temperature Data | External 3 Temperature | I2 | 0 | 9999 | 0 | 0.1°K | External TS3 temperature |
| PF Status | Device Temperature Data | External 4 Temperature | I2 | 0 | 9999 | 0 | 0.1°K | External TS4 temperature |

12.14.5 Device Gauging Data

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-----------|---------------------|---------------|------|-----|-------|---------|------|--------------------------------------|
| PF Status | Device Gauging Data | Cell 0 DOD0 | I2 | 0 | 32767 | 0 | | Cell 0 depth of discharge |
| PF Status | Device Gauging Data | Cell 1 DOD0 | I2 | 0 | 32767 | 0 | | Cell 1 depth of discharge |
| PF Status | Device Gauging Data | Cell 2 DOD0 | I2 | 0 | 32767 | 0 | | Cell 2 depth of discharge |
| PF Status | Device Gauging Data | Cell 3 DOD0 | I2 | 0 | 32767 | 0 | | Cell 3 depth of discharge |
| PF Status | Device Gauging Data | Passed Charge | I2 | 0 | 32767 | 0 | mAh | Passed charge since last QMax update |

12.14.6 AFE Regs

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|----------|-------------------|------|------|------|---------|--|
| PF Status | AFE Regs | AFE Status | H1 | 0x00 | 0xFF | 0 | Bit 0: SCD1—SCD1 0 = Inactive 1 = Active Bit 1: SCD2—SCD2 0 = Inactive 1 = Active Bit 2: SCC—SCC 0 = Inactive 1 = Active Bit 3: OCD—SCD1 0 = Inactive 1 = Active Bit 4: WDF—WDF 0 = Inactive 1 = Active Bit 5: Reserved Bit 6: PTC—PTC 0 = Inactive 1 = Active Bit 7: FUSE—FUSE 0 = Inactive 1 = Active |
| PF Status | AFE Regs | AFE State Control | H1 | 0x00 | 0xFF | 0 | Bit 0: Reserved Bit 1: SHUTDOWN—Enables device shutdown when voltage on PACK pins is removed 0 = Disabled 1 = Enabled Bit 2: WDDIS—Enables device watchdog timer 0 = Enabled 1 = Disabled Bit 3: WDRST—Enables device reset when watchdog timer times out 0 = Disabled 1 = Enabled Bit 4: RSNS—Divide OCD, SCC, SDC1 and SCD2 voltage thresholds by 2 0 = Disabled 1 = Enabled Bit 5: SCDDx2—Double SCD1 and SCD2 Delay thresholds 0 = Disabled 1 = Enabled Bit 6: CTM_ENA—Enable customer test mode 0 = Disabled 1 = Enabled Bit 7: FUSE—A part one of FUSE activation sequence 0 = Disabled 1 = Enabled |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|----------|----------------------|------|------|------|---------|--|
| PF Status | AFE Regs | AFE Control | H1 | 0x00 | 0xFF | 0 | Bit 0: LTCLR—Clear latch condition 0 = Inactive 1 = Active Bit 1: DSG 0 = Inactive 1 = Active Bit 2: CHG 0 = Inactive 1 = Active Bit 3: PCHG—CHG 0 = Inactive 1 = Active Bit 4: GPOD—CHG 0 = Inactive 1 = Active Bit 5: PMS_CHG 0 = Inactive 1 = Active Bit 6: CTM_ENB 0 = Inactive 1 = Active Bit 7: FUSEB 0 = Inactive 1 = Active |
| PF Status | AFE Regs | AFE Output Status | H1 | 0x00 | 0xFF | 0 | Bit 0: Reserved Bit 1: DSG 0 = Inactive 1 = Active Bit 2: CHG 0 = Inactive 1 = Active Bit 3: PCHG—CHG 0 = Inactive 1 = Active Bit 4: GPOD—CHG 0 = Inactive 1 = Active Bit 5: PMS_CHG 0 = Inactive 1 = Active Bit 6: CTM 0 = Inactive 1 = Active Bit 7: PMS 0 = Inactive 1 = Active |
| PF Status | AFE Regs | AFE Function Control | H1 | 0x00 | 0xFF | 0 | Bit 0: VMEN 0 = Inactive 1 = Active Bit 1: PACK 0 = Inactive 1 = Active Bit 2: BATDSG 0 = Inactive 1 = Active Bit 3: SC_REC 0 = Inactive 1 = Active Bit 5:4: RV1,RV0:RV Bit 6: Reserved Bit 7: Reserved |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|----------|-----------------|------|------|------|---------|---|
| PF Status | AFE Regs | AFE Cell Select | H1 | 0x00 | 0xFF | 0 | Bit 1:0: CELL1, CELL0 Cell Select Bit 2: CALCAL 0 = Inactive 1 = Active Bit 3: Reserved Bit 4: CB0 0 = Inactive 1 = Active Bit 5: CB1 0 = Inactive 1 = Active Bit 6: CB2 0 = Inactive 1 = Active Bit 4: CB3 0 = Inactive 1 = Active |
| PF Status | AFE Regs | AFE OCDV | H1 | 0x00 | 0xFF | 0 | Bit 3:0: Overload Trip Threshold between SRP and SRN 0x00 to 0x0F = 0.050 V to 0.200 V in 10 mV steps when RSNS = 00x00 to 0x0F = 0.025 V to 0.100 V in 5 mV steps when RSNS = 10x00 = 0.050 V or 0.025 V 0x01 = 0.060 V or 0.030 V 0x02 = 0.070 V or 0.035 V 0x03 = 0.080 V or 0.040 V 0x04 = 0.090 V or 0.045 V 0x05 = 0.100 V or 0.050 V 0x06 = 0.110 V or 0.055 V 0x07 = 0.120 V or 0.060 V 0x08 = 0.130 V or 0.065 V 0x09 = 0.140 V or 0.070 V 0x0A = 0.150 V or 0.075 V 0x0B = 0.160 V or 0.080 V 0x0C = 0.170 V or 0.085 V 0x0D = 0.180 V or 0.090 V 0x0E = 0.190 V or 0.095 V 0x0F = 0.200 V or 0.100 V |
| PF Status | AFE Regs | AFE OCDT | H1 | 0x00 | 0xFF | 0 | Bit 3:0: Overload Trip Delay 0x00 to 0x0F = 1 ms to 31 ms in 2-ms steps 0x00 = 1 ms 0x01 = 3 ms 0x02 = 5 ms 0x03 = 7 ms 0x04 = 9 ms 0x05 = 11 ms 0x06 = 13 ms 0x07 = 15 ms 0x08 = 17 ms 0x09 = 19 ms 0x0A = 21 ms 0x0B = 23 ms 0x0C = 25 ms 0x0D = 27 ms 0x0E = 29 ms |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|----------|----------|------|------|------|---------|---|
| PF Status | AFE Regs | AFE SCC | H1 | 0x00 | 0xFF | 0 | Bit 2:0: Short Circuit in Charge Threshold between SRP and SRN 0x00 to 0x04 = –0.100 V to –0.300 V in 50 mV steps when RSNS = 00x00 to 0x04 = –0.050 V to –0.150 V in 25-mV steps when RSNS = 1 0x00 = –0.100 V or –0.050 V 0x01 = –0.150 V or –0.075 V 0x02 = –0.200 V or –0.100 V 0x03 = –0.250 V or –0.125 V 0x04 = –0.300 V or –0.150 V 0x05 = Reserved 0x06 = Reserved 0x07 = Reserved Bit 3: Reserved Bit 7:4: Short Circuit in Charge Delay Time 0x00 to 0x0F = 0 µs to 915 µs in 61-µs steps 0x00 = 0 µs 0x01 = 61 µs 0x02 = 122 µs 0x03 = 183 µs 0x04 = 244 µs 0x05 = 305 µs 0x06 = 366 µs 0x07 = 427 µs 0x08 = 488 µs 0x09 = 549 µs 0x0A = 610 µs 0x0B = 671 µs 0x0C = 732 µs 0x0D = 793 µs 0x0E = 854 µs 0x0F = 915 µs |
| PF Status | AFE Regs | AFE SCD1 | H1 | 0x00 | 0xFF | 0 | Bit 2:0: Short Circuit in Discharge 1 Threshold between SRP and SRN 0x00 to 0x07 = 0.100 V to 0.300 V in 50 mV steps when RSNS = 00x00 to 0x07 = 0.050 V to 0.150 V in 25 mV steps when RSNS = 1 0x00 = 0.100 V or 0.050 V 0x01 = 0.150 V or 0.075 V 0x02 = 0.200 V or 0.100 V 0x03 = 0.250 V or 0.125 V 0x04 = 0.300 V or 0.150 V 0x05 = 0.350 V or 0.175 V 0x06 = 0.400 V or 0.200 V 0x07 = 0.450 V or 0.225 V Bit 3: Reserved |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|----------|----------|------|------|------|---------|--|
| PF Status | AFE Regs | AFE SCD1 | H1 | 0x00 | 0xFF | 0 | Bit 7:4: Short Circuit in Discharge 1 Delay Time 0x00 to 0x0F = 0 μ s to 915 μ s in 61- μ s steps when SCDDx2 = 00x00 to 0x0F = 0 μ s to 1830 μ s in 122- μ s steps when SCDDx2 = 1 0x00 = 0 μ s 0x01 = 61 μ s or 122 μ s 0x02 = 122 μ s or 244 μ s 0x03 = 183 μ s or 366 μ s 0x04 = 244 μ s or 488 μ s 0x05 = 305 μ s or 610 μ s 0x06 = 366 μ s or 732 μ s 0x07 = 427 μ s or 854 μ s 0x08 = 488 μ s or 976 μ s 0x09 = 549 μ s or 1098 μ s 0x0A = 610 μ s or 1220 μ s 0x0B = 671 μ s or 1342 μ s 0x0C = 732 μ s or 1464 μ s 0x0D = 793 μ s or 1586 μ s 0x0E = 854 μ s or 1708 μ s 0x0F = 915 μ s or 1830 μ s |
| PF Status | AFE Regs | AFE SCD2 | H1 | 0x00 | 0xFF | 0 | Bit 2:0: Short Circuit in Discharge 2 Threshold between SRP and SRN 0x00 to 0x07 = 0.100 V to 0.300 V in 50-mV steps when RSNS = 00x00 to 0x07 = 0.050 V to 0.150 V in 25-mV steps when RSNS = 10x00 = 0.100 V or 0.050 V 0x01 = 0.150 V or 0.075 V 0x02 = 0.200 V or 0.100 V 0x03 = 0.250 V or 0.125 V 0x04 = 0.300 V or 0.150 V 0x05 = 0.350 V or 0.175 V 0x06 = 0.400 V or 0.200 V 0x07 = 0.450 V or 0.225 V Bit 3: Reserved Bit 7:4: Short Circuit in Discharge 2 Delay Time 0x00 to 0x0F = 0 μ s to 915 μ s in 61- μ s steps when SCDDx2 = 00x00 to 0x0F = 0 μ s to 1830 μ s in 122- μ s steps when SCDDx2 = 10x00 = 0 μ s 0x01 = 30 μ s or 61 μ s 0x02 = 61 μ s or 122 μ s 0x03 = 91 μ s or 183 μ s 0x04 = 122 μ s or 244 μ s 0x05 = 152 μ s or 305 μ s 0x06 = 183 μ s or 366 μ s 0x07 = 213 μ s or 427 μ s 0x08 = 244 μ s or 488 μ s 0x09 = 275 μ s or 549 μ s 0x0A = 305 μ s or 610 μ s 0x0B = 335 μ s or 671 μ s 0x0C = 366 μ s or 732 μ s 0x0D = 396 μ s or 793 μ s 0x0E = 426 μ s or 854 μ s 0x0F = 458 μ s or 915 μ s |

12.15 Black Box

12.15.1 Safety Status

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|---------------|------------------------|------|--------|--------|---------|--|
| Black Box | Safety Status | 1st Safety Status 0–15 | H2 | 0x0000 | 0xFFFF | 0 | SafetyStatus() bit 0 to bit 15 Bit 0: CUV—Cell Undervoltage 0 = Inactive 1 = Detected Bit 1: COV—Cell Overvoltage 0 = Inactive 1 = Detected Bit 2: OCC1—Overcurrent in Charge 1st Tier 0 = Inactive 1 = Detected Bit 3: OCC2—Overcurrent in Charge 2nd Tier 0 = Inactive 1 = Detected Bit 4: OCD1—Overcurrent in Discharge 1st Tier 0 = Inactive 1 = Detected Bit 5: OCD2—Overcurrent in Discharge 2nd Tier 0 = Inactive 1 = Detected Bit 6: OLD—Overload in discharge 0 = Inactive 1 = Detected Bit 7: OLDL—Overload in discharge latch 0 = Inactive 1 = Detected Bit 8: SCC—Short circuit in charge 0 = Inactive 1 = Detected |
| Black Box | Safety Status | 1st Safety Status 0–15 | H2 | 0x0000 | 0xFFFF | 0 | Bit 9: SCCL—Short circuit in charge latch 0 = Inactive 1 = Detected Bit 10: SCD—Short circuit in discharge 0 = Inactive 1 = Detected Bit 11: SCDL—Short circuit in discharge latch 0 = Inactive 1 = Detected Bit 12: OTC—Overtemperature in charge 0 = Inactive 1 = Detected Bit 13: OTD—Overtemperature in discharge 0 = Inactive 1 = Detected Bit 14: CUVC—I*R compensated CUV 0 = Inactive 1 = Detected Bit 15: Reserved |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|---------------|-------------------------|------|--------|--------|---------|---|
| Black Box | Safety Status | 1st Safety Status 16–31 | H2 | 0x0000 | 0xFFFF | 0 | SafetyStatus() bit 16 to bit 31 Bit 16: OTF—FET overtemperature 0 = Inactive 1 = Detected Bit 17: HWD—SBS Host watchdog timeout 0 = Inactive 1 = Detected Bit 18: PTO—Pre-charging Timeout 0 = Inactive 1 = Detected Bit 19: PTOS—Pre-charging Timeout Suspend 0 = Inactive 1 = Detected Bit 20: CTO—Charging Timeout 0 = Inactive 1 = Detected |
| Black Box | Safety Status | 1st Safety Status 16–31 | H2 | 0x0000 | 0xFFFF | 0 | Bit 21: CTOS—Charging Timeout Suspend 0 = Inactive 1 = Detected Bit 22: OC—Overcharge 0 = Inactive 1 = Detected Bit 23: CHGC—Charging Current higher than requested 0 = Inactive 1 = Detected Bit 24: CHGV—Charging Voltage higher than requested 0 = Inactive 1 = Detected Bit 25: Reserved Bit 26: Reserved Bit 27: Reserved Bit 28: Reserved Bit 29: Reserved Bit 30: Reserved Bit 31: Reserved |
| Black Box | Safety Status | 1st Time to Next Event | U1 | 0 | 255 | 0 | Time from 1st event to 2nd event |
| Black Box | Safety Status | 2nd Safety Status 0–15 | H2 | 0x0000 | 0xFFFF | 0 | SafetyStatus() bit 0 to bit 15 Bit 0: CUV—Cell Undervoltage 0 = Inactive 1 = Detected Bit 1: COV—Cell Overvoltage 0 = Inactive 1 = Detected Bit 2: OCC1—Overcurrent in Charge 1st Tier 0 = Inactive 1 = Detected Bit 3: OCC2—Overcurrent in Charge 2nd Tier 0 = Inactive 1 = Detected Bit 4: OCD1—Overcurrent in Discharge 1st Tier 0 = Inactive 1 = Detected Bit 5: OCD2—Overcurrent in Discharge 2nd Tier 0 = Inactive 1 = Detected Bit 6: OLD—Overload in Discharge 0 = Inactive 1 = Detected |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|---------------|-------------------------|------|--------|--------|---------|--|
| Black Box | Safety Status | 2nd Safety Status 0–15 | H2 | 0x0000 | 0xFFFF | 0 | Bit 7: OLDL—Overload in discharge latch 0 = Inactive 1 = Detected Bit 8: SCC—Short circuit in charge 0 = Inactive 1 = Detected Bit 9: SCCL—Short circuit in charge latch 0 = Inactive 1 = Detected Bit 10: SCD—Short circuit in discharge 0 = Inactive 1 = Detected Bit 11: SCDL—Short circuit in discharge latch 0 = Inactive 1 = Detected Bit 12: OTC—Overtemperature in charge 0 = Inactive 1 = Detected Bit 13: OTD—Overtemperature in discharge 0 = Inactive 1 = Detected Bit 14: CUVC—I*R compensated CUV 0 = Inactive 1 = Detected Bit 15: Reserved |
| Black Box | Safety Status | 2nd Safety Status 16–31 | H2 | 0x0000 | 0xFFFF | 0 | SafetyStatus() bit 16 to bit 31 Bit 16: OTF—FET overtemperature 0 = Inactive 1 = Detected Bit 17: HWD—SBS Host watchdog timeout 0 = Inactive 1 = Detected Bit 18: PTO—Pre-charging timeout 0 = Inactive 1 = Detected Bit 19: PTOS—Pre-charging timeout suspend 0 = Inactive 1 = Detected Bit 20: CTO—Charging timeout 0 = Inactive 1 = Detected |
| Black Box | Safety Status | 2nd Safety Status 16–31 | H2 | 0x0000 | 0xFFFF | 0 | Bit 21: CTOS—Charging timeout suspend 0 = Inactive 1 = Detected Bit 22: OC—Overcharge 0 = Inactive 1 = Detected Bit 23: CHGC—ChargingCurrent higher than requested 0 = Inactive 1 = Detected Bit 24: CHGV—Charging Voltage higher than requested 0 = Inactive 1 = Detected Bit 25: Reserved Bit 26: Reserved Bit 27: Reserved Bit 28: Reserved Bit 29: Reserved Bit 30: Reserved Bit 31: Reserved |
| Black Box | Safety Status | 2nd Time to Next Event | U1 | 0 | 255 | 0 | Time from 2nd event to 3rd event |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|---------------|-------------------------|------|--------|--------|---------|--|
| Black Box | Safety Status | 3rd Safety Status 0–15 | H2 | 0x0000 | 0xFFFF | 0 | SafetyStatus() bit 0 to bit 15 Bit 0: CUV—Cell Undervoltage 0 = Inactive 1 = Detected Bit 1: COV—Cell Overvoltage 0 = Inactive 1 = Detected Bit 2: OCC1—Overcurrent in Charge 1st Tier 0 = Inactive 1 = Detected Bit 3: OCC2—Overcurrent in Charge 2nd Tier 0 = Inactive 1 = Detected Bit 4: OCD1—Overcurrent in Discharge 1st Tier 0 = Inactive 1 = Detected Bit 5: OCD2—Overcurrent in Discharge 2nd Tier 0 = Inactive 1 = Detected Bit 6: OLD—Overload in discharge 0 = Inactive 1 = Detected Bit 7: OLDL—Overload in discharge latch 0 = Inactive 1 = Detected |
| Black Box | Safety Status | 3rd Safety Status 0–15 | H2 | 0x0000 | 0xFFFF | 0 | Bit 8: SCC—Short circuit in charge 0 = Inactive 1 = Detected Bit 9: SCCL—Short circuit in charge latch 0 = Inactive 1 = Detected Bit 10: SCD—Short circuit in discharge 0 = Inactive 1 = Detected Bit 11: SCDL—Short circuit in discharge latch 0 = Inactive 1 = Detected Bit 12: OTC—Overtemperature in charge 0 = Inactive 1 = Detected Bit 13: OTD—Overtemperature in discharge 0 = Inactive 1 = Detected Bit 14: CUVC—I*R compensated CUV 0 = Inactive 1 = Detected Bit 15: Reserved |
| Black Box | Safety Status | 3rd Safety Status 16–31 | H2 | 0x0000 | 0xFFFF | 0 | SafetyStatus() bit 16 to bit 31 Bit 16: OTF—FET Overtemperature 0 = Inactive 1 = Detected Bit 17: HWDSBS—Host Watchdog Timeout 0 = Inactive 1 = Detected Bit 18: PTO—Pre-charging Timeout 0 = Inactive 1 = Detected Bit 19: PTOS—Pre-charging Timeout Suspend 0 = Inactive 1 = Detected Bit 20: CTO—Charging Timeout 0 = Inactive 1 = Detected |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|---------------|-------------------------|------|--------|--------|---------|--|
| Black Box | Safety Status | 3rd Safety Status 16–31 | H2 | 0x0000 | 0xFFFF | 0 | Bit 21: CTOS—Charging Timeout Suspend 0 = Inactive 1 = Detected Bit 22: OC—Overcharge 0 = Inactive 1 = Detected Bit 23: CHGC—Charging Current higher than requested 0 = Inactive 1 = Detected Bit 24: CHGV—Charging Voltage higher than requested 0 = Inactive 1 = Detected Bit 25: Reserved Bit 26: Reserved Bit 27: Reserved Bit 28: Reserved Bit 29: Reserved Bit 30: Reserved Bit 31: Reserved |
| Black Box | Safety Status | 3rd Time to Next Event | U1 | 0 | 255 | | Time since 3rd event |

12.15.2 PF Status

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|-----------|--------------------|------|--------|--------|---------|---|
| Black Box | PF Status | 1st PF Status 0–15 | H2 | 0x0000 | 0xFFFF | 0 | PFStatus() bit 0 to bit 15 Bit 0: CUV—Cell Undervoltage 0 = Inactive 1 = Active Bit 1: COV—Cell Overvoltage 0 = Inactive 1 = Active Bit 2: CUDEP—Copper Deposition 0 = Inactive 1 = Active Bit 3: Reserved Bit 4: OTCE—Overtemperature 0 = Inactive 1 = Active Bit 5: Reserved Bit 6: OTF—Overtemperature FET 0 = Inactive 1 = Active Bit 7: QIM—QMax Imbalance 0 = Inactive 1 = Active |
| Black Box | PF Status | 1st PF Status 0–15 | H2 | 0x0000 | 0xFFFF | 0 | Bit 8: CB—Cell Balancing 0 = Inactive 1 = Active Bit 9: IMP—Cell Impedance 0 = Inactive 1 = Active Bit 10: CD—Capacity Deterioration 0 = Inactive 1 = Active Bit 11: VIMR—Voltage Imbalance at Rest 0 = Inactive 1 = Active Bit 12: VIMA—Voltage Imbalance at Rest 0 = Inactive 1 = Active Bit 13: Reserved Bit 14: Reserved Bit 15: Reserved |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|-----------|------------------------|------|--------|--------|---------|--|
| Black Box | PF Status | 1st PF Status 16–32 | H2 | 0x0000 | 0xFFFF | 0 | PFStatus() bit 16 to bit 31 Bit 16: CFETF—Charge FET 0 = Inactive 1 = Active Bit 17: DFET—Discharge FET 0 = Inactive 1 = Active Bit 18: TH—Thermistor 0 = Inactive 1 = Active Bit 19: FUSE—Fuse 0 = Inactive 1 = Active Bit 20: AFER—AFE Register 0 = n/a 1 = Active Bit 21: AFEC—AFE Communication 0 = Inactive 1 = Active Bit 22: 2LVL—FUSE input indicating fuse trigger by external 2nd level protection 0 = Inactive 1 = Active Bit 23: PTC—PTC by AFE 0 = Inactive 1 = Active Bit 24: IFC—Instruction Flash Checksum 0 = n/a 1 = IF checksum failure Bit 25: OCECO—Open VCx 0 = n/a 1 = Active Bit 26: DFW—DF Wearout 0 = n/a 1 = Active Bit 27: Reserved Bit 28: Reserved Bit 29: Reserved Bit 30: Reserved Bit 31: Reserved |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|-----------|------------------------|------|--------|--------|---------|--|
| Black Box | PF Status | 1st PF Status 16–32 | H2 | 0x0000 | 0xFFFF | 0 | Bit 16: SDM—Shutdown activated by ManufacturerAccess() 0 = Inactive 1 = Active Bit 17: SHIPM—Ship mode activated with ManufacturerAccess() 0 = Inactive 1 = Active Bit 18: AUTH—Authentication ongoing 0 = Inactive 1 = Active Bit 19: AWD—AFE Watchdog failure 0 = Inactive 1 = Active Bit 20: FVS—Fast Voltage Sampling 0 = Inactive 1 = Active Bit 21: CALO—Raw ADC/CC offset output 0 = Inactive 1 = Active Bit 22: SDV—Shutdown activated by voltage 0 = Inactive 1 = Active Bit 23: SLEEPM—Sleep mode active by ManufacturerAccess() 0 = Inactive 1 = Active Bit 24: INIT—Initialization after full reset, cleared when SBS data calculated and available 0 = Inactive 1 = Active Bit 25: SMBLCAL—CC auto offset calibration ongoing after SBS line goes low 0 = Inactive 1 = Active Bit 26: SLEEPQMax—QMax update in Sleep mode 0 = Inactive 1 = Active Bit 27: SLEEPCC—Checking Current in Sleep mode 0 = Inactive 1 = Active Bit 28: GPOD—GPOD pin status 0 = Inactive (high) 1 = Active (low) Bit 29: Reserved Bit 30: Reserved Bit 31: Reserved |
| Black Box | PF Status | 1st Time to Next Event | U1 | 0 | 255 | 0 | Time from 1st event to 2nd event |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|-----------|-----------------------|------|--------|--------|---------|---|
| Black Box | PF Status | 2nd PF Status 0–15 | H2 | 0x0000 | 0xFFFF | 0 | PFStatus() bit 0 to bit 15 Bit 0: CUV—Cell Undervoltage 0 = Inactive 1 = Active Bit 1: COV—Cell Overvoltage 0 = Inactive 1 = Active Bit 2: CUDEP—Copper Deposition 0 = Inactive 1 = Active Bit 3: Reserved Bit 4: OTCE—Overtemperature 0 = Inactive 1 = Active Bit 5: Reserved Bit 6: OTF—Overtemperature FET 0 = Inactive 1 = Active Bit 7: QIM—QMax Imbalance 0 = Inactive 1 = Active Bit 8: CB—Cell Balancing 0 = Inactive 1 = Active Bit 9: IMP—Cell Impedance 0 = Inactive 1 = Active Bit 10: CD—Capacity Deterioration 0 = Inactive 1 = Active Bit 11: VIMR—Voltage Imbalance at Rest 0 = Inactive 1 = Active Bit 12: VIMA—Voltage Imbalance at Rest 0 = Inactive 1 = Active Bit 13: Reserved Bit 14: Reserved Bit 15: Reserved |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|-----------|------------------------|------|--------|--------|---------|--|
| Black Box | PF Status | 2nd PF Status 16–32 | H2 | 0x0000 | 0xFFFF | 0 | PFStatus() bit 16 to bit 31 Bit 16: CFETF—Charge FET 0 = Inactive 1 = Active Bit 17: DFET—Discharge FET 0 = Inactive 1 = Active Bit 18: TH—Thermistor 0 = Inactive 1 = Active Bit 19: FUSE—Fuse 0 = Inactive 1 = Active Bit 20: AFER—AFE Register 0 = n/a 1 = Active Bit 21: AFEC—AFE Communication 0 = Inactive 1 = Active Bit 22: 2LVL—FUSE input indicating fuse trigger by external 2nd level protection 0 = Inactive 1 = Active Bit 23: PTC—PTC by AFE 0 = Inactive 1 = Active Bit 24: IFC—Instruction Flash Checksum 0 = n/a 1 = IF checksum failure Bit 25: OCECO—Open VCx 0 = n/a 1 = Active Bit 26: DFW—DF wearout 0 = n/a 1 = Active Bit 27: Reserved Bit 28: Reserved Bit 29: Reserved Bit 30: Reserved Bit 31: Reserved |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|-----------|------------------------|------|--------|--------|---------|---|
| Black Box | PF Status | 2nd PF Status 16–32 | H2 | 0x0000 | 0xFFFF | 0 | Bit 16: SDM—Shutdown activated by ManufacturerAccess() 0 = Inactive 1 = Active Bit 17: SHIPM—Ship Mode activated with ManufacturerAccess() 0 = Inactive 1 = Active Bit 18: AUTH—Authentication ongoing 0 = Inactive 1 = Active Bit 19: AWD—AFE Watchdog failure 0 = Inactive 1 = Active Bit 20: FVS—Fast Voltage Sampling 0 = Inactive 1 = Active Bit 21: CALO—Raw ADC/CC offset output 0 = Inactive 1 = Active Bit 22: SDV—Shutdown activated by voltage 0 = Inactive 1 = Active Bit 23: SLEPM—Sleep mode active by ManufacturerAccess() 0 = Inactive 1 = Active Bit 24: INIT—Initialization after full reset, cleared when SBS data calculated and available 0 = Inactive 1 = Active Bit 25: SMBLCAL—CC auto offset calibration ongoing after SBS line goes low 0 = Inactive 1 = Active Bit 26: SLEEPQMax—QMax update in Sleep mode 0 = Inactive 1 = Active Bit 27: SLEEPCC—Checking current in Sleep mode 0 = Inactive 1 = Active Bit 28: GPOD—GPOD pin status 0 = Inactive (high) 1 = Active (low) Bit 29: Reserved Bit 30: Reserved Bit 31: Reserved |
| Black Box | PF Status | 2nd Time to Next Event | U1 | 0 | 255 | 0 | Time from 2nd event to 3rd event |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|-----------|-----------------------|------|--------|--------|---------|---|
| Black Box | PF Status | 3rd PF Status 0–15 | H2 | 0x0000 | 0xFFFF | 0 | PFStatus() bit 0 to bit 15 Bit 0: CUV—Cell undervoltage 0 = Inactive 1 = Active Bit 1: COV—Cell overvoltage 0 = Inactive 1 = Active Bit 2: CUDEP—Copper Deposition 0 = Inactive 1 = Active Bit 3: Reserved Bit 4: OTCE—Overtemperature 0 = Inactive 1 = Active Bit 5: Reserved Bit 6: OTF—Overtemperature FET 0 = Inactive 1 = Active Bit 7: QIM—QMax Imbalance 0 = Inactive 1 = Active Bit 8: CB—Cell balancing 0 = Inactive 1 = Active Bit 9: IMP—Cell impedance 0 = Inactive 1 = Active Bit 10: CD—Capacity Deterioration 0 = Inactive 1 = Active Bit 11: VIMR—Voltage imbalance at Rest 0 = Inactive 1 = Active Bit 12: VIMA—Voltage imbalance at Rest 0 = Inactive 1 = Active Bit 13: Reserved Bit 14: Reserved Bit 15: Reserved |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|-----------|------------------------|------|--------|--------|---------|--|
| Black Box | PF Status | 3rd PF Status 16–32 | H2 | 0x0000 | 0xFFFF | 0 | PFStatus() bit 16 to bit 31 Bit 16: CFETF—Charge FET 0 = Inactive 1 = Active Bit 17: DFET—Discharge FET 0 = Inactive 1 = Active Bit 18: TH—Thermistor 0 = Inactive 1 = Active Bit 19: FUSE—Fuse 0 = Inactive 1 = Active Bit 20: AFER—AFE Register 0 = n/a 1 = Active Bit 21: AFEC—AFE Communication 0 = Inactive 1 = Active Bit 22: 2LVL—FUSE input indicating fuse trigger by external 2nd level protection 0 = Inactive 1 = Active Bit 23: PTC—PTC by AFE 0 = Inactive 1 = Active Bit 24: IFC—Instruction Flash Checksum 0 = n/a 1 = IF checksum failure Bit 25: OCECO—Open VCx 0 = n/a 1 = Active Bit 26: DFW—DF wearout 0 = n/a 1 = Active Bit 27: Reserved Bit 28: Reserved Bit 29: Reserved Bit 30: Reserved Bit 31: Reserved |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-----------|-----------|------------------------|------|--------|--------|---------|--|
| Black Box | PF Status | 3rd PF Status 16–32 | H2 | 0x0000 | 0xFFFF | 0 | Bit 16: SDM—Shutdown activated by ManufacturerAccess() 0 = Inactive 1 = Active Bit 17: SHIPM—Ship Mode activated with ManufacturerAccess() 0 = Inactive 1 = Active Bit 18: AUTH—Authentication ongoing 0 = Inactive 1 = Active Bit 19: AWD—AFE Watchdog failure 0 = Inactive 1 = Active Bit 20: FVS—Fast Voltage Sampling 0 = Inactive 1 = Active Bit 21: CALO—Raw ADC/CC offset output 0 = Inactive 1 = Active Bit 22: SDV—Shutdown activated by voltage 0 = Inactive 1 = Active Bit 23: SLEEPM—Sleep mode active by ManufacturerAccess() 0 = Inactive 1 = Active Bit 24: INIT—Initialization after full reset, cleared when SBS data calculated and available 0 = Inactive 1 = Active Bit 25: SMBLCAL—CC auto offset calibration ongoing after SBS line goes low 0 = Inactive 1 = Active Bit 26: SLEEPQMax—QMax update in Sleep mode 0 = Inactive 1 = Active Bit 27: SLEEPCC—Checking current in Sleep mode 0 = Inactive 1 = Active Bit 28: GPOD—GPOD pin status 0 = Inactive (high) 1 = Active (low) Bit 29: Reserved Bit 30: Reserved Bit 31: Reserved |
| Black Box | PF Status | 3rd Time to Next Event | U1 | 0 | 255 | 0 | Time since 3rd event |

12.16 Calibration

12.16.1 Voltage

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-------------|----------|--------------|------|--------|-------|---------|---------------------|
| Calibration | Voltage | Cell Scale 0 | I2 | –32768 | 32767 | 20451 | VC1–VSS Cell 0 gain |
| Calibration | Voltage | Cell Scale 1 | I2 | –32768 | 32767 | 20468 | VC2–VC1 Cell 1 gain |
| Calibration | Voltage | Cell Scale 2 | I2 | –32768 | 32767 | 20520 | VC3–VC2 Cell 2 gain |
| Calibration | Voltage | Cell Scale 3 | I2 | –32768 | 32767 | 20517 | VC4–VC3 Cell 3 gain |
| Calibration | Voltage | Pack Gain | I2 | –32768 | 32767 | 44100 | PACK–VSS gain |
| Calibration | Voltage | Battery Gain | I2 | –32768 | 32767 | 44100 | VC4–VSS gain |

12.16.2 Current

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-------------|----------|---------------|------|-----------|-----------|------------|----------------------|
| Calibration | Current | CC Gain | F4 | 1.00E–001 | 4.00E+000 | 0.9419 | Coulomb Counter Gain |
| Calibration | Current | Capacity Gain | F4 | 2.98E+004 | 1.19E+006 | 280932.625 | Capacity Gain |

12.16.3 Current Offset

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-------------|----------------|--------------------------------|------|--------|-------|---------|---|
| Calibration | Current Offset | CC Offset | I2 | –32768 | 32767 | –7204 | Coulomb Counter Offset |
| Calibration | Current Offset | Coulomb Counter Offset Samples | U2 | 0 | 65535 | 64 | Coulomb Counter Offset Samples used for averaging |
| Calibration | Current Offset | Board Offset | I2 | –32768 | 32767 | 0 | PCB board offset |

12.16.4 Temperature

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|-------------|------------------------|------|------|-----|---------|-------|--|
| Calibration | Temperature | Internal Temp Offset | I1 | –128 | 127 | 0 | 0.1°C | Internal temperature sensor reading offset |
| Calibration | Temperature | External 1 Temp Offset | I1 | –128 | 127 | 0 | 0.1°C | TS1 temperature sensor reading offset |
| Calibration | Temperature | External 2 Temp Offset | I1 | –128 | 127 | 0 | 0.1°C | TS2 temperature sensor reading offset |
| Calibration | Temperature | External 3 Temp Offset | I1 | –128 | 127 | 0 | 0.1°C | TS3 temperature sensor reading offset |
| Calibration | Temperature | External 4 Temp Offset | I1 | –128 | 127 | 0 | 0.1°C | TS4 temperature sensor reading offset |

12.16.5 Internal Temp Model

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-------------|---------------------|------------------|------|--------|-------|---------|---|
| Calibration | Internal Temp Model | Int Coeff 1 | I2 | –32768 | 32768 | 0 | Internal temperature calculation polynomial value 1 |
| Calibration | Internal Temp Model | Int Coeff 2 | I2 | –32768 | 32768 | 0 | Internal temperature calculation polynomial value 2 |
| Calibration | Internal Temp Model | Int Coeff 3 | I2 | –32768 | 32768 | –11136 | Internal temperature calculation polynomial value 3 |
| Calibration | Internal Temp Model | Int Coeff 4 | I2 | –32768 | 32768 | 5754 | Internal temperature calculation polynomial value 4 |
| Calibration | Internal Temp Model | Int Minimum AD | I2 | –32768 | 32768 | 0 | Minimum AD count used for calculation |
| Calibration | Internal Temp Model | Int Maximum Temp | I2 | –32768 | 32768 | 5754 | Maximum Temperature boundary |

12.16.6 Cell Temp Model

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-------------|-----------------|----------------|------|--------|-------|---------|--|
| Calibration | Cell Temp Model | Coefficient a1 | I2 | –32768 | 32768 | –14520 | Cell Temperature calculation polynomial a1 |
| Calibration | Cell Temp Model | Coefficient a2 | I2 | –32768 | 32768 | 23696 | Cell Temperature calculation polynomial a2 |
| Calibration | Cell Temp Model | Coefficient a3 | I2 | –32768 | 32768 | –20298 | Cell Temperature calculation polynomial a3 |
| Calibration | Cell Temp Model | Coefficient a4 | I2 | –32768 | 32768 | 28073 | Cell Temperature calculation polynomial a4 |
| Calibration | Cell Temp Model | Coefficient a5 | I2 | –32768 | 32768 | 865 | Cell Temperature calculation polynomial a5 |
| Calibration | Cell Temp Model | Coefficient b1 | I2 | –32768 | 32768 | –694 | Cell Temperature calculation polynomial b1 |
| Calibration | Cell Temp Model | Coefficient b2 | I2 | –32768 | 32768 | 1326 | Cell Temperature calculation polynomial b2 |
| Calibration | Cell Temp Model | Coefficient b3 | I2 | –32768 | 32768 | –3880 | Cell Temperature calculation polynomial b3 |
| Calibration | Cell Temp Model | Coefficient b4 | I2 | –32768 | 32768 | 5127 | Cell Temperature calculation polynomial b4 |
| Calibration | Cell Temp Model | Rc0 | I2 | –32768 | 32768 | 11703 | Resistance at 25°C |
| Calibration | Cell Temp Model | Adc0 | I2 | –32768 | 32768 | 11703 | ADC reading at 25°C |
| Calibration | Cell Temp Model | Rpad | I2 | –32768 | 32768 | 0 | Pad Resistance |
| Calibration | Cell Temp Model | Rint | I2 | –32768 | 32768 | 0 | Pull up resistor resistance |

12.16.7 FET Temp Model

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-------------|----------------|----------------|------|--------|-------|---------|---|
| Calibration | FET Temp Model | Coefficient a1 | I2 | –32768 | 32768 | –14520 | FET Temperature calculation polynomial a1 |
| Calibration | FET Temp Model | Coefficient a2 | I2 | –32768 | 32768 | 23696 | FET Temperature calculation polynomial a2 |

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-------------|----------------|----------------|------|--------|-------|---------|---|
| Calibration | FET Temp Model | Coefficient a3 | I2 | –32768 | 32768 | –20298 | FET Temperature calculation polynomial a3 |
| Calibration | FET Temp Model | Coefficient a4 | I2 | –32768 | 32768 | 28073 | FET Temperature calculation polynomial a4 |
| Calibration | FET Temp Model | Coefficient a5 | I2 | –32768 | 32768 | 865 | FET Temperature calculation polynomial a5 |
| Calibration | FET Temp Model | Coefficient b1 | I2 | –32768 | 32768 | –694 | FET Temperature calculation polynomial b1 |
| Calibration | FET Temp Model | Coefficient b2 | I2 | –32768 | 32768 | 1326 | FET Temperature calculation polynomial b2 |
| Calibration | FET Temp Model | Coefficient b3 | I2 | –32768 | 32768 | –3880 | FET Temperature calculation polynomial b3 |
| Calibration | FET Temp Model | Coefficient b4 | I2 | –32768 | 32768 | 5127 | FET Temperature calculation polynomial b4 |
| Calibration | FET Temp Model | Rc0 | I2 | –32768 | 32768 | 11703 | Resistance at 25°C |
| Calibration | FET Temp Model | Adc0 | I2 | –32768 | 32768 | 11703 | ADC reading at 25°C |
| Calibration | FET Temp Model | Rpad | I2 | –32768 | 32768 | 0 | Pad Resistance |
| Calibration | FET Temp Model | Rint | I2 | –32768 | 32768 | 0 | Pull up resistor resistance |

12.16.8 Filter

| Class | Subclass | Name | Type | Min | Max | Default | Description |
|-------------|----------|------------------------|------|-----|-----|---------|---|
| Calibration | Filter | Cell Voltage 1 | U1 | 0 | 255 | 145 | <p>Low pass filter settings for averaging, sample setting values and associated low-pass filter time constants are in Table C-2. Chosen filter settings will have an effect on protection delays. Higher filter values will cause voltages and temperature to take longer to respond to stimulus to reach threshold, for example. A filter value of 50 closely matches the behavior of previous gas gauges.</p> |
| Calibration | Filter | Cell Voltage 2 | U1 | 0 | 255 | 145 | |
| Calibration | Filter | Cell Voltage 3 | U1 | 0 | 255 | 145 | |
| Calibration | Filter | Cell Voltage 4 | U1 | 0 | 255 | 145 | |
| Calibration | Filter | Pack Voltage Out | U1 | 0 | 255 | 10 | |
| Calibration | Filter | Direct Battery Voltage | U1 | 0 | 255 | 10 | |
| Calibration | Filter | Summed Battery Voltage | U1 | 0 | 255 | 145 | |
| Calibration | Filter | Cell Temperature | U1 | 0 | 255 | 145 | |
| Calibration | Filter | FET Temperature | U1 | 0 | 255 | 145 | |

12.16.9 Current Deadband

| Class | Subclass | Name | Type | Min | Max | Default | Unit | Description |
|-------------|------------------|--------------------------|------|-----|-----|---------|------|---|
| Calibration | Current Deadband | Deadband | U1 | 0 | 255 | 3 | mA | Deadband to report 0 mA |
| Calibration | Current Deadband | Coulomb Counter Deadband | U1 | 0 | 255 | 34 | μV | Coulomb counter deadband to report 0 charge |

AFE Threshold and Delay Settings

A.1 Overload in Discharge Protection (OLD)

Table A-1. Overload in Discharge Protection Threshold (Settings:AFE State Control [RSNS] = 0)

| OLD Threshold ([RSNS] = 0) | | | |
|----------------------------|-----------|---------|-----------|
| Setting | Threshold | Setting | Threshold |
| 0x00 | 0.050 V | 0x08 | 0.130 V |
| 0x01 | 0.060 V | 0x09 | 0.140 V |
| 0x02 | 0.070 V | 0x0a | 0.150 V |
| 0x03 | 0.080 V | 0x0b | 0.160 V |
| 0x04 | 0.090 V | 0x0c | 0.170 V |
| 0x05 | 0.100 V | 0x0d | 0.180 V |
| 0x06 | 0.110 V | 0x0e | 0.190 V |
| 0x07 | 0.120 V | 0x0f | 0.200 V |

Table A-2. Overload in Discharge Protection Threshold (Settings:AFE State Control [RSNS] = 1)

| OLD Threshold ([RSNS] = 1) | | | |
|----------------------------|-----------|---------|-----------|
| Setting | Threshold | Setting | Threshold |
| 0x00 | 0.025 V | 0x08 | 0.065 V |
| 0x01 | 0.030 V | 0x09 | 0.070 V |
| 0x02 | 0.035 V | 0x0a | 0.075 V |
| 0x03 | 0.040 V | 0x0b | 0.080 V |
| 0x04 | 0.045 V | 0x0c | 0.085 V |
| 0x05 | 0.050 V | 0x0d | 0.090 V |
| 0x06 | 0.055 V | 0x0e | 0.095 V |
| 0x07 | 0.060 V | 0x0f | 0.100 V |

Table A-3. Overload in Discharge Protection Delay

| Setting | Time | Setting | Time | Setting | Time | Setting | Time |
|---------|------|---------|-------|---------|-------|---------|-------|
| 0x00 | 1 ms | 0x04 | 9 ms | 0x08 | 17 ms | 0x0c | 25 ms |
| 0x01 | 3 ms | 0x05 | 11 ms | 0x09 | 19 ms | 0x0d | 27 ms |
| 0x02 | 5 ms | 0x06 | 13 ms | 0x0a | 21 ms | 0x0e | 29 ms |
| 0x03 | 7 ms | 0x07 | 15 ms | 0x0b | 23 ms | 0x0f | 31 ms |

A.2 Short Circuit in Charge (SCC)

Table A-4. Short Circuit in Charge Threshold (Settings:AFE State Control [RSNS] = 0)⁽¹⁾

| Setting | Threshold | Setting | Threshold |
|---------|-----------|---------|-----------|
| 0x00 | −0.100 V | 0x04 | −0.300 V |
| 0x01 | −0.150 V | 0x05 | N/A |
| 0x02 | −0.200 V | 0x06 | N/A |
| 0x03 | −0.250 V | 0x07 | N/A |

⁽¹⁾ Data flash setting Protection:SCC Threshold[2:0] sets the voltage threshold.

Table A-5. Short Circuit in Charge Threshold (Settings:AFE State Control [RSNS] = 1)⁽¹⁾

| Setting | Threshold | Setting | Threshold |
|---------|-----------|---------|-----------|
| 0x00 | −0.050 V | 0x04 | −0.150 V |
| 0x01 | −0.075 V | 0x05 | −0.175 V |
| 0x02 | −0.100 V | 0x06 | −0.200 V |
| 0x03 | −0.125 V | 0x07 | −0.225 V |

⁽¹⁾ Data flash setting Protection:SCC Threshold[2:0] sets the voltage threshold.

Table A-6. Short Circuit in Charge Delay⁽¹⁾

| Setting | Time | Setting | Time | Setting | Time | Setting | Time |
|---------|--------|---------|--------|---------|--------|---------|--------|
| 0x00 | 0 μs | 0x04 | 244 μs | 0x08 | 488 μs | 0x0c | 732 μs |
| 0x01 | 61 μs | 0x05 | 305 μs | 0x09 | 549 μs | 0x0d | 793 μs |
| 0x02 | 122 μs | 0x06 | 366 μs | 0x0a | 610 μs | 0x0e | 854 μs |
| 0x03 | 183 μs | 0x07 | 427 μs | 0x0b | 671 μs | 0x0f | 915 μs |

⁽¹⁾ Data flash setting Protection:SCC Threshold[7:4] sets the delay time.

A.3 Short Circuit in Discharge (SCD1 and SCD2)

Table A-7. Short Circuit in Discharge Threshold (Settings:AFE State Control [RSNS] = 0)⁽¹⁾

| Setting | Threshold | Setting | Threshold |
|---------|-----------|---------|-----------|
| 0x00 | 0.100 V | 0x04 | 0.300 V |
| 0x01 | 0.150 V | 0x05 | 0.350 V |
| 0x02 | 0.200 V | 0x06 | 0.400 V |
| 0x03 | 0.250 V | 0x07 | 0.450 V |

⁽¹⁾ Data flash setting Protection:SCD1 and SCD2 Threshold[2:0] sets the voltage threshold.

Table A-8. Short Circuit in Discharge Threshold (Settings:AFE State Control[RSNS] = 1)⁽¹⁾

| Setting | Threshold | Setting | Threshold |
|---------|-----------|---------|-----------|
| 0x00 | 0.050 V | 0x04 | 0.150 V |
| 0x01 | 0.075 V | 0x05 | 0.175 V |
| 0x02 | 0.100 V | 0x06 | 0.200 V |

⁽¹⁾ Data flash setting Protection:SCD1 and SCD2 Threshold[2:0] sets the voltage threshold.

Table A-9. Short Circuit in Discharge 1 Delay (Settings:AFE State Control[SCDDx2] = 0)⁽¹⁾

| Setting | Time | Setting | Time | Setting | Time | Setting | Time |
|---------|------|---------|--------|---------|--------|---------|--------|
| 0x00 | 0 μs | 0x04 | 244 μs | 0x08 | 488 μs | 0x0c | 732 μs |

⁽¹⁾ Data flash setting Protection:SCD1 and SCD2 Threshold[7:4] sets the delay time.

Table A-9. Short Circuit in Discharge 1 Delay (Settings:AFE State Control[SCDDx2] = 0)⁽¹⁾
(continued)

| Setting | Time | Setting | Time | Setting | Time | Setting | Time |
|---------|-------------|---------|-------------|---------|-------------|---------|-------------|
| 0x01 | 61 μ s | 0x05 | 305 μ s | 0x09 | 549 μ s | 0x0d | 793 μ s |
| 0x02 | 122 μ s | 0x06 | 366 μ s | 0x0a | 610 μ s | 0x0e | 854 μ s |
| 0x03 | 183 μ s | 0x07 | 427 μ s | 0x0b | 671 μ s | 0x0f | 915 μ s |

Table A-10. Short Circuit in Discharge 1 Delay (Settings:AFE State Control[SCDDx2] = 1)⁽¹⁾

| Setting | Time | Setting | Time | Setting | Time | Setting | Time |
|---------|-------------|---------|-------------|---------|--------------|---------|--------------|
| 0x00 | 0 μ s | 0x04 | 488 μ s | 0x08 | 976 μ s | 0x0c | 1464 μ s |
| 0x01 | 122 μ s | 0x05 | 610 μ s | 0x09 | 1098 μ s | 0x0d | 1586 μ s |
| 0x02 | 244 μ s | 0x06 | 732 μ s | 0x0a | 1220 μ s | 0x0e | 1708 μ s |
| 0x03 | 366 μ s | 0x07 | 854 μ s | 0x0b | 1342 μ s | 0x0f | 1830 μ s |

⁽¹⁾ Data flash setting Protection:SCD1 Threshold[7:4] sets the delay time.

Table A-11. Short Circuit in Discharge 2 Delay (Settings:AFE State Control[SCDDx2] = 0)⁽¹⁾

| Setting | Time | Setting | Time | Setting | Time | Setting | Time |
|---------|------------|---------|-------------|---------|-------------|---------|-------------|
| 0x00 | 0 μ s | 0x04 | 122 μ s | 0x08 | 244 μ s | 0x0c | 366 μ s |
| 0x01 | 30 μ s | 0x05 | 152 μ s | 0x09 | 275 μ s | 0x0d | 396 μ s |
| 0x02 | 61 μ s | 0x06 | 183 μ s | 0x0a | 305 μ s | 0x0e | 426 μ s |
| 0x03 | 91 μ s | 0x07 | 213 μ s | 0x0b | 335 μ s | 0x0f | 458 μ s |

⁽¹⁾ Data flash setting Protection: SCD2 Threshold[7:4] sets the delay time.

Table A-12. Short Circuit in Discharge 2 Delay (Settings:AFE State Control[SCDDx2] = 1)⁽¹⁾

| Setting | Time | Setting | Time | Setting | Time | Setting | Time |
|---------|-------------|---------|-------------|---------|-------------|---------|-------------|
| 0x00 | 0 μ s | 0x04 | 244 μ s | 0x08 | 488 μ s | 0x0c | 732 μ s |
| 0x01 | 61 μ s | 0x05 | 305 μ s | 0x09 | 549 μ s | 0x0d | 793 μ s |
| 0x02 | 122 μ s | 0x06 | 366 μ s | 0x0a | 610 μ s | 0x0e | 854 μ s |
| 0x03 | 183 μ s | 0x07 | 427 μ s | 0x0b | 671 μ s | 0x0f | 915 μ s |

⁽¹⁾ Data flash setting Protection: SCD2 Threshold[7:4] sets the delay time.

Reading and Writing to Data Flash

Use **ManufacturerAccess()** 0x01yy and **ManufacturerInput()** 0x2f to read and right to data flash, which is a 32-byte operation. First, determine the physical address of the target data flash parameter. This information is reflected by the subclass ID and offset, available in [Table B-1](#) and [Table B-2](#).

Below is an example of updating data flash setting Protections: *CUV Recovery*

Subclass ID of Protections: *CUV Recovery* = 235

Offset of Protections: *CUV Recovery* = 3.

Data Type = I2.

1. Identify the data flash row number and byte index:
 - (a) Identify the physical address of the target parameter.
The physical address of Protections: *CUV Recovery* = Subclass ID + Offset = 238.
 - (b) Find the row number of Protections: *CUV Recovery*.
Each data flash row is 32-byte long.
Row number of Protections: *CUV Recovery* = $238 \div 32 = 7$.
 - (c) Find out which byte(s) the target parameter is resided at with the row.
Byte Index = Physical location—(row number * row length).
Byte Index for Protections: *CUV Recovery* = $238 - (7 * 32) = 14$.
Since the data type of Protections: *CUV Recovery* is I2, this means the target parameter is resided at row 7, byte index 14 and 15.
2. Read data flash parameter:
 - (a) Send the data flash row number to bq30z50-R1/55 using MAC command 0x1yy.
From step A2, the row number of *CUV Recovery* is 7.
Issue SMBus write word. cmd = 0x00, word = 0x107.
Note: the row number issue through command 0x1yy must be in Hex.
 - (b) Use **ManufacturerInput()** 0x2f to read the data flash row where the target parameter is located.
Issue SMBus block read, cmd = 0x2f, length = 32.
Note: Store the read data into a memory array, e.g. yRowdataArray(0 to 31).
 - (c) Data flash parameter Protections: *CUV Recovery* is located at yRowdataArray(14) and yRowdataArray(15).
3. Update data flash parameter.
 - (a) From step B3, update the desire value of the target data flash parameter.
 - (b) Follow step B1 to set up the row number.
 - (c) Use **ManufacturerInput()** 0x2f to write the updated yRowdataArray(0 to 31) back to the device data flash.
Issue SMBus block write, cmd = 0x2f, length = 32.
 - (d) A read verify (repeat step B1 to B3) is recommend to ensure correct data is written to the data flash.

Table B-1. bq30z50-R1 Data Flash Subclass ID and Offset (Firmware v0.33)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-------------|-------------|----------|--------|-------------------------|-----------|------------|------------|---------------|-------|
| Protections | 279 | CUV | | | | | | | |
| | | | 0 | Threshold | I2 | 0 | 32767 | 2800 | mV |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| | | | 3 | Recovery | I2 | 0 | 32767 | 3000 | mV |
| Protections | 284 | CUVC | | | | | | | |
| | | | 0 | Threshold | I2 | 0 | 32767 | 2900 | mV |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| | | | 3 | Recovery | I2 | 0 | 32767 | 3000 | mV |
| Protections | 289 | COV | | | | | | | |
| | | | 0 | Threshold Low Temp | I2 | 0 | 32767 | 4250 | mV |
| | | | 2 | Threshold Standard Temp | I2 | 0 | 32767 | 4250 | mV |
| | | | 4 | Threshold High Temp | I2 | 0 | 32767 | 4250 | mV |
| | | | 6 | Threshold Rec Temp | I2 | 0 | 32767 | 4250 | mV |
| | | | 8 | Delay | U1 | 0 | 255 | 2 | s |
| | | | 9 | Recovery Low Temp | I2 | 0 | 32767 | 4150 | mV |
| | | | 11 | Recovery Standard Temp | I2 | 0 | 32767 | 4150 | mV |
| | | | 13 | Recovery High Temp | I2 | 0 | 32767 | 4150 | mV |
| | | | 15 | Recovery Rec Temp | I2 | 0 | 32767 | 4150 | mV |
| Protections | 306 | OCC1 | | | | | | | |
| | | | 0 | Threshold | I2 | -32768 | 32767 | 6000 | mA |
| | | | 2 | Delay | U1 | 0 | 255 | 6 | s |
| Protections | 309 | OCC2 | | | | | | | |
| | | | 0 | Threshold | I2 | -32768 | 32767 | 8000 | mA |
| | | | 2 | Delay | U1 | 0 | 255 | 3 | s |
| Protections | 312 | OCC | | | | | | | |
| | | | 0 | Recovery Threshold | I2 | -32768 | 32767 | -50 | mA |
| | | | 2 | Recovery Delay | U1 | 0 | 255 | 5 | s |
| Protections | 315 | OCD1 | | | | | | | |
| | | | 0 | Threshold | I2 | -32768 | 32767 | -6000 | mA |
| | | | 2 | Delay | U1 | 0 | 255 | 6 | s |
| Protections | 318 | OCD2 | | | | | | | |
| | | | 0 | Threshold | I2 | -32768 | 32767 | -8000 | mA |
| | | | 2 | Delay | U1 | 0 | 255 | 3 | s |
| Protections | 321 | OCD | | | | | | | |
| | | | 0 | Recovery Threshold | I2 | -32768 | 32767 | 50 | mA |
| | | | 2 | Recovery Delay | U1 | 0 | 255 | 5 | s |
| Protections | 324 | OLD | | | | | | | |

Table B-1. bq30z50-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-------------|-------------|----------|--------|-------------------|-----------|------------|------------|---------------|-------|
| | | | 0 | Threshold | H1 | 0 | 0f | 09 | - |
| | | | 1 | Delay | H1 | 0 | 0f | 0f | - |
| | | | 2 | Latch Limit | U1 | 0 | 255 | 0 | - |
| | | | 3 | Counter Dec Delay | U1 | 0 | 255 | 10 | s |
| | | | 4 | Recovery | U1 | 0 | 255 | 5 | s |
| | | | 5 | Reset | U1 | 0 | 255 | 15 | s |
| Protections | 330 | SCC | | | | | | | |
| | | | 0 | Threshold | H1 | 0 | ff | 77 | - |
| | | | 1 | Latch Limit | U1 | 0 | 255 | 0 | mA |
| | | | 2 | Counter Dec Delay | U1 | 0 | 255 | 10 | s |
| | | | 3 | Recovery | U1 | 0 | 255 | 5 | s |
| | | | 4 | Reset | U1 | 0 | 255 | 15 | s |
| Protections | 335 | SCD1 | | | | | | | |
| | | | 0 | Threshold | H1 | 0 | ff | 77 | - |
| Protections | 336 | SCD2 | | | | | | | |
| | | | 0 | Threshold | H1 | 0 | ff | e7 | - |
| Protections | 337 | SCD | | | | | | | |
| | | | 0 | Latch Limit | U1 | 0 | 255 | 0 | mA |
| | | | 1 | Counter Dec Delay | U1 | 0 | 255 | 10 | s |
| | | | 2 | Recovery | U1 | 0 | 255 | 5 | s |
| | | | 3 | Reset | U1 | 0 | 255 | 15 | s |
| Protections | 341 | OTC | | | | | | | |
| | | | 0 | Threshold | I2 | -400 | 1500 | 550 | 1°C |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| | | | 3 | Recovery | I2 | -400 | 1500 | 500 | 1°C |
| Protections | 346 | OTD | | | | | | | |
| | | | 0 | Threshold | I2 | -400 | 1500 | 600 | 1°C |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| | | | 3 | Recovery | I2 | -400 | 1500 | 550 | 1°C |
| Protections | 351 | OTF | | | | | | | |
| | | | 0 | Threshold | I2 | -400 | 1500 | 800 | 1°C |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| | | | 3 | Recovery | I2 | -400 | 1500 | 650 | 1°C |
| Protections | 356 | HWD | | | | | | | |
| | | | 0 | Delay | U1 | 0 | 255 | 10 | s |
| Protections | 357 | PTO | | | | | | | |
| | | | 0 | Charge Threshold | I2 | -32768 | 32767 | 2000 | mA |
| | | | 2 | Suspend Threshold | I2 | -32768 | 32767 | 1800 | mA |
| | | | 4 | Delay | U2 | 0 | 65535 | 1800 | s |
| | | | 6 | Reset | I2 | 0 | 32767 | 2 | mAh |
| Protections | 365 | CTO | | | | | | | |
| | | | 0 | Charge Threshold | I2 | -32768 | 32767 | 2500 | mA |

Table B-1. bq30z50-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|----------------|-------------|----------|--------|-------------------|-----------|------------|------------|---------------|---------|
| | | | 2 | Suspend Threshold | I2 | –32768 | 32767 | 2000 | mA |
| | | | 4 | Delay | U2 | 0 | 65535 | 54000 | s |
| | | | 6 | Reset | I2 | 0 | 32767 | 2 | mAh |
| Protections | 373 | OC | | | | | | | |
| | | | 0 | Threshold | I2 | –32768 | 32767 | 300 | mAh |
| | | | 2 | Recovery | I2 | –32768 | 32767 | 2 | mAh |
| | | | 4 | RSOC Recovery | U1 | 0 | 100 | 90 | % |
| Protections | 378 | CHGV | | | | | | | |
| | | | 0 | Threshold | I2 | –32768 | 32767 | 500 | mV |
| | | | 2 | Delay | U1 | 0 | 255 | 30 | s |
| | | | 3 | Recovery | I2 | –32768 | 32767 | –500 | mV |
| Protections | 383 | CHGC | | | | | | | |
| | | | 0 | Threshold | I2 | –32768 | 32767 | 500 | mA |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| | | | 3 | Recovery | I2 | –32768 | 32767 | 100 | mA |
| Permanent Fail | 388 | CUV | | | | | | | |
| | | | 0 | Threshold | I2 | 0 | 32767 | 2500 | mV |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| Permanent Fail | 391 | COV | | | | | | | |
| | | | 0 | Threshold | I2 | 0 | 32767 | 4400 | mV |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| Permanent Fail | 394 | CUDEP | | | | | | | |
| | | | 0 | Threshold | I2 | 0 | 32767 | 2500 | mV |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| Permanent Fail | 397 | OTCE | | | | | | | |
| | | | 0 | Threshold | I2 | –400 | 1500 | 650 | 1°C |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| Permanent Fail | 400 | OTF | | | | | | | |
| | | | 0 | Threshold | I2 | –400 | 1500 | 1000 | 1°C |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| Permanent Fail | 403 | QIM | | | | | | | |
| | | | 0 | Delta Threshold | I2 | 0 | 32767 | 500 | mAh |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | updates |
| Permanent Fail | 406 | CB | | | | | | | |
| | | | 0 | Max Threshold | I2 | 0 | 32767 | 120 | h |
| | | | 2 | Delta Threshold | U1 | 0 | 255 | 20 | h |
| | | | 3 | Delay | U1 | 0 | 255 | 2 | cycles |
| Permanent Fail | 410 | VIMR | | | | | | | |

Table B-1. bq30z50-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|----------------|-------------|----------|--------|------------------|-----------|------------|------------|---------------|--------|
| | | | 0 | Check Voltage | I2 | 0 | 5000 | 3600 | mV |
| | | | 2 | Check Current | I2 | 0 | 32767 | 10 | mA |
| | | | 4 | Delta Threshold | I2 | 0 | 5000 | 200 | mV |
| | | | 6 | Delta Delay | U1 | 0 | 255 | 2 | s |
| | | | 7 | Duration | U2 | 0 | 65535 | 100 | s |
| Permanent Fail | 419 | VIMA | | | | | | | |
| | | | 0 | Check Voltage | I2 | 0 | 5000 | 3600 | mV |
| | | | 2 | Check Current | I2 | 0 | 32767 | 10 | mA |
| | | | 4 | Delta Threshold | I2 | 0 | 5000 | 300 | mV |
| | | | 6 | Delay | U1 | 0 | 255 | 2 | s |
| Permanent Fail | 426 | IMP | | | | | | | |
| | | | 0 | Delta Threshold | I2 | 0 | 32767 | 300 | % |
| | | | 2 | Max Threshold | I2 | 0 | 32767 | 400 | % |
| | | | 4 | Ra Update Counts | U1 | 0 | 255 | 2 | counts |
| Permanent Fail | 431 | CD | | | | | | | |
| | | | 0 | Threshold | I2 | 0 | 32767 | 4200 | mAh |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | cycles |
| Permanent Fail | 434 | CFETF | | | | | | | |
| | | | 0 | OFF Threshold | I2 | 0 | 500 | 5 | mA |
| | | | 2 | OFF Delay | U1 | 0 | 255 | 2 | s |
| Permanent Fail | 437 | DFET | | | | | | | |
| | | | 0 | OFF Threshold | I2 | -500 | 0 | -5 | mA |
| | | | 2 | OFF Delay | U1 | 0 | 255 | 2 | s |
| Permanent Fail | 440 | TH | | | | | | | |
| | | | 4 | ADC Delay | U1 | 0 | 255 | 10 | s |
| Permanent Fail | 445 | FUSE | | | | | | | |
| | | | 0 | Threshold | I2 | 0 | 255 | 5 | mA |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| Permanent Fail | 448 | AFER | | | | | | | |
| | | | 0 | Threshold | U1 | 0 | 255 | 100 | - |
| | | | 1 | Delay Period | U1 | 0 | 255 | 2 | s |
| | | | 2 | Compare Period | U1 | 0 | 255 | 5 | s |

Table B-1. bq30z50-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|---------------------------|-------------|------------------------|--------|-----------------|-----------|------------|------------|---------------|-------|
| Permanent Fail | 451 | AFEC | | | | | | | |
| | | | 0 | Threshold | U1 | 0 | 255 | 100 | - |
| | | | 1 | Delay Period | U1 | 0 | 255 | 5 | s |
| Permanent Fail | 453 | 2LVL | | | | | | | |
| | | | 0 | Delay | U1 | 0 | 255 | 2 | s |
| Permanent Fail | 454 | OCECO | | | | | | | |
| | | | 0 | Threshold | I2 | 0 | 32767 | 5000 | mV |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| Advanced Charge Algorithm | 111 | Temperature Ranges | | | | | | | |
| | | | 0 | T1 Temp | I1 | -128 | 127 | 0 | °C |
| | | | 1 | T2 Temp | I1 | -128 | 127 | 12 | °C |
| | | | 2 | T5 Temp | I1 | -128 | 127 | 20 | °C |
| | | | 3 | T6 Temp | I1 | -128 | 127 | 25 | °C |
| | | | 4 | T3 Temp | I1 | -128 | 127 | 30 | °C |
| | | | 5 | T4 Temp | I1 | -128 | 127 | 55 | °C |
| | | | 6 | Hysteresis Temp | I1 | -128 | 127 | 0 | °C |
| Advanced Charge Algorithm | 118 | Low Temp Charging | | | | | | | |
| | | | 0 | Voltage | I2 | 0 | 32767 | 3000 | mV |
| | | | 2 | Current Low | I2 | 0 | 32767 | 132 | mA |
| | | | 4 | Current Med | I2 | 0 | 32767 | 352 | mA |
| | | | 6 | Current High | I2 | 0 | 32767 | 264 | mA |
| Advanced Charge Algorithm | 126 | Standard Temp Charging | | | | | | | |
| | | | 0 | Voltage | I2 | 0 | 32767 | 4200 | mV |
| | | | 2 | Current Low | I2 | 0 | 32767 | 1980 | mA |
| | | | 4 | Current Med | I2 | 0 | 32767 | 4004 | mA |
| | | | 6 | Current High | I2 | 0 | 32767 | 2992 | mA |
| Advanced Charge Algorithm | 134 | High Temp Charging | | | | | | | |
| | | | 0 | Voltage | I2 | 0 | 32767 | 4000 | mV |
| | | | 2 | Current Low | I2 | 0 | 32767 | 1012 | mA |
| | | | 4 | Current Med | I2 | 0 | 32767 | 1980 | mA |
| | | | 6 | Current High | I2 | 0 | 32767 | 1496 | mA |
| Advanced Charge Algorithm | 142 | Rec Temp Charging | | | | | | | |
| | | | 0 | Voltage | I2 | 0 | 32767 | 4100 | mV |
| | | | 2 | Current Low | I2 | 0 | 32767 | 2508 | mA |
| | | | 4 | Current Med | I2 | 0 | 32767 | 4488 | mA |
| | | | 6 | Current High | I2 | 0 | 32767 | 3520 | mA |

Table B-1. bq30z50-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|---------------------------|-------------|--------------------------|--------|-----------------------------|-----------|------------|------------|---------------|-------|
| Advanced Charge Algorithm | 150 | Pre-Charging | | | | | | | |
| | | | 0 | Current | I2 | 0 | 32767 | 88 | mA |
| Advanced Charge Algorithm | 152 | Maintenance Charging | | | | | | | |
| | | | 0 | Current | I2 | 0 | 32767 | 44 | mA |
| Advanced Charge Algorithm | 154 | Voltage Range | | | | | | | |
| | | | 0 | Charging Voltage Low | I2 | 0 | 32767 | 2500 | mV |
| | | | 2 | Charging Voltage Med | I2 | 0 | 32767 | 3600 | mV |
| | | | 4 | Charging Voltage High | I2 | 0 | 32767 | 4000 | mV |
| | | | 6 | Charging Voltage Hysteresis | U1 | 0 | 255 | 0 | mV |
| Advanced Charge Algorithm | 161 | Termination Config | | | | | | | |
| | | | 0 | Charge Term Taper Current | I2 | 0 | 32767 | 250 | mA |
| | | | 4 | Charge Term Voltage | I2 | 0 | 32767 | 75 | mV |
| Advanced Charge Algorithm | 170 | Cell Balancing Config | | | | | | | |
| | | | 0 | Bal Time/mAh Cell 0 | U2 | 0 | 65535 | 367 | s/mAh |
| | | | 2 | Bal Time/mAh Cell 1–3 | U2 | 0 | 65535 | 514 | s/mAh |
| | | | 4 | Min Start Balance Delta | U1 | 0 | 255 | 3 | mV |
| | | | 5 | Relax Balance Interval | U4 | 0 | 4294967295 | 18000 | s |
| | | | 9 | Min Rsoc for Balancing | U1 | 0 | 100 | 80 | % |
| Advanced Charge Algorithm | 180 | Charging Rate of Change | | | | | | | |
| | | | 0 | Current Rate | U1 | 1 | 255 | 1 | steps |
| | | | 1 | Voltage Rate | U1 | 1 | 255 | 1 | steps |
| Advanced Charge Algorithm | 182 | Charge Loss Compensation | | | | | | | |
| | | | 0 | CCC Current Threshold | I2 | 0 | 32767 | 3520 | mA |
| | | | 2 | CCC Voltage Threshold | I2 | 0 | 32767 | 4200 | mV |

Table B-1. bq30z50-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-------------------|-------------|-------------------|--------|---------------------------|-----------|------------|------------|--|-------|
| System Data | 640 | Manufacturer Data | | | | | | | |
| | | | 0 | Manufacturer Info | S33 | x | x | abcdefghijklm nopqrstuvwxyz 012345 | - |
| System Data | 673 | Integrity | | | | | | | |
| | | | 4 | Data Flash Checksum | H2 | 0 | ffff | 0 | - |
| SBS Configuration | 679 | Data | | | | | | | |
| | | | 0 | Remaining AH Cap. Alarm | I2 | 0 | 32767 | 300 | mAh |
| | | | 2 | Remaining WH Cap. Alarm | I2 | 0 | 32767 | 432 | cWh |
| | | | 4 | Remaining Time Alarm | U2 | 0 | 65535 | 10 | min |
| | | | 6 | Initial Battery Mode | H2 | 0 | ffff | 81 | - |
| | | | 8 | Design Voltage | I2 | 0 | 32767 | 14400 | mV |
| | | | 10 | Specification Information | H2 | 0 | ffff | 31 | - |
| | | | 12 | Manufacture Date | U2 | 0 | 65535 | 0 | date |
| | | | 14 | Serial Number | H2 | 0 | ffff | 1 | - |
| | | | 16 | Cycle Count | U2 | 0 | 65535 | 0 | - |
| | | | 18 | Cycle Count Percentage | U1 | 0 | 100 | 90 | % |
| | | | 19 | Max Error Limit | U1 | 0 | 100 | 100 | % |
| | | | 20 | Design Capacity mAh | I2 | 0 | 32767 | 4400 | mAh |
| | | | 22 | Design Capacity cWh | I2 | 0 | 32767 | 6336 | cWh |
| | | | 24 | Manufacturer Name | S21 | x | x | Texas Instruments | - |
| | | | 45 | Device Name | S21 | x | x | bq30z50-R1 | - |
| | | | 66 | Device Chemistry | S5 | x | x | LION | - |
| SBS Configuration | 750 | FD | | | | | | | |
| | | | 0 | Set Voltage Threshold | I2 | 0 | 5000 | 3000 | mV |
| | | | 2 | Clear Voltage Threshold | I2 | 0 | 5000 | 3100 | mV |
| | | | 4 | Set % RSOC Threshold | U1 | 0 | 100 | 0 | % |
| | | | 5 | Clear % RSOC Threshold | U1 | 0 | 100 | 5 | % |
| SBS Configuration | 756 | FC | | | | | | | |

Table B-1. bq30z50-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-------------------|-------------|-----------|--------|-------------------------|-----------|------------|------------|---------------|-------|
| | | | 0 | Set Voltage Threshold | I2 | 0 | 5000 | 4200 | mV |
| | | | 2 | Clear Voltage Threshold | I2 | 0 | 5000 | 4100 | mV |
| | | | 4 | Set % RSOC Threshold | U1 | 0 | 100 | 100 | % |
| | | | 5 | Clear % RSOC Threshold | U1 | 0 | 100 | 95 | % |
| SBS Configuration | 762 | TDA | | | | | | | |
| | | | 0 | Set Voltage Threshold | I2 | 0 | 5000 | 3200 | mV |
| | | | 2 | Clear Voltage Threshold | I2 | 0 | 5000 | 3300 | mV |
| | | | 4 | Set % RSOC Threshold | U1 | 0 | 100 | 10 | % |
| | | | 5 | Clear % RSOC Threshold | U1 | 0 | 100 | 15 | % |
| SBS Configuration | 768 | TCA | | | | | | | |
| | | | 0 | Set Voltage Threshold | I2 | 0 | 5000 | 4200 | mV |
| | | | 2 | Clear Voltage Threshold | I2 | 0 | 5000 | 4100 | mV |
| | | | 4 | Set % RSOC Threshold | U1 | 0 | 100 | 100 | % |
| | | | 5 | Clear % RSOC Threshold | U1 | 0 | 100 | 95 | % |
| SBS Configuration | 774 | Max Error | | | | | | | |
| | | | 3 | Time Cycle Equivalent | U1 | 0 | 255 | 12 | h |
| | | | 4 | Cycle Delta | U1 | 0 | 255 | 5 | % |
| Lifetimes | 512 | Voltage | | | | | | | |
| | | | 0 | Max Cell Voltage 0 | U1 | 0 | 255 | 0 | mV |
| | | | 1 | Max Cell Voltage 1 | U1 | 0 | 255 | 0 | mV |
| | | | 2 | Max Cell Voltage 2 | U1 | 0 | 255 | 0 | mV |
| | | | 3 | Max Cell Voltage 3 | U1 | 0 | 255 | 0 | mV |
| | | | 4 | Min Cell Voltage 0 | U1 | 0 | 255 | 255 | mV |
| | | | 5 | Min Cell Voltage 1 | U1 | 0 | 255 | 255 | mV |
| | | | 6 | Min Cell Voltage 2 | U1 | 0 | 255 | 255 | mV |
| | | | 7 | Min Cell Voltage 3 | U1 | 0 | 255 | 255 | mV |
| | | | 8 | Max Delta Cell Voltage | U1 | 0 | 255 | 0 | mV |

Table B-1. bq30z50-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-----------|-------------|---------------|--------|-----------------------|-----------|------------|------------|---------------|--------|
| Lifetimes | 521 | Current | | | | | | | |
| | | | 0 | Max Charge Current | U1 | 0 | 255 | 0 | mA |
| | | | 1 | Max Discharge Current | U1 | 0 | 255 | 0 | mA |
| | | | 2 | Max Avg Dsg Current | U1 | 0 | 255 | 0 | mA |
| | | | 3 | Max Avg Dsg Power | U1 | 0 | 255 | 0 | W |
| Lifetimes | 525 | Safety Events | | | | | | | |
| | | | 0 | No Of Cov Events | U1 | 0 | 255 | 0 | events |
| | | | 1 | Last Cov Event | U1 | 0 | 255 | 0 | cycles |
| | | | 2 | No Of Cuv Events | U1 | 0 | 255 | 0 | events |
| | | | 3 | Last Cuv Event | U1 | 0 | 255 | 0 | cycles |
| | | | 4 | No Of Ocd1 Events | U1 | 0 | 255 | 0 | events |
| | | | 5 | Last Ocd1 Event | U1 | 0 | 255 | 0 | cycles |
| | | | 6 | No Of Ocd2 Events | U1 | 0 | 255 | 0 | events |
| | | | 7 | Last Ocd2 Event | U1 | 0 | 255 | 0 | cycles |
| | | | 8 | No Of Occ1 Events | U1 | 0 | 255 | 0 | events |
| | | | 9 | Last Occ1 Event | U1 | 0 | 255 | 0 | cycles |
| | | | 10 | No Of Occ2 Events | U1 | 0 | 255 | 0 | events |
| | | | 11 | Last Occ2 Event | U1 | 0 | 255 | 0 | cycles |
| | | | 12 | No Of Old Events | U1 | 0 | 255 | 0 | events |
| | | | 13 | Last Old Event | U1 | 0 | 255 | 0 | cycles |
| | | | 14 | No Of Scd Events | U1 | 0 | 255 | 0 | events |
| | | | 15 | Last Scd Event | U1 | 0 | 255 | 0 | cycles |
| | | | 16 | No Of Scc Events | U1 | 0 | 255 | 0 | events |
| | | | 17 | Last Scc Event | U1 | 0 | 255 | 0 | cycles |
| | | | 18 | No Of Otc Events | U1 | 0 | 255 | 0 | events |
| | | | 19 | Last Otc Event | U1 | 0 | 255 | 0 | cycles |
| | | | 20 | No Of Otd Events | U1 | 0 | 255 | 0 | events |

Table B-1. bq30z50-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-----------|-------------|-----------------|--------|------------------------|-----------|------------|------------|---------------|--------|
| | | | 21 | Last Otd Event | U1 | 0 | 255 | 0 | cycles |
| | | | 22 | No Of Otf Events | U1 | 0 | 255 | 0 | events |
| | | | 23 | Last Otf Event | U1 | 0 | 255 | 0 | cycles |
| Lifetimes | 549 | Charging Events | | | | | | | |
| | | | 0 | No Valid Charge Term | U1 | 0 | 255 | 0 | events |
| | | | 1 | Last Valid Charge Term | U1 | 0 | 255 | 0 | cycles |
| Lifetimes | 551 | Gauging Events | | | | | | | |
| | | | 0 | No Of Qmax Updates | U1 | 0 | 255 | 0 | events |
| | | | 1 | Last Qmax Update | U1 | 0 | 255 | 0 | cycles |
| | | | 2 | No Of Ra Updates | U1 | 0 | 255 | 0 | events |
| | | | 3 | Last Ra Update | U1 | 0 | 255 | 0 | cycles |
| | | | 4 | No Of Ra Disable | U1 | 0 | 255 | 0 | events |
| | | | 5 | Last Ra Disable | U1 | 0 | 255 | 0 | cycles |
| Lifetimes | 557 | Power Events | | | | | | | |
| | | | 0 | No Of Shutdowns | U1 | 0 | 255 | 0 | events |
| Lifetimes | 561 | Cell Balancing | | | | | | | |
| | | | 0 | Cb Time Cell 0 | U1 | 0 | 255 | 0 | h |
| | | | 1 | Cb Time Cell 1 | U1 | 0 | 255 | 0 | h |
| | | | 2 | Cb Time Cell 2 | U1 | 0 | 255 | 0 | h |
| | | | 3 | Cb Time Cell 3 | U1 | 0 | 255 | 0 | h |
| Lifetimes | 565 | Temperature | | | | | | | |
| | | | 0 | Max Temp Cell | I1 | -128 | 127 | -128 | °C |
| | | | 1 | Min Temp Cell | I1 | -128 | 127 | 127 | °C |
| | | | 2 | Max Delta Cell Temp | I1 | -128 | 127 | 0 | °C |
| | | | 3 | Max Temp Int Sensor | I1 | -128 | 127 | -128 | °C |
| | | | 4 | Min Temp Int Sensor | I1 | -128 | 127 | 127 | °C |
| | | | 5 | Max Temp Fet | I1 | -128 | 127 | -128 | °C |
| Lifetimes | 571 | Time | | | | | | | |

Table B-1. bq30z50-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|----------|-------------|-------------------|--------|---------------------------|-----------|------------|------------|---------------|-------|
| | | | 0 | Total Fw Runtime | U2 | 0 | 65535 | 0 | h |
| | | | 2 | Time Spent In UT | U2 | 0 | 65535 | 0 | h |
| | | | 4 | Time Spent In LT | U2 | 0 | 65535 | 0 | h |
| | | | 6 | Time Spent In STL | U2 | 0 | 65535 | 0 | h |
| | | | 8 | Time Spent In RT | U2 | 0 | 65535 | 0 | h |
| | | | 10 | Time Spent In STH | U2 | 0 | 65535 | 0 | h |
| | | | 12 | Time Spent In HT | U2 | 0 | 65535 | 0 | h |
| | | | 14 | Time Spent In OT | U2 | 0 | 65535 | 0 | h |
| Settings | 187 | Fuse | | | | | | | |
| | | | 0 | PF Fuse 0–15 | H2 | 0 | ffff | 0 | - |
| | | | 2 | PF Fuse 16–31 | H2 | 0 | ffff | 0 | - |
| | | | 4 | Min Blow Fuse Voltage | I2 | 0 | 65535 | 8000 | mV |
| Settings | 193 | Manufacturing | | | | | | | |
| | | | 0 | Manufacturing Status | H2 | 0 | ffff | 8000 | - |
| Settings | 195 | Protection | | | | | | | |
| | | | 0 | Enabled Protections 0–15 | H2 | 0 | ffff | ffff | - |
| | | | 2 | Enabled Protections 16–31 | H2 | 0 | ffff | ffff | - |
| Settings | 199 | Permanent Failure | | | | | | | |
| | | | 0 | Enabled PF 0–15 | H2 | 0 | ffff | ffff | - |
| | | | 2 | Enabled PF 16–31 | H2 | 0 | ffff | ffff | - |
| Settings | 203 | Configuration | | | | | | | |
| | | | 0 | Protection Configuration | H1 | 0 | ff | 01 | - |
| | | | 1 | Temperature Configuration | H2 | 0 | ffff | 0087 | - |
| | | | 3 | LED Configuration | H2 | 0 | ffff | 00d0 | - |
| | | | 5 | Charging Configuration | H1 | 0 | ff | 0 | - |
| | | | 6 | System Configuration | H2 | 0 | 1ff | 32 | - |
| | | | 8 | Gauging Configuration | H2 | 0 | fff | 1fda | - |

Table B-1. bq30z50-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-------------|-------------|--------------------|--------|---------------------------|-----------|------------|------------|---------------|-------|
| | | | 10 | Sbs Configuration | H1 | 0 | ff | 20 | - |
| | | | 11 | Sbs Data Config. 0–15 | H2 | 0 | 0fff | 0caf | - |
| | | | 13 | Sbs Data Config. 16–23 | H1 | 0 | ff | ff | - |
| Settings | 217 | AFE | | | | | | | |
| | | | 1 | AFE State Control | H1 | 0 | ff | 0 | - |
| Power | 232 | Power | | | | | | | |
| | | | 0 | Valid Update Voltage | I2 | 0 | 32767 | 7500 | mV |
| Power | 234 | Shutdown | | | | | | | |
| | | | 0 | Shutdown Voltage | I2 | 0 | 32767 | 1750 | mV |
| | | | 2 | Shutdown Time | U1 | 0 | 255 | 10 | s |
| | | | 3 | Charger Present Threshold | I2 | 0 | 32767 | 3000 | mV |
| Power | 239 | Sleep | | | | | | | |
| | | | 0 | Sleep Current | I2 | 0 | 32767 | 10 | mA |
| | | | 7 | Voltage Time | U1 | 0 | 255 | 5 | s |
| | | | 8 | Current Time | U1 | 0 | 255 | 20 | s |
| | | | 9 | Wake | H1 | 0 | ff | 0 | - |
| Power | 249 | Ship | | | | | | | |
| | | | 0 | Delay | U1 | 0 | 255 | 5 | s |
| | | | 1 | Current | I2 | –250 | 250 | 10 | mA |
| Gas Gauging | 252 | Current Thresholds | | | | | | | |
| | | | 0 | Dsg Current Threshold | I2 | –32768 | 32767 | 100 | mA |
| | | | 2 | Chg Current Threshold | I2 | –32768 | 32767 | 50 | mA |
| | | | 4 | Quit Current | I2 | 0 | 32767 | 10 | mA |
| Gas Gauging | 888 | State | | | | | | | |
| | | | 0 | Qmax Cell 0 | I2 | 0 | 32767 | 4400 | mAh |
| | | | 2 | Qmax Cell 1 | I2 | 0 | 32767 | 4400 | mAh |
| | | | 4 | Qmax Cell 2 | I2 | 0 | 32767 | 4400 | mAh |
| | | | 6 | Qmax Cell 3 | I2 | 0 | 32767 | 4400 | mAh |
| | | | 8 | Qmax Pack | I2 | 0 | 32767 | 4400 | mAh |
| | | | 12 | Update Status | H1 | 0 | ff | 0 | - |
| | | | 13 | Cell 0 Chg Voltage at EoC | I2 | 0 | 32767 | 4200 | mV |
| | | | 15 | Cell 1 Chg Voltage at EoC | I2 | 0 | 32767 | 4200 | mV |
| | | | 17 | Cell 2 Chg Voltage at EoC | I2 | 0 | 32767 | 4200 | mV |

Table B-1. bq30z50-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-------------|-------------|------------|--------|-----------------------------|-----------|------------|------------|---------------|--------|
| | | | 19 | Cell 3 Chg Voltage at EoC | I2 | 0 | 32767 | 4200 | mV |
| | | | 21 | Current at EoC | I2 | 0 | 32767 | 250 | mA |
| | | | 23 | Avg I Last Run | I2 | –32768 | 32767 | –2000 | mA |
| | | | 25 | Avg P Last Run | I2 | –32768 | 32767 | –3022 | cW |
| | | | 27 | Delta Voltage | I2 | –32768 | 32767 | 0 | mV |
| | | | 33 | Max Avg I Last Run | I2 | –32768 | 32767 | –2000 | mA |
| | | | 35 | Max Avg P Last Run | I2 | –32768 | 32767 | –3022 | cW |
| Gas Gauging | 925 | IT Cfg | | | | | | | |
| | | | 0 | Load Select | U1 | 0 | 255 | 7 | — |
| | | | 1 | Load Mode | U1 | 0 | 255 | 0 | — |
| | | | 16 | Ra Filter | U2 | 0 | 999 | 500 | % |
| | | | 19 | Ra Max Delta | U1 | 0 | 255 | 15 | % |
| | | | 21 | Design Resistance | I2 | 1 | 32767 | 42 | mΩ |
| | | | 23 | Reference Grid | U1 | 0 | 14 | 4 | — |
| | | | 24 | Resistance Parameter Filter | U2 | 1 | 65534 | 65142 | — |
| | | | 62 | Term Voltage | I2 | 0 | 32767 | 9000 | mV |
| | | | 64 | Term Voltage Delta | I2 | 0 | 32767 | 300 | mV |
| | | | 81 | User Rate-mA | I2 | –9000 | 0 | 0 | mA |
| | | | 83 | User Rate-cW | I2 | –32768 | 0 | 0 | cW |
| | | | 85 | Reserve Cap-mAh | I2 | 0 | 9000 | 0 | mAh |
| | | | 87 | Reserve Cap-cWh | I2 | 0 | 32000 | 0 | cWh |
| | | | 93 | Remcap Smoothing Filter | U1 | 0 | 255 | 250 | — |
| | | | 94 | Fast Scale Start SOC | U1 | 0 | 100 | 10 | % |
| LED Support | 260 | LED Config | | | | | | | |
| | | | 0 | LED Flash Period | U2 | 0 | 65535 | 2048 | 488 μs |
| | | | 2 | LED Blink Period | U2 | 0 | 65535 | 4096 | 488 μs |
| | | | 4 | LED Delay | U2 | 0 | 65535 | 400 | 488 μs |
| | | | 6 | LED Hold Time | U1 | 0 | 15 | 16 | s |
| | | | 7 | CHG Flash Alarm | I1 | 0 | 100 | 10 | % |
| | | | 8 | CHG Thresh 1 | I1 | 0 | 100 | 0 | % |

Table B-1. bq30z50-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|----------|-------------|----------|--------|-----------------|-----------|------------|------------|---------------|----------------------|
| | | | 9 | CHG Thresh 2 | I1 | 0 | 100 | 20 | % |
| | | | 10 | CHG Thresh 3 | I1 | 0 | 100 | 40 | % |
| | | | 11 | CHG Thresh 4 | I1 | 0 | 100 | 60 | % |
| | | | 12 | CHG Thresh 5 | I1 | 0 | 100 | 80 | % |
| | | | 13 | DSG Flash Alarm | I1 | 0 | 100 | 10 | % |
| | | | 14 | DSG Thresh 1 | I1 | 0 | 100 | 0 | % |
| | | | 15 | DSG Thresh 2 | I1 | 0 | 100 | 20 | % |
| | | | 16 | DSG Thresh 3 | I1 | 0 | 100 | 40 | % |
| | | | 17 | DSG Thresh 4 | I1 | 0 | 100 | 60 | % |
| | | | 18 | DSG Thresh 5 | I1 | 0 | 100 | 80 | % |
| Ra Table | 1280 | R_a0 | | | | | | | |
| | | | 0 | Cell0 R_a flag | H2 | 0 | ffff | ff55 | - |
| | | | 2 | Cell0 R_a 0 | I2 | 0 | 32767 | 182 | 2 [^] -10 Ω |
| | | | 4 | Cell0 R_a 1 | I2 | 0 | 32767 | 177 | 2 [^] -10 Ω |
| | | | 6 | Cell0 R_a 2 | I2 | 0 | 32767 | 175 | 2 [^] -10 Ω |
| | | | 8 | Cell0 R_a 3 | I2 | 0 | 32767 | 167 | 2 [^] -10 Ω |
| | | | 10 | Cell0 R_a 4 | I2 | 0 | 327672 | 166 | 2 [^] -10 Ω |
| | | | 12 | Cell0 R_a 5 | I2 | 0 | 32767 | 182 | 2 [^] -10 Ω |
| | | | 14 | Cell0 R_a 6 | I2 | 0 | 32767 | 194 | 2 [^] -10 Ω |
| | | | 16 | Cell0 R_a 7 | I2 | 0 | 32767 | 203 | 2 [^] -10 Ω |
| | | | 18 | Cell0 R_a 8 | I2 | 0 | 32767 | 213 | 2 [^] -10 Ω |
| | | | 20 | Cell0 R_a 9 | I2 | 0 | 32767 | 223 | 2 [^] -10 Ω |
| | | | 22 | Cell0 R_a 10 | I2 | 0 | 32767 | 233 | 2 [^] -10 Ω |
| | | | 24 | Cell0 R_a 11 | I2 | 0 | 32767 | 241 | 2 [^] -10 Ω |
| | | | 26 | Cell0 R_a 12 | I2 | 0 | 32767 | 250 | 2 [^] -10 Ω |
| | | | 28 | Cell0 R_a 13 | I2 | 0 | 32767 | 254 | 2 [^] -10 Ω |
| | | | 30 | Cell0 R_a 14 | I2 | 0 | 32767 | 1500 | 2 [^] -10 Ω |
| Ra Table | 1344 | R_a1 | | | | | | | |
| | | | 0 | Cell1 R_a flag | H2 | 0 | ffff | ff55 | - |
| | | | 2 | Cell1 R_a 0 | I2 | 0 | 32767 | 163 | 2 [^] -10 Ω |
| | | | 4 | Cell1 R_a 1 | I2 | 0 | 32767 | 151 | 2 [^] -10 Ω |
| | | | 6 | Cell1 R_a 2 | I2 | 0 | 32767 | 152 | 2 [^] -10 Ω |
| | | | 8 | Cell1 R_a 3 | I2 | 0 | 32767 | 143 | 2 [^] -10 Ω |
| | | | 10 | Cell1 R_a 4 | I2 | 0 | 32767 | 145 | 2 [^] -10 Ω |
| | | | 12 | Cell1 R_a 5 | I2 | 0 | 32767 | 162 | 2 [^] -10 Ω |
| | | | 14 | Cell1 R_a 6 | I2 | 0 | 32767 | 178 | 2 [^] -10 Ω |
| | | | 16 | Cell1 R_a 7 | I2 | 0 | 32767 | 188 | 2 [^] -10 Ω |
| | | | 18 | Cell1 R_a 8 | I2 | 0 | 32767 | 200 | 2 [^] -10 Ω |

Table B-1. bq30z50-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|----------|-------------|----------|--------|-----------------|-----------|------------|------------|---------------|----------------------|
| | | | 20 | Cell1 R_a 9 | I2 | 0 | 32767 | 206 | 2 [^] -10 Ω |
| | | | 22 | Cell1 R_a 10 | I2 | 0 | 32767 | 216 | 2 [^] -10 Ω |
| | | | 24 | Cell1 R_a 11 | I2 | 0 | 32767 | 230 | 2 [^] -10 Ω |
| | | | 26 | Cell1 R_a 12 | I2 | 0 | 32767 | 240 | 2 [^] -10 Ω |
| | | | 28 | Cell1 R_a 13 | I2 | 0 | 32767 | 254 | 2 [^] -10 Ω |
| | | | 30 | Cell1 R_a 14 | I2 | 0 | 32767 | 1500 | 2 [^] -10 Ω |
| Ra Table | 1408 | R_a2 | | | | | | | |
| | | | 0 | Cell2 R_a flag | H2 | 0 | ffff | ff55 | - |
| | | | 2 | Cell2 R_a 0 | I2 | 0 | 32767 | 157 | 2 [^] -10 Ω |
| | | | 4 | Cell2 R_a 1 | I2 | 0 | 32767 | 147 | 2 [^] -10 Ω |
| | | | 6 | Cell2 R_a 2 | I2 | 0 | 32767 | 146 | 2 [^] -10 Ω |
| | | | 8 | Cell2 R_a 3 | I2 | 0 | 32767 | 138 | 2 [^] -10 Ω |
| | | | 10 | Cell2 R_a 4 | I2 | 0 | 32767 | 139 | 2 [^] -10 Ω |
| | | | 12 | Cell2 R_a 5 | I2 | 0 | 32767 | 156 | 2 [^] -10 Ω |
| | | | 14 | Cell2 R_a 6 | I2 | 0 | 32767 | 172 | 2 [^] -10 Ω |
| | | | 16 | Cell2 R_a 7 | I2 | 0 | 32767 | 184 | 2 [^] -10 Ω |
| | | | 18 | Cell2 R_a 8 | I2 | 0 | 32767 | 195 | 2 [^] -10 Ω |
| | | | 20 | Cell2 R_a 9 | I2 | 0 | 32767 | 204 | 2 [^] -10 Ω |
| | | | 22 | Cell2 R_a 10 | I2 | 0 | 32767 | 214 | 2 [^] -10 Ω |
| | | | 24 | Cell2 R_a 11 | I2 | 0 | 32767 | 226 | 2 [^] -10 Ω |
| | | | 26 | Cell2 R_a 12 | I2 | 0 | 32767 | 240 | 2 [^] -10 Ω |
| | | | 28 | Cell2 R_a 13 | I2 | 0 | 32767 | 254 | 2 [^] -10 Ω |
| | | | 30 | Cell2 R_a 14 | I2 | 0 | 32767 | 1500 | 2 [^] -10 Ω |
| Ra Table | 1472 | R_a3 | | | | | | | |
| | | | 0 | Cell3 R_a flag | H2 | 0 | ffff | ff55 | - |
| | | | 2 | Cell3 R_a 0 | I2 | 0 | 32767 | 68 | 2 [^] -10 Ω |
| | | | 4 | Cell3 R_a 1 | I2 | 0 | 32767 | 77 | 2 [^] -10 Ω |
| | | | 6 | Cell3 R_a 2 | I2 | 0 | 32767 | 88 | 2 [^] -10 Ω |
| | | | 8 | Cell3 R_a 3 | I2 | 0 | 32767 | 106 | 2 [^] -10 Ω |
| | | | 10 | Cell3 R_a 4 | I2 | 0 | 32767 | 103 | 2 [^] -10 Ω |
| | | | 12 | Cell3 R_a 5 | I2 | 0 | 32767 | 71 | 2 [^] -10 Ω |
| | | | 14 | Cell3 R_a 6 | I2 | 0 | 32767 | 84 | 2 [^] -10 Ω |
| | | | 16 | Cell3 R_a 7 | I2 | 0 | 32767 | 117 | 2 [^] -10 Ω |
| | | | 18 | Cell3 R_a 8 | I2 | 0 | 32767 | 112 | 2 [^] -10 Ω |
| | | | 20 | Cell3 R_a 9 | I2 | 0 | 32767 | 132 | 2 [^] -10 Ω |
| | | | 22 | Cell3 R_a 10 | I2 | 0 | 32767 | 121 | 2 [^] -10 Ω |
| | | | 24 | Cell3 R_a 11 | I2 | 0 | 32767 | 90 | 2 [^] -10 Ω |
| | | | 26 | Cell3 R_a 12 | I2 | 0 | 32767 | 89 | 2 [^] -10 Ω |
| | | | 28 | Cell3 R_a 13 | I2 | 0 | 32767 | 254 | 2 [^] -10 Ω |
| | | | 30 | Cell3 R_a 14 | I2 | 0 | 32767 | 1500 | 2 [^] -10 Ω |
| Ra Table | 1536 | R_a0x | | | | | | | |
| | | | 0 | xCell0 R_a flag | H2 | 0 | ffff | ffff | - |
| | | | 2 | xCell0 R_a 0 | I2 | 0 | 32767 | 68 | 2 [^] -10 Ω |
| | | | 4 | xCell0 R_a 1 | I2 | 0 | 32767 | 77 | 2 [^] -10 Ω |
| | | | 6 | xCell0 R_a 2 | I2 | 0 | 32767 | 88 | 2 [^] -10 Ω |

Table B-1. bq30z50-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|----------|-------------|----------|--------|-----------------|-----------|------------|------------|---------------|----------------------|
| | | | 8 | xCell0 R_a 3 | I2 | 0 | 32767 | 106 | 2 [^] -10 Ω |
| | | | 10 | xCell0 R_a 4 | I2 | 0 | 32767 | 103 | 2 [^] -10 Ω |
| | | | 12 | xCell0 R_a 5 | I2 | 0 | 32767 | 71 | 2 [^] -10 Ω |
| | | | 14 | xCell0 R_a 6 | I2 | 0 | 32767 | 84 | 2 [^] -10 Ω |
| | | | 16 | xCell0 R_a 7 | I2 | 0 | 32767 | 117 | 2 [^] -10 Ω |
| | | | 18 | xCell0 R_a 8 | I2 | 0 | 32767 | 112 | 2 [^] -10 Ω |
| | | | 20 | xCell0 R_a 9 | I2 | 0 | 32767 | 132 | 2 [^] -10 Ω |
| | | | 22 | xCell0 R_a 10 | I2 | 0 | 32767 | 121 | 2 [^] -10 Ω |
| | | | 24 | xCell0 R_a 11 | I2 | 0 | 32767 | 90 | 2 [^] -10 Ω |
| | | | 26 | xCell0 R_a 12 | I2 | 0 | 32767 | 89 | 2 [^] -10 Ω |
| | | | 28 | xCell0 R_a 13 | I2 | 0 | 32767 | 254 | 2 [^] -10 Ω |
| | | | 30 | xCell0 R_a 14 | I2 | 0 | 32767 | 1500 | 2 [^] -10 Ω |
| Ra Table | 1600 | R_a1x | | | | | | | |
| | | | 0 | xCell1 R_a flag | H2 | 0 | ffff | ffff | - |
| | | | 2 | xCell1 R_a 0 | I2 | 0 | 32767 | 68 | 2 [^] -10 Ω |
| | | | 4 | xCell1 R_a 1 | I2 | 0 | 32767 | 77 | 2 [^] -10 Ω |
| | | | 6 | xCell1 R_a 2 | I2 | 0 | 32767 | 88 | 2 [^] -10 Ω |
| | | | 8 | xCell1 R_a 3 | I2 | 0 | 32767 | 106 | 2 [^] -10 Ω |
| | | | 10 | xCell1 R_a 4 | I2 | 0 | 32767 | 103 | 2 [^] -10 Ω |
| | | | 12 | xCell1 R_a 5 | I2 | 0 | 32767 | 71 | 2 [^] -10 Ω |
| | | | 14 | xCell1 R_a 6 | I2 | 0 | 32767 | 84 | 2 [^] -10 Ω |
| | | | 16 | xCell1 R_a 7 | I2 | 0 | 32767 | 117 | 2 [^] -10 Ω |
| | | | 18 | xCell1 R_a 8 | I2 | 0 | 32767 | 112 | 2 [^] -10 Ω |
| | | | 20 | xCell1 R_a 9 | I2 | 0 | 32767 | 132 | 2 [^] -10 Ω |
| | | | 22 | xCell1 R_a 10 | I2 | 0 | 32767 | 121 | 2 [^] -10 Ω |
| | | | 24 | xCell1 R_a 11 | I2 | 0 | 32767 | 90 | 2 [^] -10 Ω |
| | | | 26 | xCell1 R_a 12 | I2 | 0 | 32767 | 89 | 2 [^] -10 Ω |
| | | | 28 | xCell1 R_a 13 | I2 | 0 | 32767 | 254 | 2 [^] -10 Ω |
| | | | 30 | xCell1 R_a 14 | I2 | 0 | 32767 | 1500 | 2 [^] -10 Ω |
| Ra Table | 1664 | R_a2x | | | | | | | |
| | | | 0 | xCell2 R_a flag | H2 | 0 | ffff | ffff | - |
| | | | 2 | xCell2 R_a 0 | I2 | 0 | 32767 | 68 | 2 [^] -10 Ω |
| | | | 4 | xCell2 R_a 1 | I2 | 0 | 32767 | 77 | 2 [^] -10 Ω |
| | | | 6 | xCell2 R_a 2 | I2 | 0 | 32767 | 88 | 2 [^] -10 Ω |
| | | | 8 | xCell2 R_a 3 | I2 | 0 | 32767 | 106 | 2 [^] -10 Ω |
| | | | 10 | xCell2 R_a 4 | I2 | 0 | 32767 | 103 | 2 [^] -10 Ω |
| | | | 12 | xCell2 R_a 5 | I2 | 0 | 32767 | 71 | 2 [^] -10 Ω |
| | | | 14 | xCell2 R_a 6 | I2 | 0 | 32767 | 84 | 2 [^] -10 Ω |

Table B-1. bq30z50-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-----------|-------------|--------------------|--------|---------------------|-----------|------------|------------|---------------|----------------------|
| | | | 16 | xCell2 R_a 7 | I2 | 0 | 32767 | 117 | 2 [^] -10 Ω |
| | | | 18 | xCell2 R_a 8 | I2 | 0 | 32767 | 112 | 2 [^] -10 Ω |
| | | | 20 | xCell2 R_a 9 | I2 | 0 | 32767 | 132 | 2 [^] -10 Ω |
| | | | 22 | xCell2 R_a 10 | I2 | 0 | 32767 | 121 | 2 [^] -10 Ω |
| | | | 24 | xCell2 R_a 11 | I2 | 0 | 32767 | 90 | 2 [^] -10 Ω |
| | | | 26 | xCell2 R_a 12 | I2 | 0 | 32767 | 89 | 2 [^] -10 Ω |
| | | | 28 | xCell2 R_a 13 | I2 | 0 | 32767 | 254 | 2 [^] -10 Ω |
| | | | 30 | xCell2 R_a 14 | I2 | 0 | 32767 | 1500 | 2 [^] -10 Ω |
| Ra Table | 1728 | R_a3x | | | | | | | |
| | | | 0 | xCell3 R_a flag | H2 | 0 | ffff | ffff | - |
| | | | 2 | xCell3 R_a 0 | I2 | 0 | 32767 | 68 | 2 [^] -10 Ω |
| | | | 4 | xCell3 R_a 1 | I2 | 0 | 32767 | 77 | 2 [^] -10 Ω |
| | | | 6 | xCell3 R_a 2 | I2 | 0 | 32767 | 88 | 2 [^] -10 Ω |
| | | | 8 | xCell3 R_a 3 | I2 | 0 | 32767 | 106 | 2 [^] -10 Ω |
| | | | 10 | xCell3 R_a 4 | I2 | 0 | 32767 | 103 | 2 [^] -10 Ω |
| | | | 12 | xCell3 R_a 5 | I2 | 0 | 32767 | 71 | 2 [^] -10 Ω |
| | | | 14 | xCell3 R_a 6 | I2 | 0 | 32767 | 84 | 2 [^] -10 Ω |
| | | | 16 | xCell3 R_a 7 | I2 | 0 | 32767 | 117 | 2 [^] -10 Ω |
| | | | 18 | xCell3 R_a 8 | I2 | 0 | 32767 | 112 | 2 [^] -10 Ω |
| | | | 20 | xCell3 R_a 9 | I2 | 0 | 32767 | 132 | 2 [^] -10 Ω |
| | | | 22 | xCell3 R_a 10 | I2 | 0 | 32767 | 121 | 2 [^] -10 Ω |
| | | | 24 | xCell3 R_a 11 | I2 | 0 | 32767 | 90 | 2 [^] -10 Ω |
| | | | 26 | xCell3 R_a 12 | I2 | 0 | 32767 | 89 | 2 [^] -10 Ω |
| | | | 28 | xCell3 R_a 13 | I2 | 0 | 32767 | 254 | 2 [^] -10 Ω |
| | | | 30 | xCell3 R_a 14 | I2 | 0 | 32767 | 1500 | 2 [^] -10 Ω |
| PF Status | 779 | Device Status Data | | | | | | | |
| | | | 0 | Safety Alert 0-15 | H2 | 0 | ffff | 0 | - |
| | | | 2 | Safety Status 0-15 | H2 | 0 | ffff | 0 | - |
| | | | 6 | PF Alert 0-15 | H2 | 0 | ffff | 0 | - |
| | | | 8 | PF Status 0-15 | H2 | 0 | ffff | 0 | - |
| | | | 12 | Safety Alert 16-31 | H2 | 0 | ffff | 0 | - |
| | | | 14 | Safety Status 16-31 | H2 | 0 | ffff | 0 | - |
| | | | 18 | PF Alert 16-31 | H2 | 0 | ffff | 0 | - |

Table B-1. bq30z50-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-----------|-------------|-------------------------|--------|------------------------|-----------|------------|------------|---------------|-------|
| | | | 20 | PF Status 16–31 | H2 | 0 | ffff | 0 | - |
| | | | 24 | Operation Status 0–15 | H2 | 0 | ffff | 0 | - |
| | | | 26 | Operation Status 16–31 | H2 | 0 | ffff | 0 | - |
| | | | 28 | Charging Status 0–15 | H2 | 0 | ffff | 0 | - |
| | | | 30 | Charging Status 16–23 | H1 | 0 | ffff | 0 | - |
| | | | 31 | Gauging Status | H2 | 0 | ffff | 0 | - |
| PF Status | 812 | Device Voltage Data | | | | | | | |
| | | | 0 | Cell Voltage 0 | I2 | –32768 | 32768 | 0 | mV |
| | | | 2 | Cell Voltage 1 | I2 | –32768 | 32768 | 0 | mV |
| | | | 4 | Cell Voltage 2 | I2 | –32768 | 32768 | 0 | mV |
| | | | 6 | Cell Voltage 3 | I2 | –32768 | 32768 | 0 | mV |
| | | | 8 | Battery Direct Voltage | I2 | –32768 | 32768 | 0 | mV |
| | | | 10 | Pack Voltage | I2 | –32768 | 32768 | 0 | mV |
| PF Status | 824 | Device Current Data | | | | | | | |
| | | | 0 | Current | I2 | –32768 | 32767 | 0 | mA |
| PF Status | 826 | Device Temperature Data | | | | | | | |
| | | | 0 | Internal Temperature | I2 | –32768 | 32768 | 0 | °C |
| | | | 2 | External 1 Temperature | I2 | –32768 | 32768 | 0 | °C |
| | | | 4 | External 2 Temperature | I2 | –32768 | 32768 | 0 | °C |
| | | | 6 | External 3 Temperature | I2 | –32768 | 32768 | 0 | °C |
| | | | 8 | External 4 Temperature | I2 | –32768 | 32768 | 0 | °C |
| PF Status | 836 | Device Gauging Data | | | | | | | |
| | | | 0 | Cell0 Dod0 | I2 | –32768 | 32767 | 0 | - |
| | | | 2 | Cell1 Dod0 | I2 | –32768 | 32767 | 0 | - |
| | | | 4 | Cell2 Dod0 | I2 | –32768 | 32767 | 0 | - |
| | | | 6 | Cell3 Dod0 | I2 | –32768 | 32767 | 0 | - |
| | | | 8 | Passed Charge | I2 | –32768 | 32768 | 0 | mAh |
| PF Status | 846 | AFE Regs | | | | | | | |
| | | | 0 | AFE Status | H1 | 0 | ff | 0 | - |
| | | | 1 | AFE State Control | H1 | 0 | ff | 0 | - |
| | | | 2 | AFE Control | H1 | 0 | ff | 0 | - |

Table B-1. bq30z50-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-------------|-------------|---------------|--------|-------------------------|-----------|------------|------------|---------------|-------|
| | | | 3 | AFE Output Status | H1 | 0 | ff | 0 | - |
| | | | 4 | AFE Function Control | H1 | 0 | ff | 0 | - |
| | | | 5 | AFE Cell Select | H1 | 0 | ff | 0 | - |
| | | | 6 | AFE OCDV | H1 | 0 | ff | 0 | - |
| | | | 7 | AFE OCDT | H1 | 0 | ff | 0 | - |
| | | | 8 | AFE SCC | H1 | 0 | ff | 0 | - |
| | | | 9 | AFE SCD1 | H1 | 0 | ff | 0 | - |
| | | | 10 | AFE SCD2 | H1 | 0 | ff | 0 | - |
| | | | 11 | AFE REF TRIM | H1 | 0 | ff | 0 | - |
| Black Box | 858 | Safety Status | | | | | | | |
| | | | 0 | 1st Status Status 0–15 | H2 | 0 | fff | 0 | - |
| | | | 2 | 1st Safety Status 16–31 | H2 | 0 | fff | 0 | - |
| | | | 4 | 1st Time to Next Event | U1 | 0 | 255 | 0 | s |
| | | | 5 | 2nd Safety Status 0–15 | H2 | 0 | fff | 0 | - |
| | | | 7 | 2nd Safety Status 16–31 | H2 | 0 | fff | 0 | - |
| | | | 9 | 2nd Time to Next Event | U1 | 0 | 255 | 0 | s |
| | | | 10 | 3rd Safety Status 0–15 | H2 | 0 | fff | 0 | - |
| | | | 12 | 3rd Safety Status 16–31 | H2 | 0 | fff | 0 | - |
| | | | 14 | 3rd Time to Next Event | U1 | 0 | 255 | 0 | s |
| Black Box | 873 | PF Status | | | | | | | |
| | | | 0 | 1st PF Status 0–15 | H2 | 0 | fff | 0 | - |
| | | | 2 | 1st PF Status 16–31 | H2 | 0 | fff | 0 | - |
| | | | 4 | 1st Time to Next Event | U1 | 0 | 255 | 0 | s |
| | | | 5 | 2nd PF Status 0–15 | H2 | 0 | fff | 0 | - |
| | | | 7 | 2nd PF Status 16–31 | H2 | 0 | fff | 0 | - |
| | | | 9 | 2nd Time to Next Event | U1 | 0 | 255 | 0 | s |
| | | | 10 | 3rd PF Status 0–15 | H2 | 0 | fff | 0 | - |
| | | | 12 | 3rd PF Status 16–31 | H2 | 0 | fff | 0 | - |
| | | | 14 | 3rd Time to Next Event | U1 | 0 | 255 | 0 | s |
| Calibration | 0 | Voltage | | | | | | | |
| | | | 0 | Cell Scale 0 | I2 | –32767 | 32767 | 20451 | - |

Table B-1. bq30z50-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-------------|-------------|------------------------|--------|--------------------------------|-----------|------------|--------------|---------------|---------|
| | | | 2 | Cell Scale 1 | I2 | –32767 | 32767 | 20468 | - |
| | | | 4 | Cell Scale 2 | I2 | –32767 | 32767 | 20520 | - |
| | | | 6 | Cell Scale 3 | I2 | –32767 | 32767 | 20517 | - |
| | | | 8 | Pack Gain | U2 | 0 | 65535 | 44100 | - |
| | | | 10 | BAT Gain | U2 | 0 | 65535 | 44100 | - |
| | 12 | Current | | | | | | | |
| | | | 0 | CC Gain | F4 | 1.00E–01 | 4.00E+00 | 0.9419 | - |
| | | | 4 | Capacity Gain | F4 | 2.9826E+04 | 1.193046E+06 | 280932.625 | - |
| Calibration | 20 | Current Offset | | | | | | | |
| | | | 0 | CC Offset | I2 | –32767 | 32767 | –7204 | - |
| | | | 2 | Coulomb Counter Offset Samples | U2 | 0 | 65535 | 64 | - |
| | | | 4 | Board Offset | I2 | –32768 | 32767 | 0 | - |
| Calibration | 26 | Temperature | | | | | | | |
| | | | 0 | Internal Temp Offset | I1 | –128 | 127 | 0 | °C |
| | | | 1 | External1 Temp Offset | I1 | –128 | 127 | 0 | °C |
| | | | 2 | External2 Temp Offset | I1 | –128 | 127 | 0 | °C |
| | | | 3 | External3 Temp Offset | I1 | –128 | 127 | 0 | °C |
| | | | 4 | External4 Temp Offset | I1 | –128 | 127 | 0 | °C |
| Calibration | 31 | Internal Temp Model | | | | | | | |
| | | | 0 | Int Coeff 1 | I2 | –32768 | 32767 | 0 | - |
| | | | 2 | Int Coeff 2 | I2 | –32768 | 32767 | 0 | - |
| | | | 4 | Int Coeff 3 | I2 | –32768 | 32767 | –11136 | - |
| | | | 6 | Int Coeff 4 | I2 | –32768 | 32767 | 5754 | - |
| | | | 8 | Int Minimum AD | I2 | –32768 | 32767 | 0 | - |
| | | | 10 | Int Maximum Temp | I2 | –32768 | 32767 | 5754 | 0.1degK |
| Calibration | 43 | Cell Temperature Model | | | | | | | |
| | | | 0 | Coeff a1 | I2 | –32768 | 32767 | –14520 | - |
| | | | 2 | Coeff a2 | I2 | –32768 | 32767 | 23696 | - |
| | | | 4 | Coeff a3 | I2 | –32768 | 32767 | –20298 | - |
| | | | 6 | Coeff a4 | I2 | –32768 | 32767 | 28073 | - |
| | | | 8 | Coeff a5 | I2 | –32768 | 32767 | 865 | - |
| | | | 10 | Coeff b1 | I2 | –32768 | 32767 | –694 | - |
| | | | 12 | Coeff b2 | I2 | –32768 | 32767 | 1326 | - |
| | | | 14 | Coeff b3 | I2 | –32768 | 32767 | –3880 | - |
| | | | 16 | Coeff b4 | I2 | –32768 | 32767 | 5127 | - |

Table B-1. bq30z50-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-------------|-------------|-----------------------|--------|--------------------------|-----------|------------|------------|---------------|-------|
| | | | 18 | Rc0 | I2 | –32768 | 32767 | 11703 | - |
| | | | 20 | Adc0 | I2 | –32768 | 32767 | 11703 | - |
| | | | 22 | Rpad | I2 | –32768 | 32767 | 0 | - |
| | | | 24 | Rint | I2 | –32768 | 32767 | 0 | - |
| Calibration | 69 | Fet Temperature Model | | | | | | | |
| | | | 0 | Coeff a1 | I2 | –32768 | 32767 | –14520 | - |
| | | | 2 | Coeff a2 | I2 | –32768 | 32767 | 23696 | - |
| | | | 4 | Coeff a3 | I2 | –32768 | 32767 | –20298 | - |
| | | | 6 | Coeff a4 | I2 | –32768 | 32767 | 28073 | - |
| | | | 8 | Coeff a5 | I2 | –32768 | 32767 | 865 | - |
| | | | 10 | Coeff b1 | I2 | –32768 | 32767 | –694 | - |
| | | | 12 | Coeff b2 | I2 | –32768 | 32767 | 1326 | - |
| | | | 14 | Coeff b3 | I2 | –32768 | 32767 | –3880 | - |
| | | | 16 | Coeff b4 | I2 | –32768 | 32767 | 5127 | - |
| | | | 18 | Rc0 | I2 | –32768 | 32767 | 11703 | - |
| | | | 20 | Adc0 | I2 | –32768 | 32767 | 11703 | - |
| | | | 22 | Rpad | I2 | –32768 | 32767 | 0 | - |
| | | | 24 | Rint | I2 | –32768 | 32767 | 0 | - |
| Calibration | 95 | Filter | | | | | | | |
| | | | 1 | Cell Voltage 1 | U1 | 0 | 255 | 145 | - |
| | | | 2 | Cell Voltage 2 | U1 | 0 | 255 | 145 | - |
| | | | 3 | Cell Voltage 3 | U1 | 0 | 255 | 145 | - |
| | | | 4 | Cell Voltage 4 | U1 | 0 | 255 | 145 | - |
| | | | 5 | Pack Voltage Out | U1 | 0 | 255 | 10 | - |
| | | | 6 | Direct Battery Voltage | U1 | 0 | 255 | 10 | - |
| | | | 7 | Summed Battery Voltage | U1 | 0 | 255 | 145 | - |
| | | | 8 | Cell Temperature | U1 | 0 | 255 | 145 | - |
| | | | 9 | FET Temperature | U1 | 0 | 255 | 145 | - |
| Calibration | 105 | Current Deadband | | | | | | | |
| | | | 0 | Deadband | U1 | 0 | 255 | 3 | mA |
| | | | 1 | Coulomb Counter Deadband | U1 | 0 | 255 | 34 | 290 V |

Table B-2. bq30z55-R1 Data Flash Subclass ID and Offset (Firmware v0.33)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-------------|-------------|----------|--------|-----------|-----------|------------|------------|---------------|-------|
| Protections | 256 | CUV | | | | | | | |
| | | | 0 | Threshold | I2 | 0 | 32767 | 2800 | mV |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| | | | 3 | Recovery | I2 | 0 | 32767 | 3000 | mV |

Table B-2. bq30z55-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-------------|-------------|----------|--------|-------------------------|-----------|------------|------------|---------------|-------|
| Protections | 261 | CUVC | | | | | | | |
| | | | 0 | Threshold | I2 | 0 | 32767 | 2900 | mV |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| | | | 3 | Recovery | I2 | 0 | 32767 | 3000 | mV |
| Protections | 266 | COV | | | | | | | |
| | | | 0 | Threshold Low Temp | I2 | 0 | 32767 | 4250 | mV |
| | | | 2 | Threshold Standard Temp | I2 | 0 | 32767 | 4250 | mV |
| | | | 4 | Threshold High Temp | I2 | 0 | 32767 | 4250 | mV |
| | | | 6 | Threshold Rec Temp | I2 | 0 | 32767 | 4250 | mV |
| | | | 8 | Delay | U1 | 0 | 255 | 2 | s |
| | | | 9 | Recovery Low Temp | I2 | 0 | 32767 | 4150 | mV |
| | | | 11 | Recovery Standard Temp | I2 | 0 | 32767 | 4150 | mV |
| | | | 13 | Recovery High Temp | I2 | 0 | 32767 | 4150 | mV |
| | | | 15 | Recovery Rec Temp | I2 | 0 | 32767 | 4150 | mV |
| Protections | 283 | OCC1 | | | | | | | |
| | | | 0 | Threshold | I2 | –32768 | 32767 | 6000 | mA |
| | | | 2 | Delay | U1 | 0 | 255 | 6 | s |
| Protections | 286 | OCC2 | | | | | | | |
| | | | 0 | Threshold | I2 | –32768 | 32767 | 8000 | mA |
| | | | 2 | Delay | U1 | 0 | 255 | 3 | s |
| Protections | 289 | OCC | | | | | | | |
| | | | 0 | Recovery Threshold | I2 | –32768 | 32767 | –50 | mA |
| | | | 2 | Recovery Delay | U1 | 0 | 255 | 5 | s |
| Protections | 292 | OCD1 | | | | | | | |
| | | | 0 | Threshold | I2 | –32768 | 32767 | –6000 | mA |
| | | | 2 | Delay | U1 | 0 | 255 | 6 | s |
| Protections | 295 | OCD2 | | | | | | | |
| | | | 0 | Threshold | I2 | –32768 | 32767 | –8000 | mA |
| | | | 2 | Delay | U1 | 0 | 255 | 3 | s |
| Protections | 298 | OCD | | | | | | | |
| | | | 0 | Recovery Threshold | I2 | –32768 | 32767 | 50 | mA |
| | | | 2 | Recovery Delay | U1 | 0 | 255 | 5 | s |
| Protections | 301 | OLD | | | | | | | |
| | | | 0 | Threshold | H1 | 0 | 0f | 09 | - |
| | | | 1 | Delay | H1 | 0 | 0f | 0f | - |
| | | | 2 | Latch Limit | U1 | 0 | 255 | 0 | - |
| | | | 3 | Counter Dec Delay | U1 | 0 | 255 | 10 | s |
| | | | 4 | Recovery | U1 | 0 | 255 | 5 | s |
| | | | 5 | Reset | U1 | 0 | 255 | 15 | s |
| Protections | 307 | SCC | | | | | | | |
| | | | 0 | Threshold | H1 | 0 | ff | 77 | - |
| | | | 1 | Latch Limit | U1 | 0 | 255 | 0 | mA |
| | | | 2 | Counter Dec Delay | U1 | 0 | 255 | 10 | s |

Table B-2. bq30z55-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-------------|-------------|----------|--------|-------------------|-----------|------------|------------|---------------|-------|
| | | | 3 | Recovery | U1 | 0 | 255 | 5 | s |
| | | | 4 | Reset | U1 | 0 | 255 | 15 | s |
| Protections | 312 | SCD1 | | | | | | | |
| | | | 0 | Threshold | H1 | 0 | ff | 77 | - |
| Protections | 313 | SCD2 | | | | | | | |
| | | | 0 | Threshold | H1 | 0 | ff | e7 | - |
| Protections | 314 | SCD | | | | | | | |
| | | | 0 | Latch Limit | U1 | 0 | 255 | 0 | mA |
| | | | 1 | Counter Dec Delay | U1 | 0 | 255 | 10 | s |
| | | | 2 | Recovery | U1 | 0 | 255 | 5 | s |
| | | | 3 | Reset | U1 | 0 | 255 | 15 | s |
| Protections | 318 | OTC | | | | | | | |
| | | | 0 | Threshold | I2 | -400 | 1500 | 550 | 1°C |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| | | | 3 | Recovery | I2 | -400 | 1500 | 500 | 1°C |
| Protections | 323 | OTD | | | | | | | |
| | | | 0 | Threshold | I2 | -400 | 1500 | 600 | 1°C |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| | | | 3 | Recovery | I2 | -400 | 1500 | 550 | 1°C |
| Protections | 328 | OTF | | | | | | | |
| | | | 0 | Threshold | I2 | -400 | 1500 | 800 | 1°C |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| | | | 3 | Recovery | I2 | -400 | 1500 | 650 | 1°C |
| Protections | 333 | HWD | | | | | | | |
| | | | 0 | Delay | U1 | 0 | 255 | 10 | s |
| Protections | 334 | PTO | | | | | | | |
| | | | 0 | Charge Threshold | I2 | -32768 | 32767 | 2000 | mA |
| | | | 2 | Suspend Threshold | I2 | -32768 | 32767 | 1800 | mA |
| | | | 4 | Delay | U2 | 0 | 65535 | 1800 | s |
| | | | 6 | Reset | I2 | 0 | 32767 | 2 | mAh |
| Protections | 342 | CTO | | | | | | | |
| | | | 0 | Charge Threshold | I2 | -32768 | 32767 | 2500 | mA |
| | | | 2 | Suspend Threshold | I2 | -32768 | 32767 | 2000 | mA |
| | | | 4 | Delay | U2 | 0 | 65535 | 54000 | s |
| | | | 6 | Reset | I2 | 0 | 32767 | 2 | mAh |
| Protections | 350 | OC | | | | | | | |
| | | | 0 | Threshold | I2 | -32768 | 32767 | 300 | mAh |
| | | | 2 | Recovery | I2 | -32768 | 32767 | 2 | mAh |
| | | | 4 | RSOC Recovery | U1 | 0 | 100 | 90 | % |
| Protections | 335 | CHGV | | | | | | | |
| | | | 0 | Threshold | I2 | -32768 | 32767 | 500 | mV |
| | | | 2 | Delay | U1 | 0 | 255 | 30 | s |
| | | | 3 | Recovery | I2 | -32768 | 32767 | -500 | mV |
| Protections | 360 | CHGC | | | | | | | |
| | | | 0 | Threshold | I2 | -32768 | 32767 | 500 | mA |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| | | | 3 | Recovery | I2 | -32768 | 32767 | 100 | mA |

Table B-2. bq30z55-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|----------------|-------------|----------|--------|------------------|-----------|------------|------------|---------------|---------|
| Permanent Fail | 365 | CUV | | | | | | | |
| | | | 0 | Threshold | I2 | 0 | 32767 | 2500 | mV |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| Permanent Fail | 368 | COV | | | | | | | |
| | | | 0 | Threshold | I2 | 0 | 32767 | 4400 | mV |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| Permanent Fail | 371 | CUDEP | | | | | | | |
| | | | 0 | Threshold | I2 | 2500 | 0 | 32767 | mV |
| | | | 2 | Delay | U1 | 2 | 0 | 255 | s |
| Permanent Fail | 374 | OTCE | | | | | | | |
| | | | 0 | Threshold | I2 | –400 | 1500 | 650 | 1°C |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| Permanent Fail | 377 | OTF | | | | | | | |
| | | | 0 | Threshold | I2 | –400 | 1500 | 1000 | 1°C |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| Permanent Fail | 380 | QIM | | | | | | | |
| | | | 0 | Delta Threshold | I2 | 0 | 32767 | 500 | mAh |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | updates |
| Permanent Fail | 383 | CB | | | | | | | |
| | | | 0 | Max Threshold | I2 | 0 | 32767 | 120 | h |
| | | | 2 | Delta Threshold | U1 | 0 | 255 | 20 | h |
| | | | 3 | Delay | U1 | 0 | 255 | 2 | cycles |
| Permanent Fail | 387 | VIMR | | | | | | | |
| | | | 0 | Check Voltage | I2 | 0 | 5000 | 3600 | mV |
| | | | 2 | Check Current | I2 | 0 | 32767 | 10 | mA |
| | | | 4 | Delta Threshold | I2 | 0 | 5000 | 200 | mV |
| | | | 6 | Delta Delay | U1 | 0 | 255 | 2 | s |
| | | | 7 | Duration | U2 | 0 | 65535 | 100 | s |
| Permanent Fail | 396 | VIMA | | | | | | | |
| | | | 0 | Check Voltage | I2 | 0 | 5000 | 3600 | mV |
| | | | 2 | Check Current | I2 | 0 | 32767 | 10 | mA |
| | | | 4 | Delta Threshold | I2 | 0 | 5000 | 300 | mV |
| | | | 6 | Delay | U1 | 0 | 255 | 2 | s |
| Permanent Fail | 403 | IMP | | | | | | | |
| | | | 0 | Delta Threshold | I2 | 0 | 32767 | 300 | % |
| | | | 2 | Max Threshold | I2 | 0 | 32767 | 400 | % |
| | | | 4 | Ra Update Counts | U1 | 0 | 255 | 2 | counts |
| Permanent Fail | 408 | CD | | | | | | | |
| | | | 0 | Threshold | I2 | 0 | 32767 | 4200 | mAh |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | cycles |
| Permanent Fail | 411 | CFETF | | | | | | | |
| | | | 0 | OFF Threshold | I2 | 0 | 500 | 5 | mA |
| | | | 2 | OFF Delay | U1 | 0 | 255 | 2 | s |
| Permanent Fail | 414 | DFET | | | | | | | |
| | | | 0 | OFF Threshold | I2 | –500 | 0 | –5 | mA |
| | | | 2 | OFF Delay | U1 | 0 | 255 | 2 | s |
| Permanent Fail | 417 | TH | | | | | | | |
| | | | 4 | ADC Delay | U1 | 0 | 255 | 10 | s |
| Permanent Fail | 422 | FUSE | | | | | | | |
| | | | 0 | Threshold | I2 | 0 | 255 | 5 | mA |

Table B-2. bq30z55-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|---------------------------|-------------|------------------------|--------|-----------------|-----------|------------|------------|---------------|-------|
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| Permanent Fail | 425 | AFER | | | | | | | |
| | | | 0 | Threshold | U1 | 0 | 255 | 100 | - |
| | | | 1 | Delay Period | U1 | 0 | 255 | 2 | s |
| | | | 2 | Compare Period | U1 | 0 | 255 | 5 | s |
| Permanent Fail | 428 | AFEC | | | | | | | |
| | | | 0 | Threshold | U1 | 0 | 255 | 100 | - |
| | | | 1 | Delay Period | U1 | 0 | 255 | 5 | s |
| Permanent Fail | 430 | 2LVL | | | | | | | |
| | | | 0 | Delay | U1 | 0 | 255 | 2 | s |
| Permanent Fail | 431 | OCECO | | | | | | | |
| | | | 0 | Threshold | I2 | 0 | 32767 | 5000 | mV |
| | | | 2 | Delay | U1 | 0 | 255 | 2 | s |
| Advanced Charge Algorithm | 109 | Temperature Ranges | | | | | | | |
| | | | 0 | T1 Temp | I1 | -128 | 127 | 0 | °C |
| | | | 1 | T2 Temp | I1 | -128 | 127 | 12 | °C |
| | | | 2 | T5 Temp | I1 | -128 | 127 | 20 | °C |
| | | | 3 | T6 Temp | I1 | -128 | 127 | 25 | °C |
| | | | 4 | T3 Temp | I1 | -128 | 127 | 30 | °C |
| | | | 5 | T4 Temp | I1 | -128 | 127 | 55 | °C |
| | | | 6 | Hysteresis Temp | I1 | -128 | 127 | 0 | °C |
| Advanced Charge Algorithm | 116 | Low Temp Charging | | | | | | | |
| | | | 0 | Voltage | I2 | 0 | 32767 | 3000 | mV |
| | | | 2 | Current Low | I2 | 0 | 32767 | 132 | mA |
| | | | 4 | Current Med | I2 | 0 | 32767 | 352 | mA |
| | | | 6 | Current High | I2 | 0 | 32767 | 264 | mA |
| Advanced Charge Algorithm | 124 | Standard Temp Charging | | | | | | | |
| | | | 0 | Voltage | I2 | 0 | 32767 | 4200 | mV |
| | | | 2 | Current Low | I2 | 0 | 32767 | 1980 | mA |
| | | | 4 | Current Med | I2 | 0 | 32767 | 4004 | mA |
| | | | 6 | Current High | I2 | 0 | 32767 | 2992 | mA |
| Advanced Charge Algorithm | 132 | High Temp Charging | | | | | | | |
| | | | 0 | Voltage | I2 | 0 | 32767 | 4000 | mV |
| | | | 2 | Current Low | I2 | 0 | 32767 | 1012 | %C |
| | | | 4 | Current Med | I2 | 0 | 32767 | 1980 | %C |
| | | | 6 | Current High | I2 | 0 | 32767 | 1496 | %C |
| Advanced Charge Algorithm | 140 | Rec Temp Charging | | | | | | | |
| | | | 0 | Voltage | I2 | 0 | 32767 | 4100 | mV |
| | | | 2 | Current Low | I2 | 0 | 32767 | 2508 | mA |
| | | | 4 | Current Med | I2 | 0 | 32767 | 4488 | mA |
| | | | 6 | Current High | I2 | 0 | 32767 | 3520 | mA |

Table B-2. bq30z55-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|---------------------------|-------------|--------------------------|--------|-----------------------------|-----------|------------|------------|--|-------|
| Advanced Charge Algorithm | 148 | Pre-Charging | | | | | | | |
| | | | 0 | Current | I2 | 0 | 32767 | 88 | mA |
| Advanced Charge Algorithm | 150 | Maintenance Charging | | | | | | | |
| | | | 0 | Current | I2 | 0 | 32767 | 44 | mA |
| Advanced Charge Algorithm | 152 | Voltage Range | | | | | | | |
| | | | 0 | Charging Voltage Low | I2 | 0 | 32767 | 2500 | mV |
| | | | 2 | Charging Voltage Med | I2 | 0 | 32767 | 3600 | mV |
| | | | 4 | Charging Voltage High | I2 | 0 | 32767 | 4000 | mV |
| | | | 6 | Charging Voltage Hysteresis | U1 | 0 | 255 | 0 | mV |
| Advanced Charge Algorithm | 159 | Termination Config | | | | | | | |
| | | | 0 | Charge Term Taper Current | I2 | 0 | 32767 | 250 | mA |
| | | | 4 | Charge Term Voltage | I2 | 0 | 32767 | 75 | mV |
| Advanced Charge Algorithm | 168 | Cell Balancing Config | | | | | | | |
| | | | 0 | Bal Time/mAh Cell 0 | U2 | 0 | 65535 | 367 | s/mAh |
| | | | 2 | Bal Time/mAh Cell 1–3 | U2 | 0 | 65535 | 514 | s/mAh |
| | | | 4 | Min Start Balance Delta | U1 | 0 | 255 | 3 | mV |
| | | | 5 | Relax Balance Interval | U4 | 0 | 4294967295 | 18000 | s |
| | | | 9 | Min Rsoc for Balancing | U1 | 0 | 100 | 80 | % |
| Advanced Charge Algorithm | 178 | Charging Rate of Change | | | | | | | |
| | | | 0 | Current Rate | U1 | 1 | 255 | 1 | steps |
| | | | 1 | Voltage Rate | U1 | 1 | 255 | 1 | steps |
| Advanced Charge Algorithm | 180 | Charge Loss Compensation | | | | | | | |
| | | | 0 | CCC Current Threshold | I2 | 0 | 32767 | 3520 | mA |
| | | | 1 | CCC Voltage Threshold | U1 | 0 | 255 | 210 | mV |
| System Data | 640 | Manufacturer Data | | | | | | | |
| | | | 0 | ManufacturerInfo | S33 | x | x | abcdefghijklmn opqrstuvwxyz01 2345 | - |
| System Data | 673 | Integrity | | | | | | | |
| | | | 4 | Data Flash Checksum | H2 | 0 | ffff | 0 | - |
| SBS Configuration | 679 | Data | | | | | | | |

Table B-2. bq30z55-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-------------------|-------------|----------|--------|---------------------------|-----------|------------|------------|-------------------|-------|
| | | | 0 | Remaining AH Cap. Alarm | I2 | 0 | 32767 | 300 | mAh |
| | | | 2 | Remaining WH Cap. Alarm | I2 | 0 | 32767 | 432 | cWh |
| | | | 4 | Remaining Time Alarm | U2 | 0 | 65535 | 10 | min |
| | | | 6 | Initial Battery Mode | H2 | 0 | ffff | 81 | - |
| | | | 8 | Design Voltage | I2 | 0 | 32767 | 14400 | mV |
| | | | 10 | Specification Information | H2 | 0 | ffff | 31 | - |
| | | | 12 | Manufacture Date | U2 | 0 | 65535 | 0 | date |
| | | | 14 | Serial Number | H2 | 0 | ffff | 1 | - |
| | | | 16 | Cycle Count | U2 | 0 | 65535 | 0 | - |
| | | | 18 | Cycle Count Percentage | U1 | 0 | 100 | 90 | % |
| | | | 19 | Max Error Limit | U1 | 0 | 100 | 100 | % |
| | | | 20 | Design Capacity mAh | I2 | 0 | 32767 | 4400 | mAh |
| | | | 22 | Design Capacity cWh | I2 | 0 | 32767 | 6336 | cWh |
| | | | 24 | Manufacturer Name | S21 | x | x | Texas Instruments | - |
| | | | 45 | Device Name | S21 | x | x | bq30z50-R1 | - |
| | | | 66 | Device Chemistry | S5 | x | x | LION | - |
| SBS Configuration | 750 | FD | | | | | | | |
| | | | 0 | Set Voltage Threshold | I2 | 0 | 5000 | 3000 | mV |
| | | | 2 | Clear Voltage Threshold | I2 | 0 | 5000 | 3100 | mV |
| | | | 4 | Set % RSOC Threshold | U1 | 0 | 100 | 0 | % |
| | | | 5 | Clear % RSOC Threshold | U1 | 0 | 100 | 5 | % |
| SBS Configuration | 756 | FC | | | | | | | |
| | | | 0 | Set Voltage Threshold | I2 | 0 | 5000 | 4200 | mV |
| | | | 2 | Clear Voltage Threshold | I2 | 0 | 5000 | 4100 | mV |
| | | | 4 | Set % RSOC Threshold | U1 | 0 | 100 | 100 | % |
| | | | 5 | Clear % RSOC Threshold | U1 | 0 | 100 | 95 | % |
| SBS Configuration | 762 | TDA | | | | | | | |
| | | | 0 | Set Voltage Threshold | I2 | 0 | 5000 | 3200 | mV |
| | | | 2 | Clear Voltage Threshold | I2 | 0 | 5000 | 3300 | mV |
| | | | 4 | Set % RSOC Threshold | U1 | 0 | 100 | 10 | % |
| | | | 5 | Clear % RSOC Threshold | U1 | 0 | 100 | 15 | % |
| SBS Configuration | 768 | TCA | | | | | | | |

Table B-2. bq30z55-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-------------------|-------------|---------------|--------|-------------------------|-----------|------------|------------|---------------|--------|
| | | | 0 | Set Voltage Threshold | I2 | 0 | 5000 | 4200 | mV |
| | | | 2 | Clear Voltage Threshold | I2 | 0 | 5000 | 4100 | mV |
| | | | 4 | Set % RSOC Threshold | U1 | 0 | 100 | 100 | % |
| | | | 5 | Clear % RSOC Threshold | U1 | 0 | 100 | 95 | % |
| SBS Configuration | 774 | Max Error | | | | | | | |
| | | | 3 | Time Cycle Equivalent | U1 | 0 | 255 | 12 | h |
| | | | 4 | Cycle Delta | U1 | 0 | 255 | 5 | % |
| Lifetimes | 512 | Voltage | | | | | | | |
| | | | 0 | Max Cell Voltage 0 | U1 | 0 | 255 | 0 | mV |
| | | | 1 | Max Cell Voltage 1 | U1 | 0 | 255 | 0 | mV |
| | | | 2 | Max Cell Voltage 2 | U1 | 0 | 255 | 0 | mV |
| | | | 3 | Max Cell Voltage 3 | U1 | 0 | 255 | 0 | mV |
| | | | 4 | Min Cell Voltage 0 | U1 | 0 | 255 | 255 | mV |
| | | | 5 | Min Cell Voltage 1 | U1 | 0 | 255 | 255 | mV |
| | | | 6 | Min Cell Voltage 2 | U1 | 0 | 255 | 255 | mV |
| | | | 7 | Min Cell Voltage 3 | U1 | 0 | 255 | 255 | mV |
| | | | 8 | Max Delta Cell Voltage | U1 | 0 | 255 | 0 | mV |
| Lifetimes | 521 | Current | | | | | | | |
| | | | 0 | Max Charge Current | U1 | 0 | 255 | 0 | mA |
| | | | 1 | Max Discharge Current | U1 | 0 | 255 | 0 | mA |
| | | | 2 | Max Avg Dsg Current | U1 | 0 | 255 | 0 | mA |
| | | | 3 | Max Avg Dsg Power | U1 | 0 | 255 | 0 | W |
| Lifetimes | 525 | Safety Events | | | | | | | |
| | | | 0 | No Of Cov Events | U1 | 0 | 255 | 0 | events |
| | | | 1 | Last Cov Event | U1 | 0 | 255 | 0 | cycles |
| | | | 2 | No Of Cuv Events | U1 | 0 | 255 | 0 | events |
| | | | 3 | Last Cuv Event | U1 | 0 | 255 | 0 | cycles |
| | | | 4 | No Of Ocd1 Events | U1 | 0 | 255 | 0 | events |
| | | | 5 | Last Ocd1 Event | U1 | 0 | 255 | 0 | cycles |
| | | | 6 | No Of Ocd2 Events | U1 | 0 | 255 | 0 | events |
| | | | 7 | Last Ocd2 Event | U1 | 0 | 255 | 0 | cycles |
| | | | 8 | No Of Occ1 Events | U1 | 0 | 255 | 0 | events |
| | | | 9 | Last Occ1 Event | U1 | 0 | 255 | 0 | cycles |

Table B-2. bq30z55-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-----------|-------------|-----------------|--------|------------------------|-----------|------------|------------|---------------|--------|
| | | | 10 | No Of Occ2 Events | U1 | 0 | 255 | 0 | events |
| | | | 11 | Last Occ2 Event | U1 | 0 | 255 | 0 | cycles |
| | | | 12 | No Of Old Events | U1 | 0 | 255 | 0 | events |
| | | | 13 | Last Old Event | U1 | 0 | 255 | 0 | cycles |
| | | | 14 | No Of Scd Events | U1 | 0 | 255 | 0 | events |
| | | | 15 | Last Scd Event | U1 | 0 | 255 | 0 | cycles |
| | | | 16 | No Of Scc Events | U1 | 0 | 255 | 0 | events |
| | | | 17 | Last Scc Event | U1 | 0 | 255 | 0 | cycles |
| | | | 18 | No Of Otc Events | U1 | 0 | 255 | 0 | events |
| | | | 19 | Last Otc Event | U1 | 0 | 255 | 0 | cycles |
| | | | 20 | No Of Otd Events | U1 | 0 | 255 | 0 | events |
| | | | 21 | Last Otd Event | U1 | 0 | 255 | 0 | cycles |
| | | | 22 | No Of Off Events | U1 | 0 | 255 | 0 | events |
| | | | 23 | Last Off Event | U1 | 0 | 255 | 0 | cycles |
| Lifetimes | 549 | Charging Events | | | | | | | |
| | | | 0 | No Valid Charge Term | U1 | 0 | 255 | 0 | events |
| | | | 1 | Last Valid Charge Term | U1 | 0 | 255 | 0 | cycles |
| Lifetimes | 551 | Gauging Events | | | | | | | |
| | | | 0 | No Of Qmax Updates | U1 | 0 | 255 | 0 | events |
| | | | 1 | Last Qmax Update | U1 | 0 | 255 | 0 | cycles |
| | | | 2 | No Of Ra Updates | U1 | 0 | 255 | 0 | events |
| | | | 3 | Last Ra Update | U1 | 0 | 255 | 0 | cycles |
| | | | 4 | No Of Ra Disable | U1 | 0 | 255 | 0 | events |
| | | | 5 | Last Ra Disable | U1 | 0 | 255 | 0 | cycles |
| Lifetimes | 557 | Power Events | | | | | | | |
| | | | 0 | No Of Shutdowns | U1 | 0 | 255 | 0 | events |
| Lifetimes | 561 | Cell Balancing | | | | | | | |
| | | | 0 | Cb Time Cell 0 | U1 | 0 | 255 | 0 | h |
| | | | 1 | Cb Time Cell 1 | U1 | 0 | 255 | 0 | h |
| | | | 2 | Cb Time Cell 2 | U1 | 0 | 255 | 0 | h |
| | | | 3 | Cb Time Cell 3 | U1 | 0 | 255 | 0 | h |
| Lifetimes | 565 | Temperature | | | | | | | |
| | | | 0 | Max Temp Cell | I1 | –128 | 127 | –128 | °C |
| | | | 1 | Min Temp Cell | I1 | –128 | 127 | 127 | °C |
| | | | 2 | Max Delta Cell Temp | I1 | –128 | 127 | 0 | °C |
| | | | 3 | Max Temp Int Sensor | I1 | –128 | 127 | –128 | °C |
| | | | 4 | Min Temp Int Sensor | I1 | –128 | 127 | 127 | °C |

Table B-2. bq30z55-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-----------|-------------|-------------------|--------|---------------------------|-----------|------------|------------|---------------|-------|
| | | | 5 | Max Temp Fet | I1 | –128 | 127 | –128 | °C |
| Lifetimes | 571 | Time | | | | | | | |
| | | | 0 | Total Fw Runtime | U2 | 0 | 65535 | 0 | h |
| | | | 2 | Time Spent In UT | U2 | 0 | 65535 | 0 | h |
| | | | 4 | Time Spent In LT | U2 | 0 | 65535 | 0 | h |
| | | | 6 | Time Spent In STL | U2 | 0 | 65535 | 0 | h |
| | | | 8 | Time Spent In RT | U2 | 0 | 65535 | 0 | h |
| | | | 10 | Time Spent In STH | U2 | 0 | 65535 | 0 | h |
| | | | 12 | Time Spent In HT | U2 | 0 | 65535 | 0 | h |
| | | | 14 | Time Spent In OT | U2 | 0 | 65535 | 0 | h |
| Settings | 185 | Fuse | | | | | | | |
| | | | 0 | PF Fuse 0–15 | H2 | 0 | ffff | 0 | - |
| | | | 2 | PF Fuse 16–31 | H2 | 0 | ffff | 0 | - |
| | | | 4 | Min Blow Fuse Voltage | I2 | 0 | 65535 | 8000 | mV |
| Settings | 191 | Manufacturing | | | | | | | |
| | | | 0 | Manufacturing Status | H2 | 0 | ffff | 8000 | - |
| Settings | 193 | Protection | | | | | | | |
| | | | 0 | Enabled Protections 0–15 | H2 | 0 | fff | fff | - |
| | | | 2 | Enabled Protections 16–31 | H2 | 0 | ffff | ffff | - |
| Settings | 197 | Permanent Failure | | | | | | | |
| | | | 0 | Enabled PF 0–15 | H2 | 0 | ffff | ffff | - |
| | | | 2 | Enabled PF 16–31 | H2 | 0 | ffff | ffff | - |
| Settings | 201 | Configuration | | | | | | | |
| | | | 0 | Protection Configuration | H1 | 0 | ff | 01 | - |
| | | | 1 | Temperature Configuration | H2 | 0 | fff | 0087 | - |
| | | | 3 | Charging Configuration | H1 | 0 | ff | 0 | - |
| | | | 4 | System Configuration | H2 | 0 | 1ff | 32 | - |
| | | | 6 | Gauging Configuration | H2 | 0 | fff | 1fda | - |
| | | | 8 | Sbs Configuration | H1 | 0 | ff | 20 | - |
| | | | 9 | Sbs Data Config. 0–15 | H2 | 0 | 0fff | 0caf | - |
| | | | 11 | Sbs Data Config. 16–23 | H1 | 0 | ff | ff | - |
| Settings | 213 | AFE | | | | | | | |
| | | | 1 | AFE State Control | H1 | 0 | ff | 0 | - |
| Power | 228 | Power | | | | | | | |

Table B-2. bq30z55-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-------------|-------------|--------------------|--------|---------------------------|-----------|------------|------------|---------------|-------|
| | | | 0 | Valid Update Voltage | I2 | 0 | 32767 | 7500 | mV |
| Power | 230 | Shutdown | | | | | | | |
| | | | 0 | Shutdown Voltage | I2 | 0 | 32767 | 1750 | mV |
| | | | 2 | Shutdown Time | U1 | 0 | 255 | 10 | s |
| | | | 3 | Charger Present Threshold | I2 | 0 | 32767 | 3000 | mV |
| Power | 235 | Sleep | | | | | | | |
| | | | 0 | Sleep Current | I2 | 0 | 32767 | 10 | mA |
| | | | 7 | Voltage Time | U1 | 0 | 255 | 5 | s |
| | | | 8 | Current Time | U1 | 0 | 255 | 20 | s |
| | | | 9 | Wake | H1 | 0 | ff | 0 | - |
| Power | 245 | Ship | | | | | | | |
| | | | 0 | Delay | U1 | 0 | 255 | 5 | s |
| | | | 1 | Current | I2 | -250 | 250 | 10 | mA |
| Gas Gauging | 248 | Current Thresholds | | | | | | | |
| | | | 0 | Dsg Current Threshold | I2 | -32768 | 32767 | 100 | mA |
| | | | 2 | Chg Current Threshold | I2 | -32768 | 32767 | 50 | mA |
| | | | 4 | Quit Current | I2 | 0 | 32767 | 10 | mA |
| Gas Gauging | 884 | State | | | | | | | |
| | | | 0 | Qmax Cell 0 | I2 | 0 | 32767 | 4400 | mAh |
| | | | 2 | Qmax Cell 1 | I2 | 0 | 32767 | 4400 | mAh |
| | | | 4 | Qmax Cell 2 | I2 | 0 | 32767 | 4400 | mAh |
| | | | 6 | Qmax Cell 3 | I2 | 0 | 32767 | 4400 | mAh |
| | | | 8 | Qmax Pack | I2 | 0 | 32767 | 4400 | mAh |
| | | | 12 | Update Status | H1 | 0 | ff | 0 | - |
| | | | 13 | Cell 0 Chg Voltage at EoC | I2 | 0 | 32767 | 4200 | mV |
| | | | 15 | Cell 1 Chg Voltage at EoC | I2 | 0 | 32767 | 4200 | mV |
| | | | 17 | Cell 2 Chg Voltage at EoC | I2 | 0 | 32767 | 4200 | mV |
| | | | 19 | Cell 3 Chg Voltage at EoC | I2 | 0 | 32767 | 4200 | mV |
| | | | 21 | Current at EoC | I2 | 0 | 32767 | 250 | mA |
| | | | 23 | Avg I Last Run | I2 | -32768 | 32767 | -2000 | mA |
| | | | 25 | Avg P Last Run | I2 | -32768 | 32767 | -3022 | cW |
| | | | 27 | Delta Voltage | I2 | -32768 | 32767 | 0 | mV |
| | | | 33 | Max Avg I Last Run | I2 | -32768 | 32767 | -2000 | mA |
| | | | 35 | Max Avg P Last Run | I2 | -32768 | 32767 | -3022 | cW |
| Gas Gauging | 921 | IT Cfg | | | | | | | |
| | | | 0 | Load Select | U1 | 0 | 255 | 7 | - |
| | | | 1 | Load Mode | U1 | 0 | 255 | 0 | - |
| | | | 16 | Ra Filter | U2 | 0 | 999 | 500 | % |
| | | | 19 | Ra Max Delta | U1 | 0 | 255 | 15 | % |
| | | | 21 | Design Resistance | I2 | 1 | 32767 | 42 | mOhms |
| | | | 23 | Reference Grid | U1 | 0 | 14 | 4 | - |

Table B-2. bq30z55-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|----------|-------------|----------|--------|-------------------------|-----------|------------|------------|---------------|----------------------|
| | | | 62 | Term Voltage | I2 | 0 | 32767 | 9000 | mV |
| | | | 64 | Term Voltage Delta | I2 | 0 | 32767 | 300 | mV |
| | | | 81 | User Rate-mA | I2 | -9000 | 0 | 0 | mA |
| | | | 83 | User Rate-cW | I2 | -32768 | 0 | 0 | cW |
| | | | 85 | Reserve Cap-mAh | I2 | 0 | 9000 | 0 | mAh |
| | | | 87 | Reserve Cap-cWh | I2 | 0 | 32000 | 0 | cWh |
| | | | 93 | Remcap Smoothing Filter | U1 | 0 | 255 | 250 | - |
| Ra Table | 1280 | R_a0 | | | | | | | |
| | | | 0 | Cell0 R_a flag | H2 | 0 | ffff | ff55 | - |
| | | | 2 | Cell0 R_a 0 | I2 | 0 | 32767 | 182 | 2 [^] -10 Ω |
| | | | 4 | Cell0 R_a 1 | I2 | 0 | 32767 | 177 | 2 [^] -10 Ω |
| | | | 6 | Cell0 R_a 2 | I2 | 0 | 32767 | 175 | 2 [^] -10 Ω |
| | | | 8 | Cell0 R_a 3 | I2 | 0 | 32767 | 167 | 2 [^] -10 Ω |
| | | | 10 | Cell0 R_a 4 | I2 | 0 | 327672 | 166 | 2 [^] -10 Ω |
| | | | 12 | Cell0 R_a 5 | I2 | 0 | 32767 | 182 | 2 [^] -10 Ω |
| | | | 14 | Cell0 R_a 6 | I2 | 0 | 32767 | 194 | 2 [^] -10 Ω |
| | | | 16 | Cell0 R_a 7 | I2 | 0 | 32767 | 203 | 2 [^] -10 Ω |
| | | | 18 | Cell0 R_a 8 | I2 | 0 | 32767 | 213 | 2 [^] -10 Ω |
| | | | 20 | Cell0 R_a 9 | I2 | 0 | 32767 | 223 | 2 [^] -10 Ω |
| | | | 22 | Cell0 R_a 10 | I2 | 0 | 32767 | 233 | 2 [^] -10 Ω |
| | | | 24 | Cell0 R_a 11 | I2 | 0 | 32767 | 241 | 2 [^] -10 Ω |
| | | | 26 | Cell0 R_a 12 | I2 | 0 | 32767 | 250 | 2 [^] -10 Ω |
| | | | 28 | Cell0 R_a 13 | I2 | 0 | 32767 | 254 | 2 [^] -10 Ω |
| | | | 30 | Cell0 R_a 14 | I2 | 0 | 32767 | 1500 | 2 [^] -10 Ω |
| Ra Table | 1344 | R_a1 | | | | | | | |
| | | | 0 | Cell1 R_a flag | H2 | 0 | ffff | ff55 | - |
| | | | 2 | Cell1 R_a 0 | I2 | 0 | 32767 | 163 | 2 [^] -10 Ω |
| | | | 4 | Cell1 R_a 1 | I2 | 0 | 32767 | 151 | 2 [^] -10 Ω |
| | | | 6 | Cell1 R_a 2 | I2 | 0 | 32767 | 152 | 2 [^] -10 Ω |
| | | | 8 | Cell1 R_a 3 | I2 | 0 | 32767 | 143 | 2 [^] -10 Ω |
| | | | 10 | Cell1 R_a 4 | I2 | 0 | 32767 | 145 | 2 [^] -10 Ω |
| | | | 12 | Cell1 R_a 5 | I2 | 0 | 32767 | 162 | 2 [^] -10 Ω |
| | | | 14 | Cell1 R_a 6 | I2 | 0 | 32767 | 178 | 2 [^] -10 Ω |
| | | | 16 | Cell1 R_a 7 | I2 | 0 | 32767 | 188 | 2 [^] -10 Ω |
| | | | 18 | Cell1 R_a 8 | I2 | 0 | 32767 | 200 | 2 [^] -10 Ω |
| | | | 20 | Cell1 R_a 9 | I2 | 0 | 32767 | 206 | 2 [^] -10 Ω |
| | | | 22 | Cell1 R_a 10 | I2 | 0 | 32767 | 216 | 2 [^] -10 Ω |
| | | | 24 | Cell1 R_a 11 | I2 | 0 | 32767 | 230 | 2 [^] -10 Ω |
| | | | 26 | Cell1 R_a 12 | I2 | 0 | 32767 | 240 | 2 [^] -10 Ω |
| | | | 28 | Cell1 R_a 13 | I2 | 0 | 32767 | 254 | 2 [^] -10 Ω |
| | | | 30 | Cell1 R_a 14 | I2 | 0 | 32767 | 1500 | 2 [^] -10 Ω |
| Ra Table | 1408 | R_a2 | | | | | | | |
| | | | 0 | Cell2 R_a flag | H2 | 0 | ffff | ff55 | - |
| | | | 2 | Cell2 R_a 0 | I2 | 0 | 32767 | 157 | 2 [^] -10 Ω |
| | | | 4 | Cell2 R_a 1 | I2 | 0 | 32767 | 147 | 2 [^] -10 Ω |
| | | | 6 | Cell2 R_a 2 | I2 | 0 | 32767 | 146 | 2 [^] -10 Ω |
| | | | 8 | Cell2 R_a 3 | I2 | 0 | 32767 | 138 | 2 [^] -10 Ω |

Table B-2. bq30z55-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|----------|-------------|----------|--------|-----------------|-----------|------------|------------|---------------|----------------------|
| | | | 10 | Cell2 R_a 4 | I2 | 0 | 32767 | 139 | 2 [^] -10 Ω |
| | | | 12 | Cell2 R_a 5 | I2 | 0 | 32767 | 156 | 2 [^] -10 Ω |
| | | | 14 | Cell2 R_a 6 | I2 | 0 | 32767 | 172 | 2 [^] -10 Ω |
| | | | 16 | Cell2 R_a 7 | I2 | 0 | 32767 | 184 | 2 [^] -10 Ω |
| | | | 18 | Cell2 R_a 8 | I2 | 0 | 32767 | 195 | 2 [^] -10 Ω |
| | | | 20 | Cell2 R_a 9 | I2 | 0 | 32767 | 204 | 2 [^] -10 Ω |
| | | | 22 | Cell2 R_a 10 | I2 | 0 | 32767 | 214 | 2 [^] -10 Ω |
| | | | 24 | Cell2 R_a 11 | I2 | 0 | 32767 | 226 | 2 [^] -10 Ω |
| | | | 26 | Cell2 R_a 12 | I2 | 0 | 32767 | 240 | 2 [^] -10 Ω |
| | | | 28 | Cell2 R_a 13 | I2 | 0 | 32767 | 254 | 2 [^] -10 Ω |
| | | | 30 | Cell2 R_a 14 | I2 | 0 | 32767 | 1500 | 2 [^] -10 Ω |
| Ra Table | 1472 | R_a3 | | | | | | | |
| | | | 0 | Cell3 R_a flag | H2 | 0 | ffff | ff55 | - |
| | | | 2 | Cell3 R_a 0 | I2 | 0 | 32767 | 68 | 2 [^] -10 Ω |
| | | | 4 | Cell3 R_a 1 | I2 | 0 | 32767 | 77 | 2 [^] -10 Ω |
| | | | 6 | Cell3 R_a 2 | I2 | 0 | 32767 | 88 | 2 [^] -10 Ω |
| | | | 8 | Cell3 R_a 3 | I2 | 0 | 32767 | 106 | 2 [^] -10 Ω |
| | | | 10 | Cell3 R_a 4 | I2 | 0 | 32767 | 103 | 2 [^] -10 Ω |
| | | | 12 | Cell3 R_a 5 | I2 | 0 | 32767 | 71 | 2 [^] -10 Ω |
| | | | 14 | Cell3 R_a 6 | I2 | 0 | 32767 | 84 | 2 [^] -10 Ω |
| | | | 16 | Cell3 R_a 7 | I2 | 0 | 32767 | 117 | 2 [^] -10 Ω |
| | | | 18 | Cell3 R_a 8 | I2 | 0 | 32767 | 112 | 2 [^] -10 Ω |
| | | | 20 | Cell3 R_a 9 | I2 | 0 | 32767 | 132 | 2 [^] -10 Ω |
| | | | 22 | Cell3 R_a 10 | I2 | 0 | 32767 | 121 | 2 [^] -10 Ω |
| | | | 24 | Cell3 R_a 11 | I2 | 0 | 32767 | 90 | 2 [^] -10 Ω |
| | | | 26 | Cell3 R_a 12 | I2 | 0 | 32767 | 89 | 2 [^] -10 Ω |
| | | | 28 | Cell3 R_a 13 | I2 | 0 | 32767 | 254 | 2 [^] -10 Ω |
| | | | 30 | Cell3 R_a 14 | I2 | 0 | 32767 | 1500 | 2 [^] -10 Ω |
| Ra Table | 1536 | R_a0x | | | | | | | |
| | | | 0 | xCell0 R_a flag | H2 | 0 | ffff | ffff | - |
| | | | 2 | xCell0 R_a 0 | I2 | 0 | 32767 | 68 | 2 [^] -10 Ω |
| | | | 4 | xCell0 R_a 1 | I2 | 0 | 32767 | 77 | 2 [^] -10 Ω |
| | | | 6 | xCell0 R_a 2 | I2 | 0 | 32767 | 88 | 2 [^] -10 Ω |
| | | | 8 | xCell0 R_a 3 | I2 | 0 | 32767 | 106 | 2 [^] -10 Ω |
| | | | 10 | xCell0 R_a 4 | I2 | 0 | 32767 | 103 | 2 [^] -10 Ω |
| | | | 12 | xCell0 R_a 5 | I2 | 0 | 32767 | 71 | 2 [^] -10 Ω |
| | | | 14 | xCell0 R_a 6 | I2 | 0 | 32767 | 84 | 2 [^] -10 Ω |
| | | | 16 | xCell0 R_a 7 | I2 | 0 | 32767 | 117 | 2 [^] -10 Ω |
| | | | 18 | xCell0 R_a 8 | I2 | 0 | 32767 | 112 | 2 [^] -10 Ω |
| | | | 20 | xCell0 R_a 9 | I2 | 0 | 32767 | 132 | 2 [^] -10 Ω |
| | | | 22 | xCell0 R_a 10 | I2 | 0 | 32767 | 121 | 2 [^] -10 Ω |
| | | | 24 | xCell0 R_a 11 | I2 | 0 | 32767 | 90 | 2 [^] -10 Ω |
| | | | 26 | xCell0 R_a 12 | I2 | 0 | 32767 | 89 | 2 [^] -10 Ω |
| | | | 28 | xCell0 R_a 13 | I2 | 0 | 32767 | 254 | 2 [^] -10 Ω |
| | | | 30 | xCell0 R_a 14 | I2 | 0 | 32767 | 1500 | 2 [^] -10 Ω |
| Ra Table | 1600 | R_a1x | | | | | | | |
| | | | 0 | xCell1 R_a flag | H2 | 0 | ffff | ffff | - |
| | | | 2 | xCell1 R_a 0 | I2 | 0 | 32767 | 68 | 2 [^] -10 Ω |
| | | | 4 | xCell1 R_a 1 | I2 | 0 | 32767 | 77 | 2 [^] -10 Ω |
| | | | 6 | xCell1 R_a 2 | I2 | 0 | 32767 | 88 | 2 [^] -10 Ω |
| | | | 8 | xCell1 R_a 3 | I2 | 0 | 32767 | 106 | 2 [^] -10 Ω |

Table B-2. bq30z55-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-----------|-------------|--------------------|--------|--------------------|-----------|------------|------------|---------------|----------------------|
| | | | 10 | xCell1 R_a 4 | I2 | 0 | 32767 | 103 | 2 [^] -10 Ω |
| | | | 12 | xCell1 R_a 5 | I2 | 0 | 32767 | 71 | 2 [^] -10 Ω |
| | | | 14 | xCell1 R_a 6 | I2 | 0 | 32767 | 84 | 2 [^] -10 Ω |
| | | | 16 | xCell1 R_a 7 | I2 | 0 | 32767 | 117 | 2 [^] -10 Ω |
| | | | 18 | xCell1 R_a 8 | I2 | 0 | 32767 | 112 | 2 [^] -10 Ω |
| | | | 20 | xCell1 R_a 9 | I2 | 0 | 32767 | 132 | 2 [^] -10 Ω |
| | | | 22 | xCell1 R_a 10 | I2 | 0 | 32767 | 121 | 2 [^] -10 Ω |
| | | | 24 | xCell1 R_a 11 | I2 | 0 | 32767 | 90 | 2 [^] -10 Ω |
| | | | 26 | xCell1 R_a 12 | I2 | 0 | 32767 | 89 | 2 [^] -10 Ω |
| | | | 28 | xCell1 R_a 13 | I2 | 0 | 32767 | 254 | 2 [^] -10 Ω |
| | | | 30 | xCell1 R_a 14 | I2 | 0 | 32767 | 1500 | 2 [^] -10 Ω |
| Ra Table | 1664 | R_a2x | | | | | | | |
| | | | 0 | xCell2 R_a flag | H2 | 0 | ffff | ffff | - |
| | | | 2 | xCell2 R_a 0 | I2 | 0 | 32767 | 68 | 2 [^] -10 Ω |
| | | | 4 | xCell2 R_a 1 | I2 | 0 | 32767 | 77 | 2 [^] -10 Ω |
| | | | 6 | xCell2 R_a 2 | I2 | 0 | 32767 | 88 | 2 [^] -10 Ω |
| | | | 8 | xCell2 R_a 3 | I2 | 0 | 32767 | 106 | 2 [^] -10 Ω |
| | | | 10 | xCell2 R_a 4 | I2 | 0 | 32767 | 103 | 2 [^] -10 Ω |
| | | | 12 | xCell2 R_a 5 | I2 | 0 | 32767 | 71 | 2 [^] -10 Ω |
| | | | 14 | xCell2 R_a 6 | I2 | 0 | 32767 | 84 | 2 [^] -10 Ω |
| | | | 16 | xCell2 R_a 7 | I2 | 0 | 32767 | 117 | 2 [^] -10 Ω |
| | | | 18 | xCell2 R_a 8 | I2 | 0 | 32767 | 112 | 2 [^] -10 Ω |
| | | | 20 | xCell2 R_a 9 | I2 | 0 | 32767 | 132 | 2 [^] -10 Ω |
| | | | 22 | xCell2 R_a 10 | I2 | 0 | 32767 | 121 | 2 [^] -10 Ω |
| | | | 24 | xCell2 R_a 11 | I2 | 0 | 32767 | 90 | 2 [^] -10 Ω |
| | | | 26 | xCell2 R_a 12 | I2 | 0 | 32767 | 89 | 2 [^] -10 Ω |
| | | | 28 | xCell2 R_a 13 | I2 | 0 | 32767 | 254 | 2 [^] -10 Ω |
| | | | 30 | xCell2 R_a 14 | I2 | 0 | 32767 | 1500 | 2 [^] -10 Ω |
| Ra Table | 1728 | R_a3x | | | | | | | |
| | | | 0 | xCell3 R_a flag | H2 | 0 | ffff | ffff | - |
| | | | 2 | xCell3 R_a 0 | I2 | 0 | 32767 | 68 | 2 [^] -10 Ω |
| | | | 4 | xCell3 R_a 1 | I2 | 0 | 32767 | 77 | 2 [^] -10 Ω |
| | | | 6 | xCell3 R_a 2 | I2 | 0 | 32767 | 88 | 2 [^] -10 Ω |
| | | | 8 | xCell3 R_a 3 | I2 | 0 | 32767 | 106 | 2 [^] -10 Ω |
| | | | 10 | xCell3 R_a 4 | I2 | 0 | 32767 | 103 | 2 [^] -10 Ω |
| | | | 12 | xCell3 R_a 5 | I2 | 0 | 32767 | 71 | 2 [^] -10 Ω |
| | | | 14 | xCell3 R_a 6 | I2 | 0 | 32767 | 84 | 2 [^] -10 Ω |
| | | | 16 | xCell3 R_a 7 | I2 | 0 | 32767 | 117 | 2 [^] -10 Ω |
| | | | 18 | xCell3 R_a 8 | I2 | 0 | 32767 | 112 | 2 [^] -10 Ω |
| | | | 20 | xCell3 R_a 9 | I2 | 0 | 32767 | 132 | 2 [^] -10 Ω |
| | | | 22 | xCell3 R_a 10 | I2 | 0 | 32767 | 121 | 2 [^] -10 Ω |
| | | | 24 | xCell3 R_a 11 | I2 | 0 | 32767 | 90 | 2 [^] -10 Ω |
| | | | 26 | xCell3 R_a 12 | I2 | 0 | 32767 | 89 | 2 [^] -10 Ω |
| | | | 28 | xCell3 R_a 13 | I2 | 0 | 32767 | 254 | 2 [^] -10 Ω |
| | | | 30 | xCell3 R_a 14 | I2 | 0 | 32767 | 1500 | 2 [^] -10 Ω |
| PF Status | 779 | Device Status Data | | | | | | | |
| | | | 0 | Safety Alert 0-15 | H2 | 0 | ffff | 0 | - |
| | | | 2 | Safety Status 0-15 | H2 | 0 | ffff | 0 | - |
| | | | 6 | PF Alert 0-15 | H2 | 0 | ffff | 0 | - |

Table B-2. bq30z55-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-----------|-------------|-------------------------|--------|------------------------|-----------|------------|------------|---------------|-------|
| | | | 8 | PF Status 0–15 | H2 | 0 | ffff | 0 | - |
| | | | 12 | Safety Alert 16–31 | H2 | 0 | ffff | 0 | - |
| | | | 14 | Safety Status 16–31 | H2 | 0 | ffff | 0 | - |
| | | | 18 | PF Alert 16–31 | H2 | 0 | ffff | 0 | - |
| | | | 20 | PF Status 16–31 | H2 | 0 | ffff | 0 | - |
| | | | 24 | Operation Status 0–15 | H2 | 0 | ffff | 0 | - |
| | | | 26 | Operation Status 16–31 | H2 | 0 | ffff | 0 | - |
| | | | 28 | Charging Status 0–15 | H2 | 0 | ffff | 0 | - |
| | | | 30 | Charging Status 16–23 | H1 | 0 | ffff | 0 | - |
| | | | 31 | Gauging Status | H2 | 0 | ffff | 0 | - |
| PF Status | 812 | Device Voltage Data | | | | | | | |
| | | | 0 | Cell Voltage 0 | I2 | –32768 | 32768 | 0 | mV |
| | | | 2 | Cell Voltage 1 | I2 | –32768 | 32768 | 0 | mV |
| | | | 4 | Cell Voltage 2 | I2 | –32768 | 32768 | 0 | mV |
| | | | 6 | Cell Voltage 3 | I2 | –32768 | 32768 | 0 | mV |
| | | | 8 | Battery Direct Voltage | I2 | –32768 | 32768 | 0 | mV |
| | | | 10 | Pack Voltage | I2 | –32768 | 32768 | 0 | mV |
| PF Status | 824 | Device Current Data | | | | | | | |
| | | | 0 | Current | I2 | –32768 | 32767 | 0 | mA |
| PF Status | 826 | Device Temperature Data | | | | | | | |
| | | | 0 | Internal Temperature | I2 | –32768 | 32768 | 0 | °C |
| | | | 2 | External 1 Temperature | I2 | –32768 | 32768 | 0 | °C |
| | | | 4 | External 2 Temperature | I2 | –32768 | 32768 | 0 | °C |
| PF Status | 832 | Device Gauging Data | | | | | | | |
| | | | 0 | Cell0 Dod0 | I2 | –32768 | 32767 | 0 | - |
| | | | 2 | Cell1 Dod0 | I2 | –32768 | 32767 | 0 | - |
| | | | 4 | Cell2 Dod0 | I2 | –32768 | 32767 | 0 | - |
| | | | 6 | Cell3 Dod0 | I2 | –32768 | 32767 | 0 | - |
| | | | 8 | Passed Charge | I2 | –32768 | 32768 | 0 | mAh |
| PF Status | 842 | AFE Regs | | | | | | | |
| | | | 0 | AFE Status | H1 | 0 | ff | 0 | - |
| | | | 1 | AFE State Control | H1 | 0 | ff | 0 | - |
| | | | 2 | AFE Control | H1 | 0 | ff | 0 | - |
| | | | 3 | AFE Output Status | H1 | 0 | ff | 0 | - |
| | | | 4 | AFE Function Control | H1 | 0 | ff | 0 | - |
| | | | 5 | AFE Cell Select | H1 | 0 | ff | 0 | - |
| | | | 6 | AFE OCDV | H1 | 0 | ff | 0 | - |
| | | | 7 | AFE OCDT | H1 | 0 | ff | 0 | - |

Table B-2. bq30z55-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-------------|-------------|----------------|--------|--------------------------------|-----------|------------|--------------|---------------|-------|
| | | | 8 | AFE SCC | H1 | 0 | ff | 0 | - |
| | | | 9 | AFE SCD1 | H1 | 0 | ff | 0 | - |
| | | | 10 | AFE SCD2 | H1 | 0 | ff | 0 | - |
| | | | 11 | AFE REF TRIM | H1 | 0 | ff | 0 | - |
| Black Box | 854 | Safety Status | | | | | | | |
| | | | 0 | 1st Status Status 0–15 | H2 | 0 | ffff | 0 | - |
| | | | 2 | 1st Safety Status 16–31 | H2 | 0 | ffff | 0 | - |
| | | | 4 | 1st Time to Next Event | U1 | 0 | 255 | 0 | s |
| | | | 5 | 2nd Safety Status 0–15 | H2 | 0 | ffff | 0 | - |
| | | | 7 | 2nd Safety Status 16–31 | H2 | 0 | ffff | 0 | - |
| | | | 9 | 2nd Time to Next Event | U1 | 0 | 255 | 0 | s |
| | | | 10 | 3rd Safety Status 0–15 | H2 | 0 | ffff | 0 | - |
| | | | 12 | 3rd Safety Status 16–31 | H2 | 0 | ffff | 0 | - |
| | | | 14 | 3rd Time to Next Event | U1 | 0 | 255 | 0 | s |
| Black Box | 869 | PF Status | | | | | | | |
| | | | 0 | 1st PF Status 0–15 | H2 | 0 | ffff | 0 | - |
| | | | 2 | 1st PF Status 16–31 | H2 | 0 | ffff | 0 | - |
| | | | 4 | 1st Time to Next Event | U1 | 0 | 255 | 0 | s |
| | | | 5 | 2nd PF Status 0–15 | H2 | 0 | ffff | 0 | - |
| | | | 7 | 2nd PF Status 16–31 | H2 | 0 | ffff | 0 | - |
| | | | 9 | 2nd Time to Next Event | U1 | 0 | 255 | 0 | s |
| | | | 10 | 3rd PF Status 0–15 | H2 | 0 | ffff | 0 | - |
| | | | 12 | 3rd PF Status 16–31 | H2 | 0 | ffff | 0 | - |
| | | | 14 | 3rd Time to Next Event | U1 | 0 | 255 | 0 | s |
| Calibration | 0 | Voltage | | | | | | | |
| | | | 0 | Cell Scale 0 | I2 | –32767 | 32767 | 20451 | - |
| | | | 2 | Cell Scale 1 | I2 | –32767 | 32767 | 20468 | - |
| | | | 4 | Cell Scale 2 | I2 | –32767 | 32767 | 20520 | - |
| | | | 6 | Cell Scale 3 | I2 | –32767 | 32767 | 20517 | - |
| | | | 8 | Pack Gain | U2 | 0 | 65535 | 44100 | - |
| | | | 10 | BAT Gain | U2 | 0 | 65535 | 44100 | - |
| Calibration | 12 | Current | | | | | | | |
| | | | 0 | CC Gain | F4 | 1.00E–01 | 4.00E+00 | 0.9419 | - |
| | | | 4 | Capacity Gain | F4 | 2.9826E+04 | 1.193046E+06 | 280932.625 | - |
| Calibration | 20 | Current Offset | | | | | | | |
| | | | 0 | CC Offset | I2 | –32767 | 32767 | –7204 | - |
| | | | 2 | Coulomb Counter Offset Samples | U2 | 0 | 65535 | 64 | - |

Table B-2. bq30z55-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-------------|-------------|------------------------|--------|-----------------------|-----------|------------|------------|---------------|---------|
| | | | 4 | Board Offset | I2 | –32768 | 32767 | 0 | - |
| Calibration | 26 | Temperature | | | | | | | |
| | | | 0 | Internal Temp Offset | I1 | –128 | 127 | 0 | °C |
| | | | 1 | External1 Temp Offset | I1 | –128 | 127 | 0 | °C |
| | | | 2 | External2 Temp Offset | I1 | –128 | 127 | 0 | °C |
| Calibration | 29 | Internal Temp Model | | | | | | | |
| | | | 0 | Int Coeff 1 | I2 | –32768 | 32767 | 0 | - |
| | | | 2 | Int Coeff 2 | I2 | –32768 | 32767 | 0 | - |
| | | | 4 | Int Coeff 3 | I2 | –32768 | 32767 | –11136 | - |
| | | | 6 | Int Coeff 4 | I2 | –32768 | 32767 | 5754 | - |
| | | | 8 | Int Minimum AD | I2 | –32768 | 32767 | 0 | - |
| | | | 10 | Int Maximum Temp | I2 | –32768 | 32767 | 5754 | 0.1degK |
| Calibration | 41 | Cell Temperature Model | | | | | | | |
| | | | 0 | Coeff a1 | I2 | –32768 | 32767 | –14520 | - |
| | | | 2 | Coeff a2 | I2 | –32768 | 32767 | 23696 | - |
| | | | 4 | Coeff a3 | I2 | –32768 | 32767 | –20298 | - |
| | | | 6 | Coeff a4 | I2 | –32768 | 32767 | 28073 | - |
| | | | 8 | Coeff a5 | I2 | –32768 | 32767 | 865 | - |
| | | | 10 | Coeff b1 | I2 | –32768 | 32767 | –694 | - |
| | | | 12 | Coeff b2 | I2 | –32768 | 32767 | 1326 | - |
| | | | 14 | Coeff b3 | I2 | –32768 | 32767 | –3880 | - |
| | | | 16 | Coeff b4 | I2 | –32768 | 32767 | 5127 | - |
| | | | 18 | Rc0 | I2 | –32768 | 32767 | 11703 | - |
| | | | 20 | Adc0 | I2 | –32768 | 32767 | 11703 | - |
| | | | 22 | Rpad | I2 | –32768 | 32767 | 0 | - |
| | | | 24 | Rint | I2 | –32768 | 32767 | 0 | - |
| Calibration | 67 | Fet Temperature Model | | | | | | | |
| | | | 0 | Coeff a1 | I2 | –32768 | 32767 | –14520 | - |
| | | | 2 | Coeff a2 | I2 | –32768 | 32767 | 23696 | - |
| | | | 4 | Coeff a3 | I2 | –32768 | 32767 | –20298 | - |
| | | | 6 | Coeff a4 | I2 | –32768 | 32767 | 28073 | - |
| | | | 8 | Coeff a5 | I2 | –32768 | 32767 | 865 | - |
| | | | 10 | Coeff b1 | I2 | –32768 | 32767 | –694 | - |
| | | | 12 | Coeff b2 | I2 | –32768 | 32767 | 1326 | - |
| | | | 14 | Coeff b3 | I2 | –32768 | 32767 | –3880 | - |
| | | | 16 | Coeff b4 | I2 | –32768 | 32767 | 5127 | - |
| | | | 18 | Rc0 | I2 | –32768 | 32767 | 11703 | - |
| | | | 20 | Adc0 | I2 | –32768 | 32767 | 11703 | - |
| | | | 22 | Rpad | I2 | –32768 | 32767 | 0 | - |
| | | | 24 | Rint | I2 | –32768 | 32767 | 0 | - |
| Calibration | 93 | Filter | | | | | | | |
| | | | 1 | Cell Voltage 1 | U1 | 0 | 255 | 145 | - |
| | | | 2 | Cell Voltage 2 | U1 | 0 | 255 | 145 | - |
| | | | 3 | Cell Voltage 3 | U1 | 0 | 255 | 145 | - |
| | | | 4 | Cell Voltage 4 | U1 | 0 | 255 | 145 | - |

Table B-2. bq30z55-R1 Data Flash Subclass ID and Offset (Firmware v0.33) (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min. Value | Max. Value | Default Value | Units |
|-------------|-------------|------------------|--------|--------------------------|-----------|------------|------------|---------------|-------|
| | | | 5 | Pack Voltage Out | U1 | 0 | 255 | 10 | - |
| | | | 6 | Direct Battery Voltage | U1 | 0 | 255 | 10 | - |
| | | | 7 | Summed Battery Voltage | U1 | 0 | 255 | 145 | - |
| | | | 8 | Cell Temperature | U1 | 0 | 255 | 145 | - |
| | | | 9 | FET Temperature | U1 | 0 | 255 | 145 | - |
| Calibration | 103 | Current Deadband | | | | | | | |
| | | | 0 | Deadband | U1 | 0 | 255 | 3 | mA |
| | | | 1 | Coulomb Counter Deadband | U1 | 0 | 255 | 34 | 290 V |

Sample Filter Settings

Table C-1. Sample Remcap Filter Settings and Associated Low-Pass Filter Time Constants

| Remcap Smoothing Filter | Effective Low-Pass Time Constant |
|-------------------------|----------------------------------|
| 200 | 11 seconds |
| 230 | 22 seconds |
| 240 | 36 seconds |
| 245 | 54 seconds |
| 250 | 100 seconds |
| 252 | 146 seconds |
| 253 | 3.2 minutes |
| 254 | 4.8 minutes |
| 255 (max) | 9.6 minutes |

Table C-2. Sample V/I/T Filter Settings and Associated Low-Pass Filter Time Constants

| V/I/T Smoothing Filter | Effective Low-Pass Time Constant |
|------------------------|----------------------------------|
| 10 | 0.25 seconds |
| 50 | 0.5 seconds |
| 145 | 1 second |
| 200 | 3 seconds |

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