Resume

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<tr><td colspan="2">Name</td><td>Awais Hussain</td><td>Advisor</td><td>Tsung-Han Tsai</td><td rowspan="3">  </td></tr>
<tr><td colspan="2">Address</td><td colspan="3">E1-410, Electrical Engineering Building, National Central University, Zhongli, Taiwan.</td></tr>
<tr><td colspan="2">E-Mail</td><td>awais.hussain6@gmail.com</td><td>Mobile No.</td><td>+886-984389184</td></tr>
<tr><td rowspan="5">Education</td><td>Academics</td><td>Institute</td><td colspan="2">Department</td><td>Grades</td></tr>
<tr><td>PhD</td><td>National Central University, Taoyuan</td><td colspan="2">Electrical Engineering (2019-2~Present)</td><td>87.6%</td></tr>
<tr><td>Master</td><td>National Central University, Taoyuan</td><td colspan="2">Electrical Engineering (2016-9~2018-6)</td><td>90.75%; Position: 7/117 (Top 5%)</td></tr>
<tr><td>Bachelor</td><td>University of Bradford, UK</td><td colspan="2">Electrical Engineering (2011-9~2015-9)</td><td>72% (First class honors)</td></tr>
<tr><td>Senior High School</td><td>F.B.I.S.E, Pakistan</td><td colspan="2">Pre-Engineering (2009-5~2011-5)</td><td>79%</td></tr>
<tr><td colspan="2" rowspan="4">Skill Set</td><td colspan="4">Development of designing and verification flow for VLSI design</td></tr>
<tr><td colspan="4">Frontend (Verilog) and Backend (Physical Design layout) experience</td></tr>
<tr><td colspan="4">Familiarity with industry-standard circuit design and verification tools, flows and methodologies</td></tr>
<tr><td colspan="4">Superior written and oral English communication skills</td></tr>
<tr><td rowspan="2">Technical Skills</td><td>Programming</td><td colspan="4">C, C++, Verilog, VHDL</td></tr>
<tr><td>CAD tool</td><td colspan="4">Matlab, Xilinx ISE, Xilinx Vivado, Altera Quartus; Visual Studio; Synopsys Design Compiler, Synopsys IC Compiler</td></tr>
<tr><td colspan="2">Projects</td><td colspan="4">1. Learning on Chip
For PhD research, I have been working on the implementation of transfer learning on chip. This research will help to perform transfer learning on the edge where low power devices can be utilized to perform training on the edge.
2. Implementation of FBCOT encoding in FPGA
Fast Block Coding with Optimized Truncation (FBCOT) is new proposed engine for data compression in JPEG2000. It is intended to replace EBCOT due to its low latency and high throughput. For encoder module, variable length coding, MEL coding, significance pattern coding, bit stuffing and bit packing modules were implemented. This design was completed to have high throughput while using minimum resources. For</td></tr>
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	this project, collaboration work was performed with Professor David Taubman from University of New South Wales, Australia and a team from University of Stuttgart, Germany. For implementation of algorithm module, I worked on implementation of encoder part and German team has been working on decoder part. 3. **Designing of ECG compression chip (Master Thesis)** Complete digital design and layout of ECG compression design was performed using TSMC90nm and TSMC0.18um technology. Synthesis of implemented design was done using Design Compiler. Floor planning, placement, clock tree synthesis and routing was completed in IC Compiler. DRC and LVS were performed in Calibre. **4. Development of a hand-gesture recognition system using Convolutional Neural Network (CNN) (Under Progress)** A hand-gesture recognition system was developed using Deep Convolutional Neural Networks (CNN) to recognize different hand gestures. **5. Automatic Iris segmentation and recognition** Automatic iris segmentation and recognition was performed using total variation model. This project is implemented using Matlab. Main purpose of this project was to increase the speed of segmentation while maintaining highest accuracy. **6. Implementation of Blow Fish encryption algorithm in FPGA (Bachelor Project)** Blow Fish Encryption algorithm was implemented in FPGA using Verilog. It largely reduced time required to perform heavy calculations as compared to CPU.
Experience	**1. Research Assistant** 2016-04 ~ 2016-07 Worked as research assistant for the project of "Integration of design thinking and TRIZ for prospective engineers". The basic responsibilities included data collection, analysis, and conducting sessions with research participants and teaching developing professional skills course. **2. Research Assistant cum Teaching Assistant** 2016-01 ~ 2016-03 The basic responsibilities included managing class and conducting activities in "Developing Professional Skills". The research responsibilities included the research on the change of behavior of students through the course by analyzing the data through qualitative research.
Internship	**1. Innovative design thinking** 2015-06~ 2015-08 This internship included courses on innovative design thinking process and TRIZ (a tool for problem solving). The project of this internship was redesigning of final year project lab.

Honors & Awards	1. Awarded full scholarship by National Central University, Taiwan 2. Awarded 90% scholarship by Namal College, Pakistan 3. Qualified for Quarterfinals in Robosprint Competition 2013 4. Serving as the general secretary of Students Welfare Association Mianwali (SWAMI) 5. Selected as member of Namal Society for Social Impact
Publications	1. "A Bi-directional Prototype Mobile Robot to Experiment Light Scale Object-Transportation Schemes", M. Bilal Khan, **M. Awais Hussain**, Khurram Ch., Umar T., Sajid Nawaz, R. Jawad Ali, IEEE ICET, Islamabad, Pakistan, 2014. 2. "FPGA Based Implementation Scenarios of TEA Block Cipher", **M. Awais Hussain**, Rabiah Badar, IEEE FIT, Islamabad, Pakistan, 2015. 3. "VLSI Implementation of ECG Compression Algorithm using Golomb Rice Coding", Tsung-Han Tsai, **M. Awais Hussain,** Ping-Zen Hao, IEEE ICEE-Taiwan, Taichung, Taiwan, 2018. ***(Best Paper Award)*** 4. I. Althamary, **M. A. Hussain**, Y. Li, "An Improved Framework of Accurate Iris Segmentation Under Relaxed Imaging Constraints Using Total Variation Model," in CVGIP, Taitung, Taiwan, 2019. 5. T. Tsai, C. Huang, C. Chang and **M. A. Hussain**, "Design of Wireless Vision Sensor Network for Smart Home," in *IEEE Access*, vol. 8, pp. 60455-60467, 2020. 6. T. Tsai and **M. A. Hussain**, "VLSI Implementation of Lossless ECG Compression Algorithm for Low Power Devices," in *IEEE Transactions on Circuits and Systems II: Express Briefs*., 2020
Volunteer Work	**1. Flood relief activities in 2015** Volunteered for flood relief activities in different areas of Mianwali with Imran Khan Foundation. It included survey of affected area, distribution of aid and data entry of different people.
Extra-curricular activities	Gymnasium, Badminton, e-gaming
References	**1. <u>Tsung-Han Tsai</u>** Professor, Dept. of Electrical Engineering, National Central University, Taiwan. Email: han@ee.ncu.edu.tw Contact number: +886-03-422-7151 ext: 34472 **2. <u>Yung-Hui Li</u>** Assistant Professor, Dept. of Computer Science and Information Engineering, National Central University, Taiwan. Email: yunghui@csie.ncu.edu.tw Contact number: +886-03-422-7151 ext: 35204