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ANNUAL TECHNICAL FEST OF ELECTRONICS ENGINEERING SOCIETY

ROUND-1

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Part 1 : Smart EVM Machine

You went to cast your vote for the annual committee elections in Kashi Local Town Hall , however you found out that they still use old school paper and pen based ballot elections .

This has already caught the attention of many townsmen , who criticize the present systems of elections . Pen and paper based ballot elections have lost the faith of the citizens due to cheating in the elections , and have ultimately caused removal of faith from the election system in the city itself .

As a proponent of “Smart Kashi” and a technically budding and aspiring engineer , you decided to take this problem into your hands and make a digital electronic based solution for the same .

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You are required to implement a Proteus simulation and a PCB design for this
"EVM – Electronic Voting Machine" , and further restore peace to the city of Kashi .

Circuit Requirements:

- The bare minimum requirement of this circuit would be to be able to store the value of the number of votes of the candidates standing in elections , when the button is pressed the number of votes should increase by 1 for that candidate.

- You are required to make an EVM assuming **4 candidates** only. The schematic should be made using Proteus and the PCB using EagleCAD.

- The simplest solution is attaching 4 push buttons to counters which is also an acceptable solution , but to score more points you are required to think of innovative features that can be added to such a machine .

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Circuit Requirements:

- Two mandatory features are:
  - Keep a count button which once pressed compares the votes of the 4 candidates and displays the votes of the winner and the winner as logic-probes. (0 if first candidate wins, 1 if second candidate wins and so on)
  - Disable the machine for the next 3 seconds every time a push button is pressed. This is to account for debouncing which happens in real push buttons.
- Example optional features (you can come up with more):
  - Multiple candidate voting allowed. (Let each candidate have a total voting time of 15 seconds within which he can vote for any number of candidates but at most one vote per candidate. Remember to disable the machine for three seconds every time a button is pressed)
  - Reverse the last vote casted by a candidate.

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Part 2 : Exploring the Ghats of Kashi

The first college semester is over and the enthusiastic freshers are out on the streets of Kashi to explore!!

Manali, one of them, is now eager to explore the mesmerizing ghats at night on foot, with her friends. A fun fact for those who have never been to the ghats of Kashi, they are all connected in a straight line.

So to start off, she calls up her friends to know the starting ghat of their expedition.
Within an hour they all assemble at the starting point and now Manali wonders, on which ghats they should stop at and spend some time (probably vibe to songs).

As a proponent of “Smart Kashi”, you have provided them a list of the main ghats where tourists visit but in a unique way.

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At the starting point, they choose a random direction and start moving. When they reach a ghat where they should stop, they get to know the name of the next ghat to stop at and the previous ghat they stopped at. This list continues until the next forward stop is given as the Ganga.

Unfortunately, this leaves out the ghats in the other direction. So to save time, they take an auto and go back to the starting ghat and then start walking in the opposite direction until again the next stop becomes the Ganga, at which they go to Kashi Chat Bhandar for refreshments.

Manali wants you to tell her the **least time** they spent among all the ghats and **the ghat at which they spent the least time**.

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Task:

- The above storyline resembles a data structure called **Doubly Linked List.**

- You are given an array of elements in a binary file which will be stored in a ROM (2732).

- Now, every node of the list has three parts-
  1. At Address X ===> The 8 bit data (time spent)
  2. At Address X+1 ===> The 5 bit address of the next node (next ghat)
  3. At Address X+2 ===> The 5 bit address of the previous node (previous ghat)

- You are given a 5 bit starting point address of the starting node in the list through logic-states.(Not necessarily head of the list)

- If the address of the next node/previous node is 255 then it signifies the tail and head of the list respectively.

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Task:

- To find the node containing the minimum data you have to traverse the entire list in both the directions from the starting point and find the minimum data. You are free to come up with your own approaches as well to traverse the list.

- If the minimum data is in two nodes, then the answer will be the node with the **least absolute address**.

- The objective will be to complete the following task with **minimum hardware cost**.

- Display the **minimum data** and the **address of the node containing the minimum data** through logic-probes.

Significant Bonus points - Use seven segment displays to display the answers (cost not included)

Constraints:

0 <= Data <= 255

0 <= Address of Node <= 29

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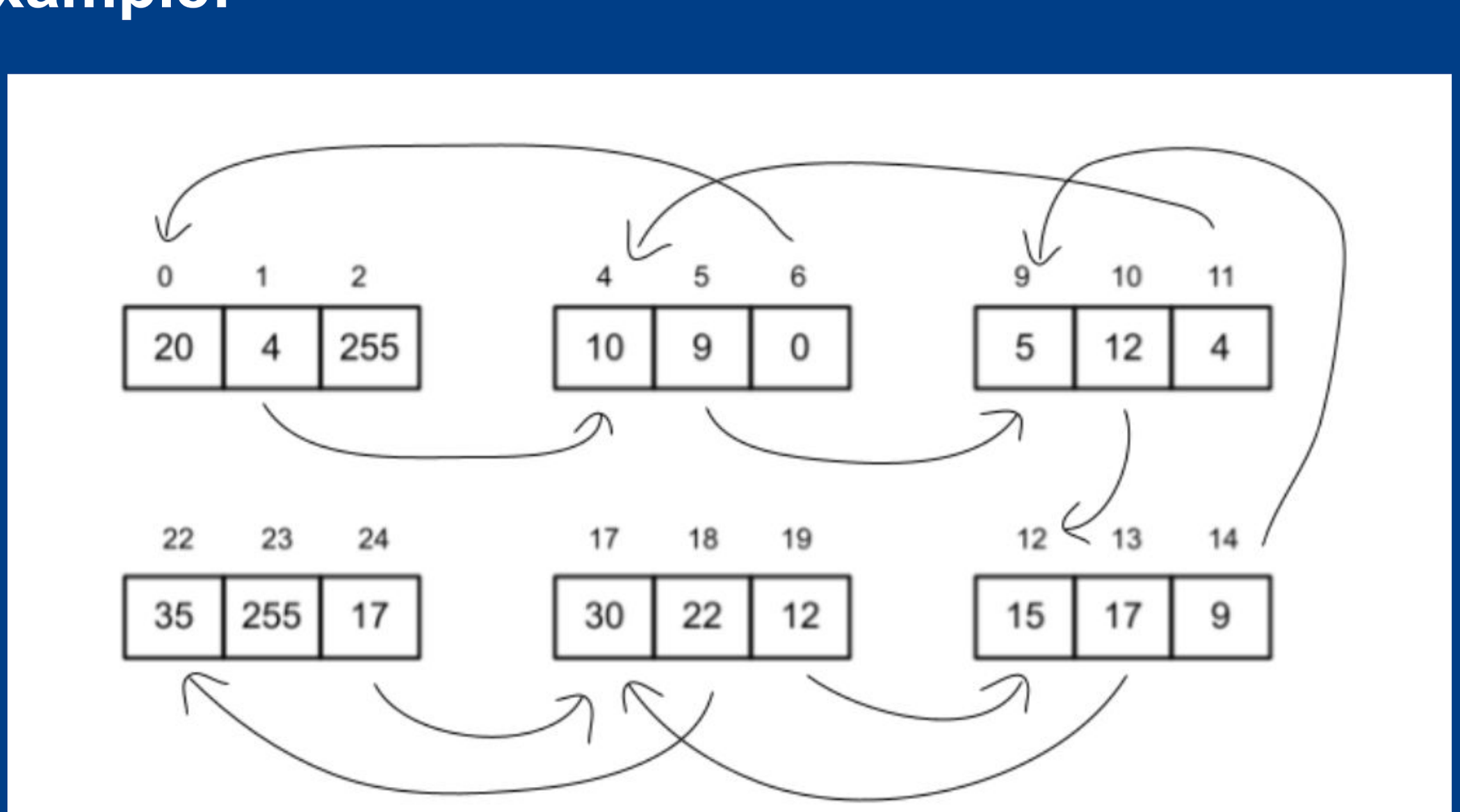
Example:



Given array:

[20,4,255,8,10,9,0,6,2,5,12,4,15,17,9,1,2,30,22,12,19,18,35,255,17]

Start Point = 01001 = 9 in decimal

Let the **input starting point** be **address 9** taken through logic states.

Now we can take any random direction, say right, and traverse till the end of the list. So at address 9, data is 5. Now the address of the next node is at address 9+1=10. So the next node is at address 12. Now you go to address 12 which has data 15 and address 12+1=13 has the address of the next node which is 17 and so on till the address of the next node is 255.

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Example:

Now time to travel in the opposite direction, left, to the beginning of the list. Start from the input starting point again at address 9. Now the address of the previous node is at address 9+2=11. So the previous node is at address 4. Now you go to address 4 which has data 10 and address 4+2=6 has the address of the previous node which is 0 and so on till the address of the previous node is 255.

While traversing, update the minimum data and the **answer** here is **5** at **address 9** itself.

(*If the data 10 of node at address 4 is replaced by data 5, then the answer would have been 5 at address 4 instead since 4 < 9.*)

Binary File for this example:
https://drive.google.com/drive/folders/1grLkKMn3MZ1P_hP4wqZKUAEg2dcqCi0I?usp=share_link

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List of components allowed:

ROM (2732)

Comparator (7485)

Register (74179/74194)

Adder (74283)

Multiplexer (74157/74153)

Counter (74LS590, 74161, 74163, 74LS169)

Decoder (74LS139/74HC154)

Encoder (74HC148)

Buffer (74HC241/74125)

Flip flops (74273/7474, 74LS175, 74LS109)

BCD to 7 segment decoder (74LS347/7448)

7 Segment/BCD Display

Logic Gates

Clock

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Cost of Components:

IC	COST
ROM(2732)	75
Clock	40
74273	4
7485, 74283, 74157, 74153, 74179, 74194, 74161, 74163, 74LS590, 74LS169, 74HC154, 74HC241, 74LS175, 7448, 74LS347	2
74LS139, 74HC148 ,7474, 74LS109	1
3 input Logic gates	0.2
Logic gates, 74125	0.1
Logic states, Logic probes	Free

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Evaluation Criteria:

- A maximum of **350 points** will be awarded to the team on completing Part 1 and **650 points** on completing Part 2.

- For Part 1, points will be given based on the innovative thinking and the implementation of features.

- For Part 2, the cost of the circuit will be deducted from the score obtained.

- Bonus marks (max **300 points**) will be given based on following factors:

  1. Time taken for submission
  2. Addition of innovative features (seven segment display)
  3. Readability/Clarity of circuit and its labelling
  4. Technical complexity/efficiency
  5. Structure and reusability

- If multiple ROM(s) are used all of them shall be fed with the same binary file.

- Simulations based on components other than the ones specified should be avoided.

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Submission Instructions:

- The deadline for completion of PS-1 is – **22nd March, 2023 EOD**.
- You are required to submit the folder drive link OR Github repo link consisting of two folders Part 1 and Part 2:
  - Part 1:
    - A PDF file having a list of features you have invented as well as implemented in the schematic as well as the PCB . The features must be well documented with photos as well as explanation in the pdf.
    - The Proteus DSN files/Project , the Proteus simulation video(screen recording) , the Eagle Schematic File , the Eagle Board file and the Gerber Files.
  - Part 2:
    - A PDF file containing description of your approach, the number of each component used and the total cost in a tabular format.
    - Screen Recording of the circuit for the given example list.
    - The Proteus Design file or the project file

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