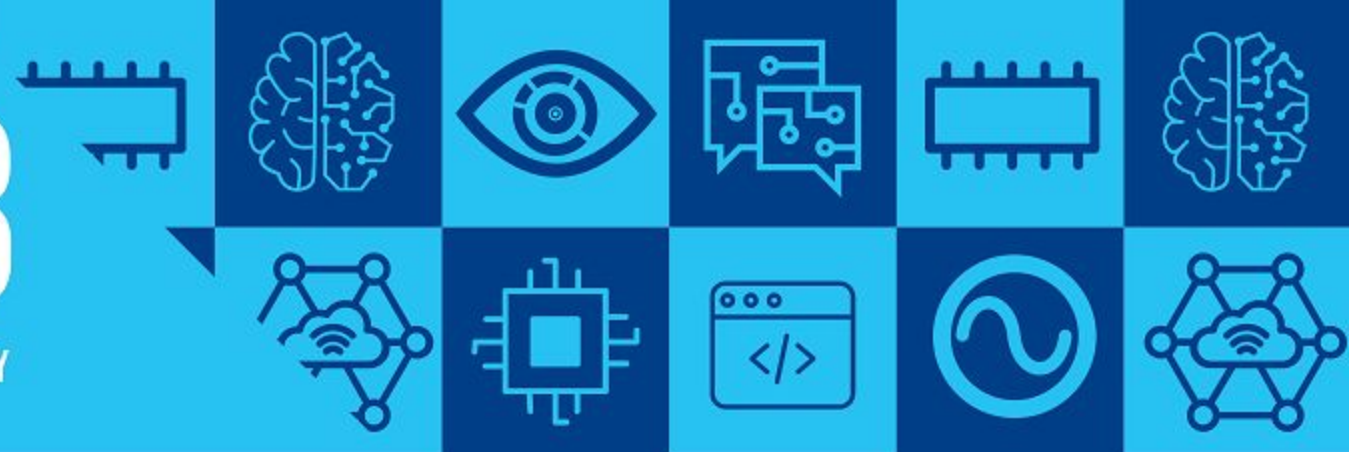




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## ROUND-2

# DIGISIM

Hope you enjoyed solving the PS1 of Digisim based on EVM , PCB Design and doubly linked list . Now get ready for Round 2 .

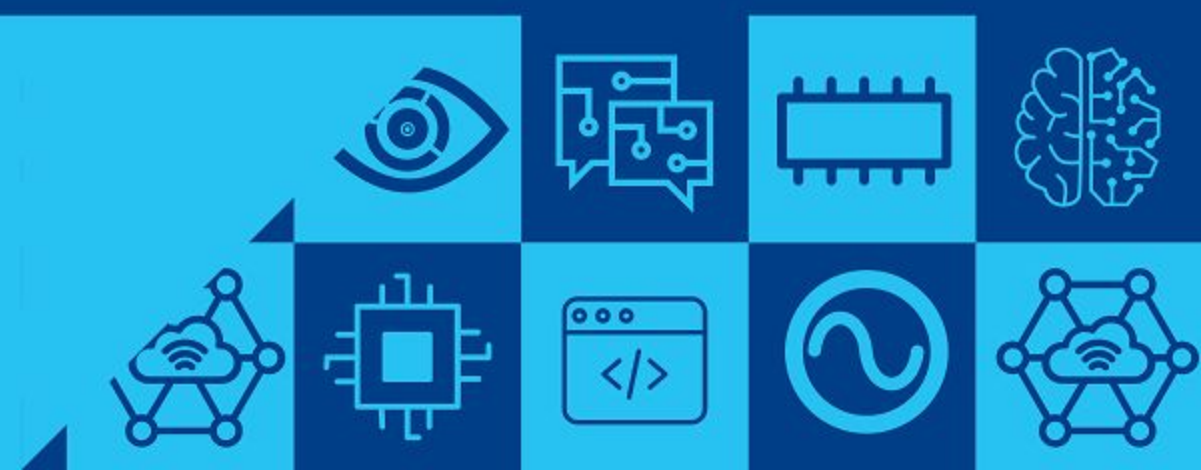
Manali and her friends from PS1 are awestruck by the solutions you made but they now face the wrath of a dangerous black-hat hacker Mr Hexplex0xff who is a vehement opposer of the steps taken towards a Smart City Kashi.

To prevent the hacker from tampering with the data of the linked list containing the ghat stops and the time at each ghat, you decided to convert the linked list into a simplified model blockchain by:

- Making it a singly linked list with only the next ghat address at each node.
- Hashing the address of the next node by cyclic shifting right by 3 bits.



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## DIGISIM

But unfortunately, as the hashing algorithm was weak and Mr Hexplex0xff was highly skilled in exploiting vulnerabilities, he successfully tampered with the blockchain and modified the next address of the last tail node and made a loop in the blockchain by pointing back to a previous node.

Mr Hexplex0xff has openly claimed that he has successfully done the above and effectively destroyed Manali and her friends night expedition, by sending them in an infinite loop.

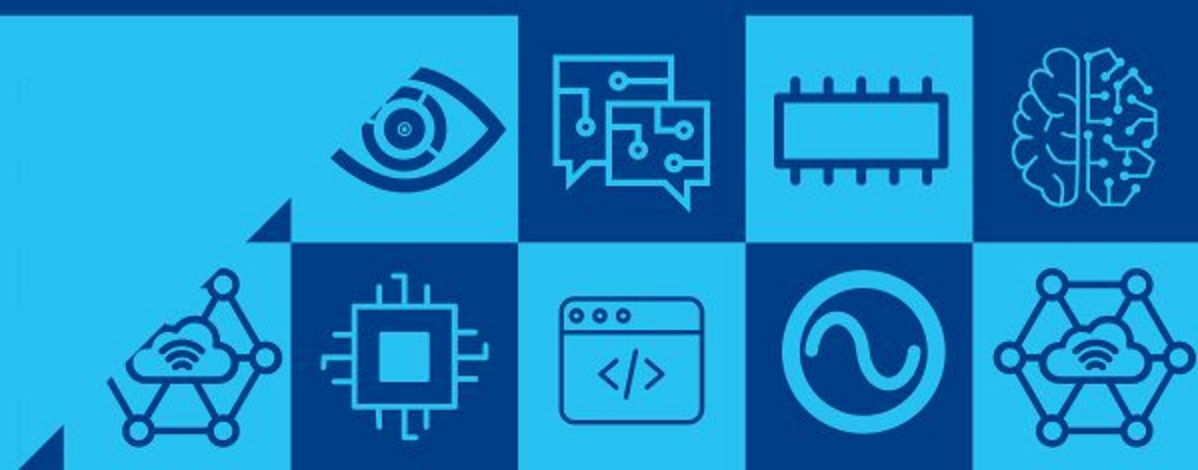
It is time for you to step in and save the day again.

Manali wants you to first **detect** if the hacker is speaking the truth and has indeed been able to tamper with the data and **create a loop**.

If he has indeed done so, then Manali wants you to further **find the node where the original tail node points to now**.



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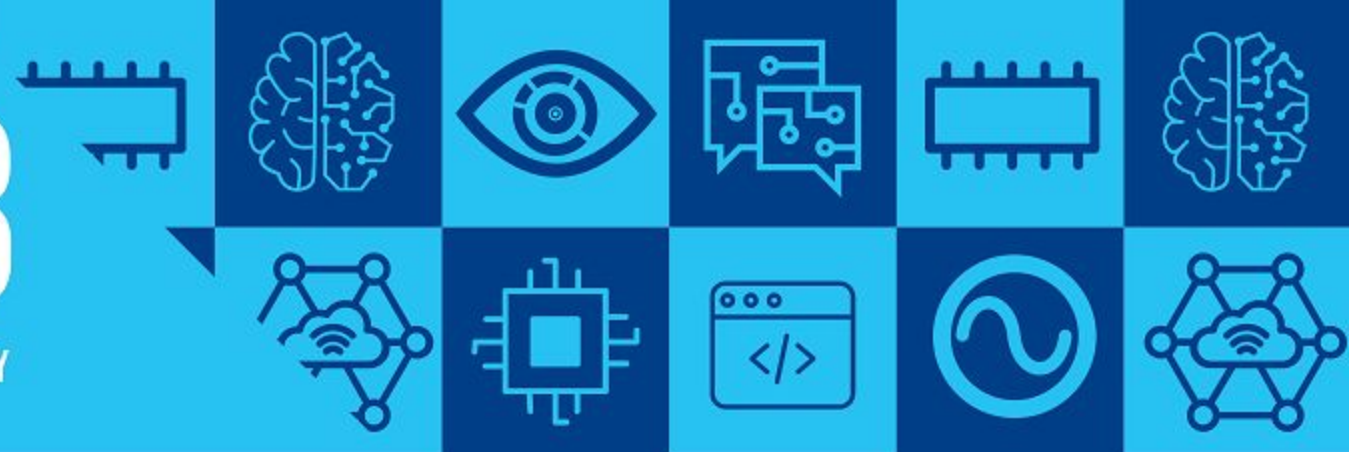






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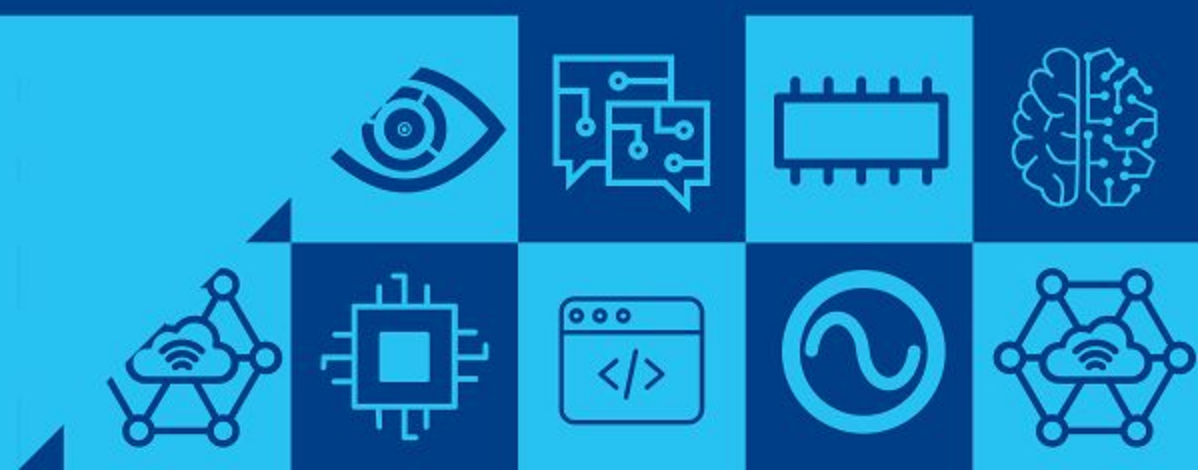
## DIGISIM

### Task:

- The above storyline resembles a simplified blockchain or in other words a **singly linked list** with the **next node address hashed**.
- Hashing has been done by **right cyclic shifting** of the next node address by **3 bits** assuming an 8 bit number.
- You are given an array of elements in a binary file which will be stored in a ROM (2732).
- Now, every node of the list has two parts-
  1. At Address X ==> The **unhashed** 8 bit data (time spent)
  2. At Address X+1 ==> The **hashed** 5 bit address of the next node (next ghat)
- You are given a 5 bit **unhashed starting point address** of the first node in the list through logic-states. (**Head of the list**)
- If the address of the next node is 255 then it signifies the tail of the list which obviously means that there is no loop in the list.



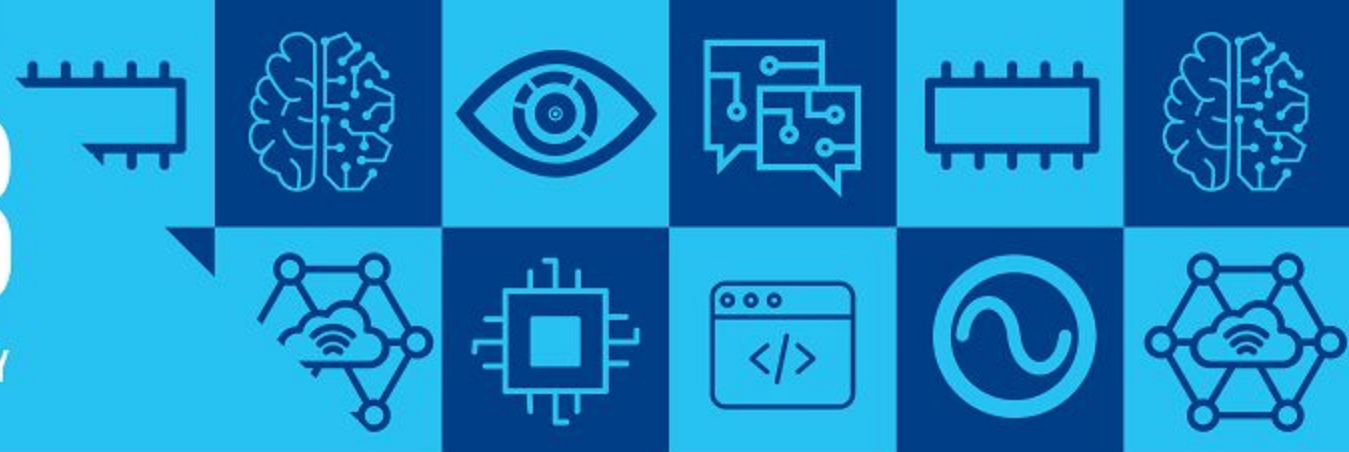
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## DIGISIM

### Task:

- You have to first detect whether a cycle exists in the blockchain and if it exists the same circuit should also be able to find and display the node where the original tail node points to.

*Hint :* [Use Floyd's cycle finding algorithm](#)

- Display whether a cycle/loop exists using a logic-probe and also display the unhashed data and address of the node at which loop back occurs, using logic-probes.
- The objective will be to complete the above task with **minimum hardware cost**.

*Significant Bonus points - Use seven segment displays to display the answers (cost not included)*

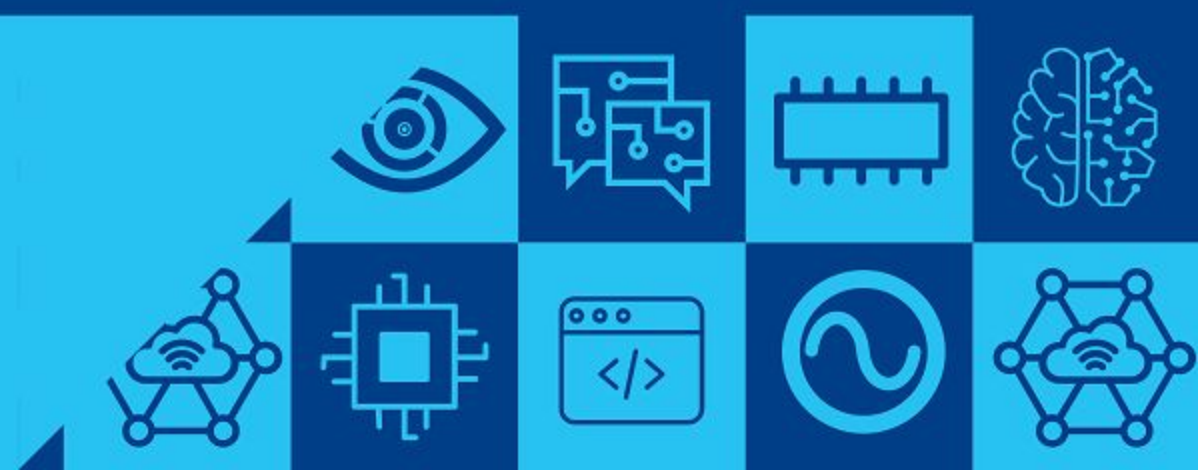
### Constraints:

$0 \leq \text{Data} \leq 255$

$0 \leq \text{Address of Node} \leq 29$



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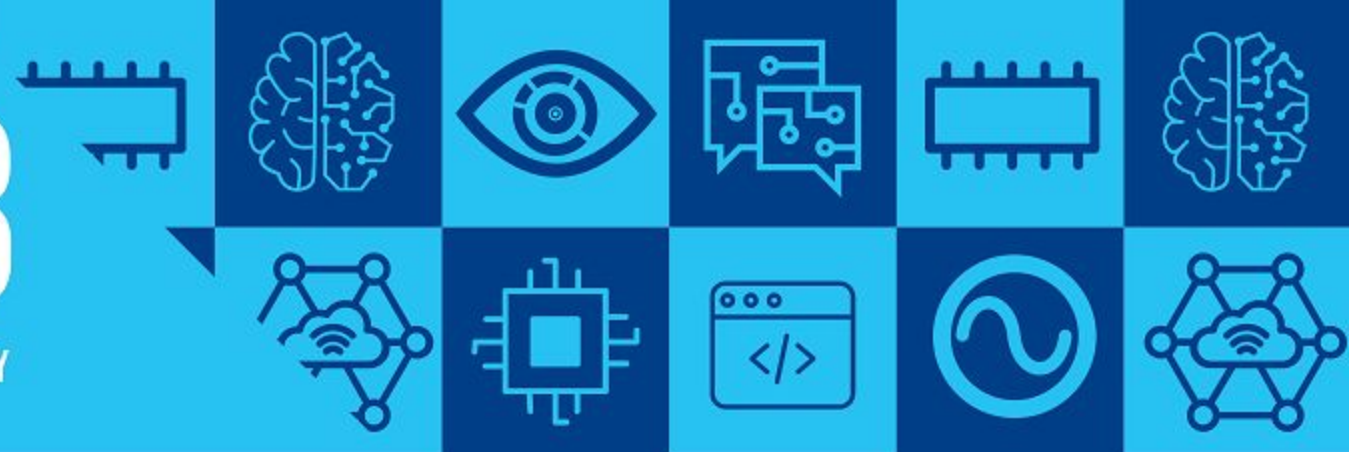






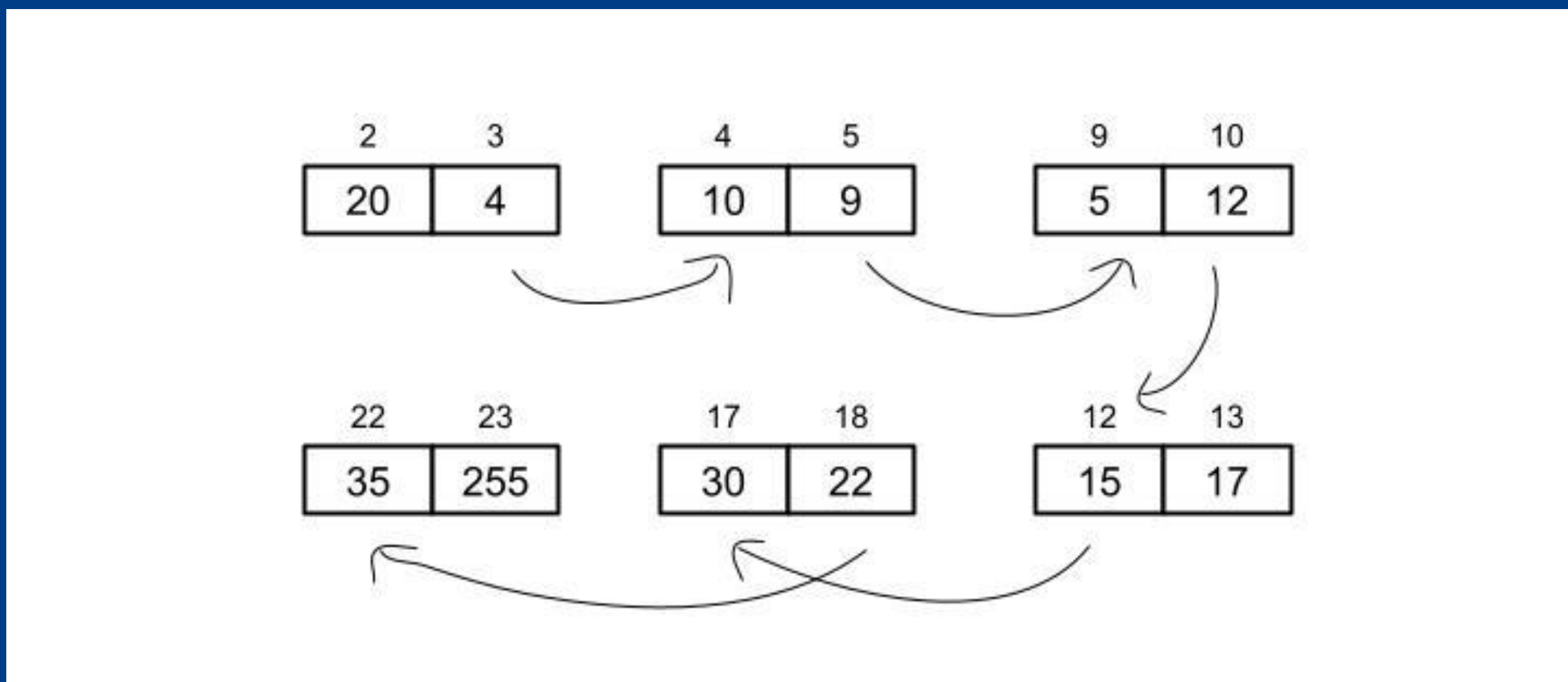
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## DIGISIM

Example:



Here as you can see there is no cycle so display 0 as answer through a logic-probe

Given Hashed array in the ROM:

[8,3,20,128,10,33,78,85,23,5,129,11,15,34,31,25,65,30,194,19,44,66,35,255]

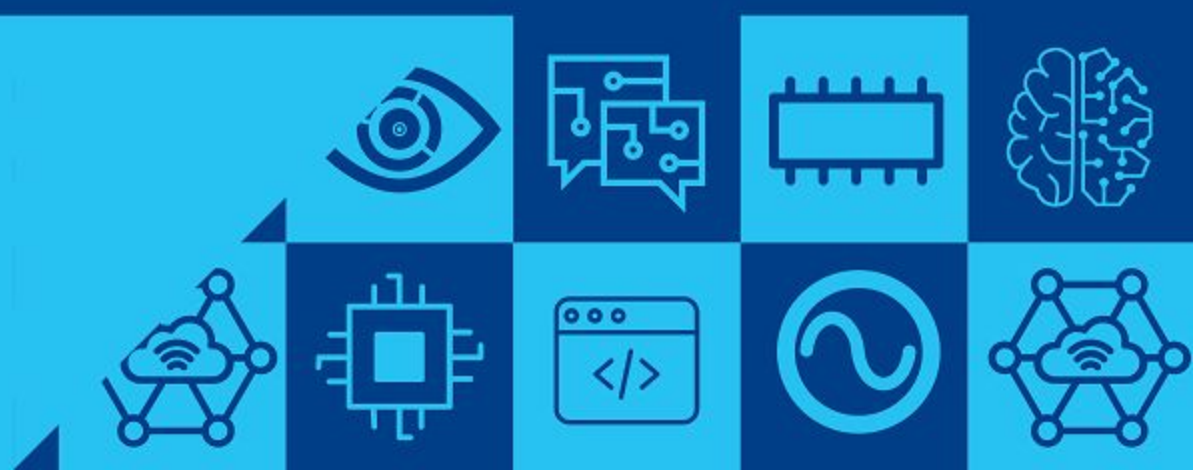
Corresponding Unhashed Array: (shown in figure)

[8,3,20,4,10,9,78,85,23,5,12,11,15,17,31,25,65,30,22,19,44,66,35,255]

Start Point (Head) : 00010 = 2 in decimal



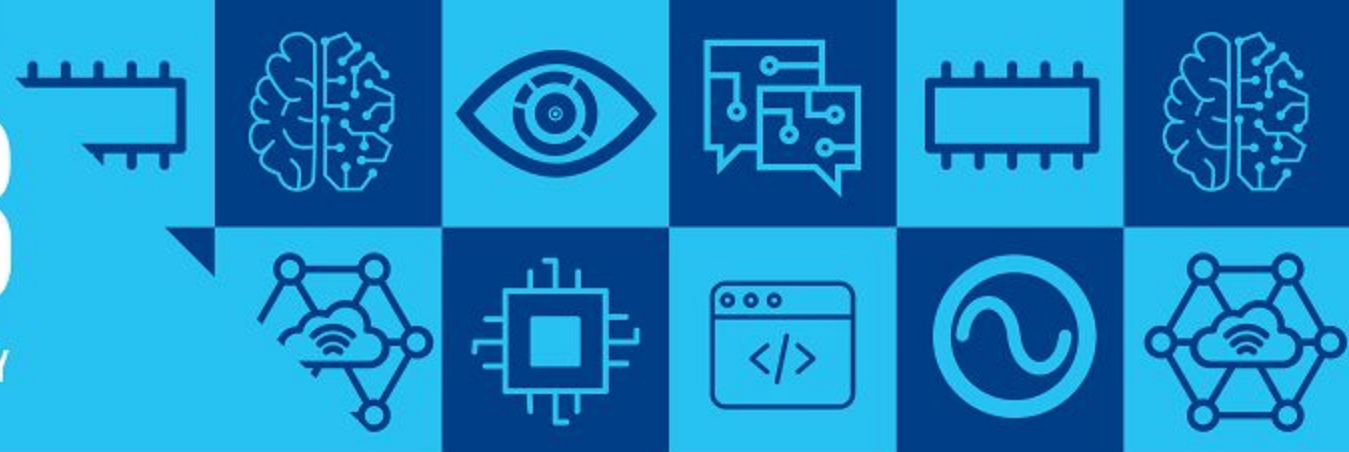
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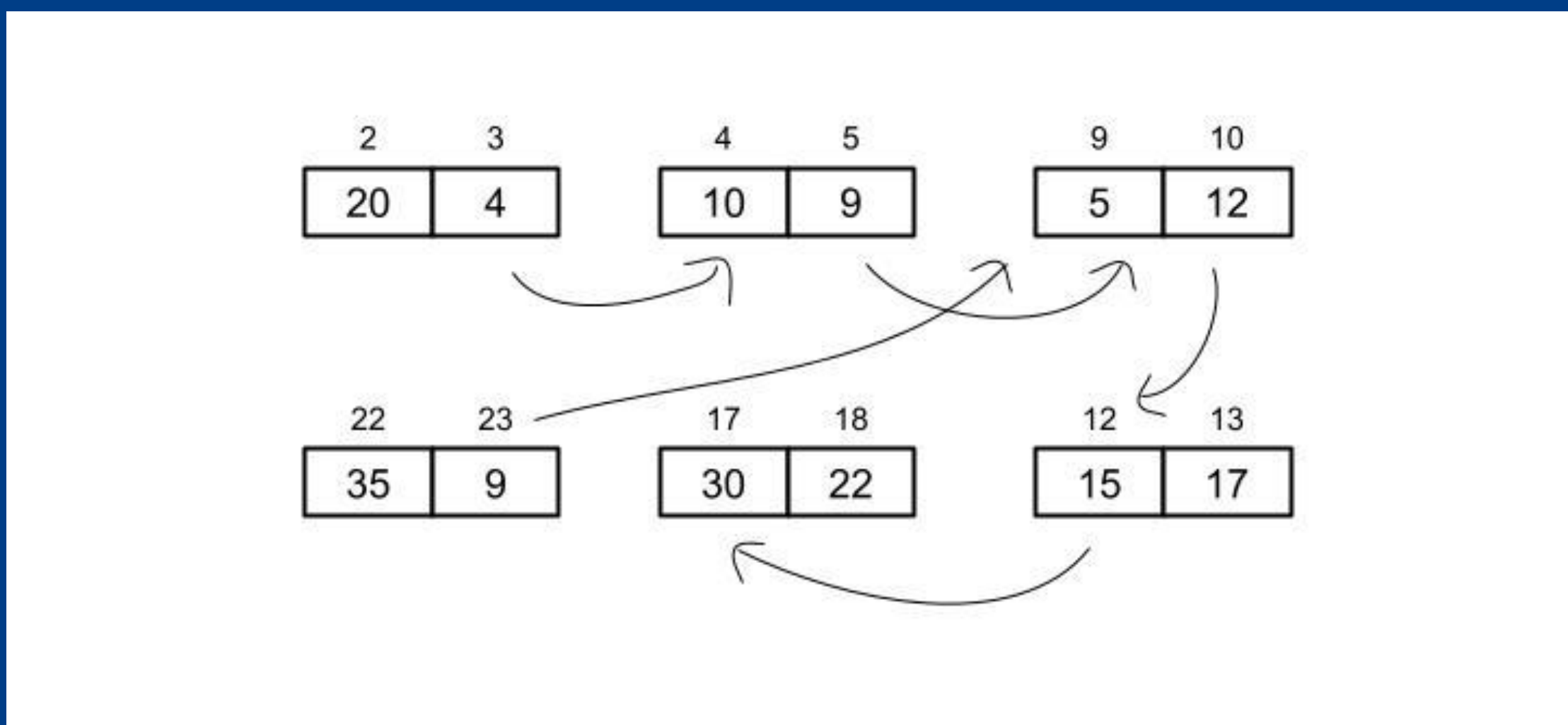
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## DIGISIM

Example:



Here as you can see there is a cycle so display 1 as answer through a logic-probe and the node at address 9

Given Hashed array in the ROM:

[8,3,20,128,10,33,78,85,23,5,129,11,15,34,31,25,65,30,194,19,44,66,35,33]

Corresponding Unhashed Array: (shown in figure)

[8,3,20,4,10,9,78,85,23,5,12,11,15,17,31,25,65,30,22,19,44,66,35,9]

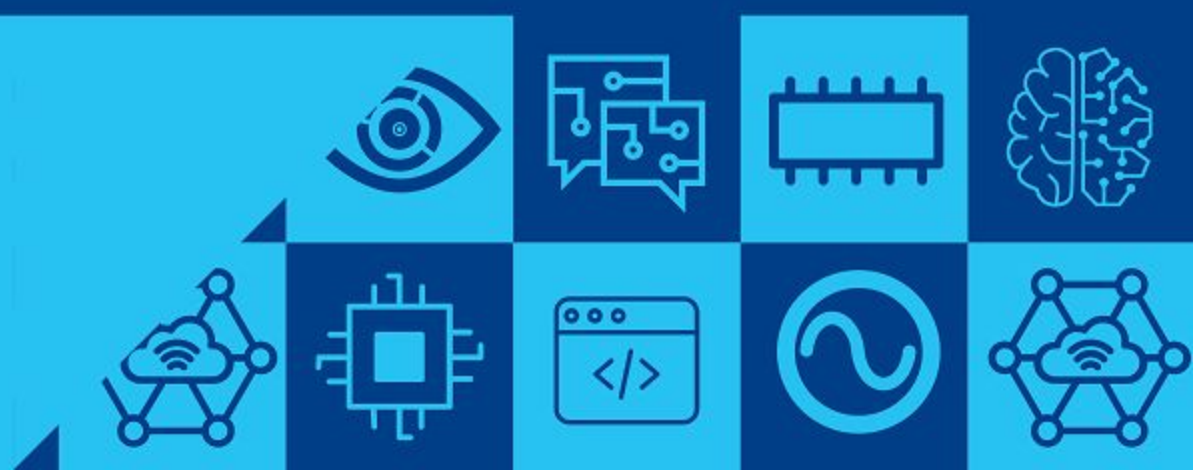
Start Point (Head) : 00010 = 2 in decimal

There is a loop in the list with nodes at addresses 9-12-17-22.

So the answer will be **1** for **cycle detection** and also display **data 5** and **address 9** since that is the node at which the original tail node at address 22 points back to.



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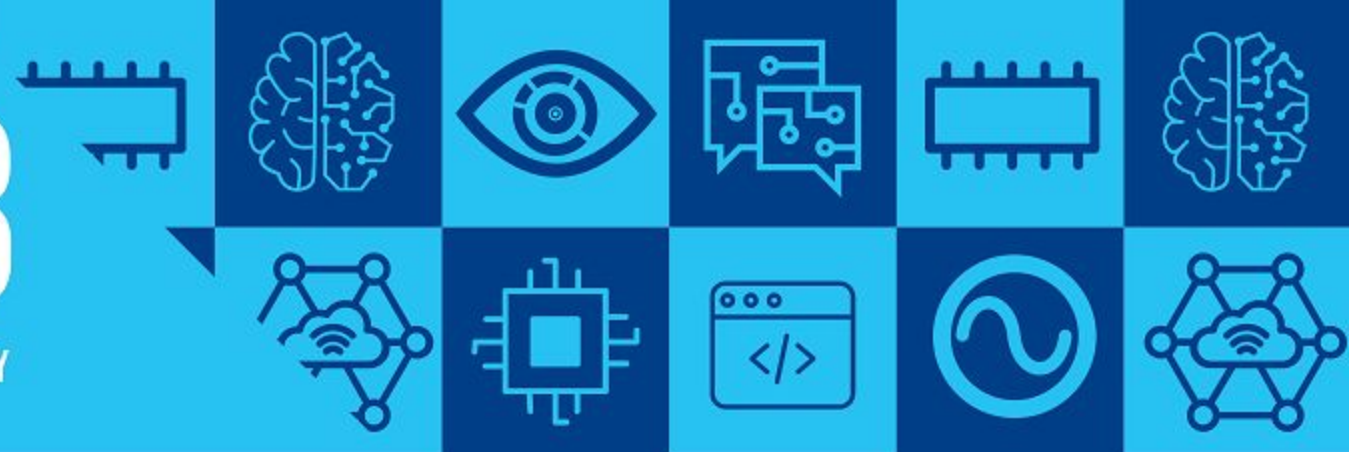






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## DIGISIM

### Hashing Example:

Hashing is done by cyclic right shifting by 3 bits, assuming an 8 bit number.

Only the address of the next node is hashed in every node.  
So only 9,12,17,22,9 will be hashed.

Unhashed Array:

[8,3,20,4,10,9,78,85,23,5,12,11,15,17,31,25,65,30,22,19,44,66,35,9]

4 = 0000100 -> hash -> 10000000 = 128

9 = 00001001 -> hash -> 00100001 = 33

12 = 00001100 -> hash -> 10000001 = 129 and similarly for the rest...

Corresponding Hashed array in the ROM:

[8,3,20,128,10,33,78,85,23,5,129,11,15,34,31,25,65,30,194,19,44,66,35,33]

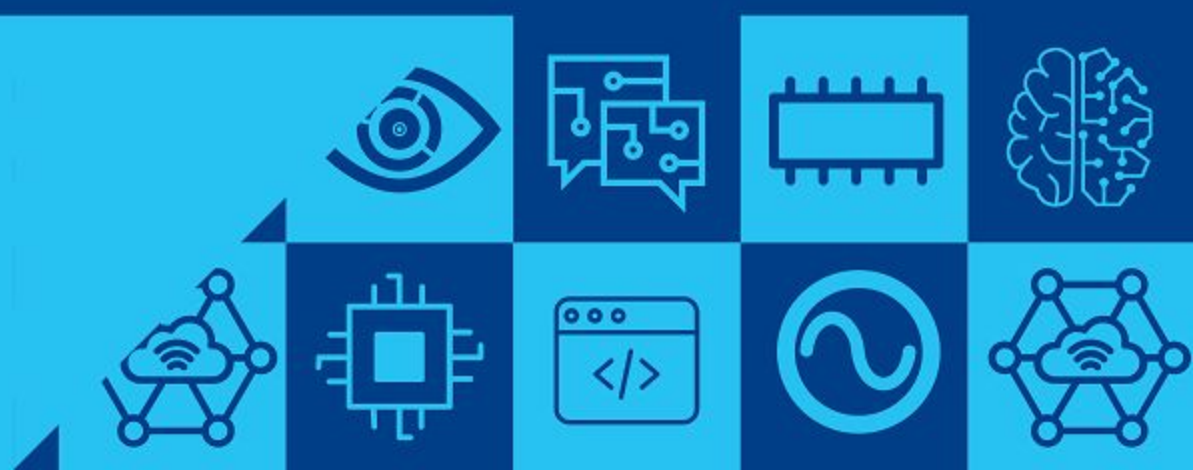
You will be given this **hashed** array in the ROM. Make sure that the answer you display is unhashed.

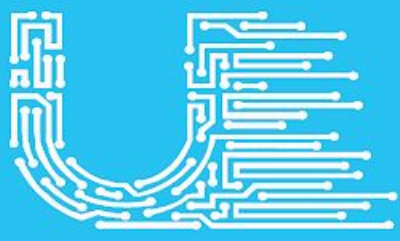
Example binary files :

[https://drive.google.com/drive/folders/1qAAucbAiocMsBr6LnX21P004nnrPyJpE?usp=share\\_link](https://drive.google.com/drive/folders/1qAAucbAiocMsBr6LnX21P004nnrPyJpE?usp=share_link)



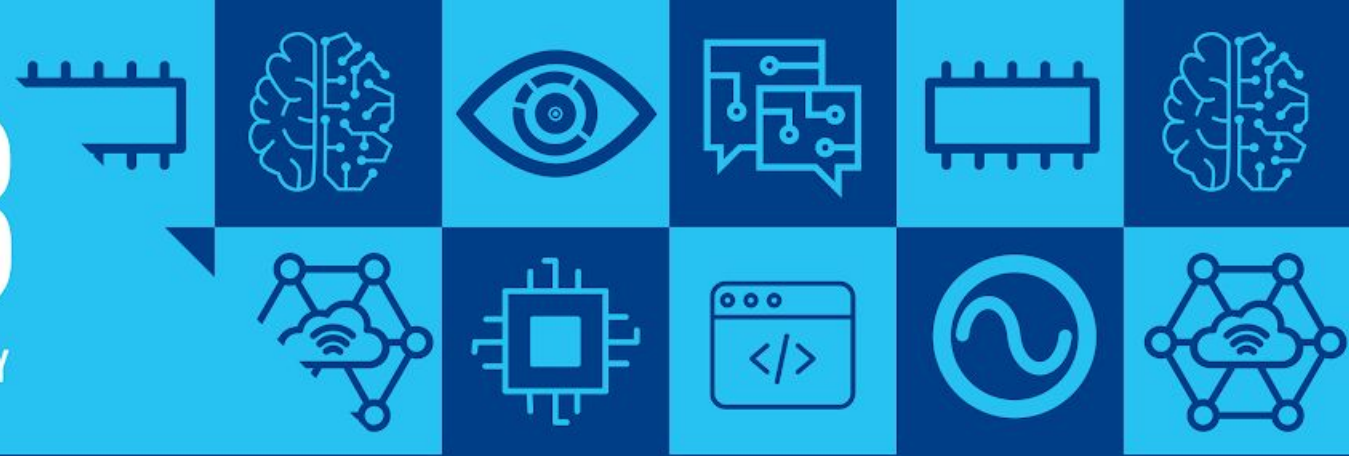
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## DIGISIM

### List of components allowed:

ROM (2732)

Comparator (7485)

Register (74179/74194)

Adder (74283)

Multiplexer (74157/74153)

Counter (74LS590, 74161, 74163, 74LS169)

Decoder (74LS139/74HC154)

Encoder (74HC148)

Buffer (74HC241/74125)

Flip flops (74273/7474, 74LS175, 74LS109)

BCD to 7 segment decoder (74LS347/7448)

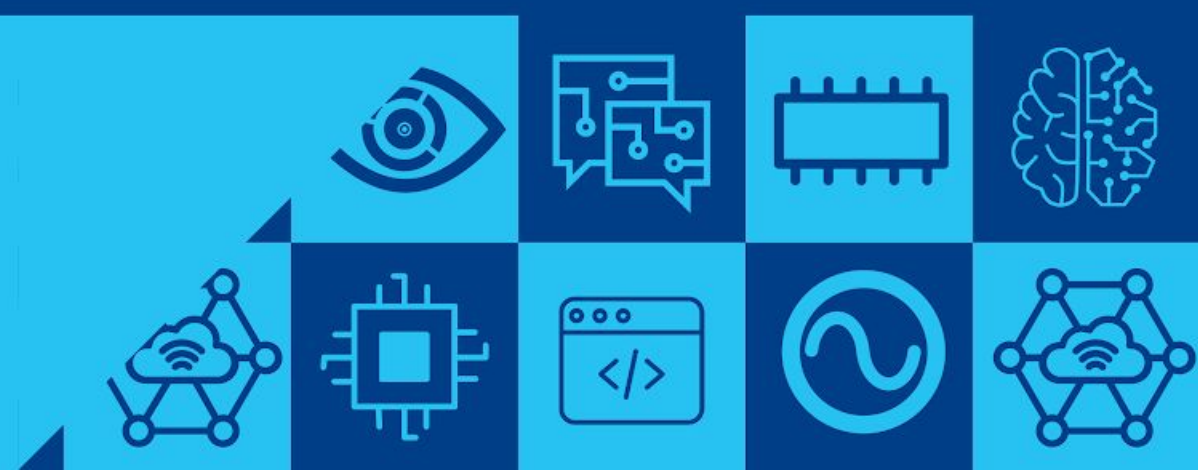
7 Segment/BCD Display

Logic Gates

Clock



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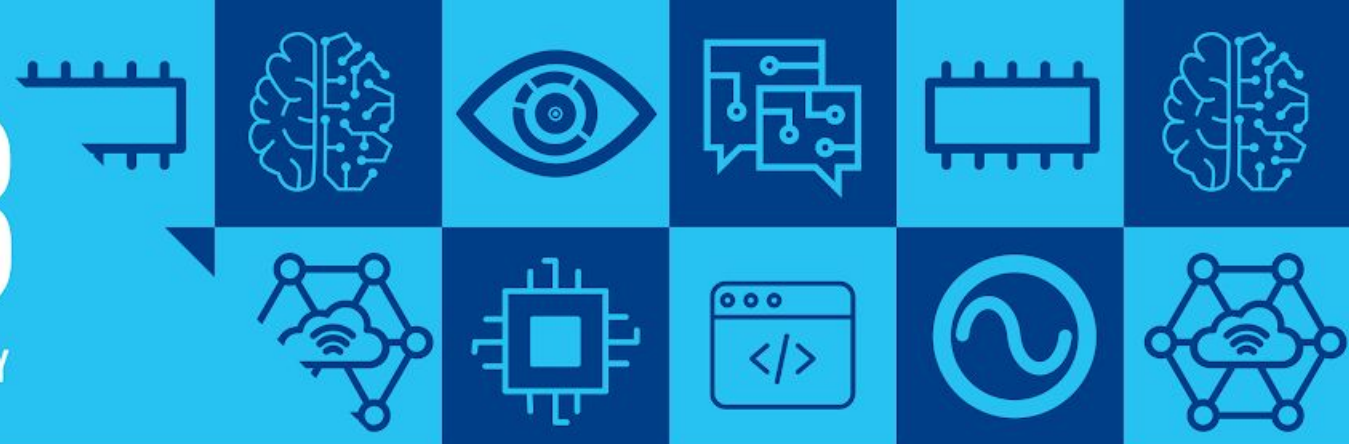






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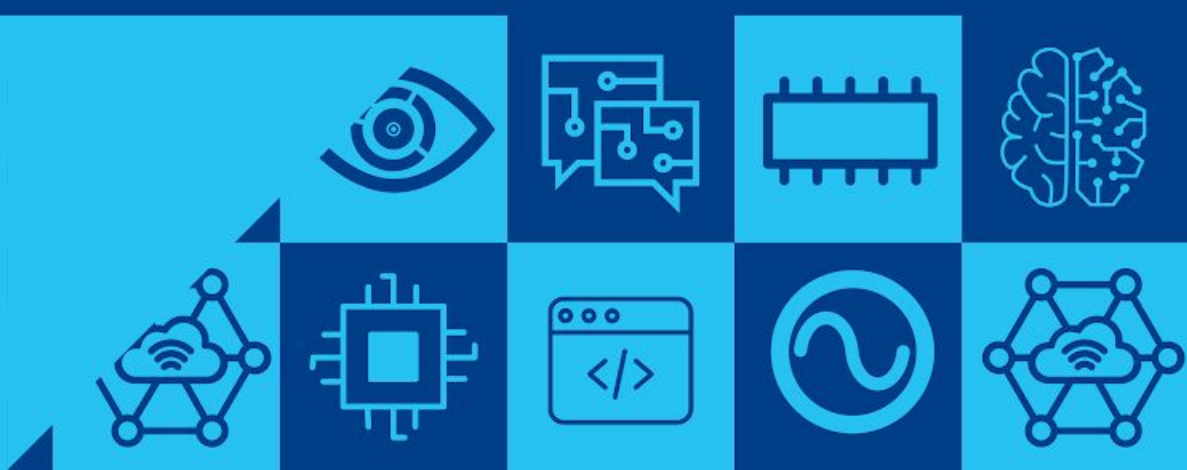
## DIGISIM

### Cost of Components:

IC	COST
ROM(2732)	75
Clock	40
74273	4
7485, 74283, 74157, 74153, 74179, 74194, 74161, 74163, 74LS590, 74LS169, 74HC154, 74HC241, 74LS175, 7448, 74LS347	2
74LS139, 74HC148 ,7474, 74LS109	1
3 input Logic gates	0.2
Logic gates, 74125	0.1
Logic states, Logic probes	Free



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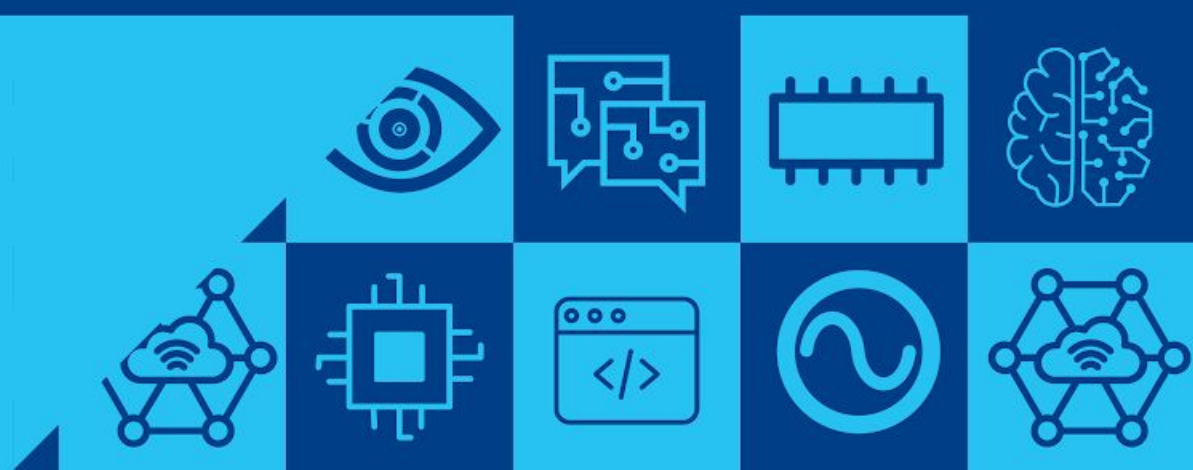
## DIGISIM

### Evaluation Criteria:

- A maximum of **400 points** will be awarded for cycle detection and **600 points** for finding the node where loop back occurs.
- The cost of the circuit will be deducted from the score obtained.
- Bonus marks (max **300 points**) will be given based on following factors:
  1. Time taken for submission
  2. Addition of innovative features (seven segment display)
  3. Readability/Clarity of circuit and its labelling
  4. Technical complexity/efficiency
  5. Structure and reusability
- If multiple ROM(s) are used all of them shall be fed with the same binary file.
- Simulations based on components other than the ones specified should be avoided.



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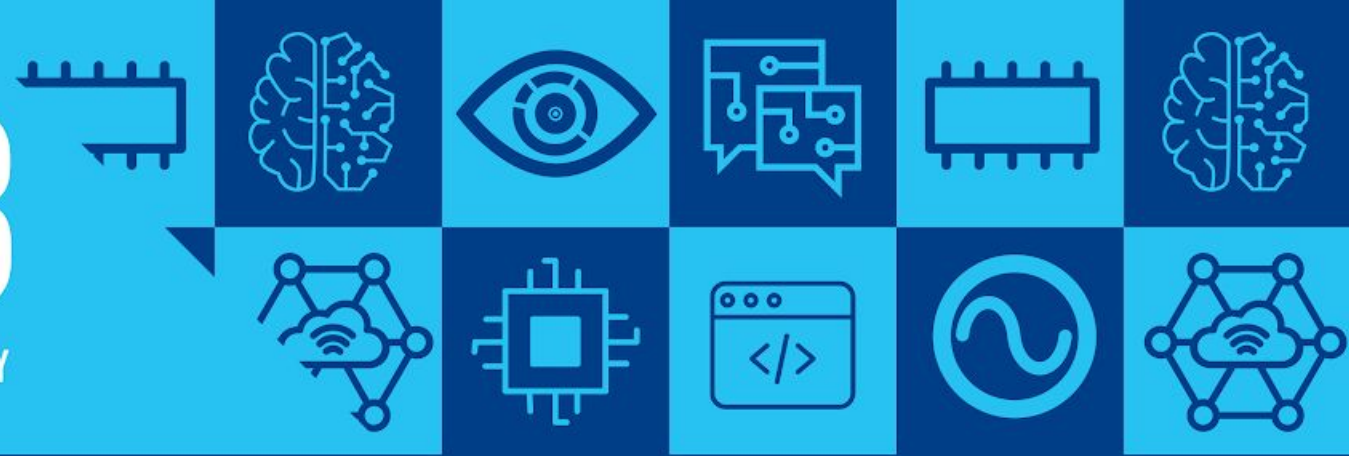






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## DIGISIM

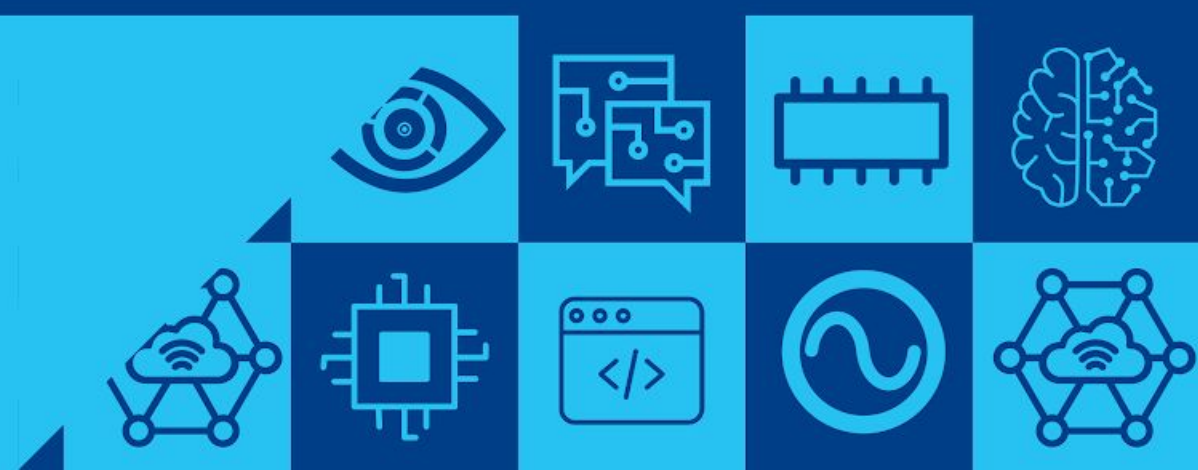
### Submission Instructions:

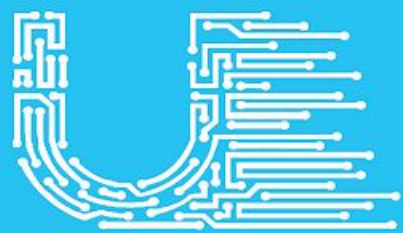
- The deadline for completion of PS-2 is – **8th April, 2023 EOD.**
- You are required to submit the folder drive link OR Github repo link consisting of :
  - A PDF file containing description of your approach, the number of each component used and the total cost in a tabular format.
  - Screen Recording of the circuit for the given example list with cycle.
  - The Proteus Design file or the Project file.

*Have Fun!!!!*



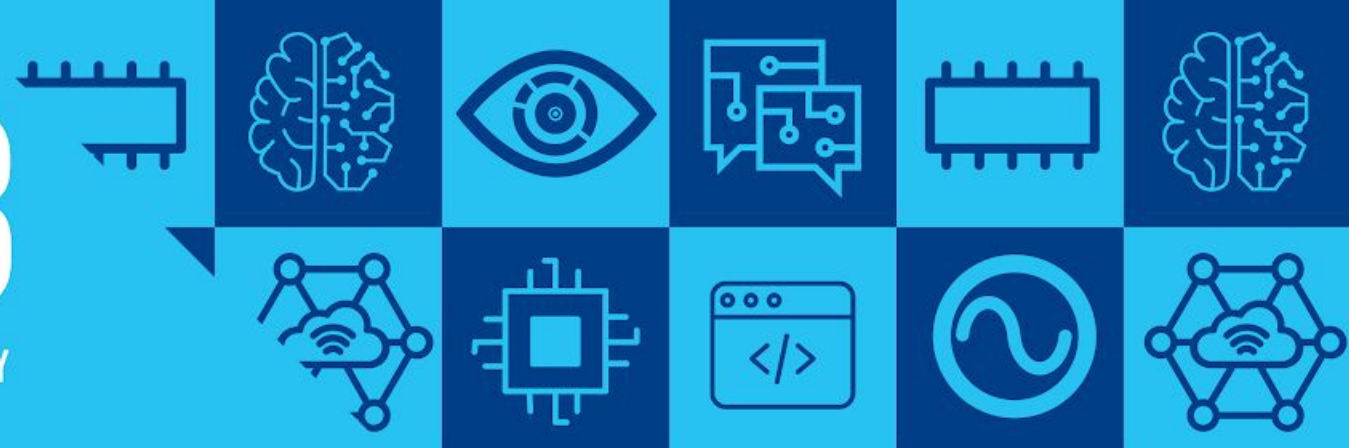
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## DIGISIM

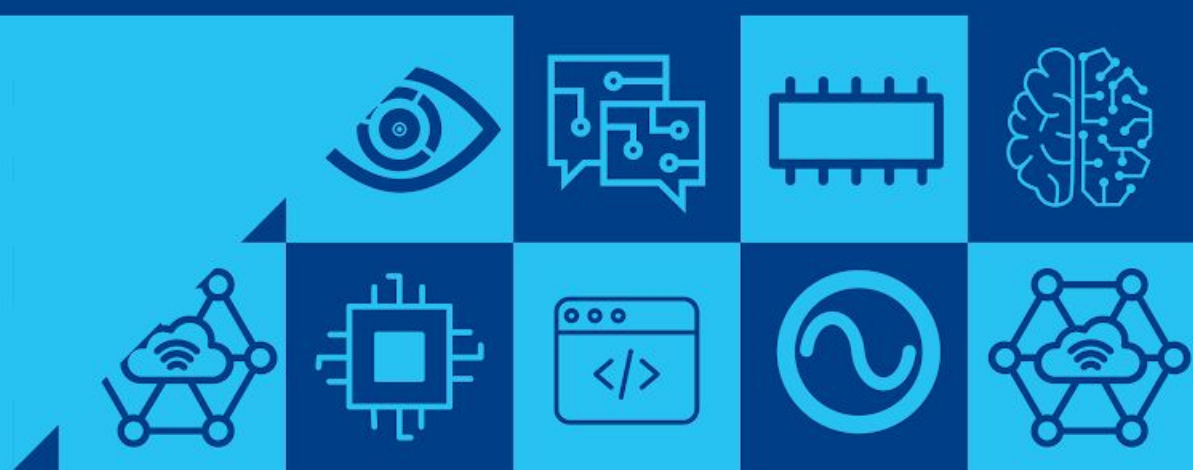
**For any doubts and queries feel free to reach out:**

**Ayush Agarwal**      (+919112647721)

**Sandeepan Ghosh**      (+919674130192)



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