Phase Lock Loop Design Project

Author
Aaron Brown
Boise State University
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Abstract

The goal of the project was to design a PLL, phase lock loop, that could output a wide range of higher frequencies based on a given reference frequency. The PLL needed to be able to lock to the desired output quickly and also produce a stable waveform. Other considerations for the PLL design were minimizing power, noise, and total capacitance.

1. Introduction

A PLL is a negative feedback network that uses four blocks, a (PFD) phase frequency detector, charge pump, (VCO) voltage controlled oscillator, and a divider. There is also a loop filter involved with the PLL that consists of two capacitors and one resistor making the system a type II, third order response. The input frequency that was used in this project was 6.25 MHz supplied from a proposed crystal oscillator. The desired output frequency was at least 100 MHz and higher, and the divider was set to a value of 16. The supply voltage for the PLL was set to 1.8v using an 180nm CMOS processes.

2. Stability Analysis

Two main requirements for stability were that the PLL's open loop response had a phase margin of 60 degrees. Phase margin is a measurement of the distance away from -180 degrees for phase plot at a frequency of Wu,loop, which occurs at unity gain. A phase margin of 60 degrees results in a control system with the fastest settling time compared to the amount of ringing that also occurs in the system. For comparison, a 90 degree phase margin wouldn't have any ringing but have a much longer settling time, while a 45 degree phase margin would have a large amount of ringing but a very fast settling time.

The second requirement was to have Wu,loop, the frequency at which unity gain occurs, be much smaller than the reference frequency in (rad/sec). In order to meet this a Wu,loop was chosen that was ten times smaller than Wref, where Wref was 6.25 MHz x 2π which equals 39.3 Mrad/sec. Both the phase margin and the Wu,loop values are a function of the loop filter parameters. The loop filter parameters are R, the resistance value, C1, and C2, the capacitor values, and the current passing through the loop filter, Io, which is controlled by the charge pump. Another two important parameters that affect Wu,loop and phase margin that exist outside the loop filter are Kvco, the linearity gain of the VCO, and the divider ratio. The divider ratio, N, was fixed at 16 and Kvco was measured to be 181.5 MHz/v discussed in section 3.1. The chosen loop filter parameters were then R = 6.25kOhms, C1 = 140 pF, C2 = 10pF, and Io = 50uA. Also see Table 4.1 for tabulated view of chosen parameters. With these values the phase margin was 60.241degrees and Wu,loop was 3.42 Mrad/sec which is less than a tenth of Wref at 39.3 Mrad/sec. Also the third pole of the system created by C2 was located at 17.14 Mrad/sec which is less than half of Wref. This third pole helps with filtering out noise rejection and classifies this PLL as a third order system, which is most commonly used in PLL design. One of the design tradeoffs was more bandwidth while sacrificing for a larger C1 value and power consumption from a 50uA current source. The open loop response with these chosen parameters can be seen below in Figure 2.1.

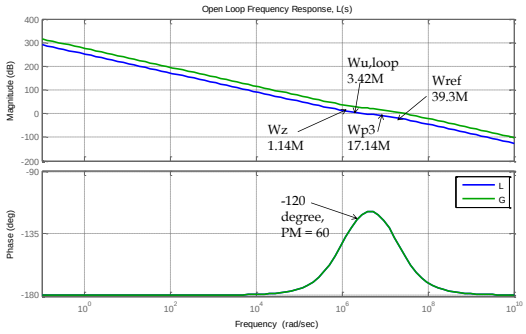

Figure 2.1: Plot of open loop response

The closed loop response can then be seen in Figure 2.2, which has a minimal amount of ringing but a fast settling time of about 3.5 us.

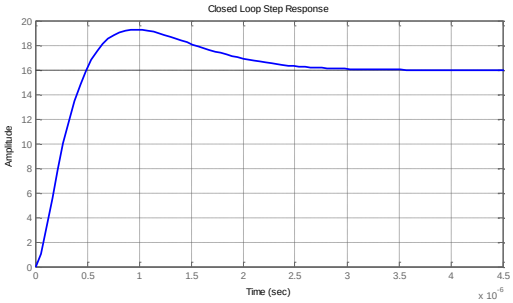

Figure 2.2: Closed loop response

3. Layout and Design

Once the stability analysis was complete and the loop filter parameters were chosen, the design phase could begin. Each of the four main function blocks needed to be implemented on the transistor level. An overall layout of the PLL can be seen in Figure 3.1 which shows the function blocks and the loop filter.

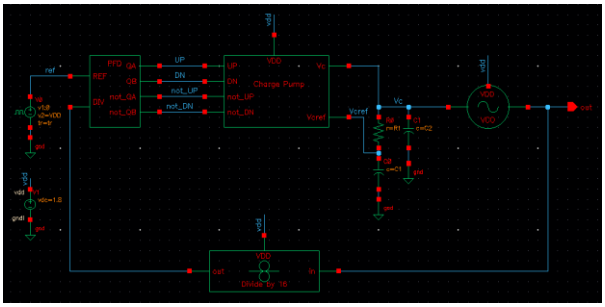

Figure 3.1: PLL Incremental Model

3.1 VCO Design

The first function block that was created was VCO which is the most complex block to create and is the most important in regard to stability and noise. The VCO was designed using a simple 5 stage ring oscillator where input voltage controlled a degenerated current source. As more current is supplied to the current starved ring oscillator, the faster the charge and discharge times become for the inverter stages which results in a higher output frequency. The transistor layout for the VCO can be seen in Figure 3.2.

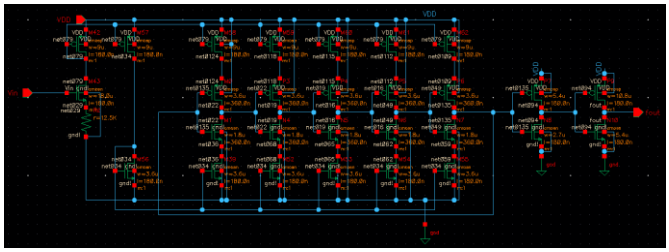

Figure 3.2: Transistor layout of the VCO

The right hand side of Figure 3.2 is the input which is using a current mirror configuration to biases the oscillator. The sizing of the degenerated NMOS transistor was made very wide so it would have a more linear voltage to current relationship. Also the resistance value on the source of the NMOS was selected so that when Vin was at about .9v, half of VDD, the output frequency would be 100 MHz, the minimum amount of desired output range. The sizing for the inverter transistors was made weaker than the current sourcing transistors to avoid fighting nodes. Also the output was driven by two buffers that increased in drive strength by a factor of 2.
The Kvco and frequency measurements for the VCO were done using PSS analysis in cadence. The plot results for Kvco and frequency output are seen in Figure 3.3. Notice that the maximum output frequency that can be achieved by this VCO is 230 MHz.

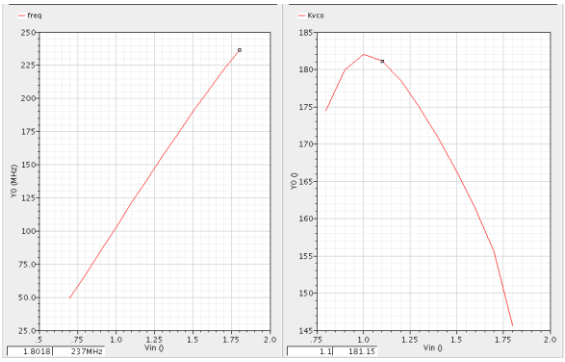

Figure 3.3: VCO Kvco and frequency plots

3.2 PFD Design

The PFD block controls the direction of current for the charge pump. The PFD has two inputs which are a reference frequency and an input frequency. If the reference frequency is leading the input then the UP signal has the highest average active time while if the reference frequency is lagging the input then the DN signal has the highest average active time. The other outputs from the PFD are the inverse signals of UP and

DN which also feed into the charge pump. The layout for the charge pump can be seen in Figure 3.4.

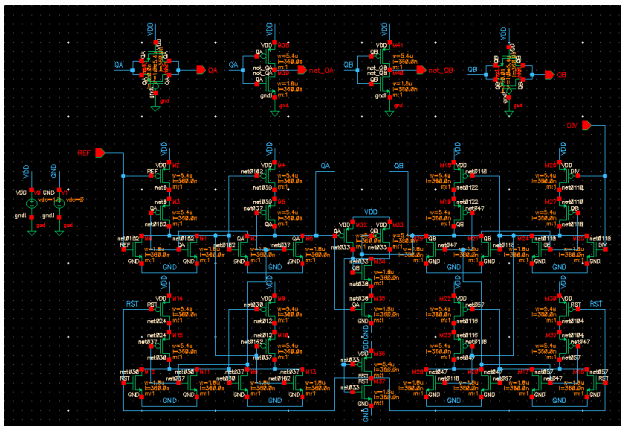

Figure 3.4: Transistor layout of PFD

Also in Figure 3.4 it's possible to see how the output signals are fed out of the device with inverse signals using an inverter and regular logic signals using a buffer. This is done to avoid having inverted logic signals lagging regular logic signals which could create disturbances in Vc, the input to the VCO. Figure 3.5 shows the plot of the average difference of UP and DN verses phase difference between the reference and input.

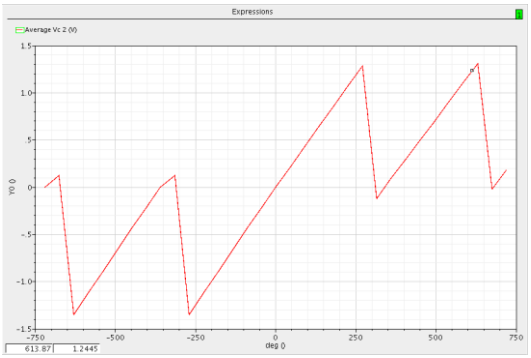

Figure 3.5: PFD phase plot

The phase plot in Figure 3.5 shows that both phase and frequency can be tracked since average output is always positive when reference rises eariler than the input and average output is always negative when reference rises latter than the input.

3.3 Charge Pump Design

The charge pump is basically a current switching system that either pushes current into the loop filter if UP signal is high or pulls current if DN signal is high. By pulling and pushing current the charge pump does the difference operation between the UP and DN signals of the PFD. When current is passed through the capacitors in the loop filter a voltage potential is created across the capacitor which is the integration of the time varying current. The overall result is when the feedback reference is higher than the reference, the Vc voltage drops and if the feedback reference is lower than the reference, the Vc voltage rises. Figure 3.6 shows the layout for the charge pump.

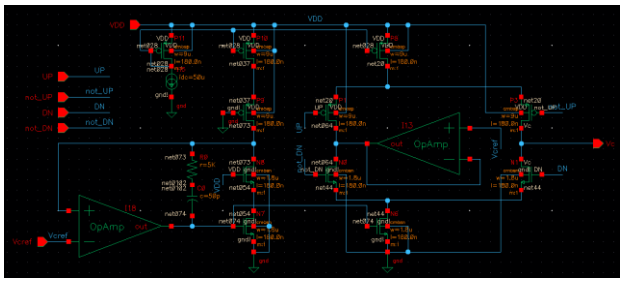

Figure 3.6: Transistor layout of charge pump

This specific charge pump topology assures that current is always flowing, so instead of being shut off it is simply redirected. Always having the current on avoids problems in mismatch where channel length modulation could create problems in stability for Vc. The transistors act as active high switches where if UP is on, current is pushed into the loop filter and if DN is on, current is pulled from the loop filter. If both DN and UP are off however current can still pass just not through the loop filter. Biasing is very important for this topology which uses a follower operation amplifier on the right side of the schematic and reflective mirror biasing with negative feedback support on the left side. Both amplifiers are ideal as well as the current source which replaces the presence of a BMR reference device. The current source is 50uA, the Io value discussed earlier in section 2 for control stability. There are two high impedance nodes in this layout so to compensate the system a capacitor in series with a resistor is used to connect the two nodes. The Vcref value is the average value of Vc, which is pulled from the loop filter between the first resistor and capacitor, depicted in Figure 3.1.

3.4 Divider Design

The divider's function is to take an input pulse and divide its period down by 16 in this case. This procedure can be achieved by using transistor level latches. First, a divider that could scale pulse's time periods down by a half was created, then this divider would be connected in series four times to get the desired 16 divider. The layout for the half divider is shown in Figure 3.7.

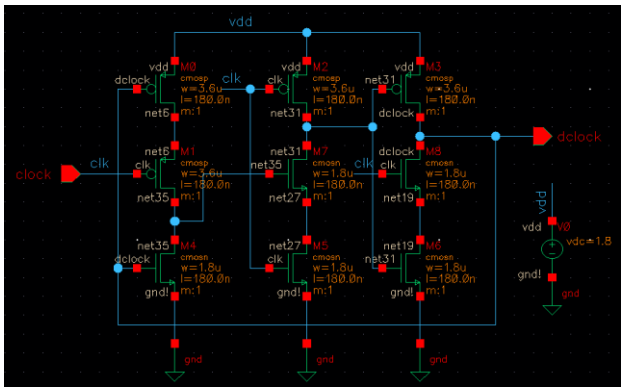

Figure 3.7: Transistor layout of half divider

The full 16 divider is shown in Figure 3.8 which also buffers the output. If the output were not buffered then the PFD would distort the signal too much and locking would not be achieved.

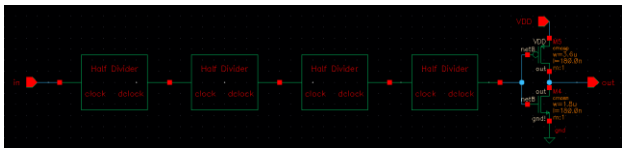

Figure 3.8: 16 divider ratio with output buffer

4.1 PLL Tests and Measurements

When the overall PLL was tested with discussed transistor level function blocks and control parameters the PLL successfully displayed locking at 100 MHz up to 230 MHz. Figure 4.1 shows the PLL locking response and how both output frequency locks to 100 MHz and Vc locks at around 1v.

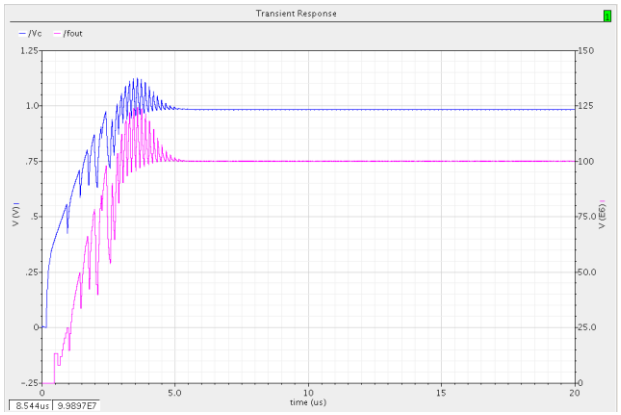

Figure 4.1: PLL transistor level locking response

The transisor level PLL response and the matlab closed loop response are quite similar, comparing Figure 4.1 and Figure 2.2. They both have about the same amount of overshoot and settling time. The settling time for the PLL response was about 5us while the simulated response was 3.5us. The reason why the transistor level settling time took slightly longer than the simulated version is because of parastic values on the circuit as well as time delays from output buffer stages.

4.2 Power Consumption

The power consumption of the overall PLL and individual blocks was measured by observing each current being pulled from the power supply. The average power was then calculated as VDD multiplied by the average current. In Figure 4.2 the current for each of the four function blocks can be seen for the first 10us of operation time.

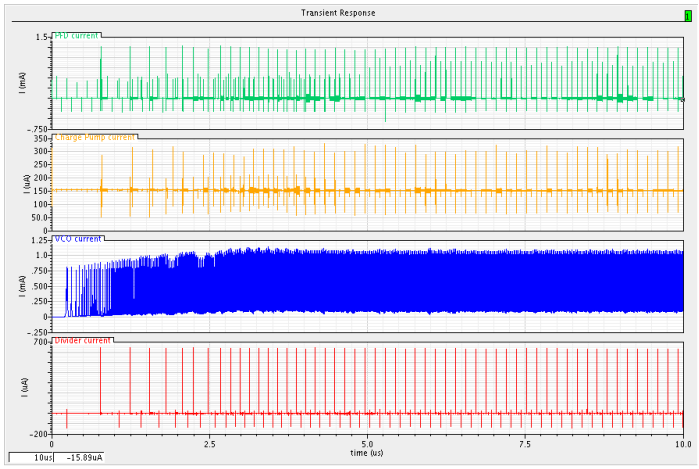

Figure 4.2: Current measurement for PFD, charge pump, VCO, and divider

Using cadence spectre the average current was then calculated for each of the four plots in Figure 4.2. The average current for the VCO was the highest at 165uA, with the pump charge comparable at 153uA. The PFD only had an average current of 10uA and the divider had the smallest average current at 370nA. Overall then the PLL had a total average power of 1.8v(165u + 153u + 10u + .37u) = 591uW. Figure 4.3 shows a pie chart power distribution of each of the four blocks.

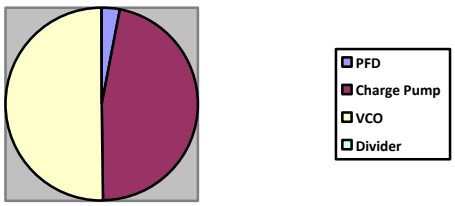

Figure 4.3: Power distribution chart

4.3 Conclusion

This project successfully showed the process from design and simulation stage of stability to full transistor level PLL creation. The PLL had five main components including the PFD, charge pump, VCO, divider, and Loop Filter. The PLL was able to lock at 100 MHz up to the VCO limited frequency output of 230 MHz. Power consumption measurements showed that the VCO consumed about half the total average power of the system with the Charge Pump consuming roughly the other half. Total power consumed was 591uW which is respectable. Table 4.1 summarizes the parameter values used for control stability.

R	6.25Kohms
C1	140pF
C2	10pF
Io	50uA
Kvco	181.5 MHz/v
N	16

Table 4.1: Parameter Values

Future work in this project could include redesigning the VCO using a Maneatis Cell in order to obtain higher frequency output and get a wider range for the PLL. Also noise analysis could be done on the PLL for each of the individual function blocks.

4.5 Acknowledgments

Acknowledgments go to Dr. Vishal Saxena and his Memory Architecture and Clock Synchronization course at Boise State University.

4.6 References

[1] Dr. Vishal Saxena. PFD Circuit Implementation [Online]. Available:http://lumerink.com/courses/ECE518/Handouts/PFD%20Circuits.pdf

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