Operational Amplifier Design Project

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ECE 411
May 8th, 2013

Abstract

The goal of the project was to design an operational amplifier that could handle a load of 100 KΩs in parallel with 1pF. The amplifier needed to be stable with a phase margin no less than 63degrees. The amplifier also needed to have a gain greater than 70dB and a bandwidth of at least 100 MHz.

1. Introduction

The application of this project was to design an operational amplifier using the 180nm processes that could be used in signal processing or analog to digital converters. When designing the amplifier it was important to include a second stage to maintain high gain even when driving a small resistive load. A small resistive load comes in parallel with the amplifiers output resistance which can drastically decrease the gain. By using a second stage amplifier, the gain on the first stage is preserved by having the second stage shield it. Another consideration was that the first stage needed to be differential because the input had two leads, also the second stage needed to have an AB topology to drive rail to rail.

The first stage of the amplifier was designed using a Folded-cascode. A cascode amplifier has a larger amount of output resistance because transistors are doubled up, and leads to a higher gain. The typical gain for a differential cascode amplifier, also known as a Telescopic amplifier is the transconductance value of the transistor multiplied by the Ro value squared. By then taking the cascode amplifier and using a folded topology a larger amount of headroom is achieved which makes biasing more relaxed. The drawback to using a folded amplifier though is more current is needed which then consumes more power.

In Figure 1.1 the schematic for the operational amplifier can be seen. The sizes for all the transistors were scaled up by a factor of ten from what was being used in the bias circuit. By scaling the transistor's sizes larger, more current could be supplied to the amplifier which allowed for improved specifications such as bandwidth and slew rate.

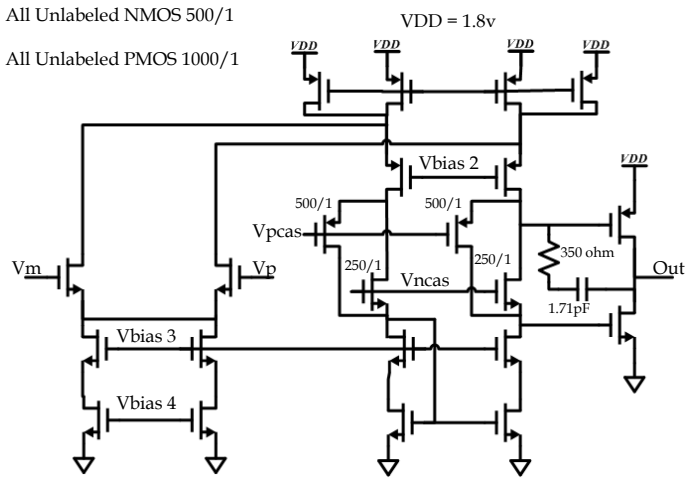

Figure 1.1: Operation Amplifier Schematic

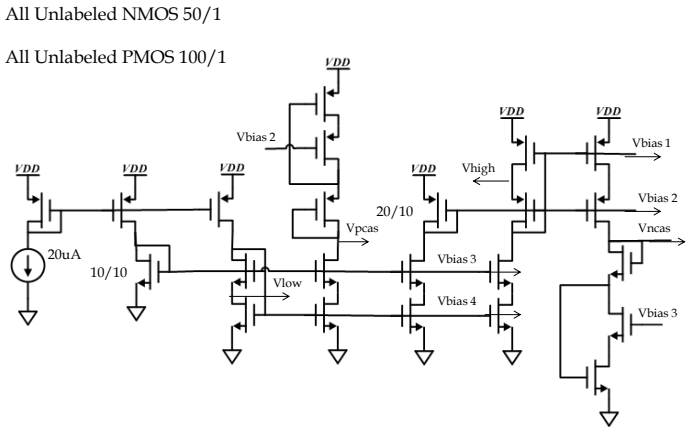

Figure 1.2: Short Channel Biasing Circuit

The circuit used to bias the amplifier can be seen in Figure 1.2 which is a typical circuit used for short channel devices. Simulations were done on the biasing circuit to make sure every transistor was in the active region and about 20uA of current was running through each branch. Figure 1.3 shows the annotated simulation results for the biasing circuit in Cadence.

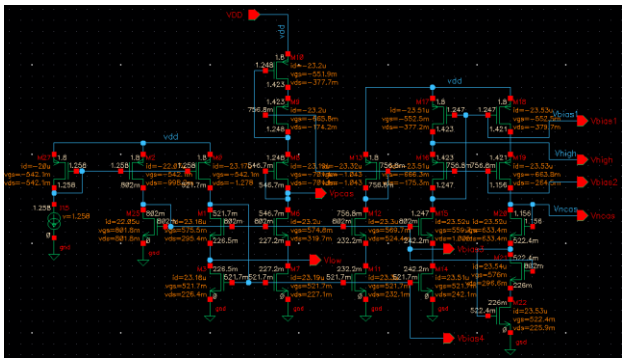

Figure 1.3: Biasing circuit Cadence simulation results

As can be seen in Figure 1.3 the current didn't deviate much from the 20uA reference current. The highest current offset from the reference was about 23.53uA in the last branch. The voltage values are also annotated in Figure 1.3 showing that as expected the Vbias1 reference was higher than the Vbias4. This is because Vbias1 has a voltage level of VDD-Vsg while Vbias4 has a potential of just Vgs. To make sure that all the transistors were in saturation the Vdsat for each transistor was observed to be smaller than Vds. It was important to make sure the biasing circuit was reliable or else the overall amplifier might not function correctly.

2. Stability Analysis

One of the important requirements for the amplifier was to have a phase margin of at least 63 degrees. Matlab was used to simulate the gain and phase response of the system. Figure 2.1 shows the simple model used to represent a two stage amplifier, note that in this model the zero nulling resistor is not included.

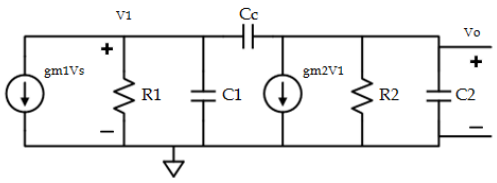

Figure 2.1: Generic model used for stability

Cadence was used to measure the first and second stage gm values which were 5.4m and 9.83m respectively. The R1 value was the output resistance from the first stage amplifier which was calculated to be 3.3 KΩs from using measurements of ro values in Cadence's dc operating point print out. C1 was then just the Cgs parasitic capacitance value from the first stage which was approximated as 6fF, and C2 was the load capacitance of 1pF. R2 was then also just the load resistance of 100 KΩs. The simulation results can be seen in Figure 2.2, which was used to help select a value for Cc, the compensating capacitor.

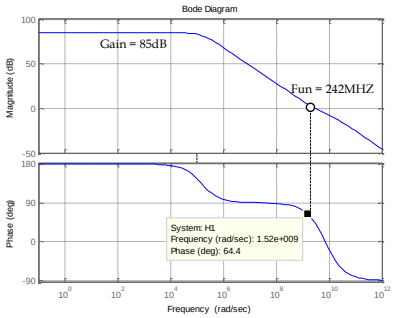

Figure 2.2: Matlab simulation results for stability

From the simulations it was shown that a Cc value at about 2 pF should be used in order to achieve a phase margin a little greater than 63 degrees. The Matlab simulations also provided information on the pole-zero plot of the system seen in Figure 2.3. From the pole-zero plot it appears that the dominant pole, the pole closest to the origin, is at zero, but actually it just appears like this because of the scaling. The second pole is pushed out much further than the first in response to the compensating capacitor which makes the system have a better phase margin. Also apparent from Figure 2.3 is the right half plane zero which is usually undesirable. In order to make the RHP zero less influential to the system a zero nulling resistor will be used in series with Cc to push it out further in the actual system.

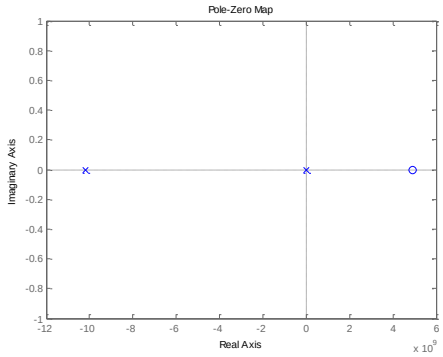

Figure 2.3: Matlab Pole-Zero Plot

3. Operational Amplifier Results

The operational amplifier was tested in Cadence using the stb analysis. The values used for the compensating capacitor was 1.71 pF which was found to be the lowest value before the phase margin became less than 63 degrees. The zero nulling resistor also helped with phase margin and was selected to be the optimal value of 350 Ohms from Cadence parametric analysis measurements. Figure 3.1 shows the Bode plots for the amplifier in Cadence.

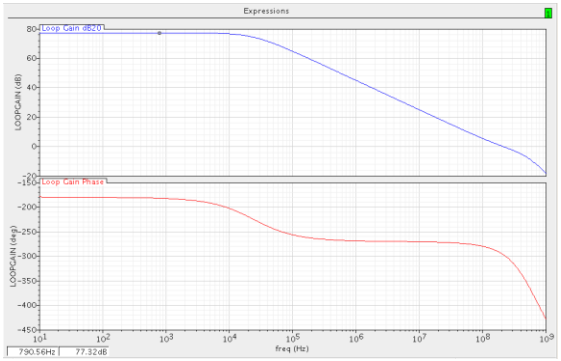

Figure 3.1: Bode plots in Cadence simulation

Cadence automatically prints out the values for phase margin and unity gain frequency in the stb analysis. The phase margin was measured as 63.2 degrees and unity gain frequency was at 213 MHz, both of these values meet the requirement specifications. The gain of the amplifier was at 77.32dB which is greater than the 70dB requirement gain. As stated in the requirements, these measurements were obtained while the amplifier was pulling a 100 KΩ load in parallel with 1pF capacitance. Figure 3.2 shows the overall test bench layout in Cadence.

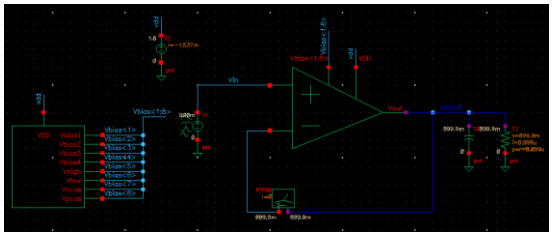

Figure 3.2: Cadence test bench layout

Next the amplifier was tested on how well it could respond to both small and large step responses. In Figure 3.3 the amplifier is tested with a small signal response and as expected from the phase margin, responds quickly with minimal ringing.

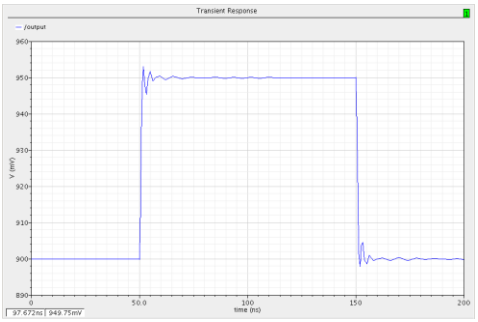

Figure 3.3: Small signal step response

Then it was tested how well the amplifier responded to large signal steps and to measure slew rate, this can be seen in Figure 3.4. The required slew rate for the amplifier was 500V/1us, this is a very fast response. This means that the amplifier needs to be able to increase by 500mV in only 1ns. In Figure 3.4 the slew rate was measured going from 900mV to 1.4V in 1.964ns, a slew rate of about 255V/1us. Slew rate is measured by the current in the first stage divided by the Cc capacitor so it can either be improved by boosting current or using a smaller compensating capacitor. The issue then was the Cc value was already the minimum value it could in order to satisfy the phase margin requirement. The only way to increase slew rate would then be to drastically increase the current being pulled by the amplifier by increasing the sizing of the transistors but this would also increase the power needed. In order to minimize power consumption to only a couple of milliwatts it was decided that a slew rate of 255V/1us was acceptable. It's also worth noting that having an AB topology second stage amplifier helps with slew rate since it can both pull and push current with respect to the square law equation by varying the transistor's gate voltages. In other topologies a fixed current is used that cannot be adjusted which leads to slow slew rate in the falling edge.

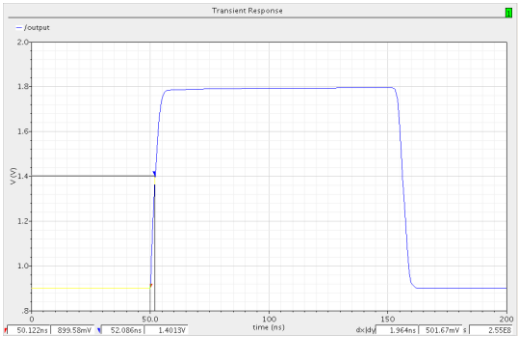

Figure 3.4: Slew rate measurement

When testing the CMRR, common mode rejection ratio of the operational amplifier the gain was tested when the common mode voltage was applied to both input terminals of the operational amplifier. The gain

then for CMRR was measured to be at around 85 dB when frequency was low. The CMRR was measured by taking the differential gain and subtracting Av,cm, the gain when both terminals are at Vcm and the output is floating. To measure the gain of Av,cm an AC analysis was done in Cadence. Figure 3.5 shows the CMRR as frequency is varied.

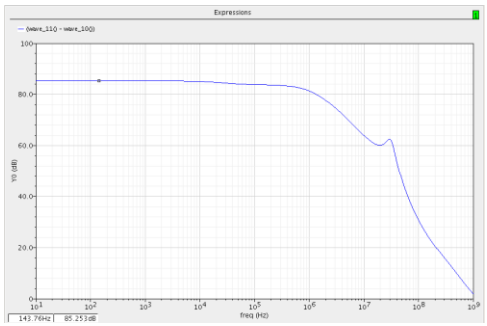

Figure 3.5: Measuring CMRR as frequency varies

Next the PSRR was tested by doing an AC analysis when the frequency of the voltage supply was varied. The results for PSRR can be seen in Figure 3.6 where the best PSRR is at low frequencies. The PSRR value is negative because it shows how much noise is rejected or attenuated by.

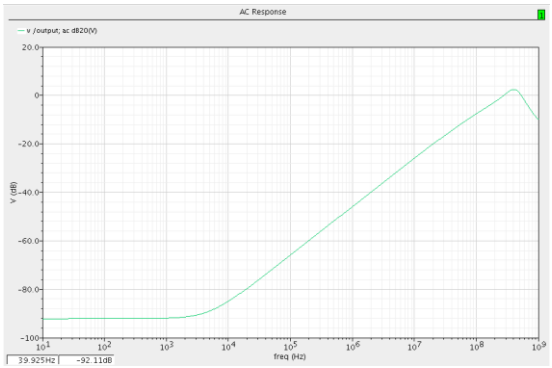

Figure 3.6: Measuring PSRR as frequency varies

Temperature variation was also tested from 0 to 100 degrees Celsius. The summarized results can be seen in Figure 3.6.

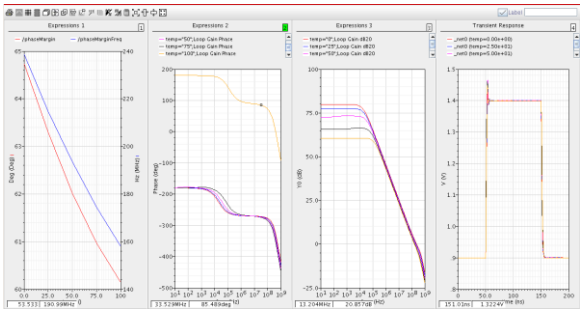

Figure 3.6: Temperature variation measurements

A couple of observations could be made by how temperature affects the amplifier's characteristics. Both phase margin and unity gain frequency decreased when temperature increased. Also the gain decreased as well from an increase in temperature. The only parameter that actually improved when temperature increased was the slew rate.

The final measurement for the operational amplifier was the power consumption. This could be simply measured by seeing how much current was being drawn by the power supply. For the operational amplifier alone the power consumed was 2.5mW while for the overall system including the biasing circuit consumed 2.8mW. It is apparent that the amplifier consumes a lot more power than the biasing circuit, this is because the amplifier uses more current to achieve high unity gain frequency and slew rate.

4. Conclusion

A two stage operational amplifier was successfully tested and met the specifications with a gain of 77.32 dB, unity gain frequency of 213 MHz, and a phase margin of 63.2 degrees. The one specification that the amplifier fell short of was having a slew rate of 255V/1us vs the required 500V/1us, but this was to limit the amount of power consumption to less than 3mW. The first stage of the amplifier was a folded cascode which allowed for high gain and output swing. The second stage was an AB topology amplifier which gave full output swing and improved slew rate limitations. The amplifier was tested in Matlab first to help select the compensating capacitor to allow for stability. In the final design the Cc value was selected to be 1.71 pF, close to the 2pF value in Matlab, and the zero nulling resistor was selected to be 350Ω.

5. References

[1] Dr. Vishal Saxena. Loop Stability Analysis [Online]. Available:http:http://lumerink.com/courses/ece5411/Handouts/Loop%20Stability%20Analysis.pdf

[2] Visio Schematic Symbols. Available [Online] Avaliable: http://lumerink.com/courses/ece5411/s13/ECE5411.htm

[3] Dr. Vishal Saxena. CommonSourceFreqResp1 [Matlab code] Available: http://lumerink.com/courses/ece5411/s13/ECE5411.htm