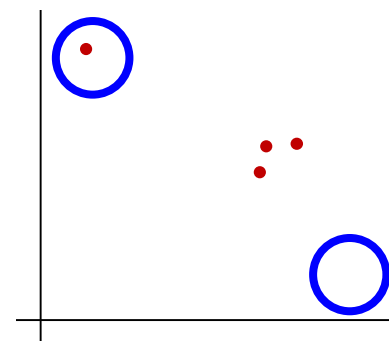
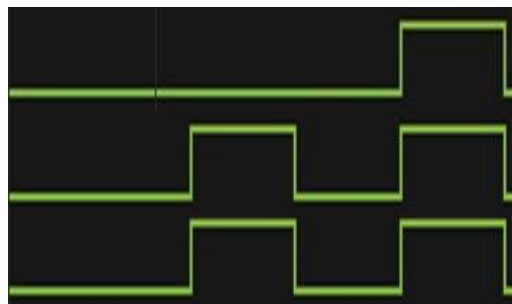
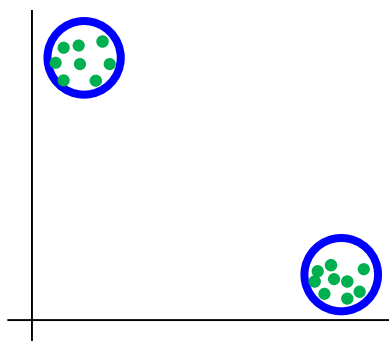

Teaching Computers to Validate Themselves

Andrew DeOrio

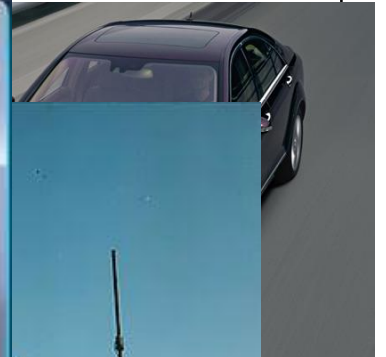
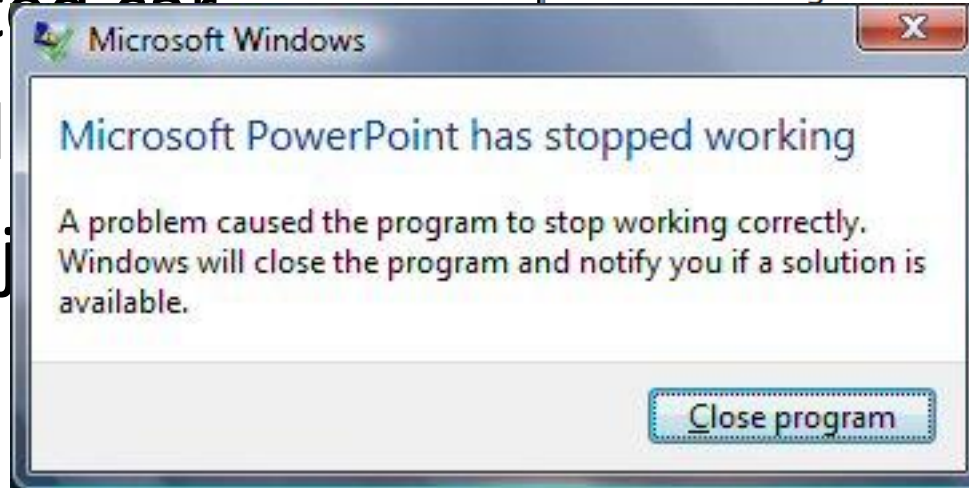
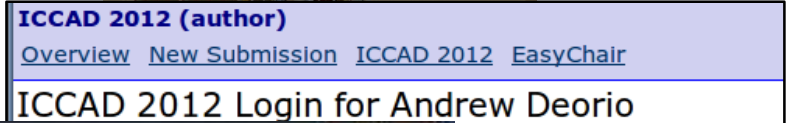
awdeorio@umich.edu

andrewdeorio.com

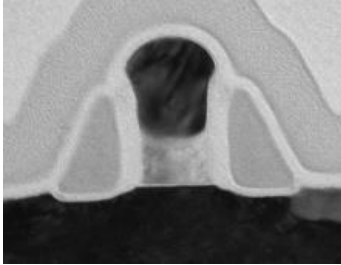


Five worst times for computers to fail

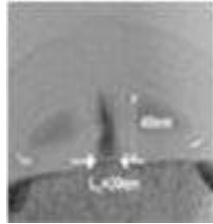
5. Using your credit card
4. Submitting a paper
3. Automated car
2. Missile d
1. Giving a j



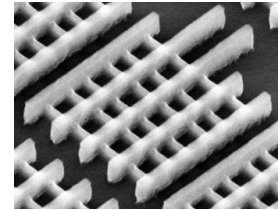
Trends in today's processors



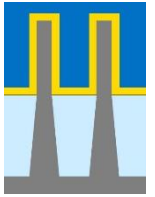
45nm



32nm



22nm



14nm

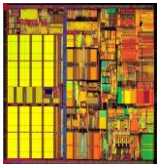
Shrinking transistor size

Increasing cores and complexity

waning reliability

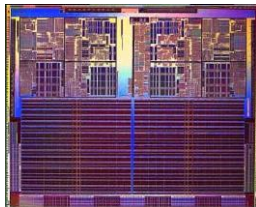
verification challenges

Intel
Pentium4



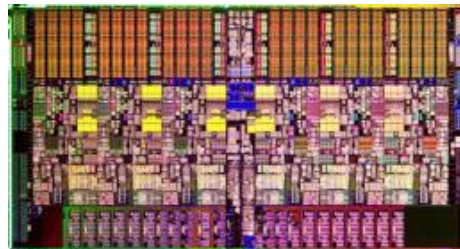
1 core, 2000

AMD
Opteron



2 cores, 2005

Intel Core i7



6 cores, 2010

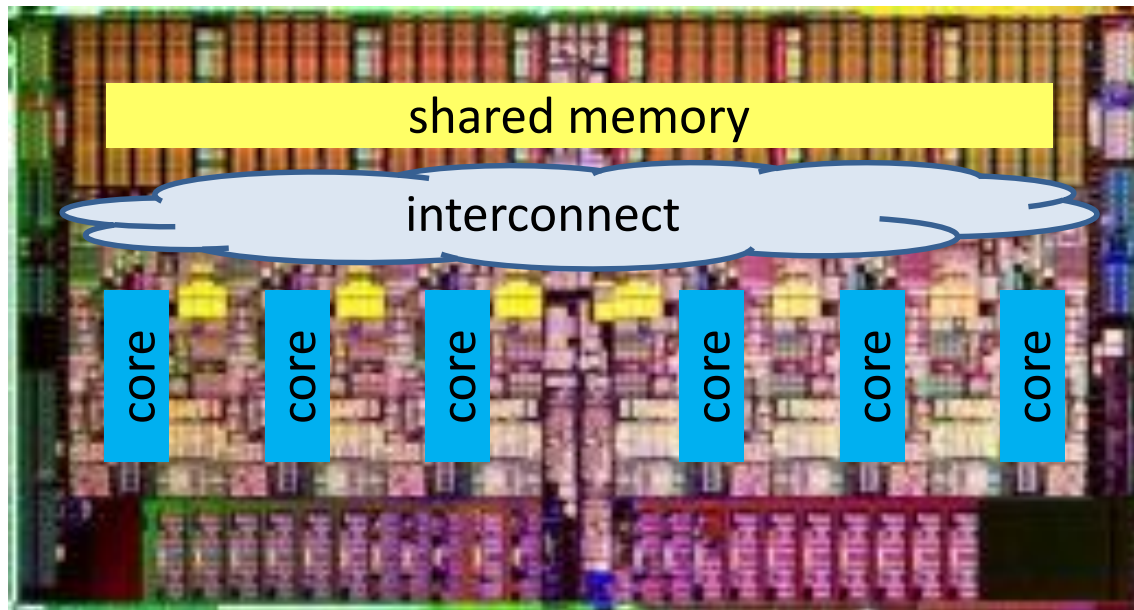
Tilera TILE-Gx72



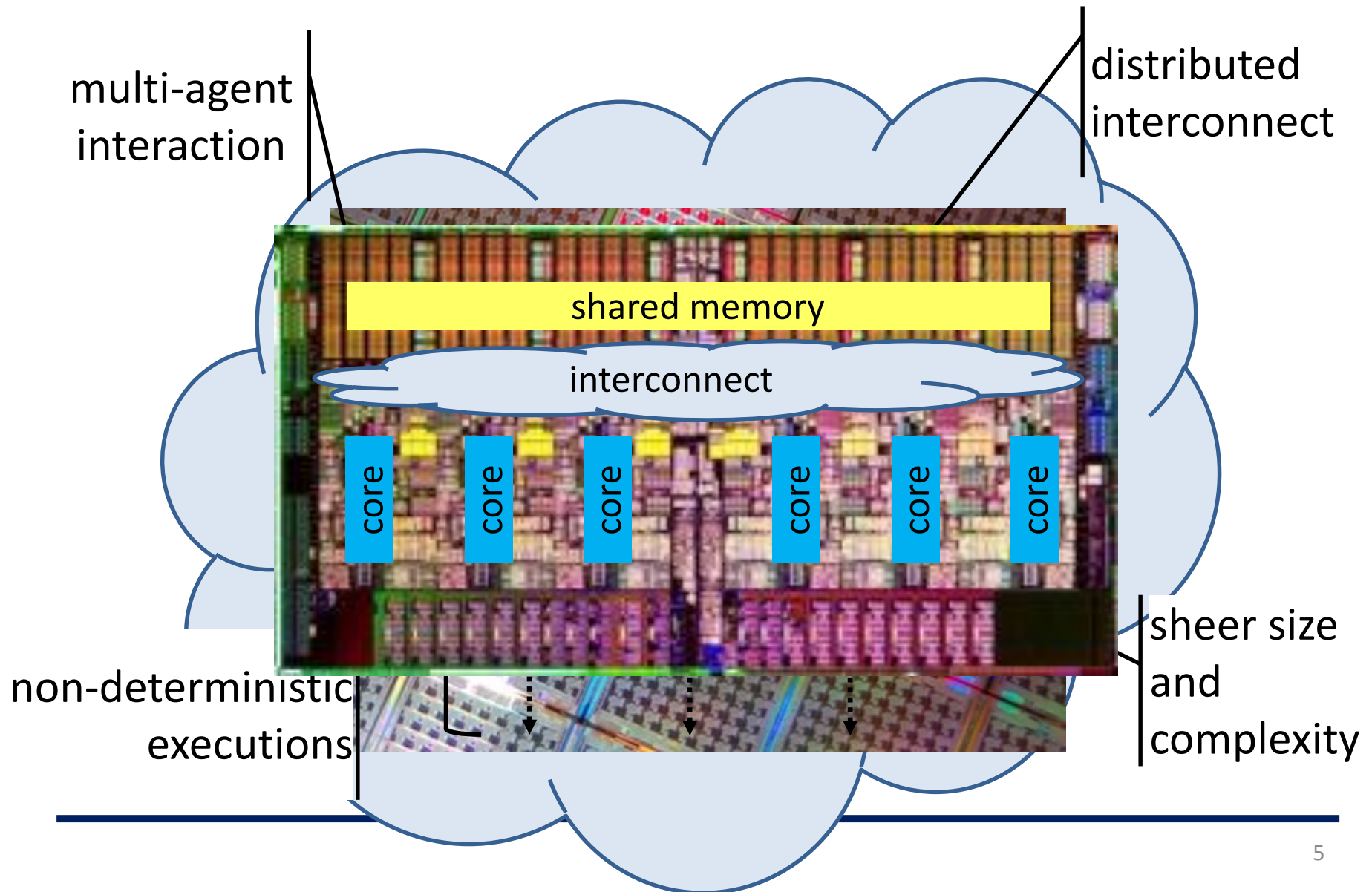
72 cores, 2013

Today's multi-core / SoC

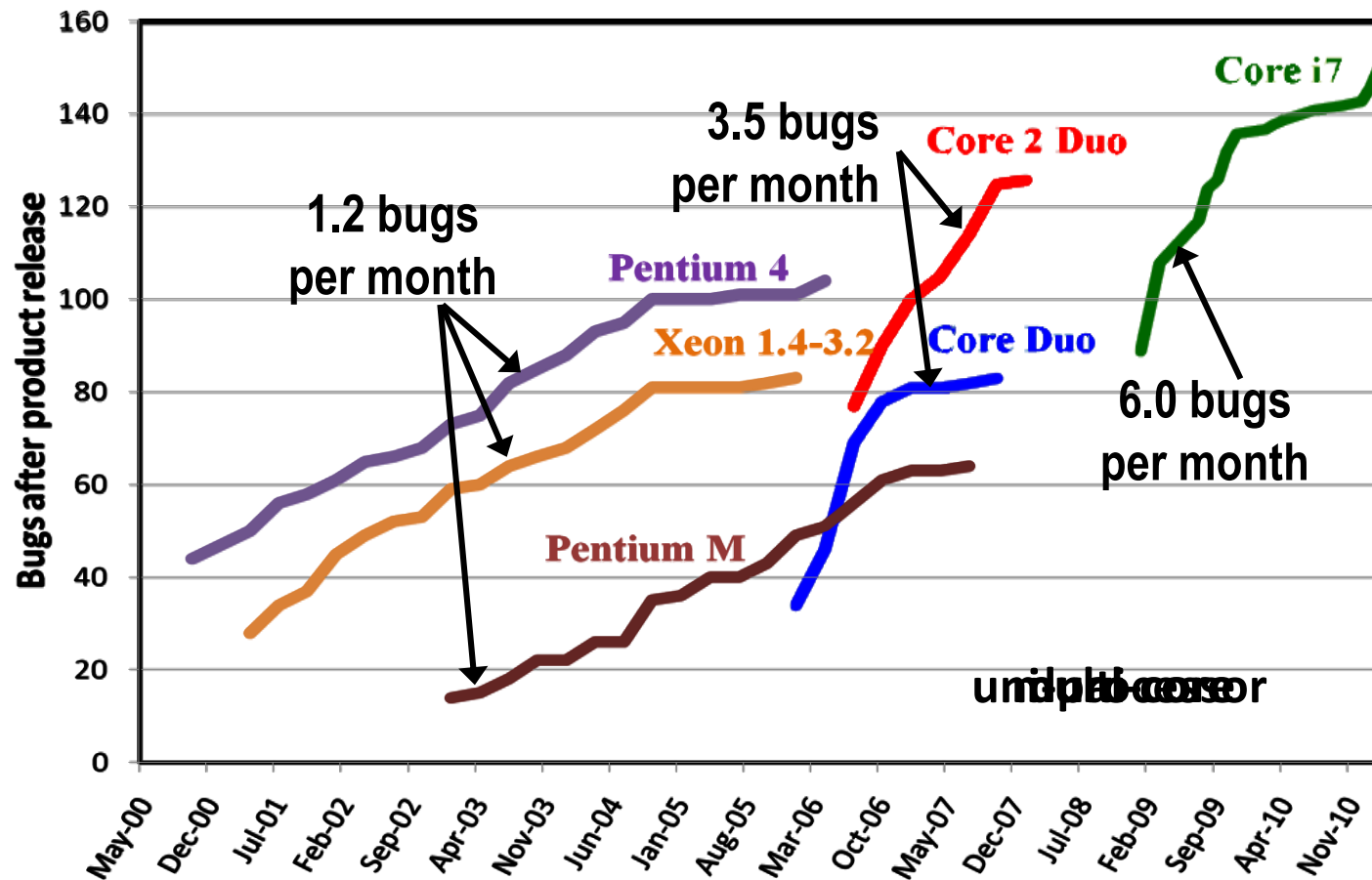
- Many IPs communicate through interconnect
- Recent system → new verification challenges



Tomorrow's multi-core / SoC



Escaped errors in final products



10-13% of bugs are communication related

A problem has been detected and windows has been shut down to prevent damage to your computer.

The problem seems to be caused by the following file: SPCMDCON.SYS

PAGE_FAULT_IN_NONPAGED_AREA

If this is the first time you've seen this Stop error screen, restart your computer. If this screen appears again, follow these steps:

Check to make sure any new hardware or software is properly installed. If this is a new installation, ask your hardware or software manufacturer for any windows updates you might need.

If problems continue, disable or remove any newly installed hardware or software. Disable BIOS memory options such as caching or shadowing. If you need to use a removable hard drive, remove it and restart your computer, press F8 to select Advanced Startup Options, and then select Safe Mode.

Technical information:

*** STOP: 0x00000050 (0xFD3094C2,0x00000001,0xFBFE7617,0x00000000)

*** SPCMDCON.SYS - Address FBFE7617 base at FBFE5000, DateStamp 3d6dd67c

**1 in 190 windows crashes
are due to HW errors**
[Nightingale, *et al.* 2011]

Impact of errors

- Functional bugs



2014

- Electrical failures



2007

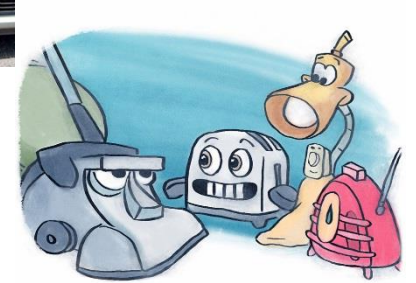
- Transistor faults



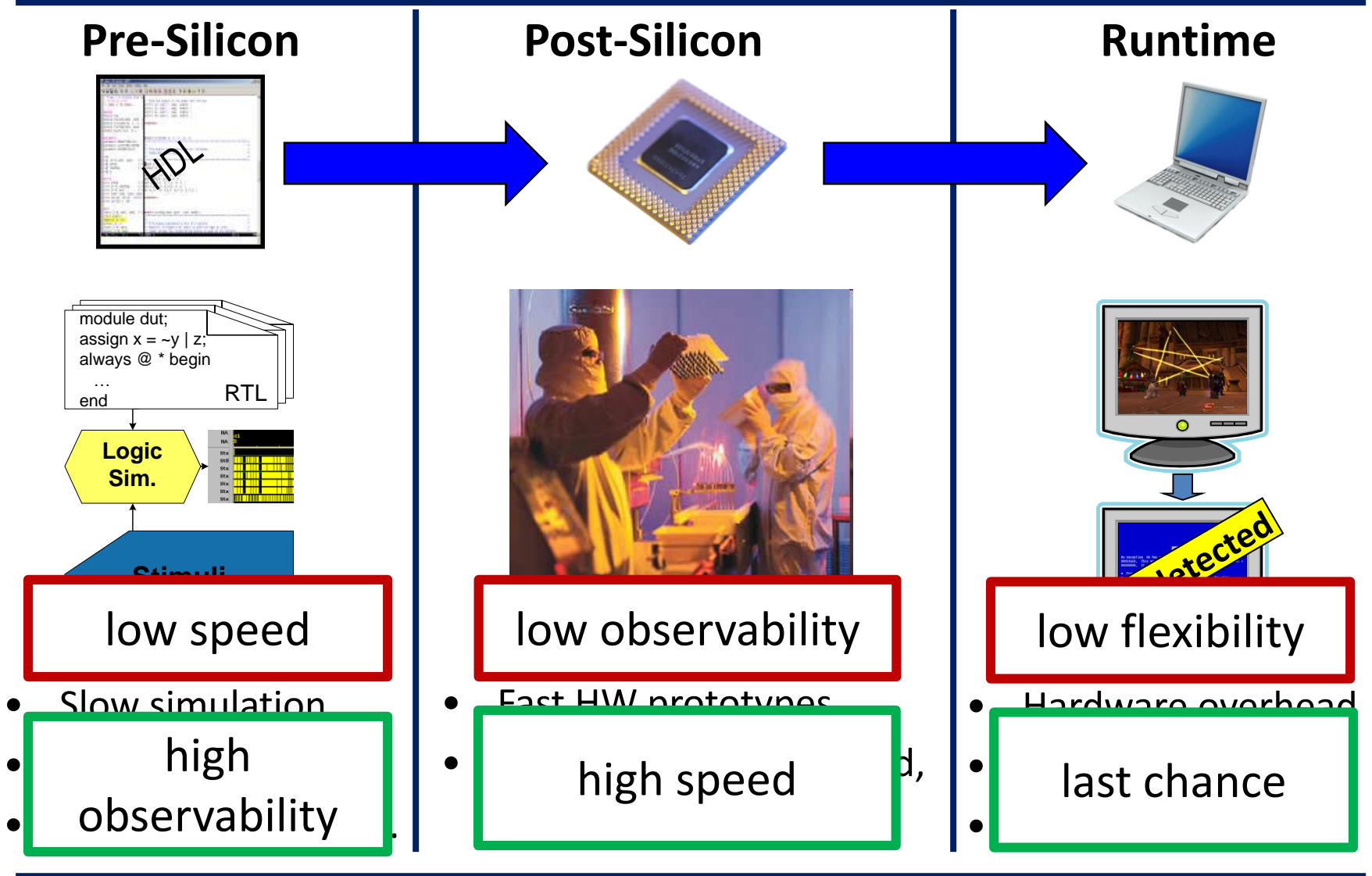
2011

Future impact of errors

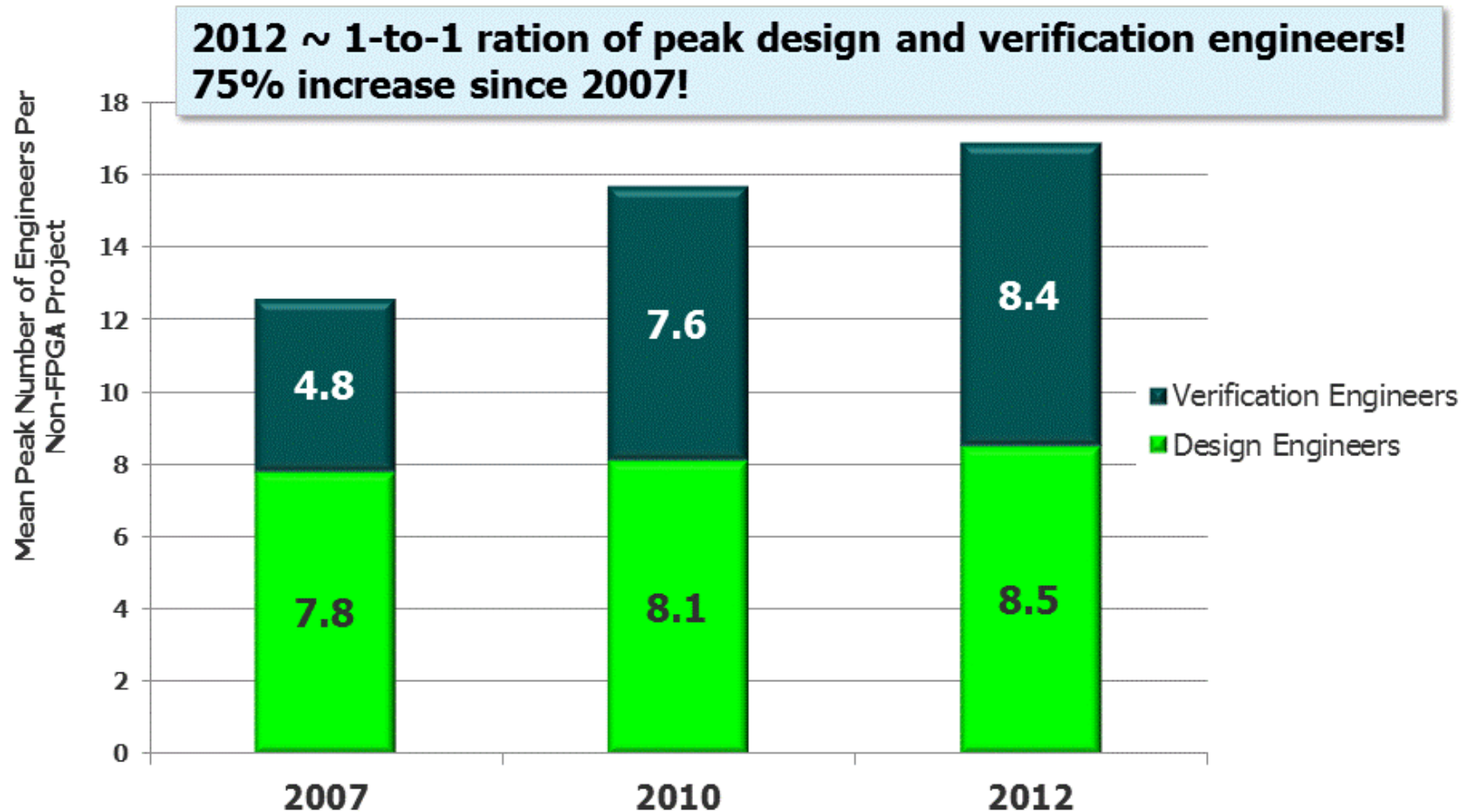
- The impact of errors will get worse as we rely more on computers
- Wearables
- Self-driving cars
- Internet of things
- Security depends on hardware correctness!



Verification today

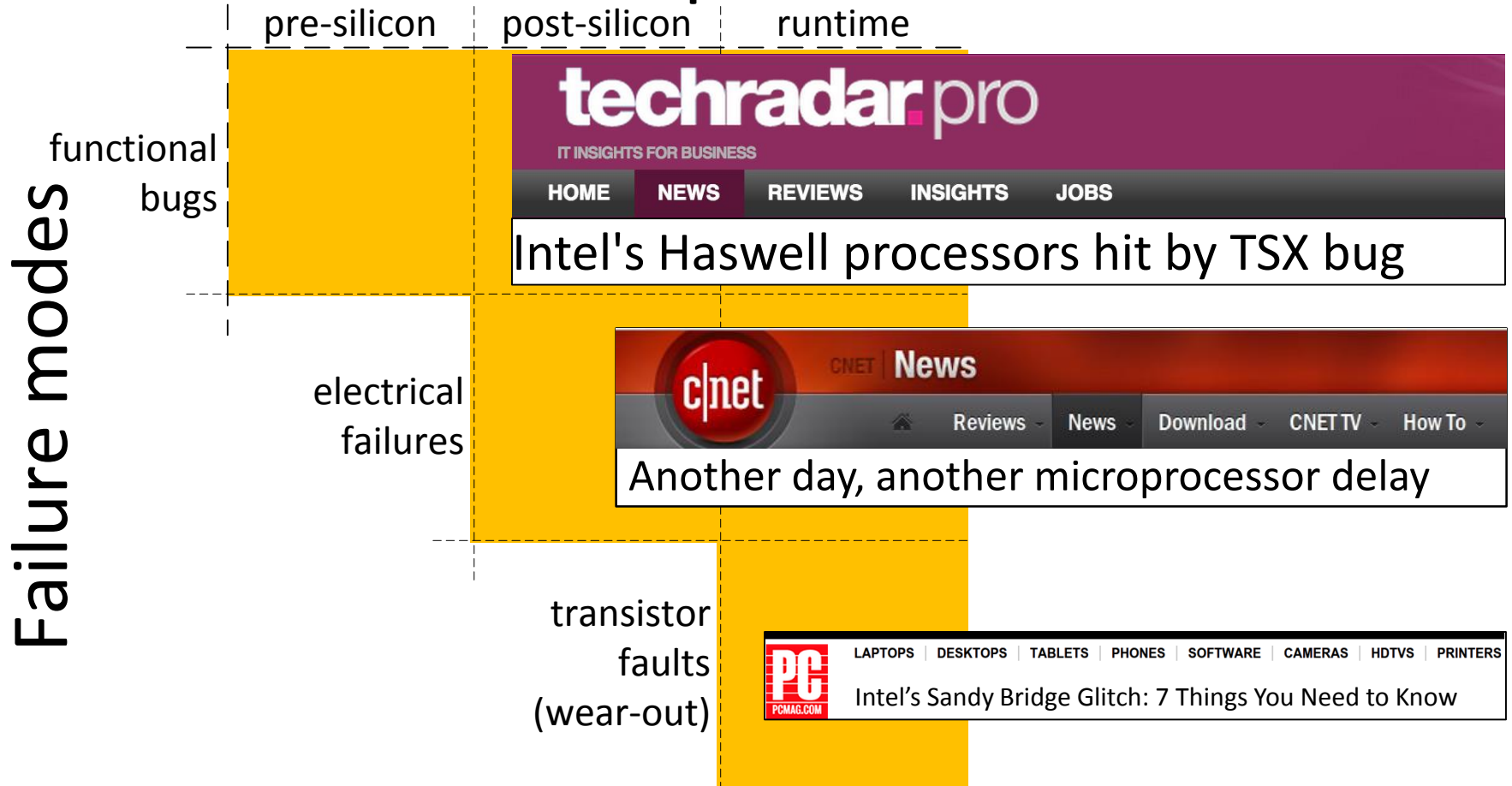


Verification today



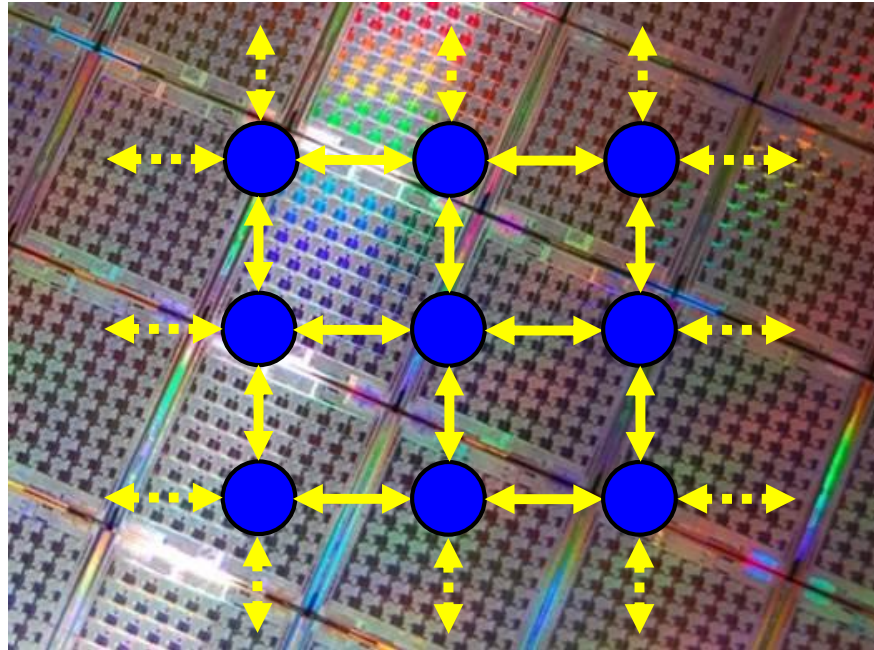
How errors are addressed

Verification phases



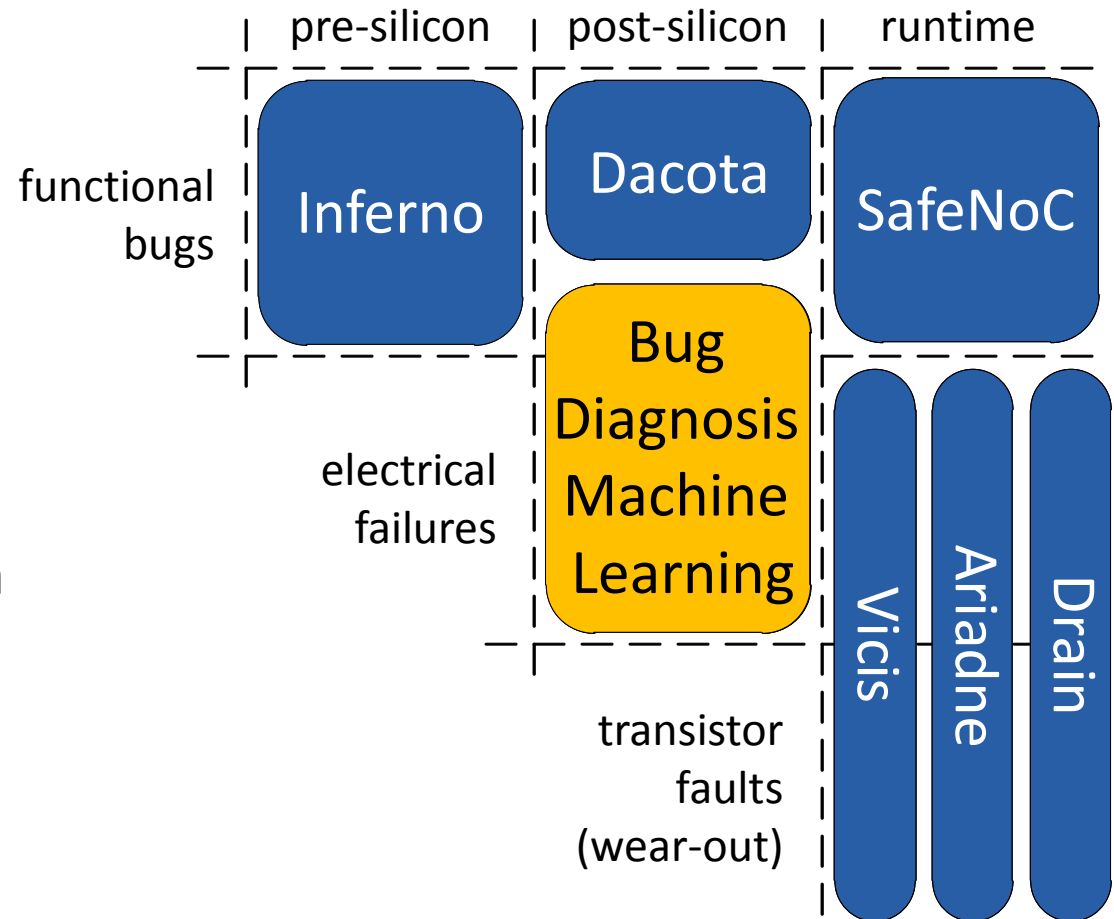
My research

Ensure **correct** operation
of **digital designs**
throughout the **lifetime** of the chip



My research

- Breadth of work across the verification spectrum
- Depth of work in several areas, such as post-si validation



Post-silicon validation

Pre-silicon



Post-silicon



Runtime



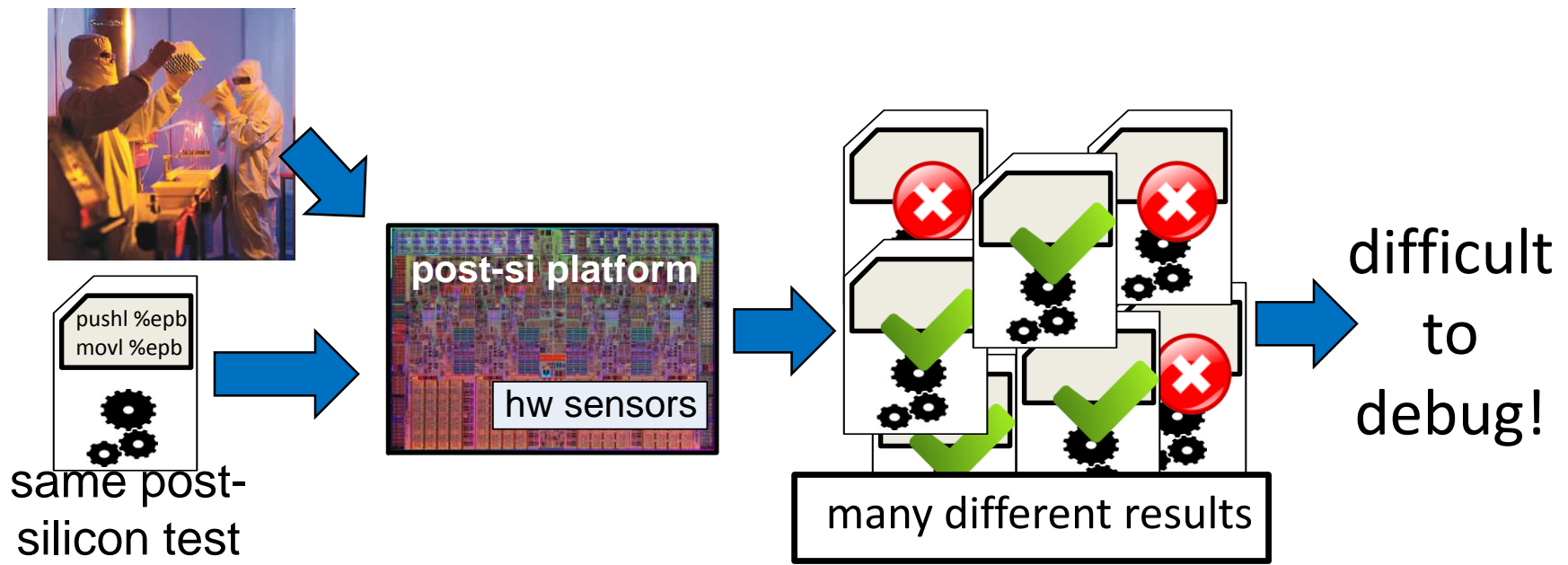
Goal: locate bug

- + Fast prototypes
- + High coverage
- + Test full system
- + Find deep bugs

- Poor observability
- Slow off-chip transfer
- Noisy
- Intermittent bugs

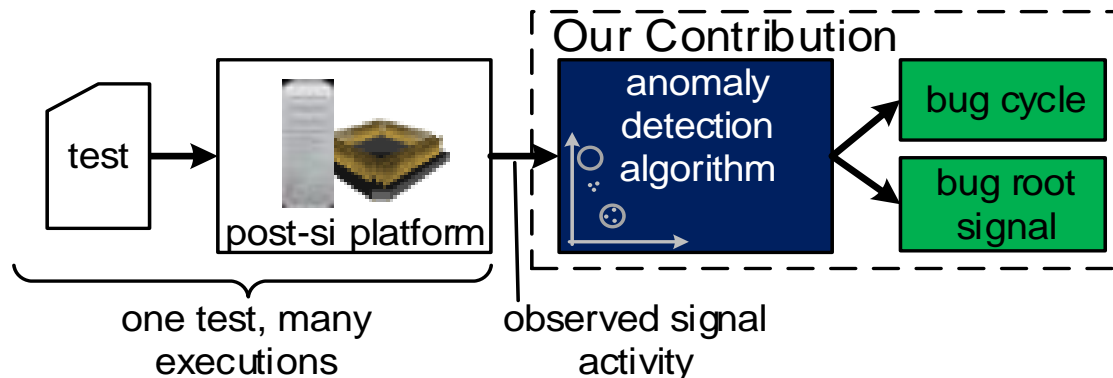
The most challenging post-silicon bugs

- A same test does not expose the bug in every run
- Each run exhibits different behaviors

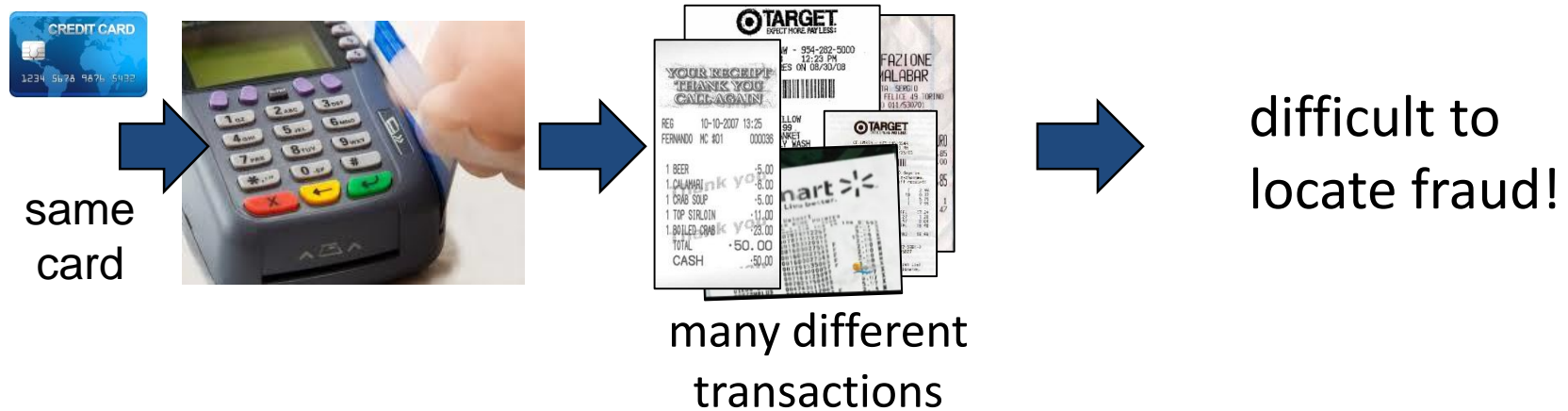
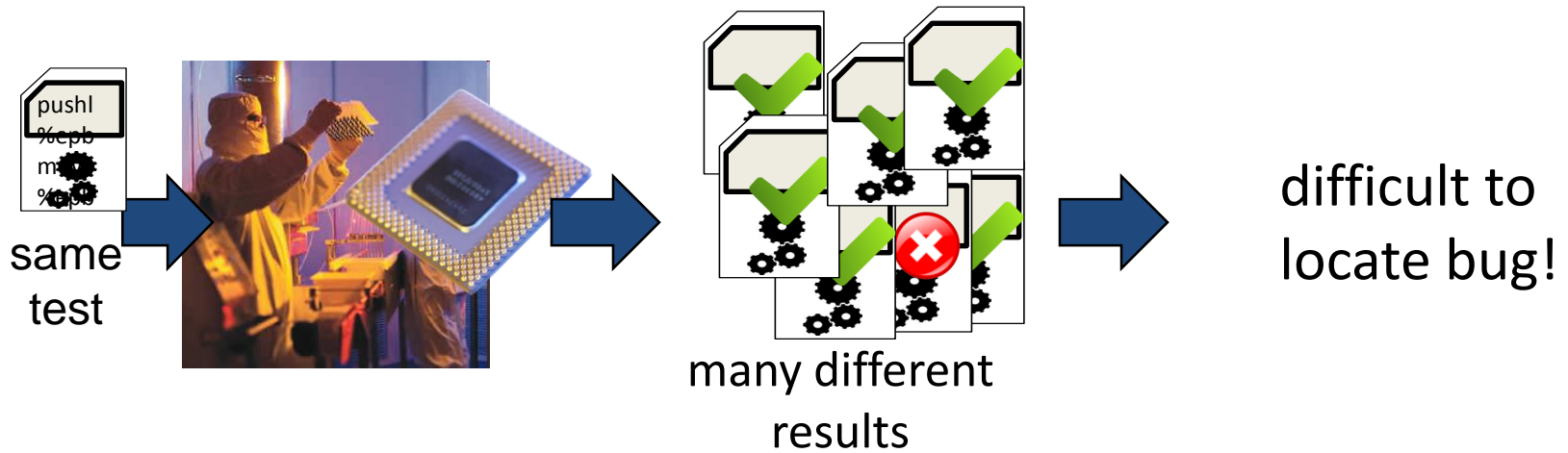


Debugging intermittent failures

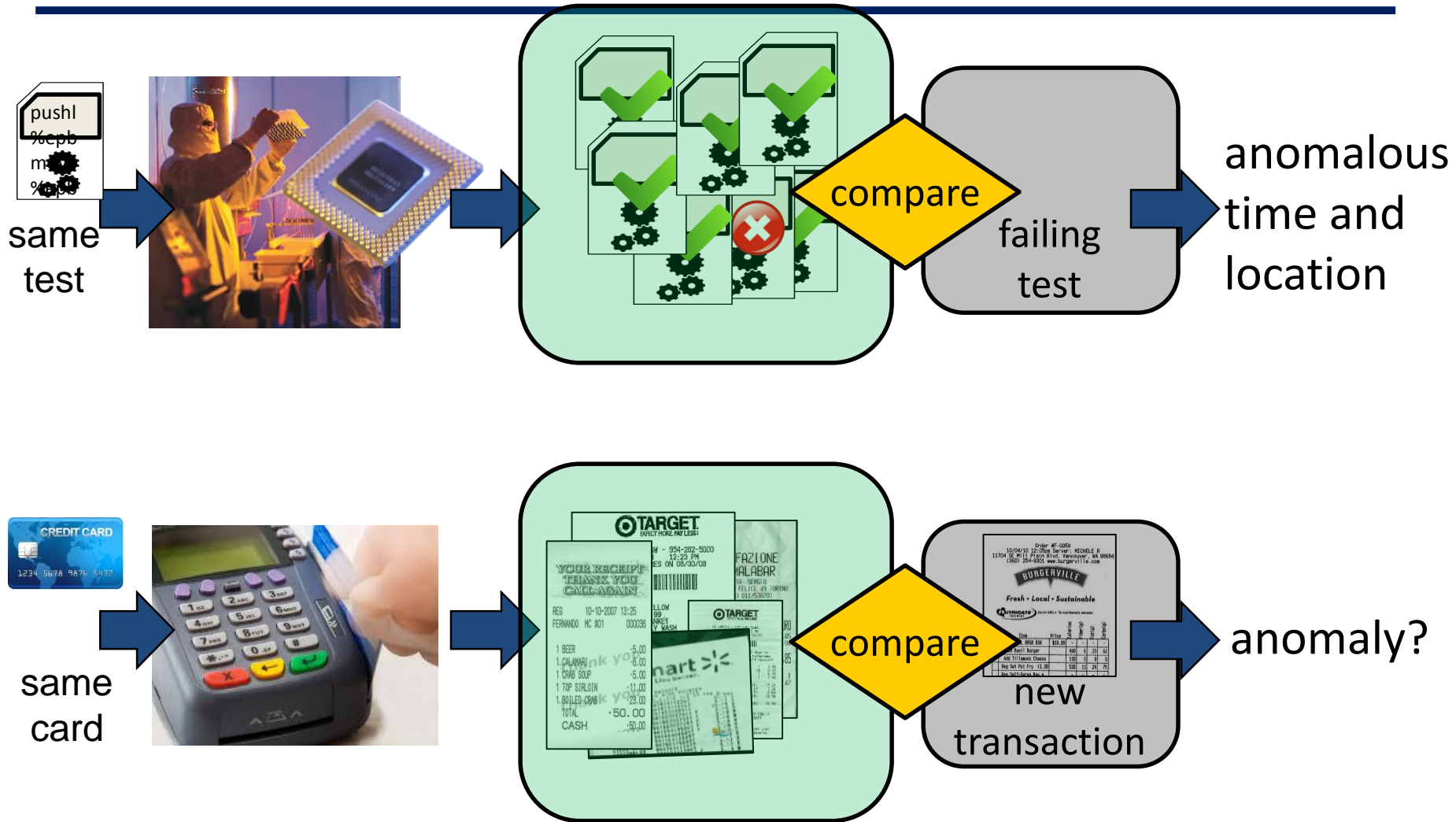
- Localize failures
 - Time (cycle) and space (signals)
- Tolerate non-repeatable executions
 - Statistical machine learning approach
- Scalable, adaptable to many HW subsystems



Post-silicon and credit cards



Post-silicon and credit cards



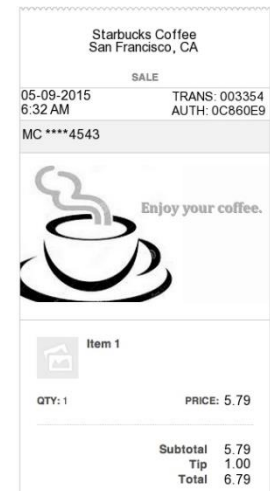
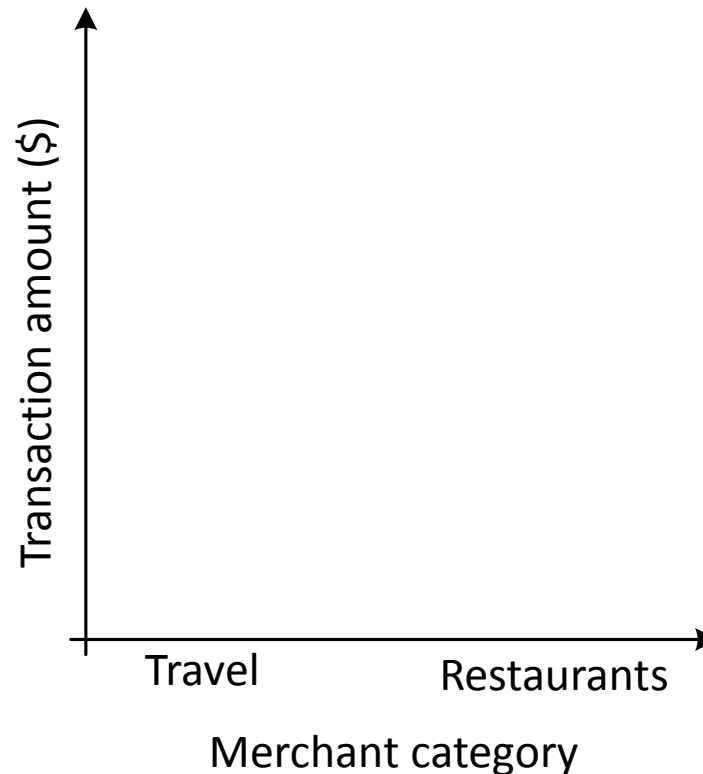
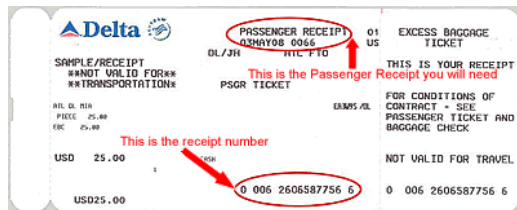
Machine learning background

- Goal: build a statistical model from examples
- Use model to make predictions for new examples



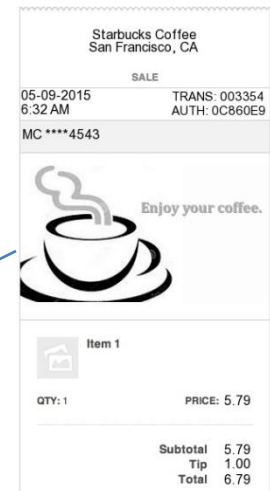
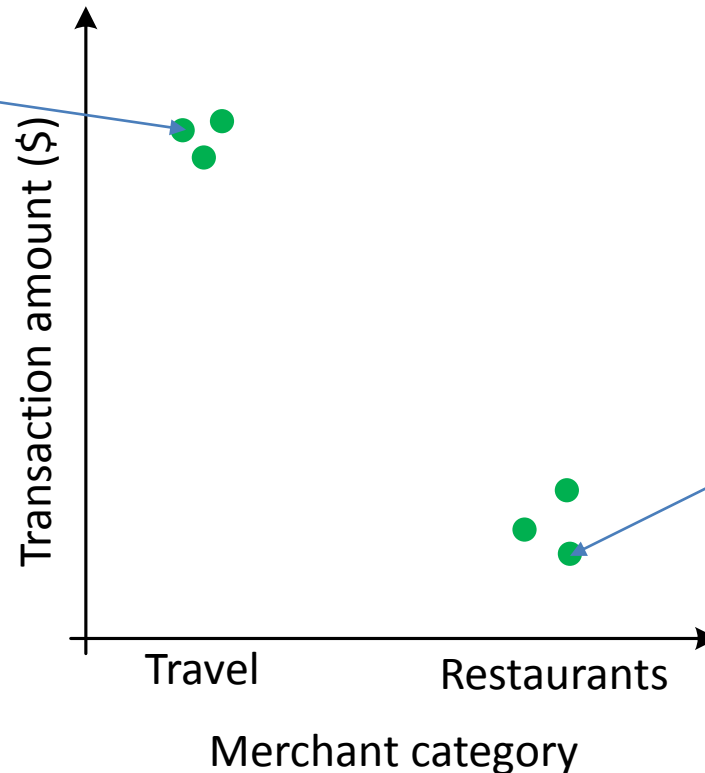
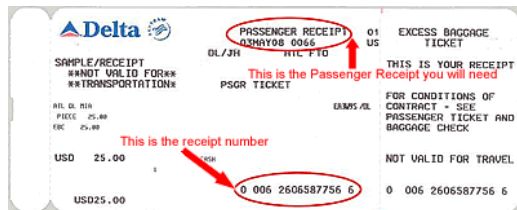
Machine learning background

- Each example described by *features*
 - Merchant, \$ amount, location, etc.



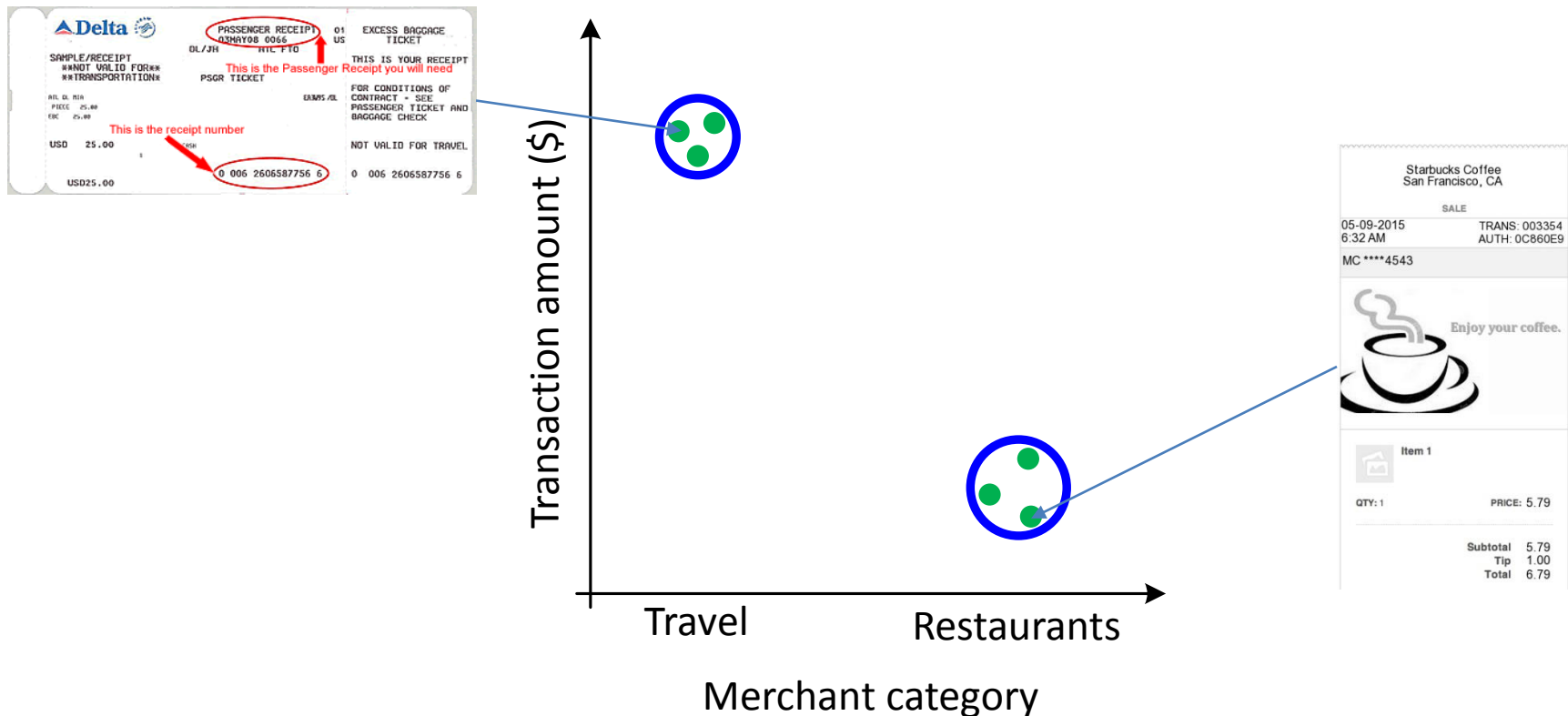
Machine learning background

- Learn correct behavior using *training data*
 - *Positive* labeled examples in this application



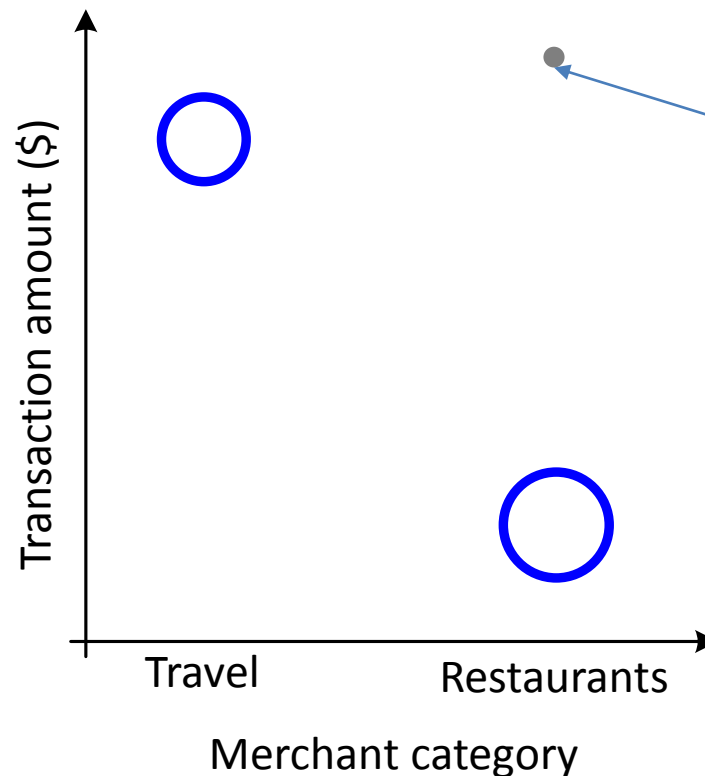
Machine learning background

- Clustering: a machine learning algorithm that groups examples with similar characteristics



Machine learning background

- *One-class learning* requires only a single label
- Good for anomaly detection

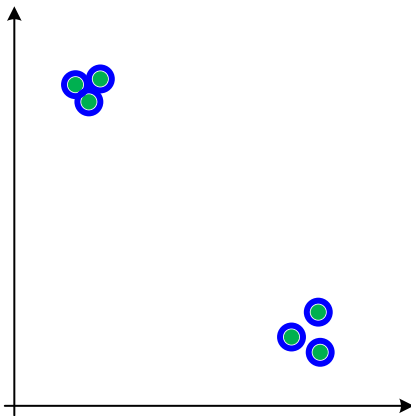


unknown
example

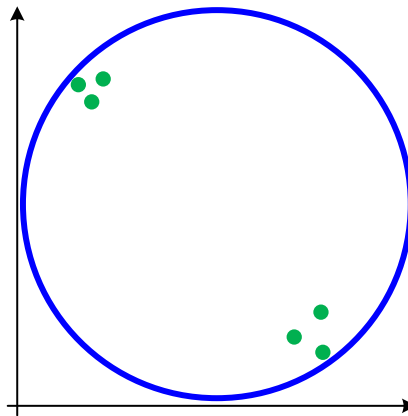
Machine learning background

- Overfitting: model is too specific
 - Everything looks like an anomaly
- Underfitting: model is too general
 - Nothing looks like an anomaly

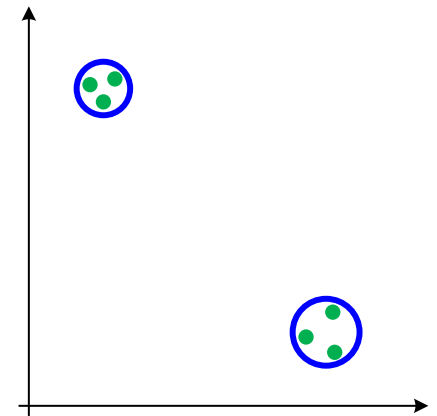
Overfitting



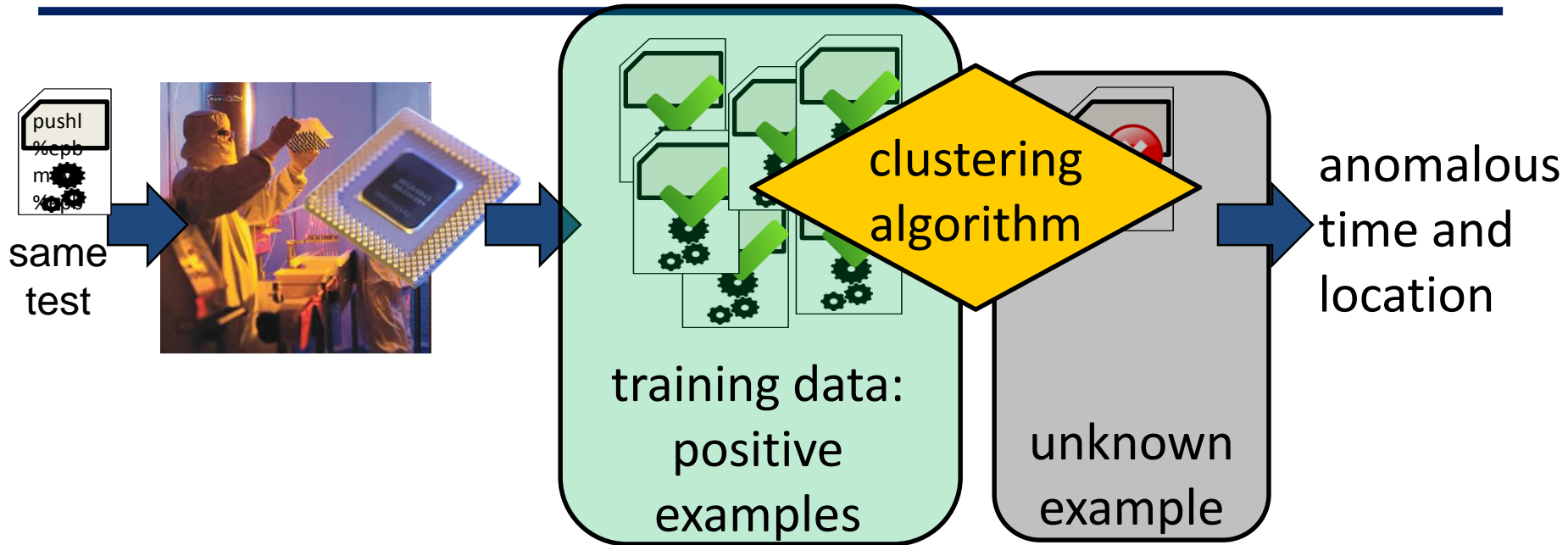
Underfitting



Good fit



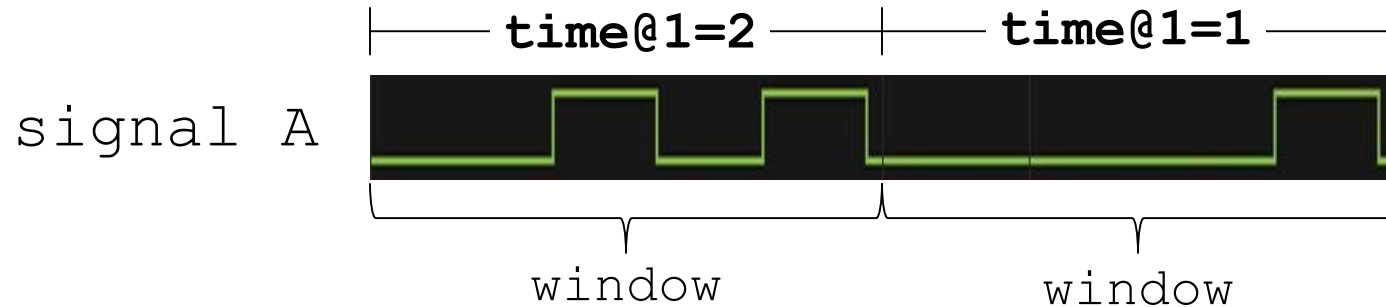
Features for post-silicon tests



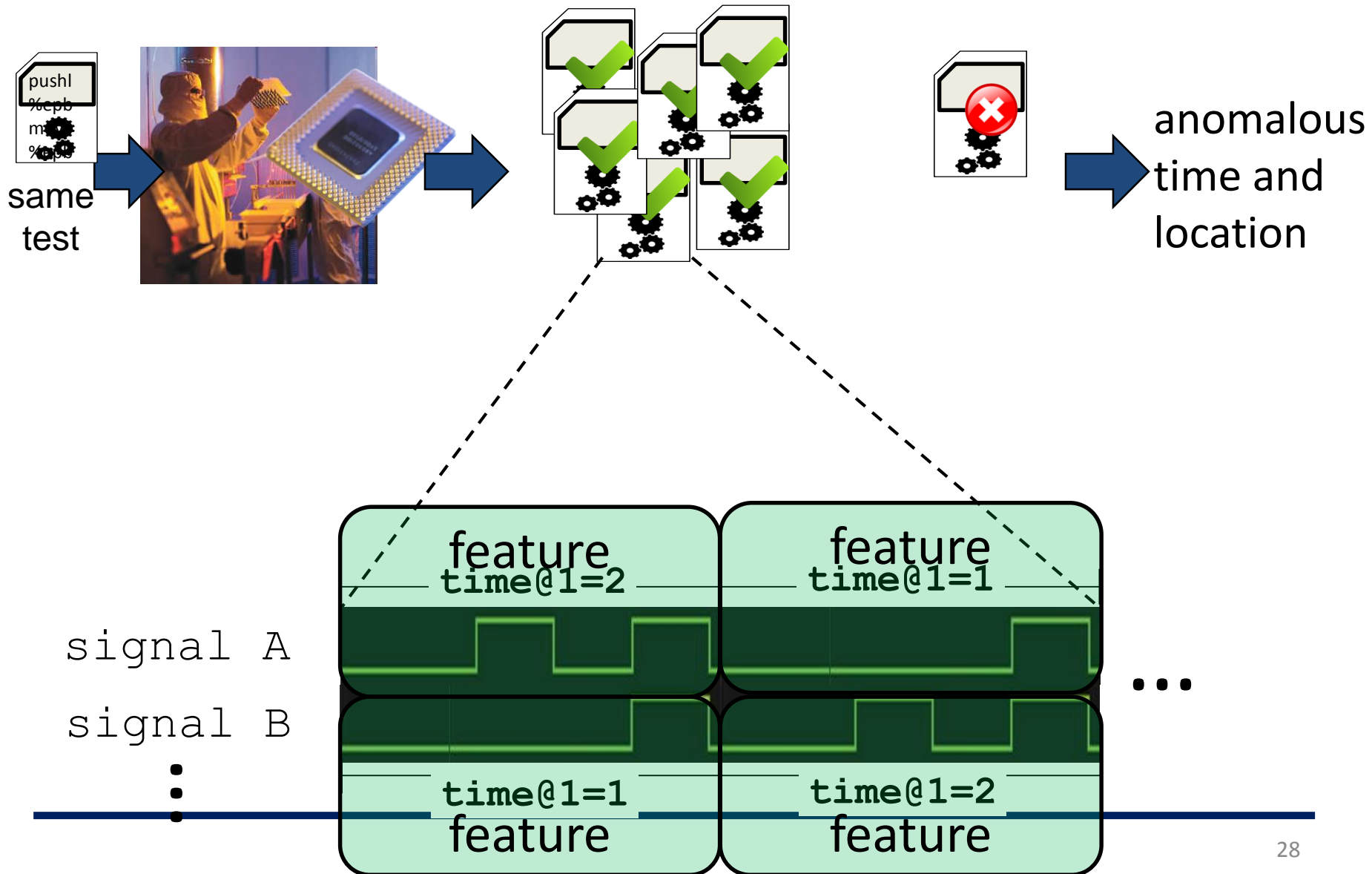
- What are some possible features that could be used to describe a post-silicon test execution?

Features

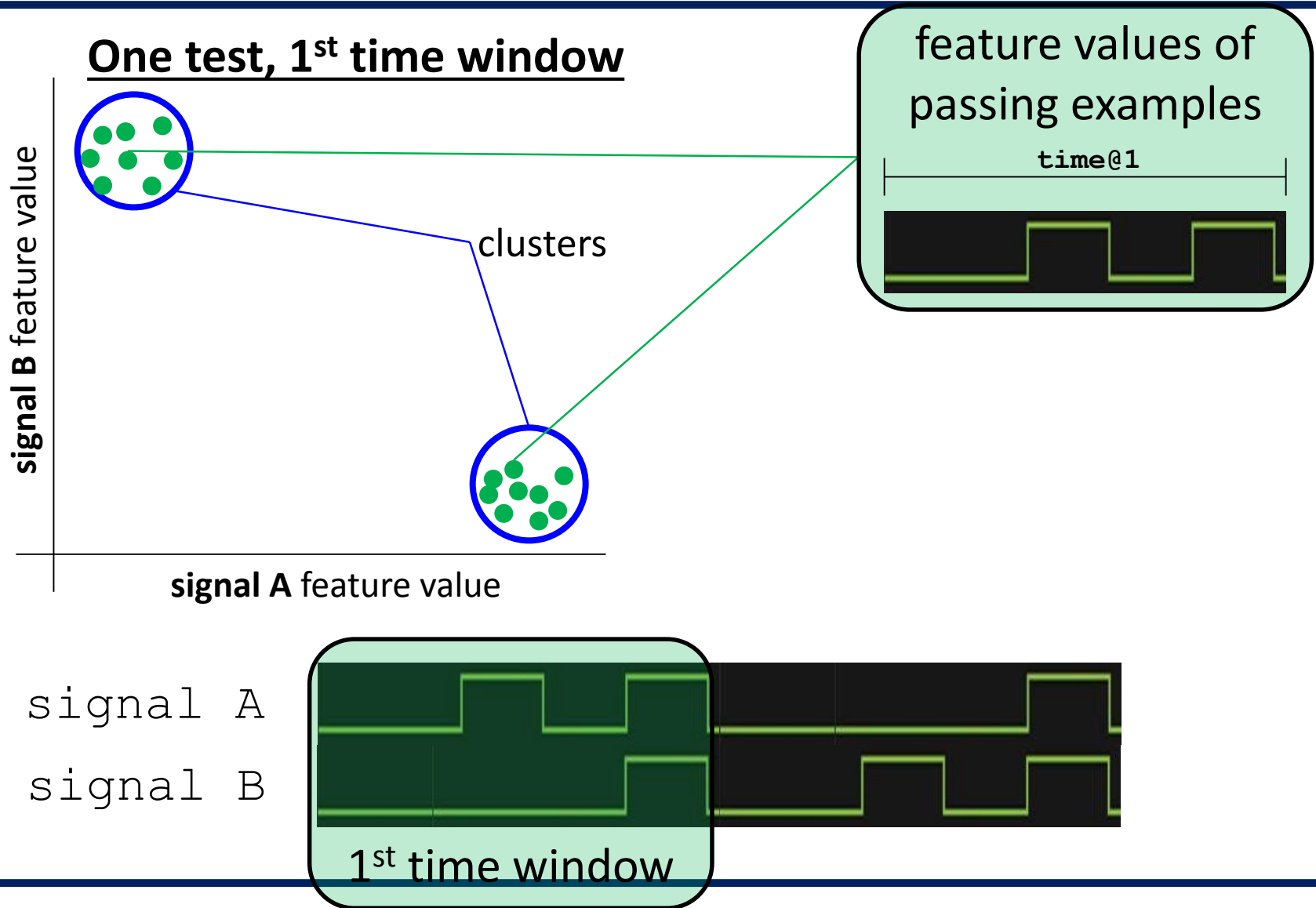
- Goal: summarize signal value
- Encodings (hamming, CRC, etc.)
 - Large hardware
 - Small change in input -> large change in output
- Counting schemes (time@1, toggle count)



Features



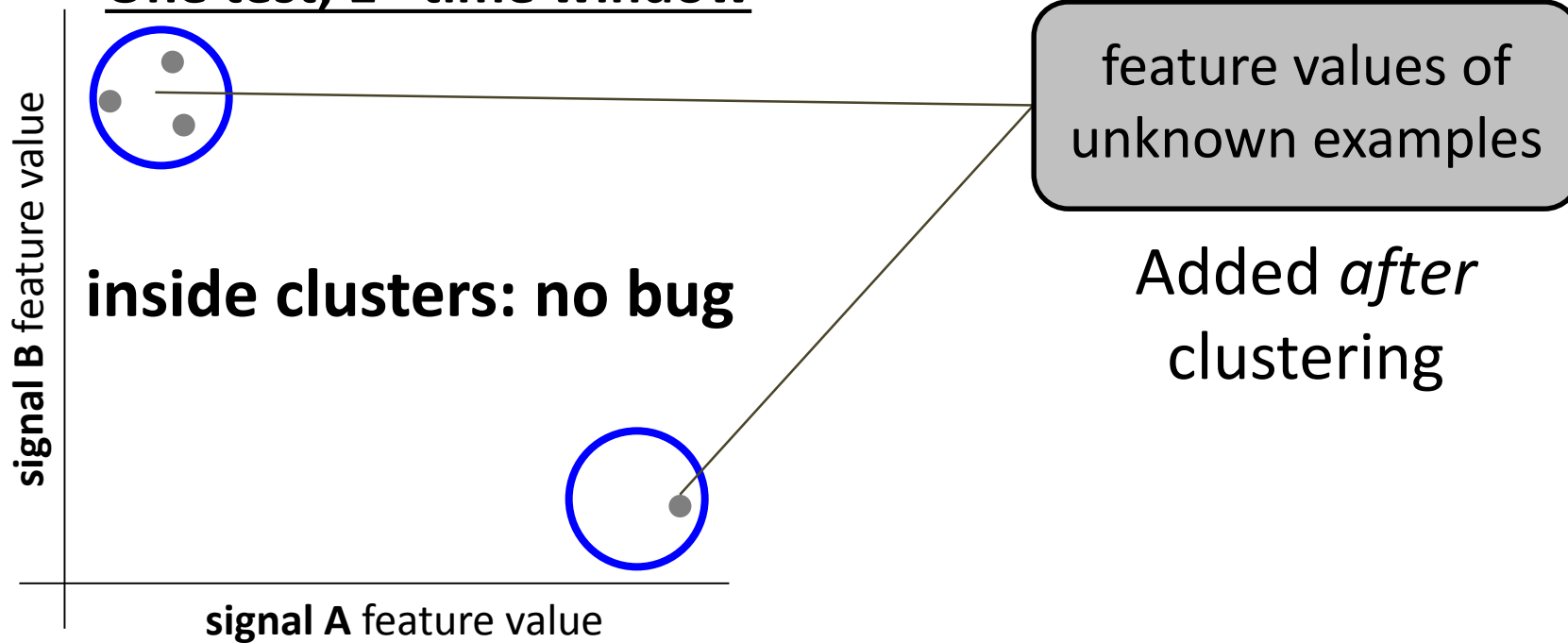
Learning clusters



Searching for anomalies

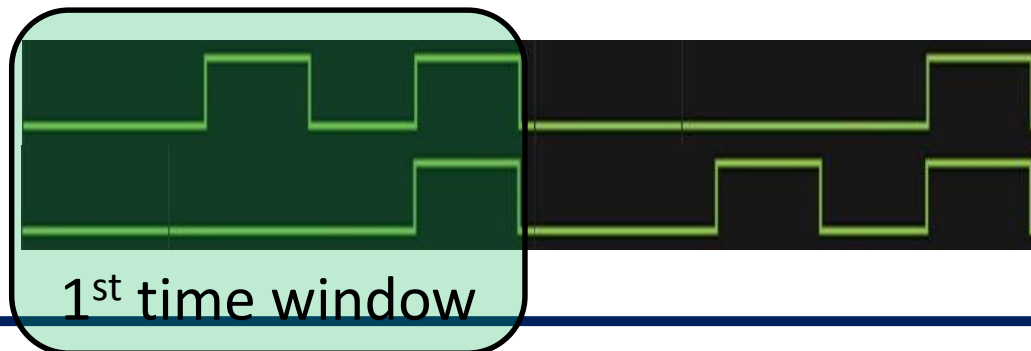
clustering
algorithm

One test, 1st time window



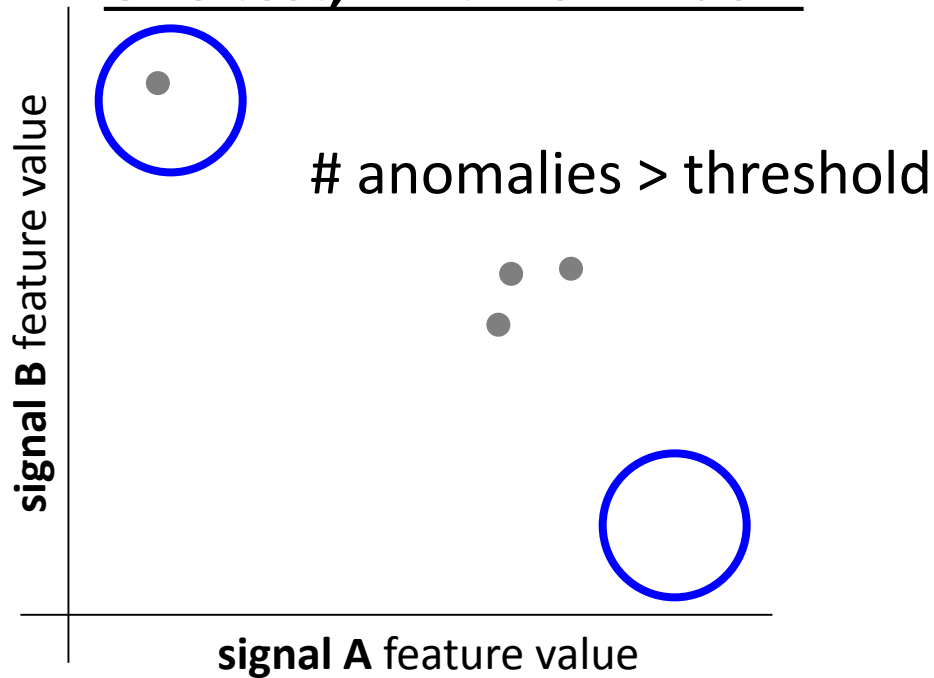
signal A

signal B



Searching for anomalies

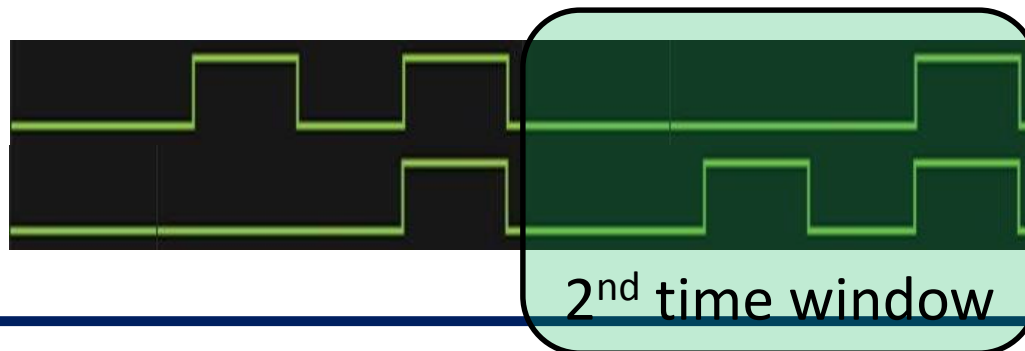
One test, 2nd time window



**Outside clusters:
bug found**

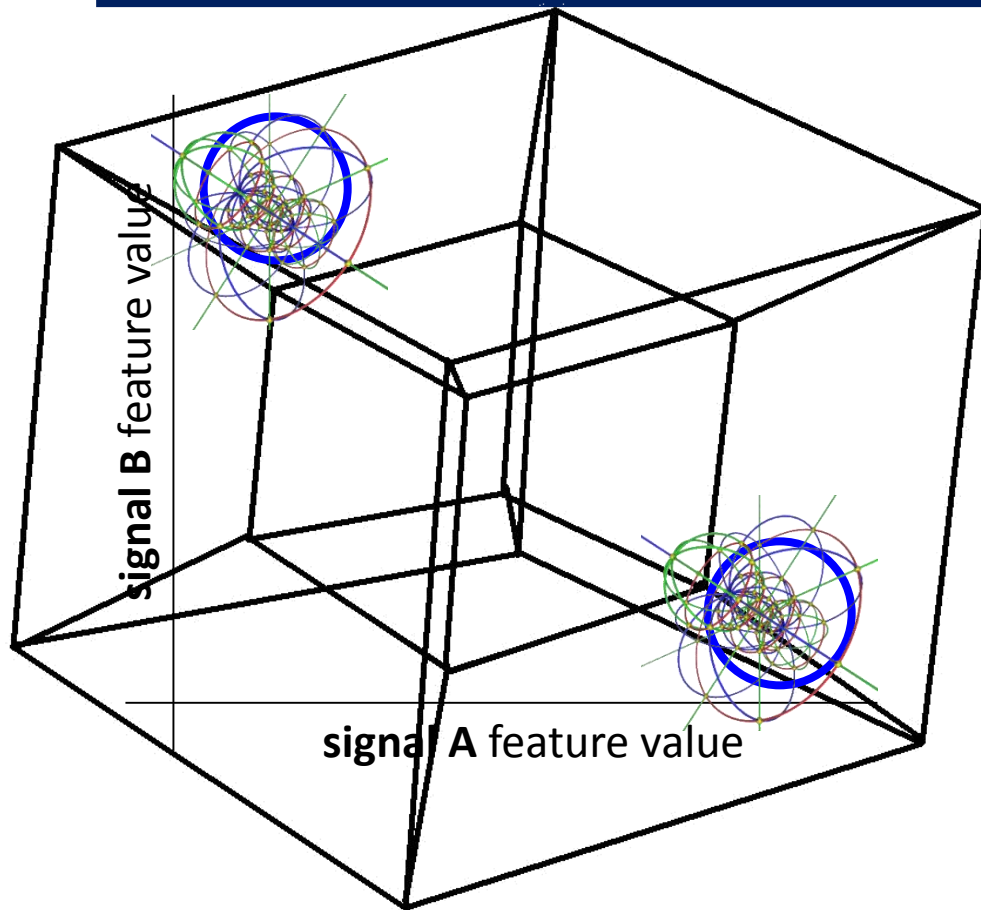
signal A

signal B



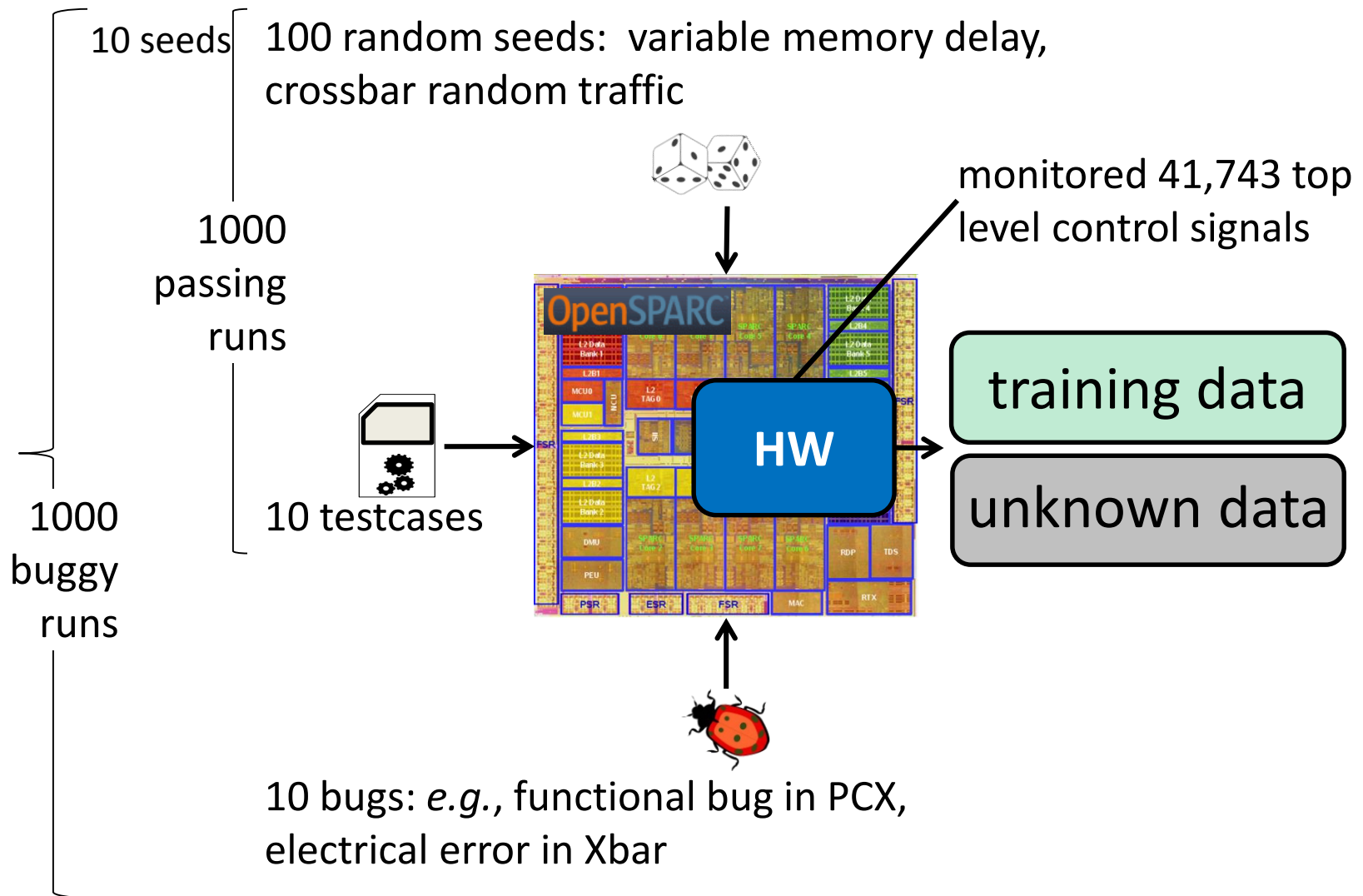
Clustering in X,000 dimensions

clustering
algorithm



- Each signal is a dimension
 - Circular clusters become hyper-spheres
 - High dimensionality is a challenge
- In practice:
 - Cap #signals in one clustering set (500)
 - Group signals by module(s) (100-500 signals)
 - Apply clustering to each group

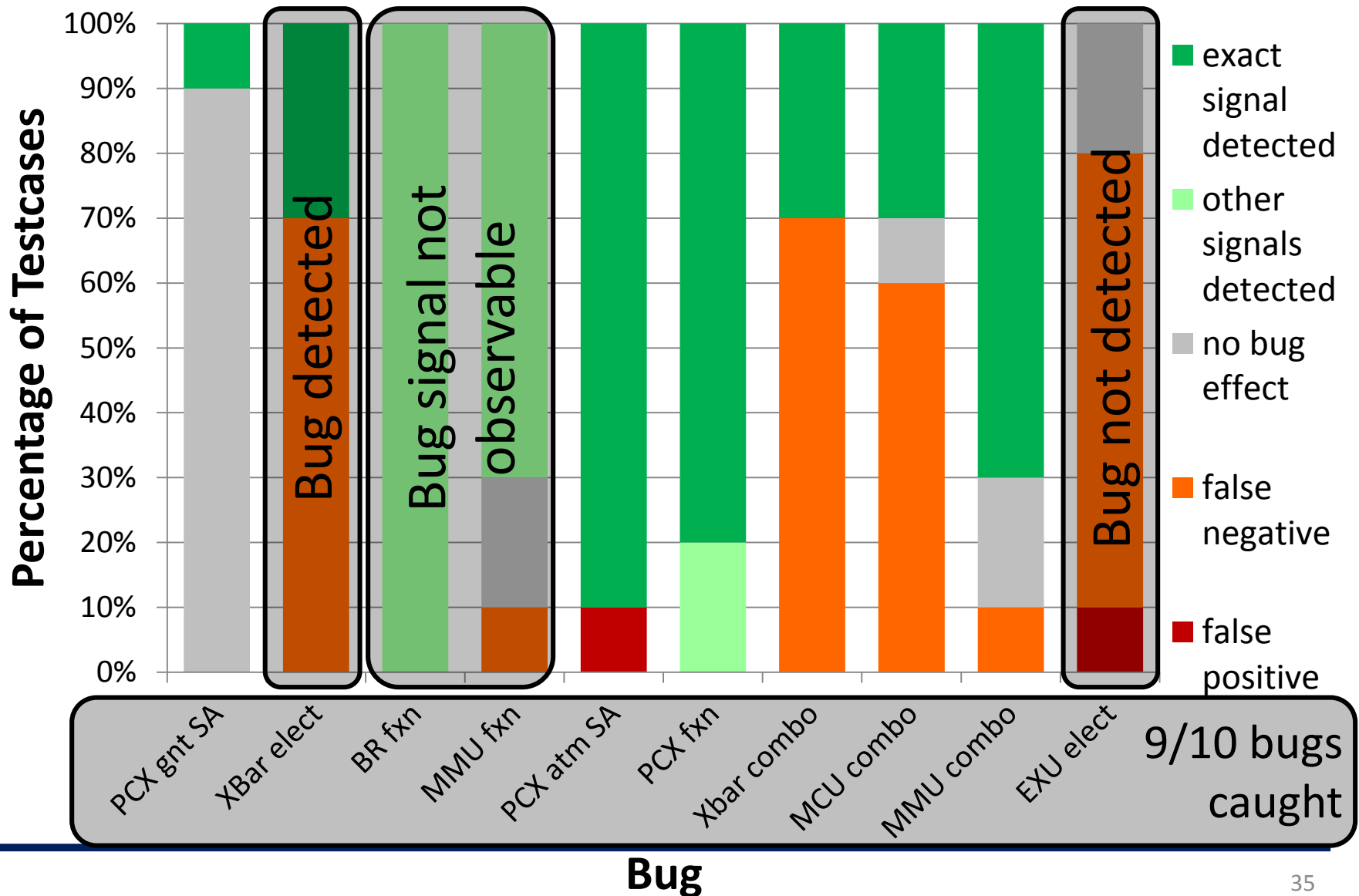
Experimental setup



Bug injection

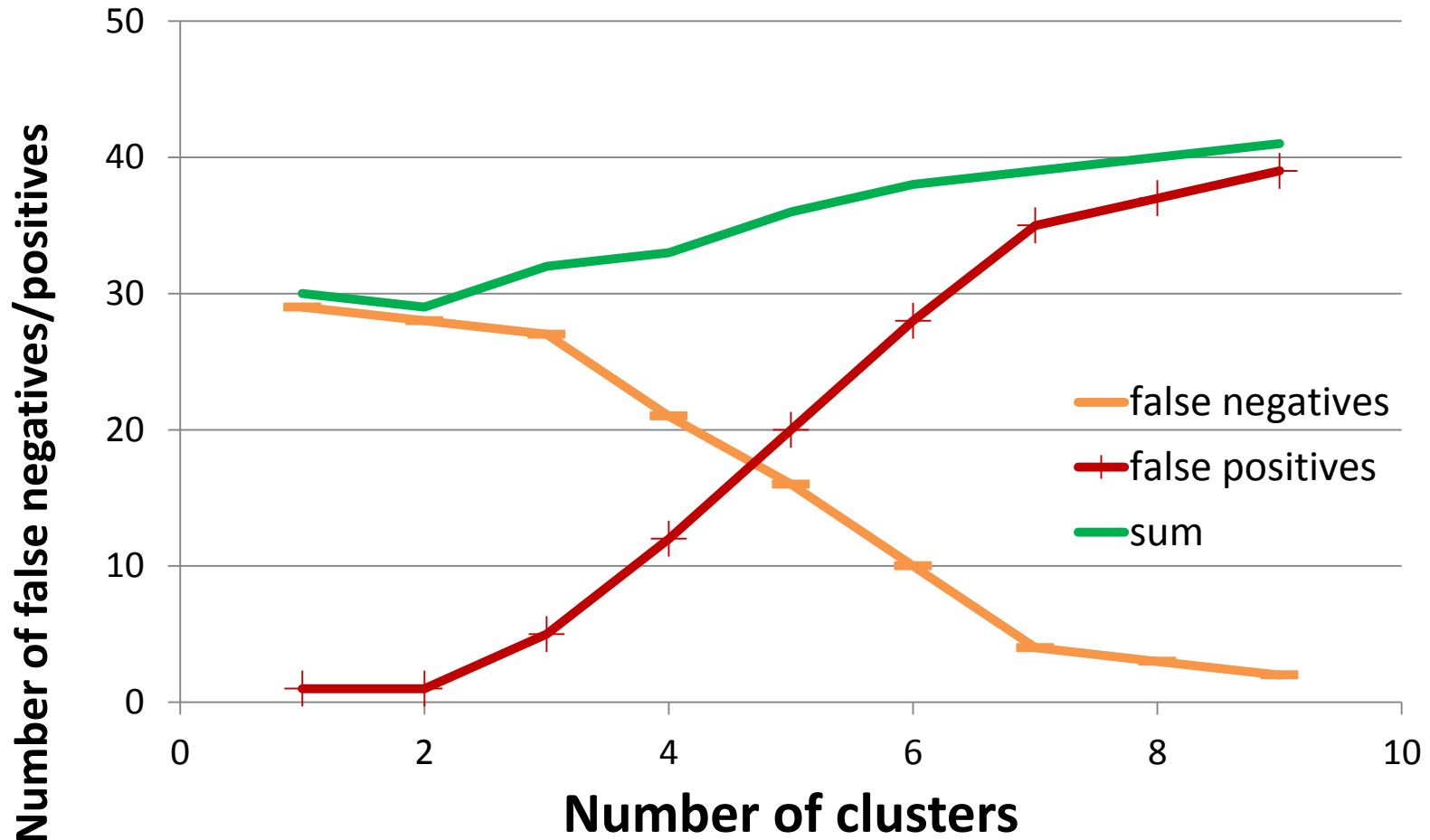
Bug	Description
PCX_gnt SA	Stuck-at in PCX grant
Xbar elect	Electrical error in crossbar
BR fxn	Functional bug in branch logic
MMU fxn	Functional bug in memory controller
PCX_atm SA	Stuck-at in PCX atomic grant
PCX fxn	Functional bug in PCX
XBar combo	Combined electrical errors in Xbar/PCX
MCU combo	Combined electrical errors in mem/PCX
MMU combo	Combined functional bugs in MMU/PCX
EXU elect	Electrical error in execute unit

Bug detection on OpenSPARC T2

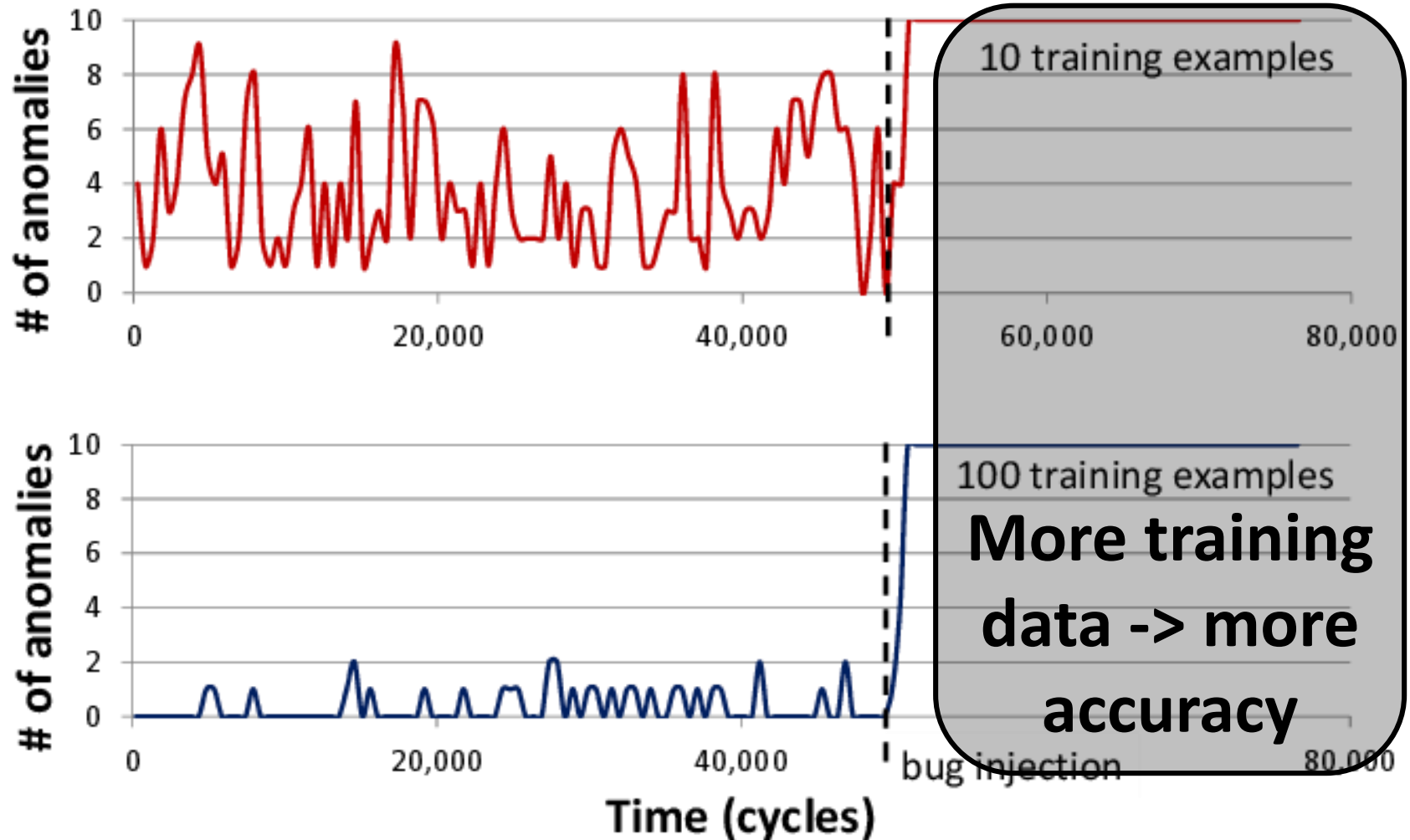


Number of clusters

Exercise: where does overfitting occur? Underfitting?

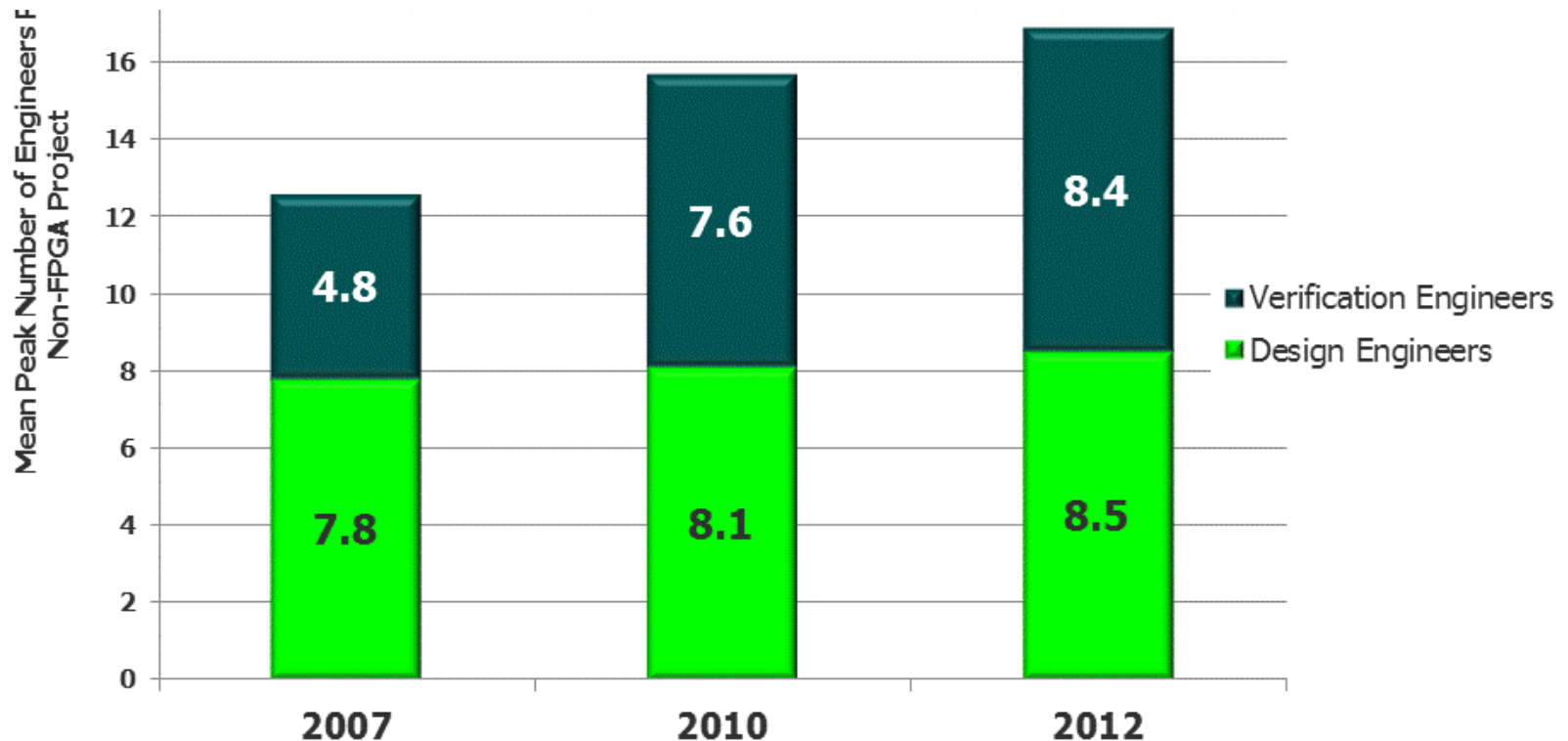


Bug signal vs. noise



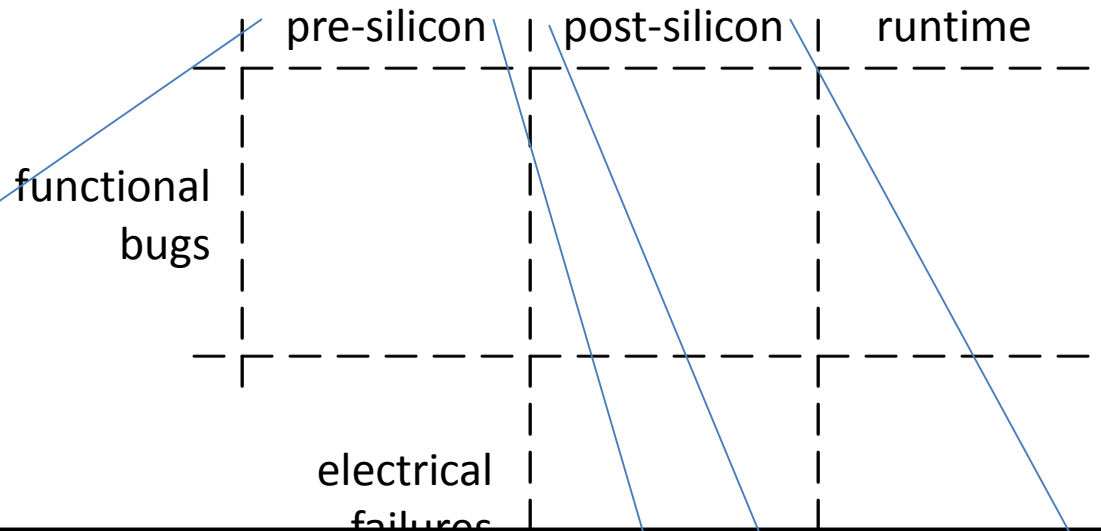
Impact

- Improved diagnosis of difficult bugs
- Improved verification efficiency

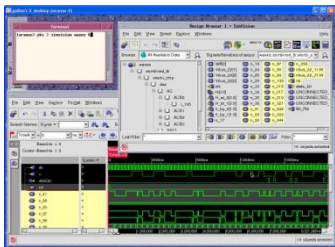


Future trends in verification

- Increasing high-speed verification
- Increasing data generated during verification



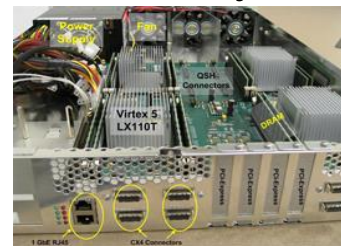
SW Simulation
1-10 cycles/s



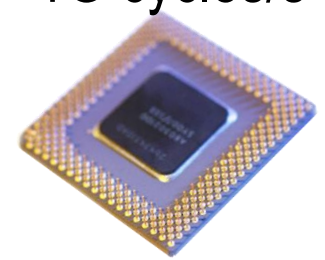
Acceleration
10-100k cycles/s



Emulation
10-100M cycles/s

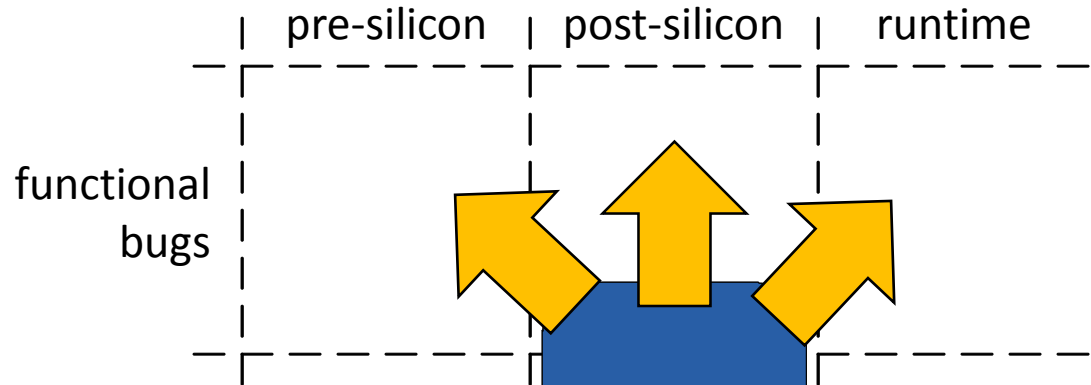


Silicon
1G cycles/s

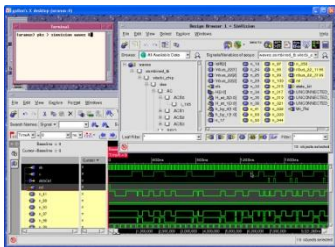


Future trends in verification

- Increasing high-speed verification
- Increasing data generated during verification



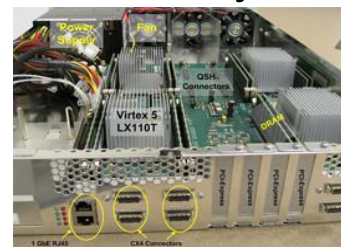
SW Simulation
1-10 cycles/s



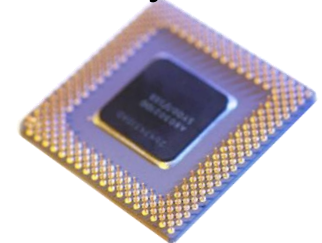
Acceleration
10-100k cycles/s



Emulation
10-100M cycles/s



Silicon
1G cycles/s



Research vision

Traditional
machine
learning
research

My research

How can
processors
help Big
Data?

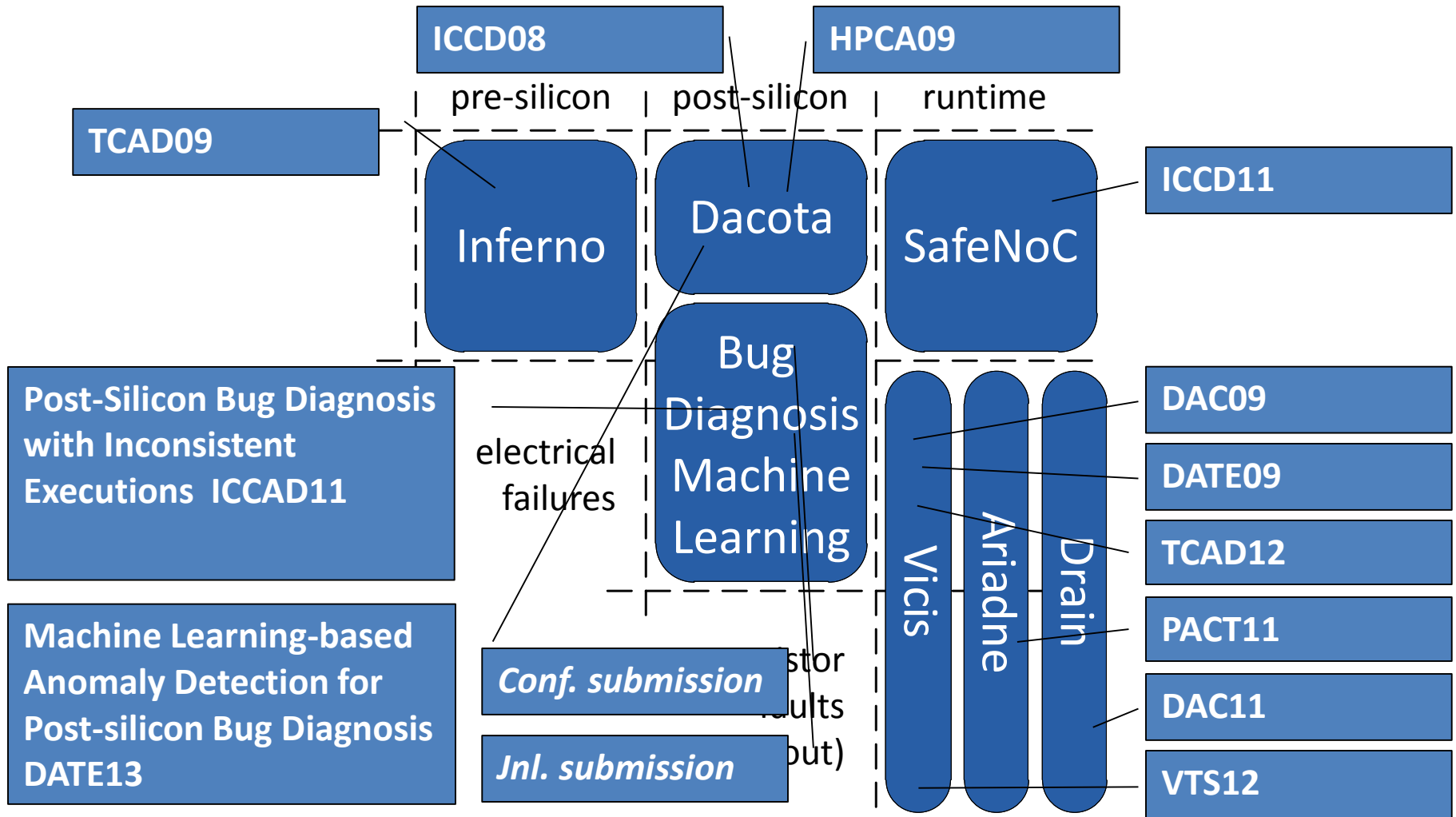
How can
Big Data
help
processors?

Data science for digital design

Research vision

- **Correctness** is the driving force behind my research
- My research brings a **data science approach** to electronic design automation
- Use machine learning techniques to enable verification to **keep up with growing design complexity**

Selected publications



More at andrewdeorio.com/research

Conclusion

- With a data science approach to electronic design automation, we can teach computers to verify themselves

