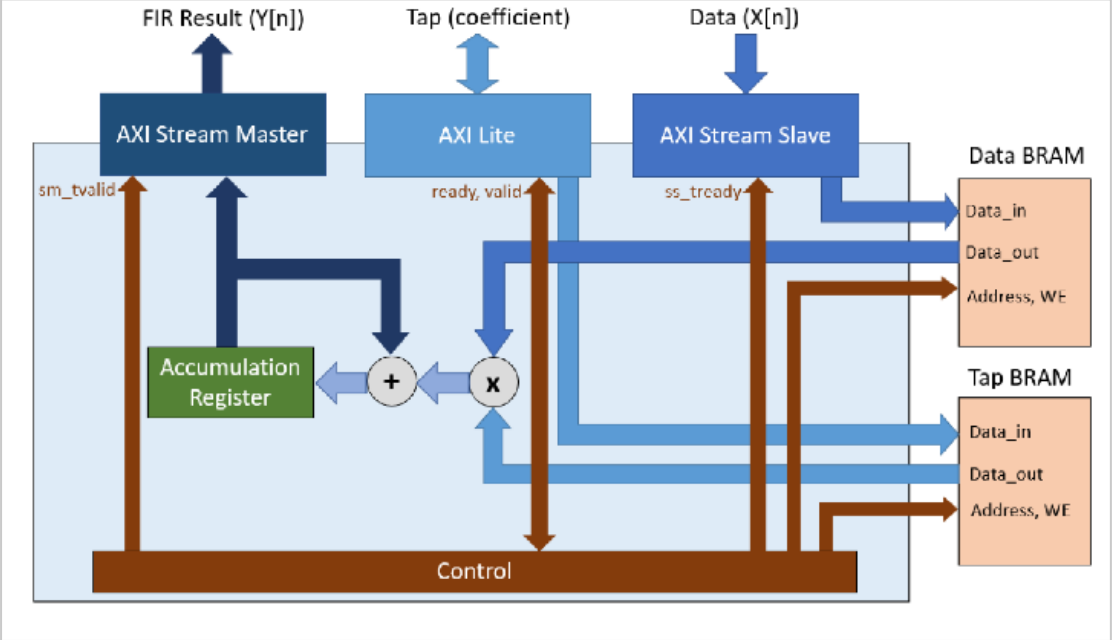
SOC Lab3 report

Overall system：

本次實驗和 lab2大致相同，只是此次需要撰寫 RTL code，實現具有 AXI-Lite、AXI-Stream interface 的 FIR。

Block Diagram：



Describe operation：

此次實驗的 data 和 tap 都是存於 BRAM 中，而又限定只能使用一個乘法器和一個加法器，所以我相乘累加了 11 個 cycle，才完成 FIR 的運算。

Resource usage：

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	212	0	0	53200	0.40
LUT as Logic	212	0	0	53200	0.40
LUT as Memory	0	0	0	17400	0.00
Slice Registers	118	0	0	106400	0.11
Register as Flip Flop	115	0	0	106400	0.11
Register as Latch	3	0	0	106400	<0.01
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

* Warning! The Final LUT count, after physical optimizations and full implem

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2. Memory
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+----------------+------+-------+------------+-----------+-------+
|    Site Type   | Used | Fixed | Prohibited | Available | Util% |
+----------------+------+-------+------------+-----------+-------+
| Block RAM Tile |    0 |     0 |          0 |       140 |  0.00 |
|   RAMB36/FIFO* |    0 |     0 |          0 |       140 |  0.00 |
|   RAMB18       |    0 |     0 |          0 |       280 |  0.00 |
+----------------+------+-------+------------+-----------+-------+
* Note: Each Block RAM Tile only has one FIFO logic available and the


3. DSP
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|    Site Type   | Used | Fixed | Prohibited | Available | Util% |
+----------------+------+-------+------------+-----------+-------+
| DSPs           |    3 |     0 |          0 |       220 |  1.36 |
|   DSP48E1 only |    3 |       |            |           |       |
+----------------+------+-------+------------+-----------+-------+
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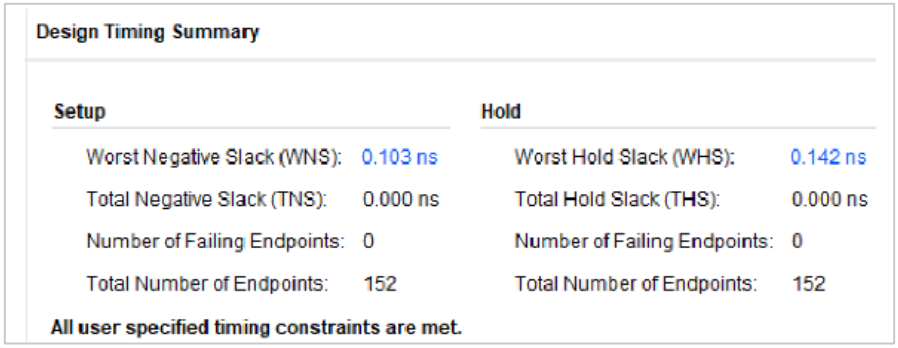
Timing Report：



Design Timing Summary

Setup		Hold	
Worst Negative Slack (WNS):	0.103 ns	Worst Hold Slack (WHS):	0.142 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	152	Total Number of Endpoints:	152

All user specified timing constraints are met.

Waveform：