112-1 SoC Design Laboratory
Lab4-2 submission guide

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Requirements

- Refer to https://github.com/bol-edu/caravel-soc_fpga-lab/blob/main/lab-caravel_fir/Lab4_2-caravel-fir.pdf

Submission (1/3)

- Hierarchy:
  - StudentID_lab4-2/
    - Report.pdf
    - .hex
    - fir.c
    - fir.h
    - User
      - bram.v
      - design.v
    - Github link
- Your Github link should attach the file
  - Design, Synthesis report(Including FF, LUT, Bram), Waveform, simulation.log, makefile,…etc.
  - Report

Submission (2/3)

- Github
  - README.md – introduce the content of the work, and how to replicate the work. (replicate to run simulation)
  - Design sources, user_project design, including Exmem, FIR RTL, Firmware code, Testbench
  - Synthesis area report, timing report, and simulation log files generated in the process.
- Report
  - Design block diagram – datapath, control-path
  - The interface protocol between firmware, user project and testbench
  - Waveform and analysis of the hardware/software behavior.
  - What is the FIR engine theoretical throughput, i.e. data rate? Actually measured throughput?
  - What is latency for firmware to feed data?
  - What techniques used to improve the throughput?
  - Does bram12 give better performance, in what way?
  - Can you suggest other method to improve the performance?
  - Any other insights ?

Submission (3/3)

- Compress all above files in a single zip file named
  - StudentID_lab4-2.zip
- Submit to Submit to NYCU E3
- Deadline: **11/2 (Thu.) 23:59**
  - 20% off for the late submission penalty within 3 days