Lab5 – Caravel FPGA

Objectives

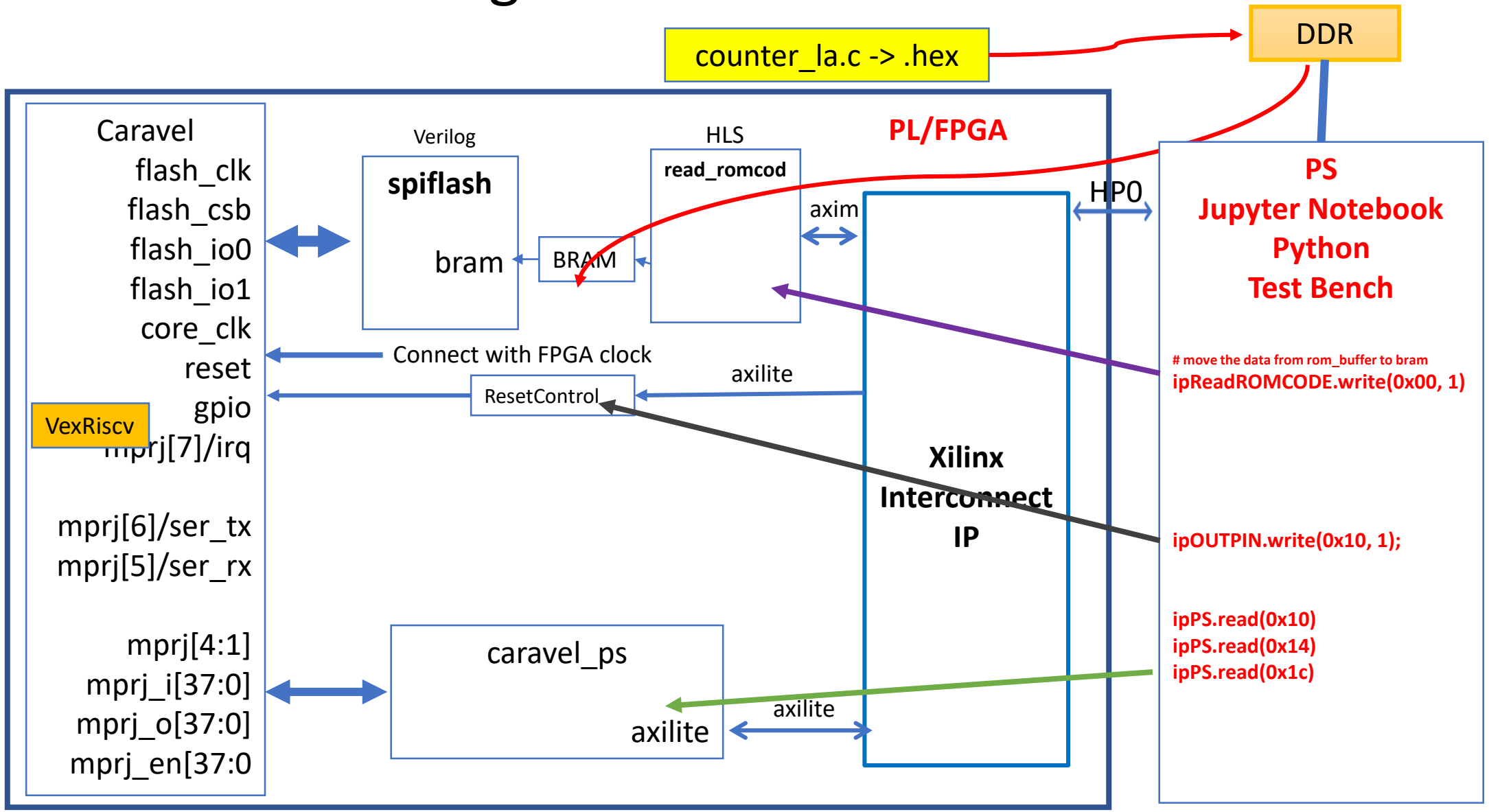
In Lab 4-0 (Caravel SOC Simulation), you know

- Caravel SOC design structure, and its spiflash, mprj interface
- Firmware compilation, and interaction with user project and testbench
- Testbench structure and how it interacts with Caravel SOC.

In this lab, you will understand

- Put the whole Caravel SOC simulation environment into FPGA
- Integrate IPs with Caravel SOC
  - spiflash,
  - romcode download (read_romcode),
  - mmio to access mprj (caravel-ps), and
  - mmio reset control
- Convert the verilog testbench to PS Python code

CaravelFPGA Block Diagram



Lab#5 – Caravel FPGA - build from each IP

- Reference - https://github.com/bol-edu/caravel-soc_fpga-lab/tree/main/labi
- Caravel FPGA introduction ppt:
  - Video: https://www.youtube.com/watch?v=EF3vXdaVof0&t=3826s
  - ppt: https://github.com/bol-edu/caravel-soc_fpga-lab/files/12035595/Caravel.FPGA.Introduction.pdf

Note： labi integrates the following three ip

- Lab1 – ROMCode : https://github.com/bol-edu/caravel-soc_fpga-lab/tree/main/lab1
- Lab2 – Spiflash : https://github.com/bol-edu/caravel-soc_fpga-lab/tree/main/lab2
- Lab3 – GPIO pins: https://github.com/bol-edu/caravel-soc_fpga-lab/tree/main/lab3

- Youtube – TA introduce Lab5
  - Lab5 Introduction : https://youtu.be/pTKtCEnLfpQ
  - Lab5 Block Design Flow: https://youtu.be/ha0d7D-oesA
- Implementation
  - Build the three IP: caravel_ps, read_romcode, output_pin
  - Build the FPGA bitstream – integrate the Caravel soc and the three IPs
  - Validate it on FPGA with the Jupyter Notebook run on PS
- Observe the following
  - AXI master to download the firmware code
  - Boot up with spiflash access
  - cpu wb cycles interaction with user project area
  - cpu interface with user project with la
  - User project output mprj pin
- Submission guideline – report

https://github.com/bol-edu/caravel-soc_fpga (IP is ready)