



112-1 SoC Design Laboratory

Lab2 submission guide

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Lab2 Contents

- Complete course-lab_2
 - FIR Design based on High-Level-Synthesis
 - Interface with Host by AXI Master, and Stream Interface
 - Deploy on PNYQ-Z2 / KV260
 - [OnlineFPGA manual](#)
- Report
- [course-lab_2 github](#)



Co-Simulation Log

- C-simulation log (TopFunctionName_csim.log)
 - Transcript of your testbench
 - Usually located at VitisHLSProjectName/solution1/csim/report
- Co-simulation log (TopFunctionName_cosim.rpt)
 - Transcript of your testbench
 - Usually located at VitisHLSProjectName/solution1/sim/report

```
INFO: [SIM 2] ***** CSIM start *****
INFO: [SIM 4] CSIM will launch GCC as the compiler.
make: 'csim.exe' is up to date.
>> Start test!
>> Comparing against output data...
>> Test passed!
-----
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] ***** CSIM finish *****
```

Simulation tool : xsim.

RTL	Status	Latency(Clock Cycles)			Interval(Clock Cycles)			Total Execution Time (Clock Cycles)
		min	avg	max	min	avg	max	
VHDL	NA	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	6779	6779	6779	NA	NA	NA	6779



Synthesis Report

- Synthesis Summary Report (csynth.rpt)
 - Summary report of your IP
- Synthesis Detail Report (TopFunctionName_csynth.rpt)
 - Detailed reports of your top function and sub-function
- Usually located at VitisHLSProjectName/solution1/syn/report

<pre>===== Vitis HLS Report for 'multp_2num' ===== * Date: Wed Jun 28 20:35:44 2023 * Version: 2022.1 (Build 3526262 on Mon Apr 18 15:47:01 MDT 2022) * Project: hls_ip * Solution: solution1 (Vivado IP Flow Target) * Product Family: zynq * Target device: xc7z020-clg400-1 ===== Performance Estimates ===== * Timing: * Summary: Clock Target Estimated Uncertainty ----- ----- ----- ----- ap_clk 10.00 ns 6.912 ns 2.70 ns * Latency: * Summary: Latency (cycles) Latency (absolute) Interval Pipeline min max min max min max Type ----- ----- ----- ----- ----- ----- ----- 3 3 30.000 ns 30.000 ns 4 4 no * Detail: * Instance: N/A * Loop: N/A ===== Utilization Estimates ===== * Summary: Name BRAM 18K1_DSP FF LUT URAM ----- ----- ----- ----- ----- ----- multp_2num 0 0 0 0 0 </pre>	<pre>===== Synthesis Summary Report of 'multp_2num' ===== * General Information: * Date: Wed Jun 28 20:35:44 2023 * Version: 2022.1 (Build 3526262 on Mon Apr 18 15:47:01 MDT 2022) * Project: hls_ip * Solution: solution1 (Vivado IP Flow Target) * Product Family: zynq * Target device: xc7z020-clg400-1 * Performance & Resource Estimates: PS: '*' for module; 'o' for loop; '*' for dataflow Modules Issue Latency Latency Iteration Trip Pipeline BRAM DSP FF LUT URAM & Loops Type Slack (cycles) (ns) Latency Interval Count ----- ----- ----- ----- ----- ----- ----- ----- ----- ----- ----- ----- multp_2num - 0.39 3 30.000 - 4 - no - 3 (1K) 409 (-0K) 307 (-0K) - </pre> <pre>===== HW Interfaces ===== * S_AXILITE Interfaces Interface Data Width Address Width Offset Register ----- ----- ----- ----- ----- s_axi_control 32 6 16 0 * S_AXILITE Registers Interface Register Offset Width Access Description Bit Fields ----- ----- ----- ----- ----- ----- ----- s_axi_control n32In1 0x10 32 W Data signal of n32In1 s_axi_control n32In2 0x18 32 W Data signal of n32In2 s_axi_control pn32ResOut 0x20 32 R Data signal of pn32ResOut s_axi_control pn32ResOut_ctrl 0x24 32 R Control signal of pn32ResOut 0=pn32ResOut_ap_vld * TOP LEVEL CONTROL Interface Type Ports ----- ----- ----- s_axi_control control 0 </pre>
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Bitstream and Hardware Handoff

- Bitstream (.bit)

- Contains the programming information for FPGA device
- Usually located at :
 - VivadoProjectName/ VivadoProjectName.runs/impl_1/design_1_wrapper.bit

```
> vwd_Multip2Num > vwd_Multip2Num.runs > impl_1
```

```
design_1_wrapper.bit
```

- Hardware Handoff (.hwh)

- Contain block design information and is used by software tools to a targeted application
- Usually located at :
 - VivadoProjectName/VivadoProjectName.gen/sources_1/bd/design_1/hw_handoff/design_1.hwh

```
> vwd_Multip2Num > vwd_Multip2Num.gen > sources_1 > bd > design_1 > hw_handoff
```

```
design_1.hwh
```



Online FPGA Remote Login

- We have set up some PYNQ-Z2/KV260 boards in the lab. You can use them remotely
- Refer to OnlineFPGA使用者手冊_20230620.pdf
- IP : 140.112.207.200 : 1000
- Specify username : boledupynq
- password : boledupynq



Lab2 Submission File

- Folder Hierarchy:
 - StudentID_lab2/
 - Lab2/
 - FIRN11MAXI/
 - .hwh, .bit (generated from vivado)
 - csynth.rpt, xxx_csynth.rpt, xxx_csim.log, xxx_cosim.rpt (generated from vitis_hls)
 - FIRN11Stream/
 - .hwh, .bit (generated from vivado)
 - csynth.rpt, xxx_csynth.rpt, xxx_csim.log, xxx_cosim.rpt (generated from vitis_hls)
 - report.pdf
 - Compress all above files in a single zip file named **StudentID_lab2.zip**
 - Submit to NYCU E3
 - **Deadline : 10/5 (Thu.) 23:59**
 - 30% off for the late submission penalty



Report

- Brief introduction about the overall system
- What is observed & learned
 - Differences between MAXI and Stream interface
 - Differences between csim and cosim
- Screen dump
 - Performance
 - Utilization
 - Interface
 - Co-simulation transcript/waveform
 - Jupyter Notebook execution results