I. Overall system：

FIR with Interface AXI-Master：

FIR 的 in、out 都是由 AXI-master 去傳輸，至於 FIR 的參數則是用 AXI-Lite。所以 Master 產生的 ip 是由 AXI-Lite 和 AXI-Master 的 interface 去做溝通。而 AXI-Lite 的溝通方式是透過 interconnect 接到 PS side 的 GP port。而 AXI-master 則是透過 interconnect 接到 PS side 的 HP port。

FIR with Interface AXI-Stream：

而此實驗 FIR 的 in、out 則改為使用 stream 去傳輸。也因此它無法直接透過 interconnect 接到 PS side，它需要在中間多一個 DMA，所以對於 in、out 的連接，需要多2個 DMA。其餘大致就和前面的實驗相同。

II. What is observed & learned：

學到 AXI-Master、AXI-Stream 協議的內容，知道它們 in、out 怎麼和 PS side 做溝通，也更熟悉 lab1 的流程，對 SOC 也稍微有一些概念了。而 Master、Stream 的差異在上述有大致說明了。至於 csim、cosim 的差異則是在其 kernel 的不同，前者是使用 C，而後者是使用 verilog 完成的。

III. Screen dump：

由於兩個實驗大致相同，所以這邊我只放 AXI-master 的 FIR。

1. Performance

```
================================================================
== Performance Estimates
================================================================
+ Timing:
    * Summary:
    +--------+----------+----------+------------+
    |  Clock |  Target  | Estimated| Uncertainty|
    +--------+----------+----------+------------+
    |ap_clk  |  10.00 ns|  7.300 ns|     2.70 ns|
    +--------+----------+----------+------------+

+ Latency:
    * Summary:
    +---------+---------+----------+----------+-----+-----+---------+
    |  Latency (cycles) |  Latency (absolute) |  Interval | Pipeline|
    |   min   |   max   |    min   |    max   | min | max |   Type  |
    +---------+---------+----------+----------+-----+-----+---------+
    |        ?|        ?|         ?|         ?|    ?|    ?|       no|
    +---------+---------+----------+----------+-----+-----+---------+

    + Detail:
        * Instance:
        +-----------------------------------------+---------------------------------+---------+---------+----------+----------+-----+-----+---------+
        |                                         |                                 |  Latency (cycles) |  Latency (absolute) |  Interval | Pipeline|
        |                 Instance                |              Module             |   min   |   max   |    min   |    max   | min | max |   Type  |
        +-----------------------------------------+---------------------------------+---------+---------+----------+----------+-----+-----+---------+
        |grp_fir_n11_maxi_Pipeline_XFER_LOOP_fu_242  |fir_n11_maxi_Pipeline_XFER_LOOP  |        ?|        ?|         ?|         ?|    ?|    ?|       no|
        +-----------------------------------------+---------------------------------+---------+---------+----------+----------+-----+-----+---------+

        * Loop:
        N/A
```

2. Utilization

```
================================================================
== Utilization Estimates
================================================================
* Summary:
+-----------------+---------+-----+--------+-------+-----+
|       Name      | BRAM_18K| DSP |   FF   |  LUT  | URAM|
+-----------------+---------+-----+--------+-------+-----+
|DSP              |        -|    -|       -|      -|    -|
|Expression       |        -|    -|       0|     40|    -|
|FIFO             |        -|    -|       -|      -|    -|
|Instance         |        0|   33|    3806|   2838|    -|
|Memory           |        -|    -|       -|      -|    -|
|Multiplexer      |        -|    -|       -|    175|    -|
|Register         |        -|    -|     650|      -|    -|
+-----------------+---------+-----+--------+-------+-----+
|Total            |        0|   33|    4456|   3053|    0|
+-----------------+---------+-----+--------+-------+-----+
|Available        |      280|  220|  106400|  53200|    0|
+-----------------+---------+-----+--------+-------+-----+
|Utilization (%)  |        0|   15|       4|      5|    0|
+-----------------+---------+-----+--------+-------+-----+
```

3. Interface

```
================================================================
== Interface
================================================================
* Summary:
+-----------------------+-----+-----+------------+--------------+--------------+
|       RTL Ports       | Dir | Bits|  Protocol  | Source Object|    C Type    |
+-----------------------+-----+-----+------------+--------------+--------------+
|s_axi_control_AWVALID  |   in|    1|       s_axi|       control|         array|
|s_axi_control_AWREADY  |  out|    1|       s_axi|       control|         array|
|s_axi_control_AWADDR   |   in|    7|       s_axi|       control|         array|
|s_axi_control_WVALID   |   in|    1|       s_axi|       control|         array|
|s_axi_control_WREADY   |  out|    1|       s_axi|       control|         array|
|s_axi_control_WDATA    |   in|   32|       s_axi|       control|         array|
|s_axi_control_WSTRB    |   in|    4|       s_axi|       control|         array|
|s_axi_control_ARVALID  |   in|    1|       s_axi|       control|         array|
|s_axi_control_ARREADY  |  out|    1|       s_axi|       control|         array|
|s_axi_control_ARADDR   |   in|    7|       s_axi|       control|         array|
|s_axi_control_RVALID   |  out|    1|       s_axi|       control|         array|
|s_axi_control_RREADY   |   in|    1|       s_axi|       control|         array|
|s_axi_control_RDATA    |  out|   32|       s_axi|       control|         array|
|s_axi_control_RRESP    |  out|    2|       s_axi|       control|         array|
|s_axi_control_BVALID   |  out|    1|       s_axi|       control|         array|
|s_axi_control_BREADY   |   in|    1|       s_axi|       control|         array|
|s_axi_control_BRESP    |  out|    2|       s_axi|       control|         array|
|ap_clk                 |   in|    1|  ap_ctrl_hs|  fir_n11_maxi|  return value|
|ap_rst_n               |   in|    1|  ap_ctrl_hs|  fir_n11_maxi|  return value|
|interrupt              |  out|    1|  ap_ctrl_hs|  fir_n11_maxi|  return value|
|m_axi_gmem_AWVALID     |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWREADY     |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWADDR      |  out|   64|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWID        |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWLEN       |  out|    8|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWSIZE      |  out|    3|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWBURST     |  out|    2|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWLOCK      |  out|    2|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWCACHE     |  out|    4|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWPROT      |  out|    3|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWQOS       |  out|    4|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWREGION    |  out|    4|       m_axi|          gmem|       pointer|
|m_axi_gmem_AWUSER      |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_WVALID      |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_WREADY      |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_WDATA       |  out|   32|       m_axi|          gmem|       pointer|
|m_axi_gmem_WSTRB       |  out|    4|       m_axi|          gmem|       pointer|
|m_axi_gmem_WLAST       |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_WID         |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_WUSER       |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARVALID     |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARREADY     |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARADDR      |  out|   64|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARID        |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARLEN       |  out|    8|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARSIZE      |  out|    3|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARBURST     |  out|    2|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARLOCK      |  out|    2|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARCACHE     |  out|    4|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARPROT      |  out|    3|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARQOS       |  out|    4|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARREGION    |  out|    4|       m_axi|          gmem|       pointer|
|m_axi_gmem_ARUSER      |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_RVALID      |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_RREADY      |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_RDATA       |   in|   32|       m_axi|          gmem|       pointer|
|m_axi_gmem_RLAST       |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_RID         |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_RUSER       |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_RRESP       |   in|    2|       m_axi|          gmem|       pointer|
|m_axi_gmem_BVALID      |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_BREADY      |  out|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_BRESP       |   in|    2|       m_axi|          gmem|       pointer|
|m_axi_gmem_BID         |   in|    1|       m_axi|          gmem|       pointer|
|m_axi_gmem_BUSER       |   in|    1|       m_axi|          gmem|       pointer|
+-----------------------+-----+-----+------------+--------------+--------------+
```

4. Co-simulation transcript /waveform

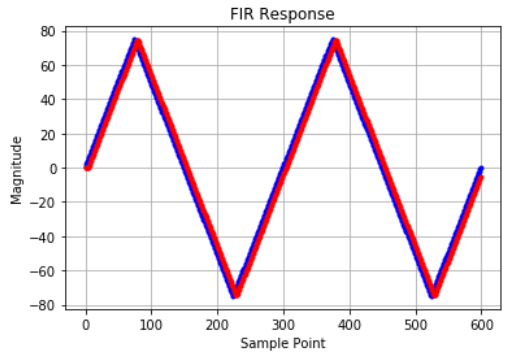
```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling ../../../../hls_FIRN11MAXI/FIRTester.cpp in debug mode
   Generating csim.exe
>> Start test!
>> Comparing against output data...
>> Test passed!
------------------------
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************
```

5. Jupyter Notebook execution results

```
    plt.grid(True)
    plt.show() # In Jupyter, press Tab + Shift keys to show plot then redo run

    print("============================")
    print("Exit process")


Entry: /usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py
System argument(s): 3
Start of "/usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py"
Kernel execution time: 0.0005750656127929688 s
```




```
============================
Exit process
```