112-1 SoC Design Laboratory Lab2 submission guide

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Lab2 Contents

- ## Complete course-lab_2
  - ### FIR Design based on High-Level-Synthesis
  - ### Interface with Host by AXI Master, and Stream Interface
  - ### Deploy on PNYQ-Z2 / KV260
    - #### OnlineFPGA_manual
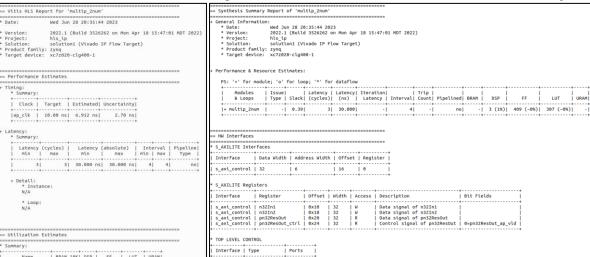
- ## Report

- ## course-lab_2 github

Co-Simulation Log

- C-simulation log (TopFunctionName_csim.log)
  - Transcript of your testbench
  - Usually located at VitisHLSProjectName/solution1/csim/report
- Co-simulation log (TopFunctionName_cosim.rpt)
  - Transcript of your testbench
  - Usually located at VitisHLSProjectName/solution1/sim/report

```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
make: 'csim.exe' is up to date.
>> Start test!
>> Comparing against output data...
>> Test passed!
-------------------------
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************
```

```
Simulation tool  : xsim.
+--------+--------+---------------------------------+-----------------------------+------------------+
|        |        |      Latency(Clock Cycles)      |    Interval(Clock Cycles)   | Total Execution Time |
+  RTL   + Status +---------------------------------+-----------------------------+   (Clock Cycles)     +
|        |        |   min   |   avg   |    max      |  min   |  avg   |   max     |                      |
|  VHDL  |     NA |      NA |      NA |      NA     |     NA |     NA |     NA    |                   NA |
| Verilog|   Pass |    6779 |    6779 |    6779     |     NA |     NA |     NA    |                 6779 |
+--------+--------+---------------------------------+-----------------------------+------------------+
```

Synthesis Report

- Synthesis Summary Report (csynth.rpt)
  - Summary report of your IP

- Synthesis Detail Report (TopFunctionName_csynth.rpt)
  - Detailed reports of your top function and sub-function

- Usually located at VitisHLSProjectName/solution1/syn/report

Bitstream and Hardware Handoff

- Bitstream (.bit)
  - Contains the programming information for FPGA device
  - Usually located at：
    - VivadoProjectName/ VivadoProjectName.runs/impl_1/design_1_wrapper.bit

> vvd_Multip2Num > vvd_Multip2Num.runs > impl_1

design_1_wrapper.bit

- Hardware Handoff (.hwh)
  - Contain block design information and is used by software tools to a targeted application
  - Usually located at：
    - VivadoProjectName/VivadoProjectName.gen/sources_1/bd/design_1/hw_handoff/design_1.hwh

> vvd_Multip2Num > vvd_Multip2Num.gen > sources_1 > bd > design_1 > hw_handoff

design_1.hwh

Online FPGA Remote Login

- We have set up some PYNQ-Z2/KV260 boards in the lab. You can use them remotely
- Refer to OnlineFPGA使用者手冊_20230620.pdf
- IP：140.112.207.200：1000
- Specify username：boledupynq
- password：boledupynq

Lab2 Submission File

- Folder Hierarchy:
  - StudentID_lab2/
    - Lab2/
      - FIRN11MAXI/
        - .hwh, .bit (generated from vivado)
        - csynth.rpt, xxx_csynth.rpt, xxx_csim.log, xxx_cosim.rpt (generated from vitis_hls)
      - FIRN11Stream/
        - .hwh, .bit (generated from vivado)
        - csynth.rpt, xxx_csynth.rpt, xxx_csim.log, xxx_cosim.rpt (generated from vitis_hls)
      - report.pdf
  - Compress all above files in a single zip file named **StudentID_lab2.zip**
  - Submit to NYCU E3
  - **Deadline：10/5 (Thu.) 23:59**
    - 30% off for the late submission penalty

Report

- Brief introduction about the overall system

- What is observed & learned
  - Differences between MAXI and Stream interface
  - Differences between csim and cosim

- Screen dump
  - Performance
  - Utilization
  - Interface
  - Co-simulation transcript/waveform
  - Jupyter Notebook execution results