Block Design Guide

SoC Design

Block Design Guide

- In Lab1 and Lab2, you may know how to create a block design and connect each IP.
- In this document, I'll introduce how to build block design by TCL script

Create Project

```
set _xil_proj_name “vvd_caravel_fpga”
create_project ${_xil_proj_name} ./${_xil_proj_name} -part xc7z020clg400-1
set proj_dir [get_property directory [current_project]]
set origin_dir “.”
set obj [get_filesets sources_1]
```

Add files

```
set files [list \
 [file normalize "${origin_dir}/vitis_prj/verilog_spiflash/spiflash.v"] \
 [file normalize "${origin_dir}/vvd_srcs/caravel_soc/vip/RAM256.v"] \
 [file normalize "${origin_dir}/vvd_srcs/caravel_soc/vip/RAM128.v"] \
 [file normalize "${origin_dir}/vvd_srcs/caravel_soc/rtl/soc/VexRiscv_MinDebugCache.v"] \
 [file normalize "${origin_dir}/vvd_srcs/caravel_soc/rtl/soc/chip_io.v"] \
 [file normalize "${origin_dir}/vvd_srcs/caravel_soc/rtl/soc/gpio_control_block.v"] \
 [file normalize "${origin_dir}/vvd_srcs/caravel_soc/rtl/soc/gpio_defaults_block.v"] \
 [file normalize "${origin_dir}/vvd_srcs/caravel_soc/rtl/soc/housekeeping.v"] \
 [file normalize "${origin_dir}/vvd_srcs/caravel_soc/rtl/soc/housekeeping_spi.v"] \
 [file normalize "${origin_dir}/vvd_srcs/caravel_soc/rtl/soc/mgmt_core.v"] \
 [file normalize "${origin_dir}/vvd_srcs/caravel_soc/rtl/soc/mgmt_core_wrapper.v"] \
 [file normalize "${origin_dir}/vvd_srcs/caravel_soc/rtl/soc/mprj_io.v"] \
 [file normalize "${origin_dir}/vvd_srcs/caravel_soc/rtl/soc/caravel.v"] \
 [file normalize "${origin_dir}/vvd_srcs/caravel_soc/rtl/user/${user_design_file}"] \
 [file normalize "${origin_dir}/vvd_srcs/caravel_soc/rtl/user/bram.v"] \
 [file normalize "${origin_dir}/vvd_srcs/caravel_soc/rtl/user/user_project_wrapper.v"] \
 [file normalize "${origin_dir}/vvd_srcs/caravel_soc/rtl/header/user_defines.v"] \
 [file normalize "${origin_dir}/vvd_srcs/caravel_soc/rtl/header/defines.v"] \
]
add_files -norecurse -fileset $obj $files
```

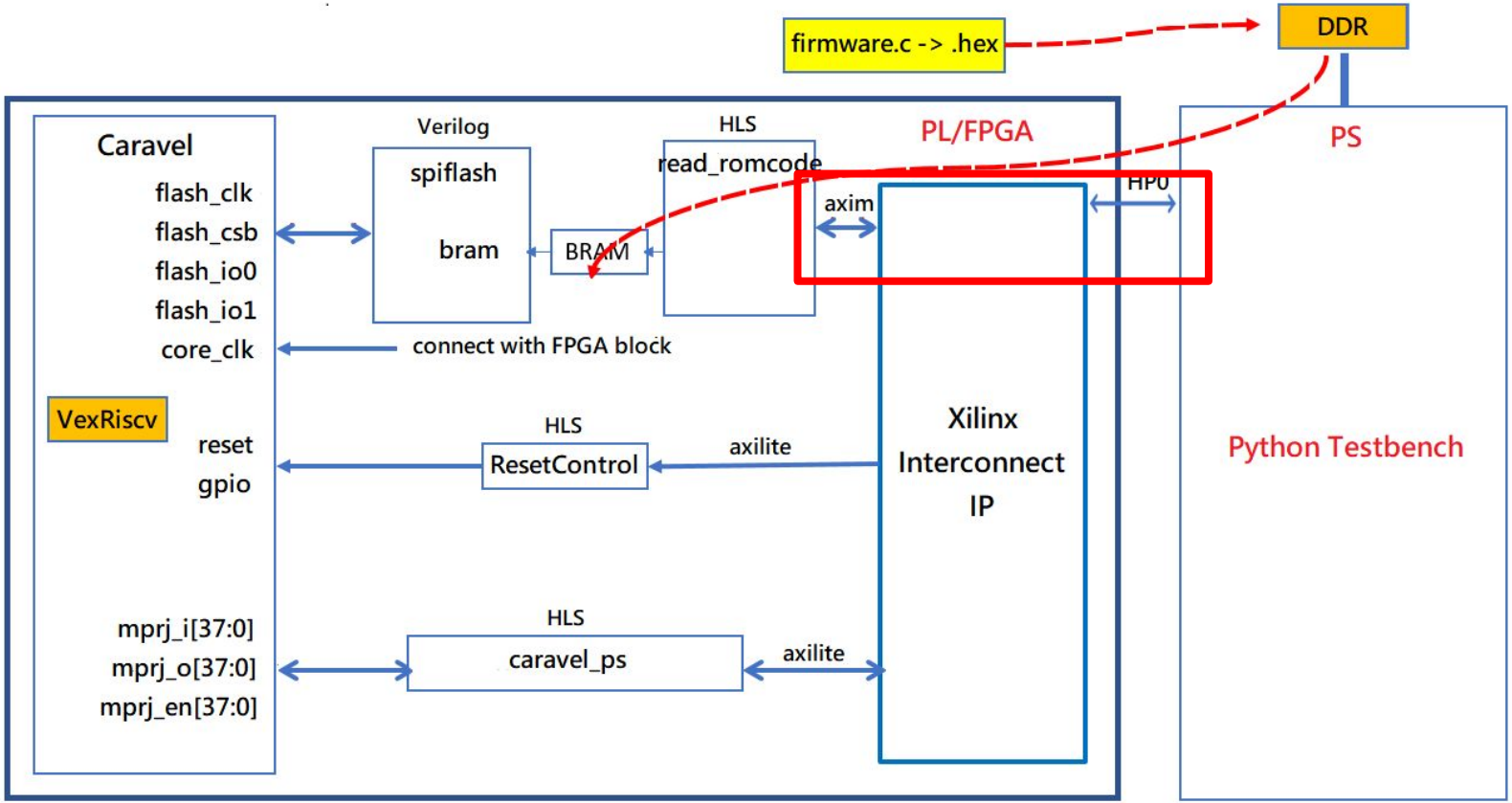
Add Define and Pre-builded IP

```
set file "$origin_dir/vvd_srcs/caravel_soc/rtl/header/user_defines.v"
set file [file normalize $file]
set file_obj [get_files -of_objects [get_filesets sources_1] [list "*$file"]]
set_property -name "file_type" -value "Verilog Header" -objects $file_obj
set_property -name "is_global_include" -value "1" -objects $file_obj

set file "$origin_dir/vvd_srcs/caravel_soc/rtl/header/defines.v"
set file [file normalize $file]
set file_obj [get_files -of_objects [get_filesets sources_1] [list "*$file"]]
set_property -name "file_type" -value "Verilog Header" -objects $file_obj
set_property -name "is_global_include" -value "1" -objects $file_obj

set obj [get_filesets sources_1]
set_property "ip_repo_paths" "[file normalize "$origin_dir/vitis_prj/hls_caravel_ps"]
                              [file normalize "$origin_dir/vitis_prj/hls_output_pin"]
                              [file normalize "$origin_dir/vitis_prj/hls_read_romcode"]" $obj
update_ip_catalog -rebuild
```

Create Block Design

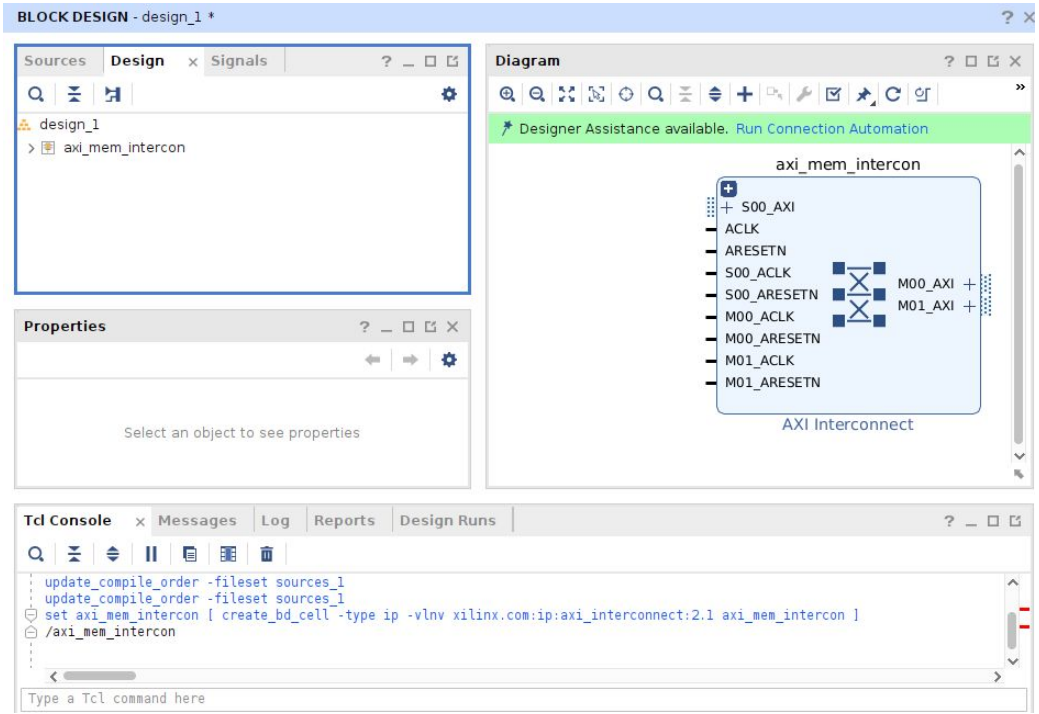
```
set design_name design_1
create_bd_design $design_name
```

Create AXI Interconnect for readmem



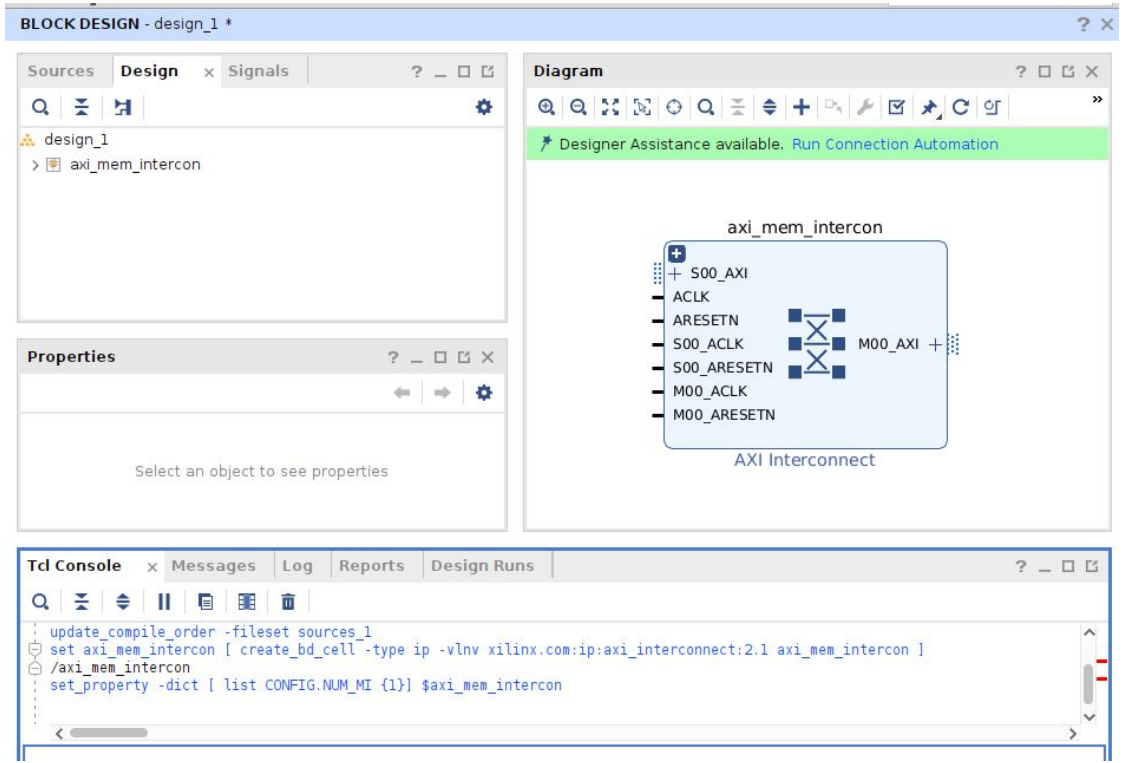
Create AXI Interconnect for readmem- (1)

```
set axi_mem_intercon [ create_bd_cell -type ip -vlnv xilinx.com:ip:axi_interconnect:2.1
axi_mem_intercon ]
```



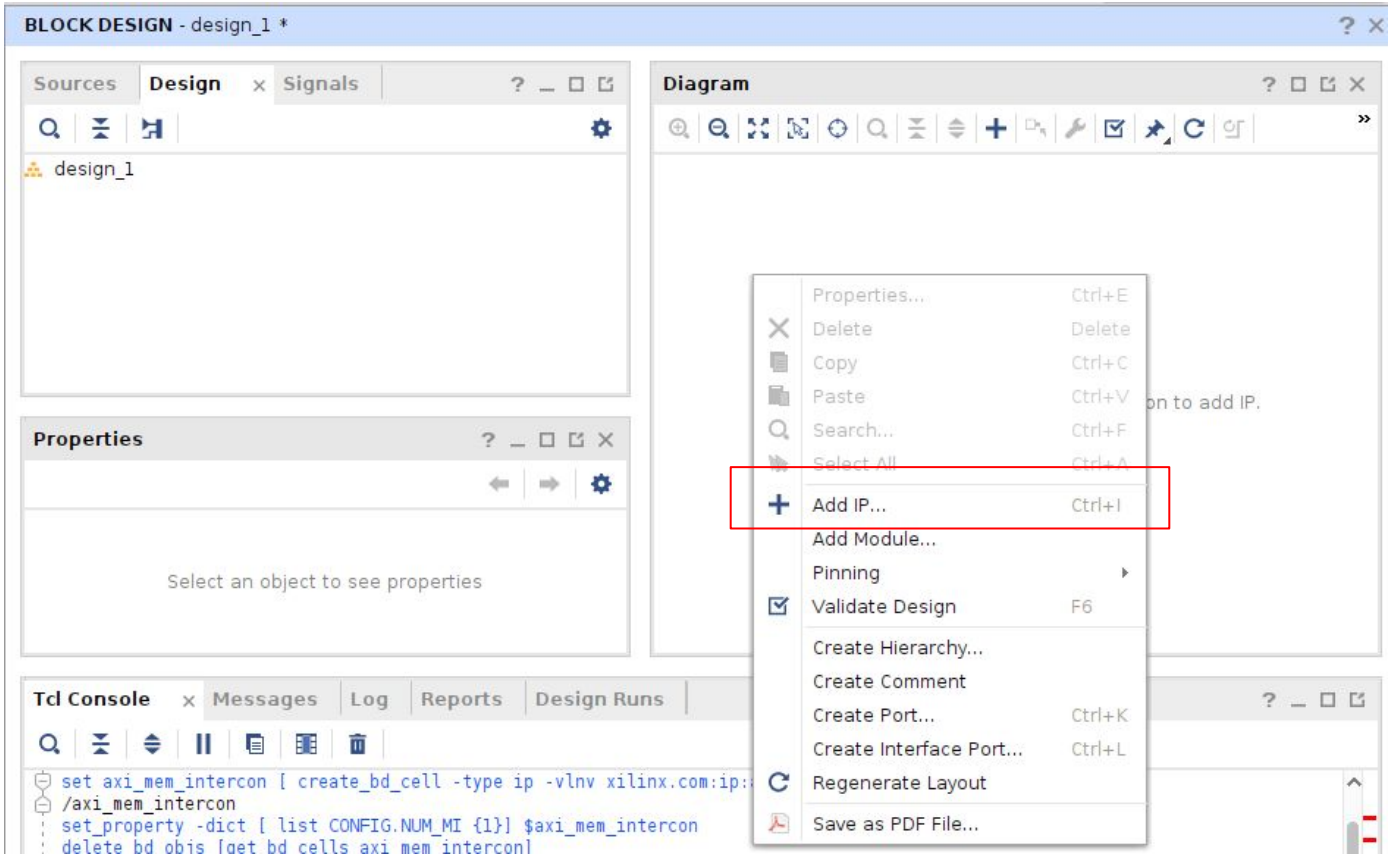
Create AXI Interconnect for readmem- (2)

```
set_property -dict [ list CONFIG.NUM_MI {1}] $axi_mem_intercon
```

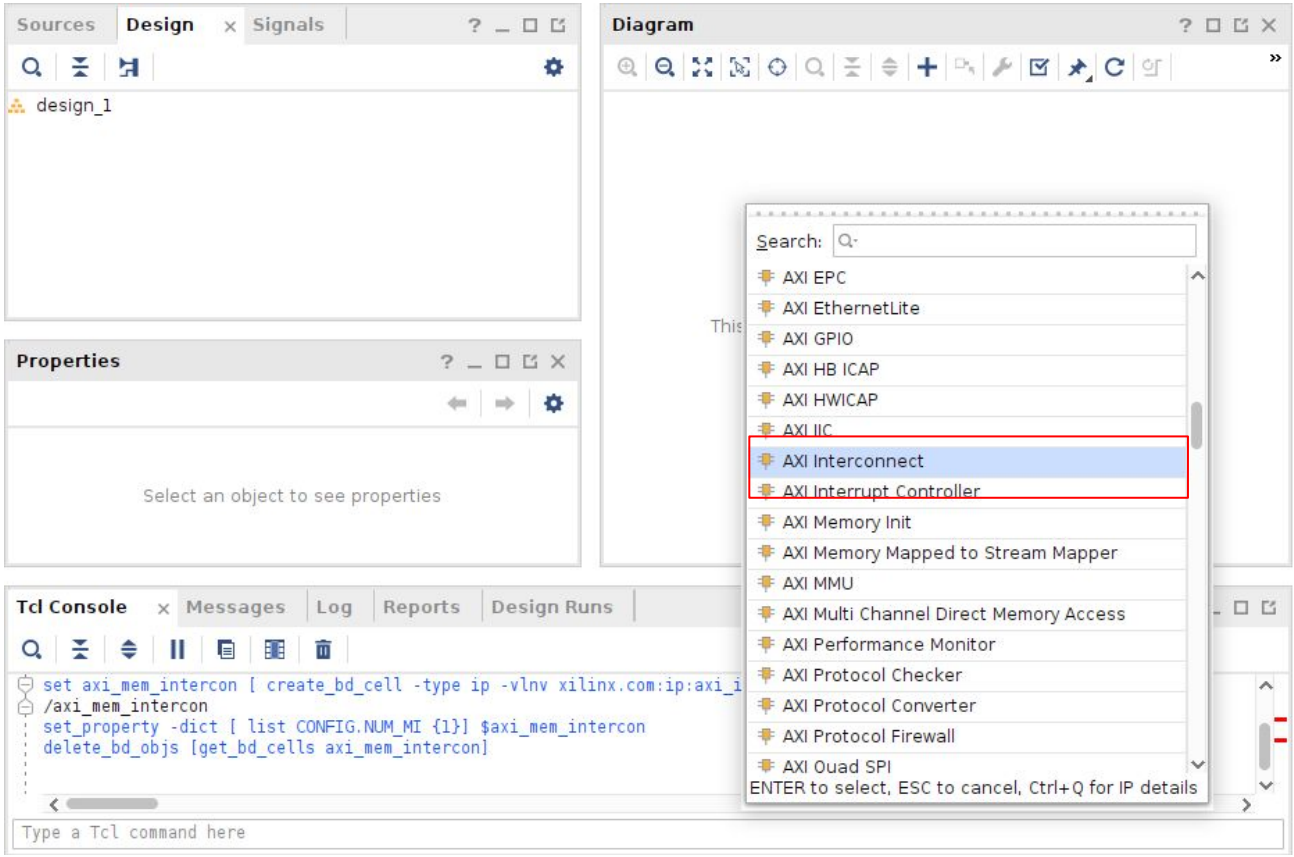


- Set one master channel

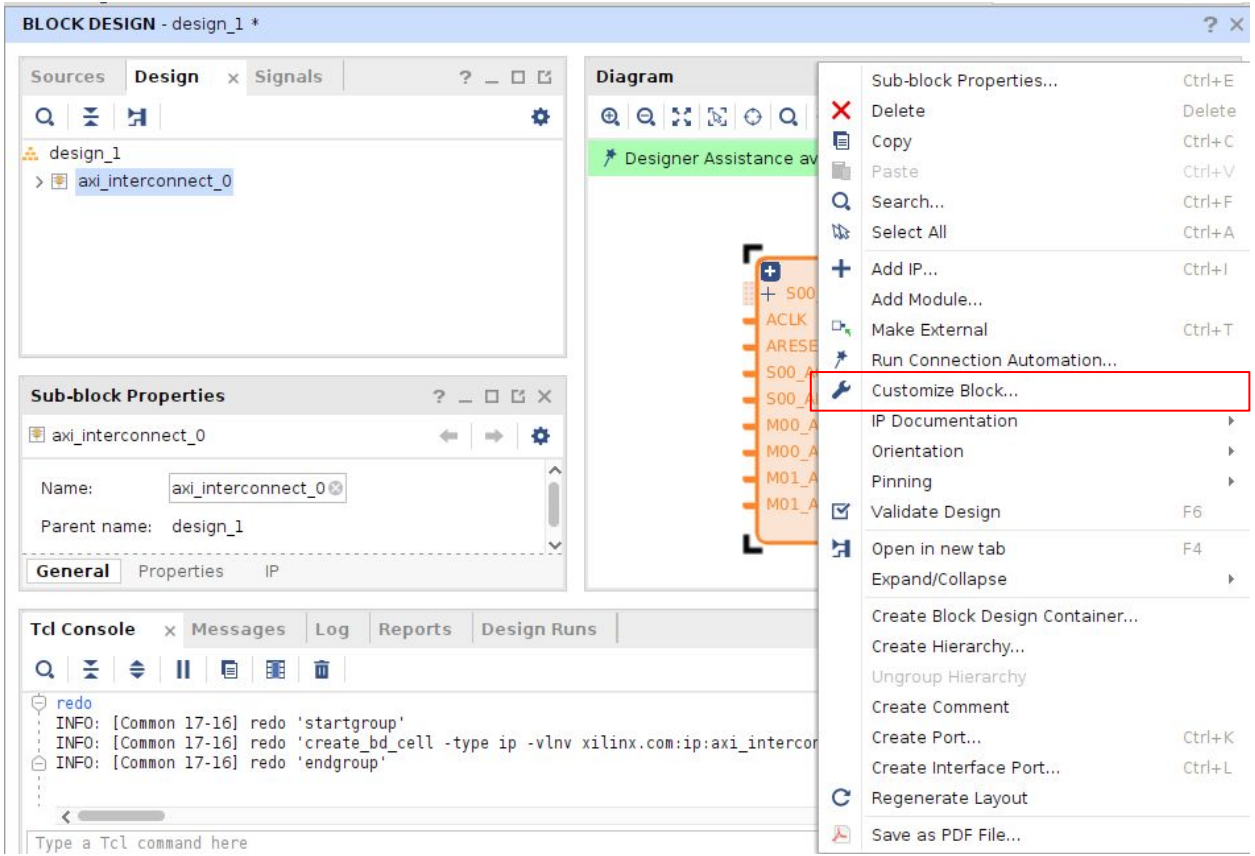
Create AXI Interconnect without TCL - (1)



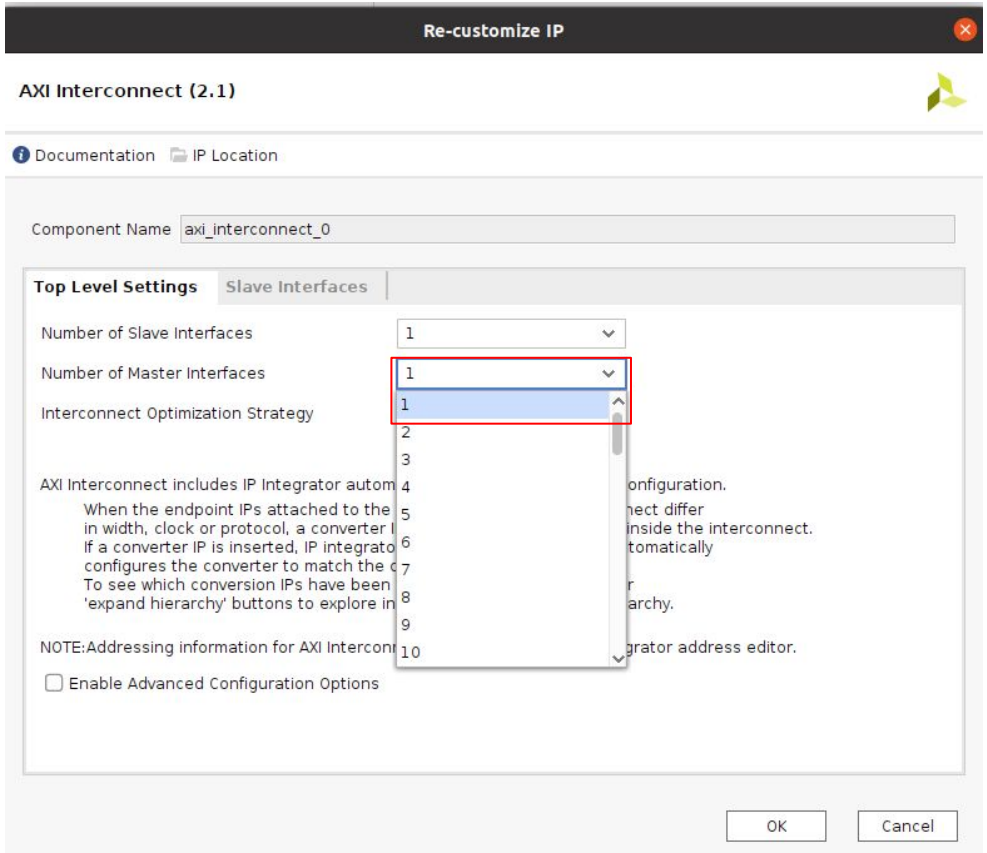
Create AXI Interconnect without TCL - (2)



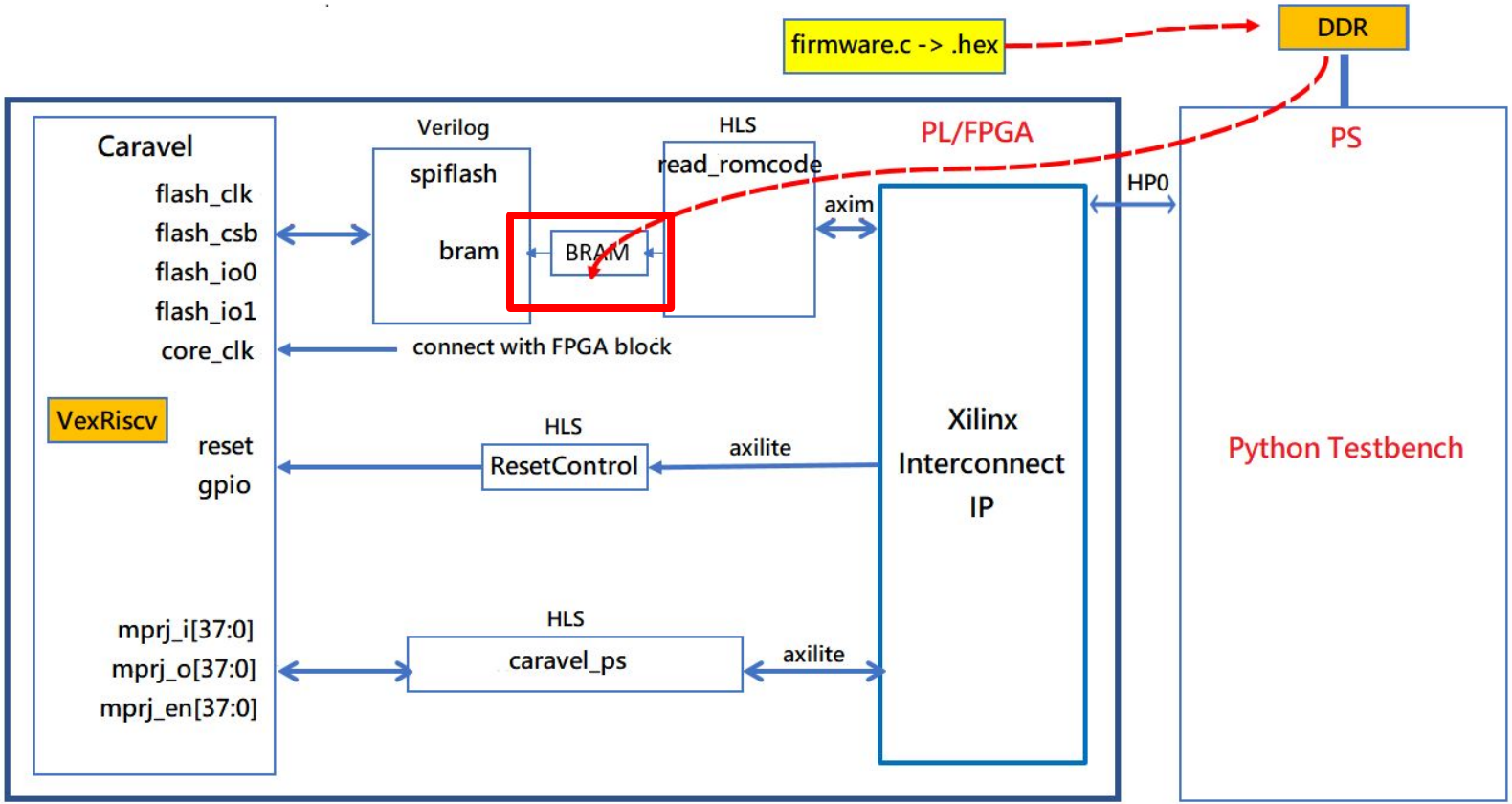
Create AXI Interconnect without TCL - (3)



Create AXI Interconnect without TCL - (4)

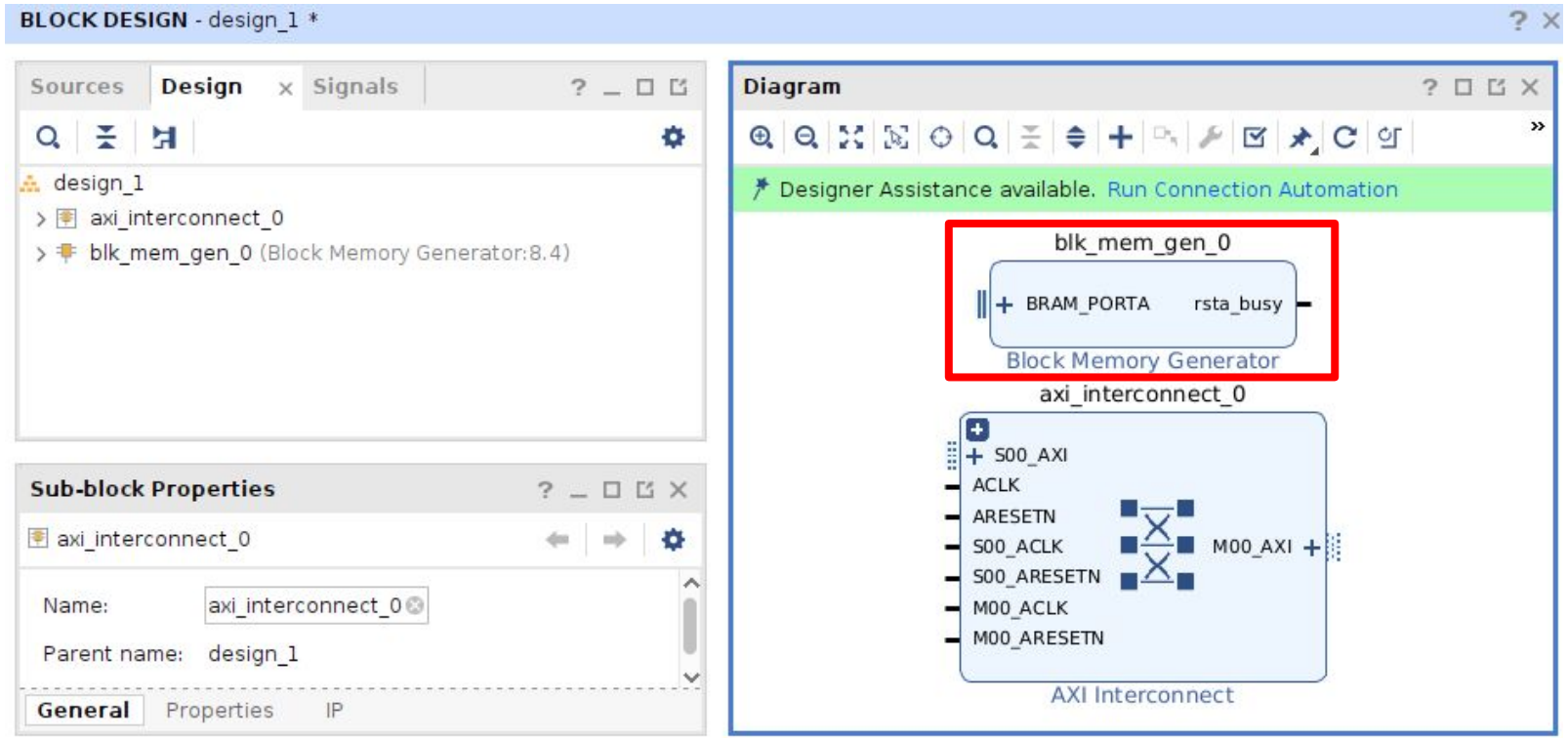


Create BRAM


firmware.c -> .hex
DDR
Caravel
flash_clk
flash_csb
flash_io0
flash_io1
core_clk
VexRiscv
reset
gpio
mprj_i[37:0]
mprj_o[37:0]
mprj_en[37:0]
Verilog
spiflash
bram
BRAM
HLS
read_romcode
connect with FPGA block
PL/FPGA
axim
HP0
PS
HLS
ResetControl
axilite
Xilinx
Interconnect
IP
Python Testbench
HLS
caravel_ps
axilite

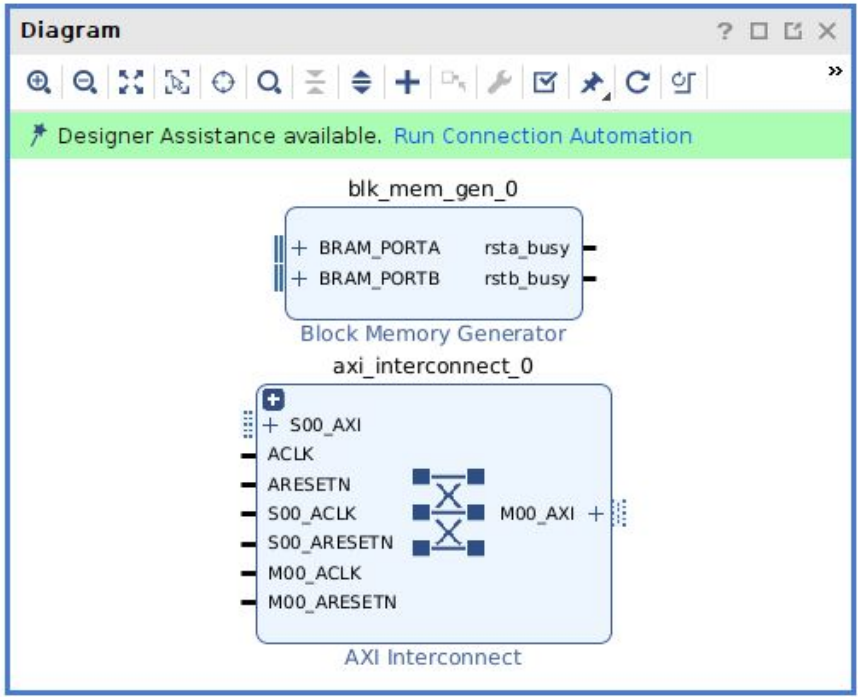
Create BRAM – (1)

```
set blk_mem_gen_0 [ create_bd_cell -type ip -vlnv xilinx.com:ip:blk_mem_gen:8.4 blk_mem_gen_0 ]
```

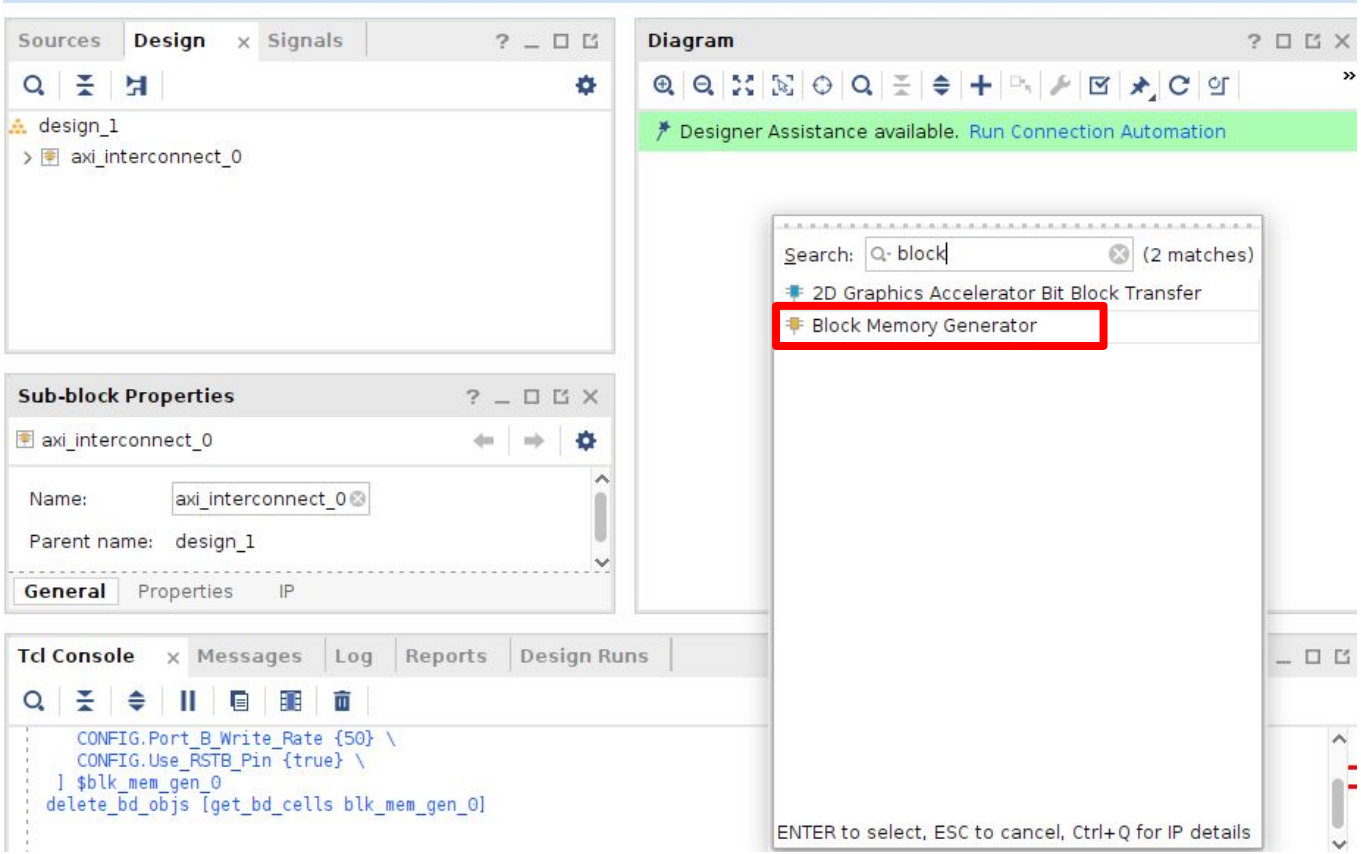


Create BRAM – (2)

```
set_property -dict [ list \
   CONFIG.Enable_B {Use_ENB_Pin} \
   CONFIG.Memory_Type {True_Dual_Port_RAM} \
   CONFIG.Port_B_Clock {100} \
   CONFIG.Port_B_Enable_Rate {100} \
   CONFIG.Port_B_Write_Rate {50} \
   CONFIG.Use_RSTB_Pin {true} \
 ] $blk_mem_gen_0
```



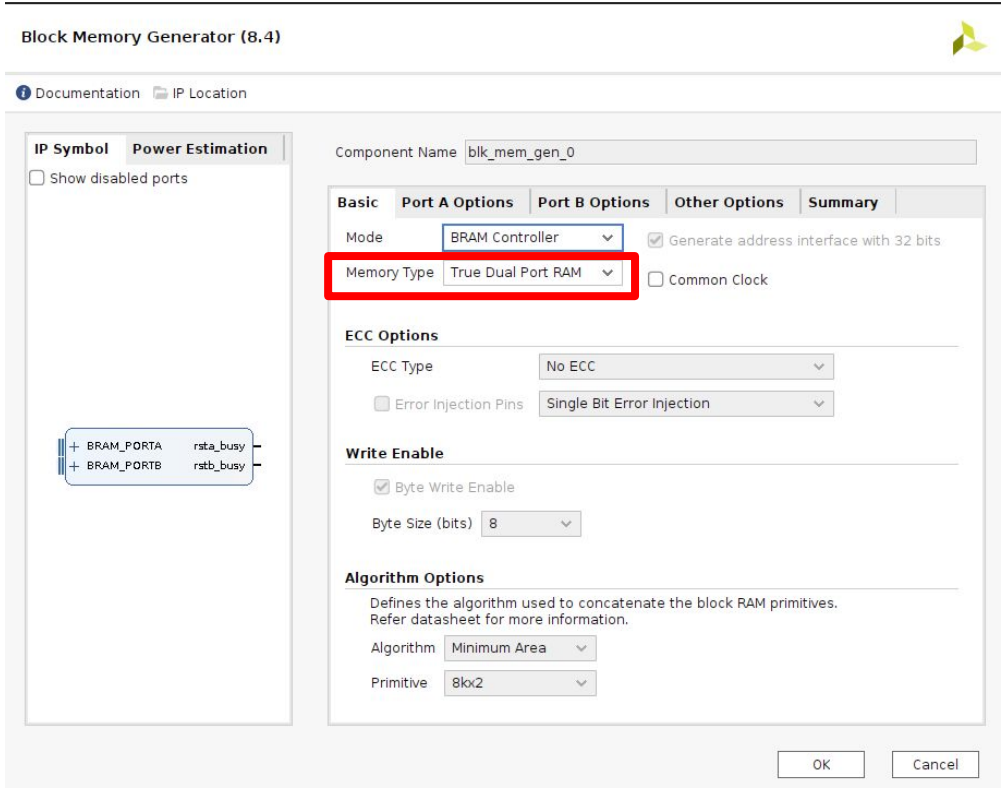
Create BRAM without TCL – (1)



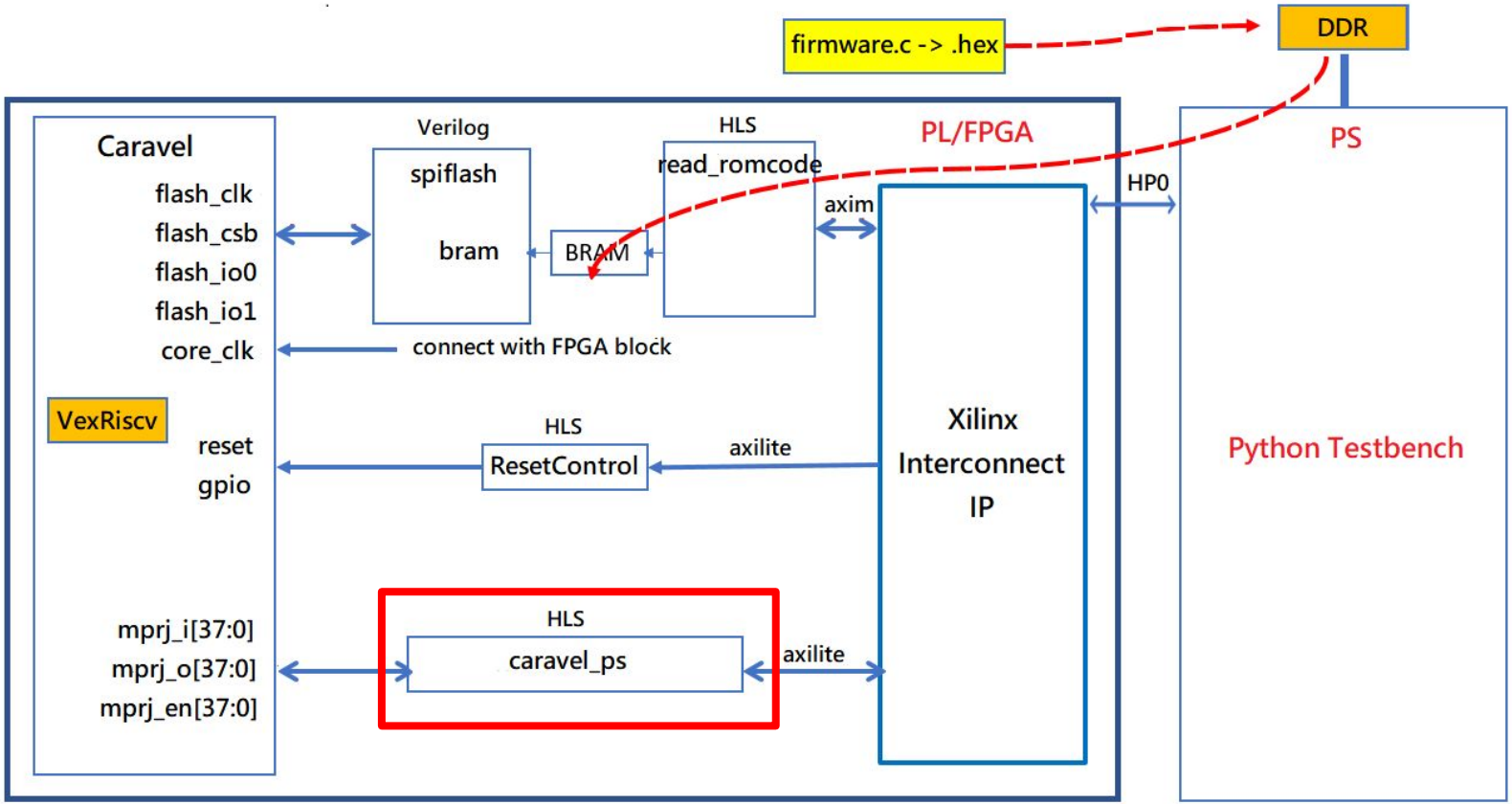
Create BRAM without TCL – (2)

- Customize Block
- Set memory type to dual port RAM
- Other attributes are set by default

```
set_property -dict [ list \
   CONFIG.Enable_B {Use_ENB_Pin} \
   CONFIG.Memory_Type {True_Dual_Port_RAM} \
   CONFIG.Port_B_Clock {100} \
   CONFIG.Port_B_Enable_Rate {100} \
   CONFIG.Port_B_Write_Rate {50} \
   CONFIG.Use_RSTB_Pin {true} \
 ] $blk_mem_gen_0
```

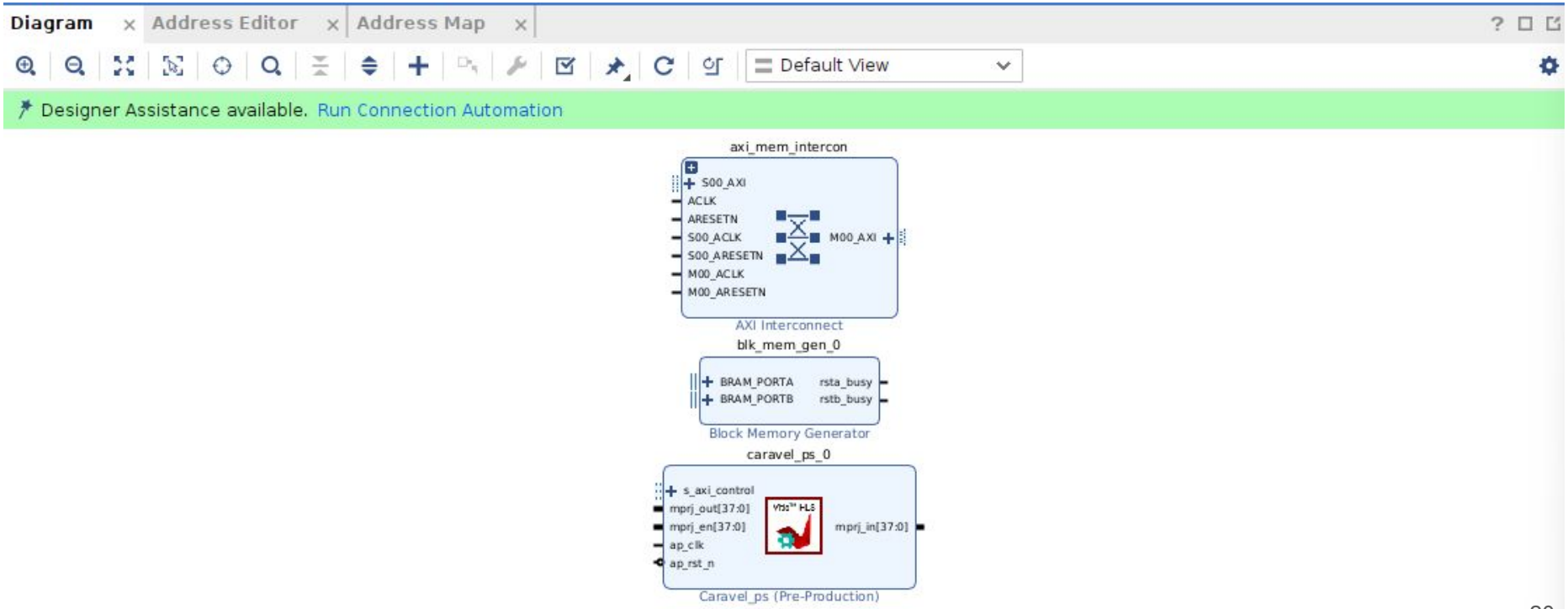


Create Caravel PS



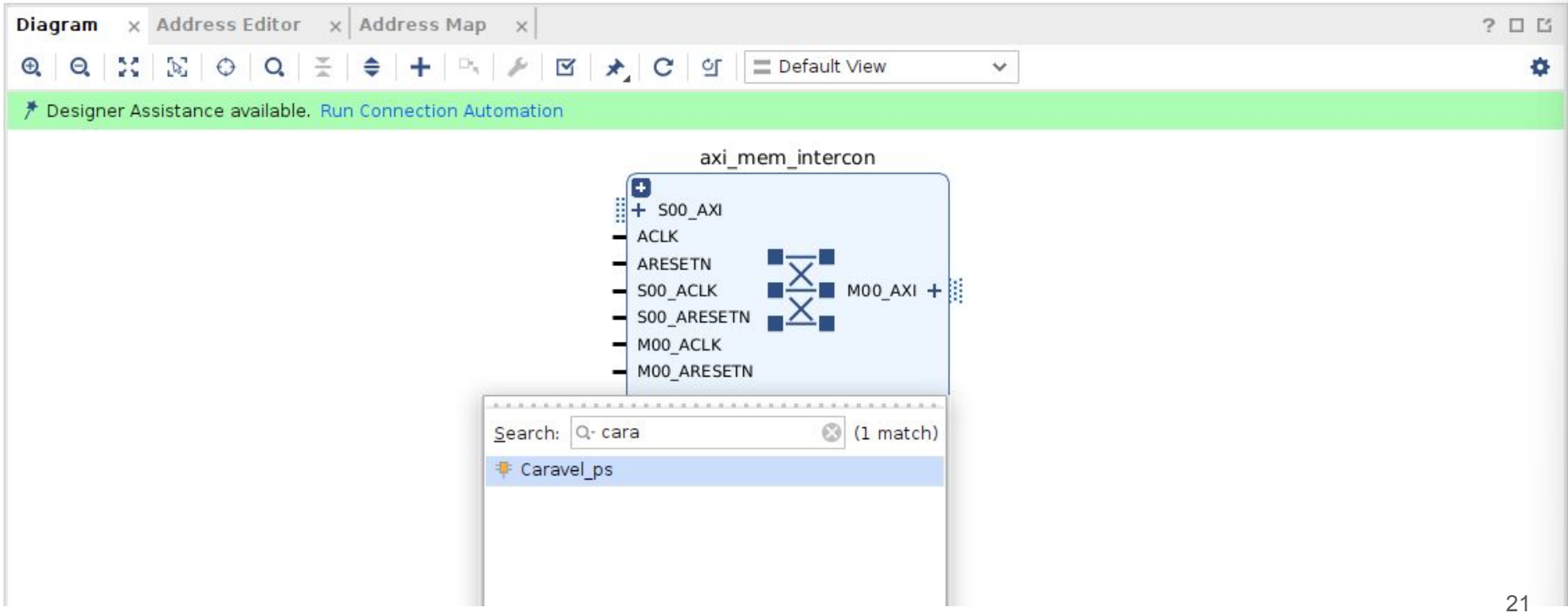
Create Caravel PS

```
set caravel_ps_0 [ create_bd_cell -type ip -vlnv xilinx.com:hls:caravel_ps:0.0 caravel_ps_0 ]
```

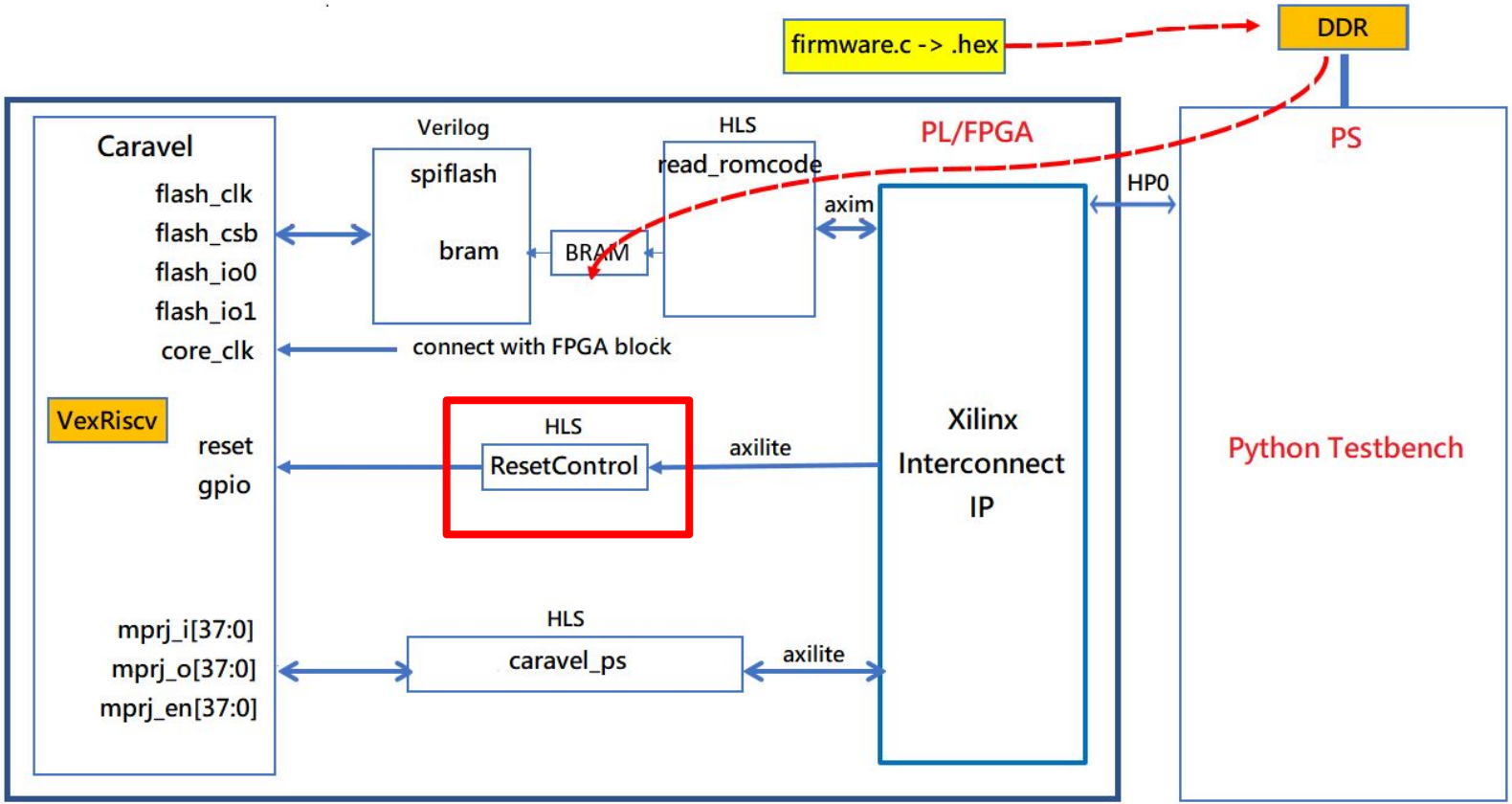


Create Caravel PS without TCL

- Add IP

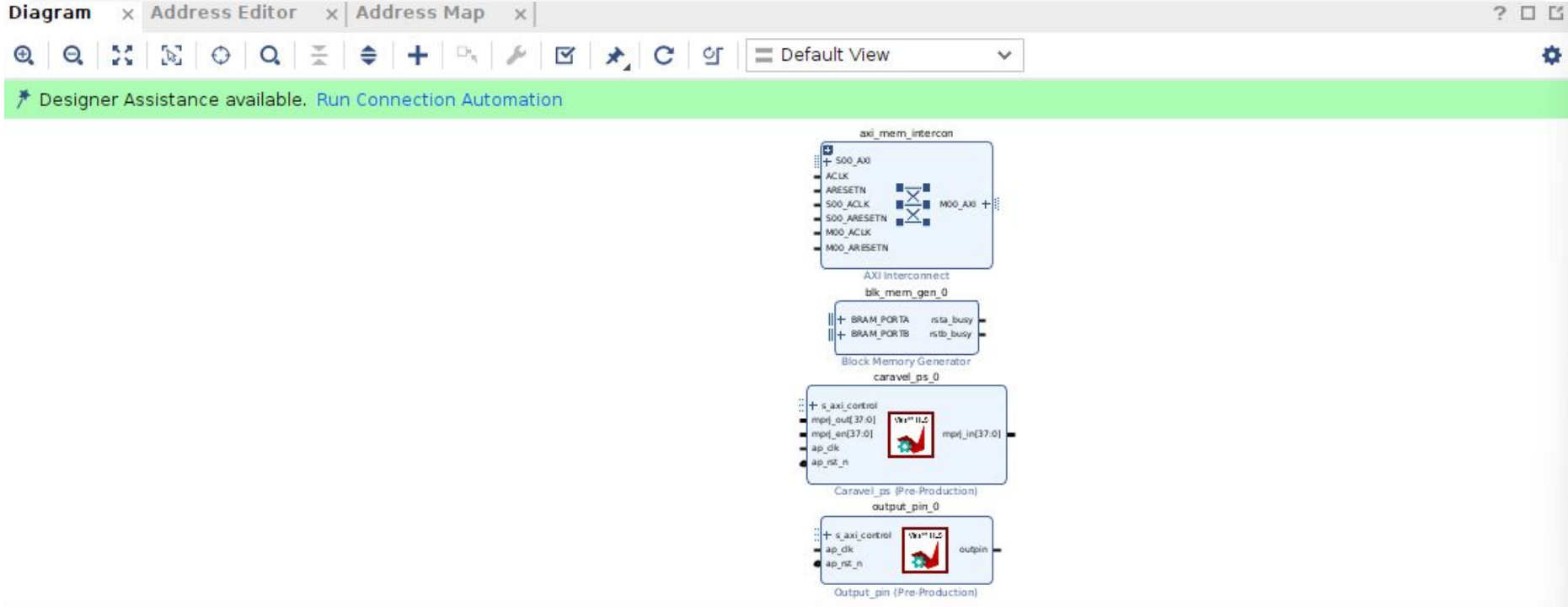


Create Output Pin

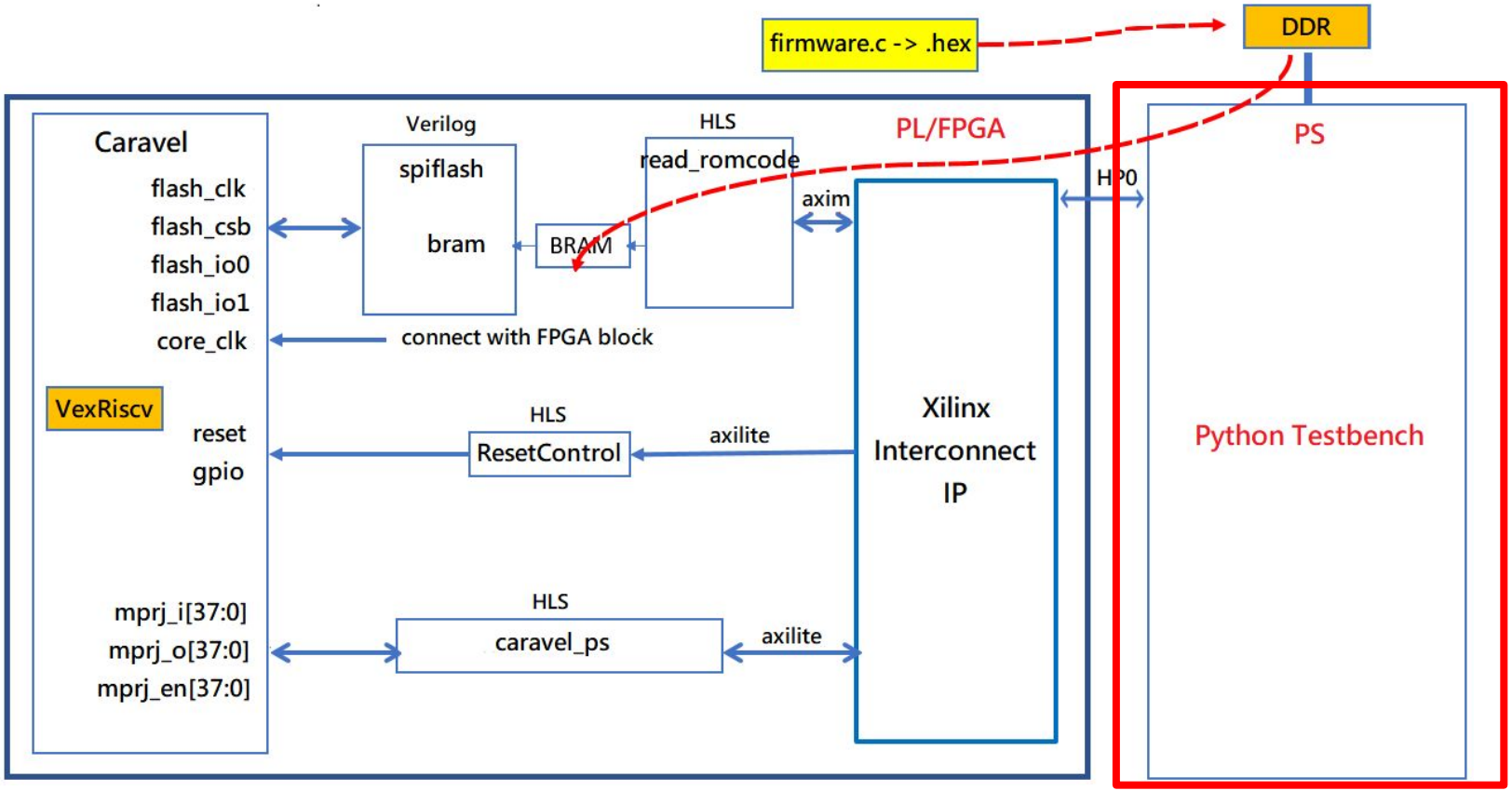


Create Output Pin

```
set output_pin_0 [ create_bd_cell -type ip -vlnv xilinx.com:hls:output_pin:0.0 output_pin_0 ]
```

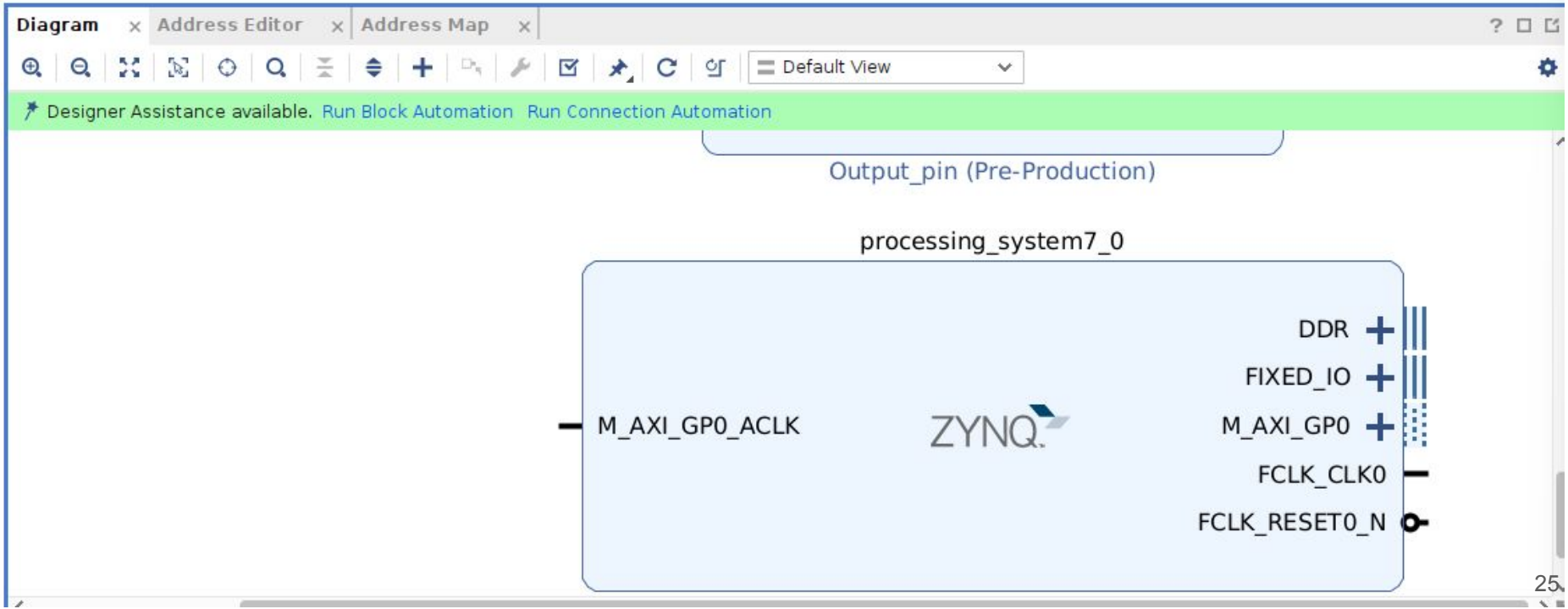


Create PS


firmware.c -> .hex
DDR
Caravel
flash_clk
flash_csb
flash_io0
flash_io1
core_clk
VexRiscv
reset
gpio
mprj_i[37:0]
mprj_o[37:0]
mprj_en[37:0]
Verilog
spiflash
bram
BRAM
HLS
read_romcode
connect with FPGA block
PL/FPGA
axim
HP0
HLS
ResetControl
axilite
Xilinx
Interconnect
IP
HLS
caravel_ps
axilite
PS
Python Testbench

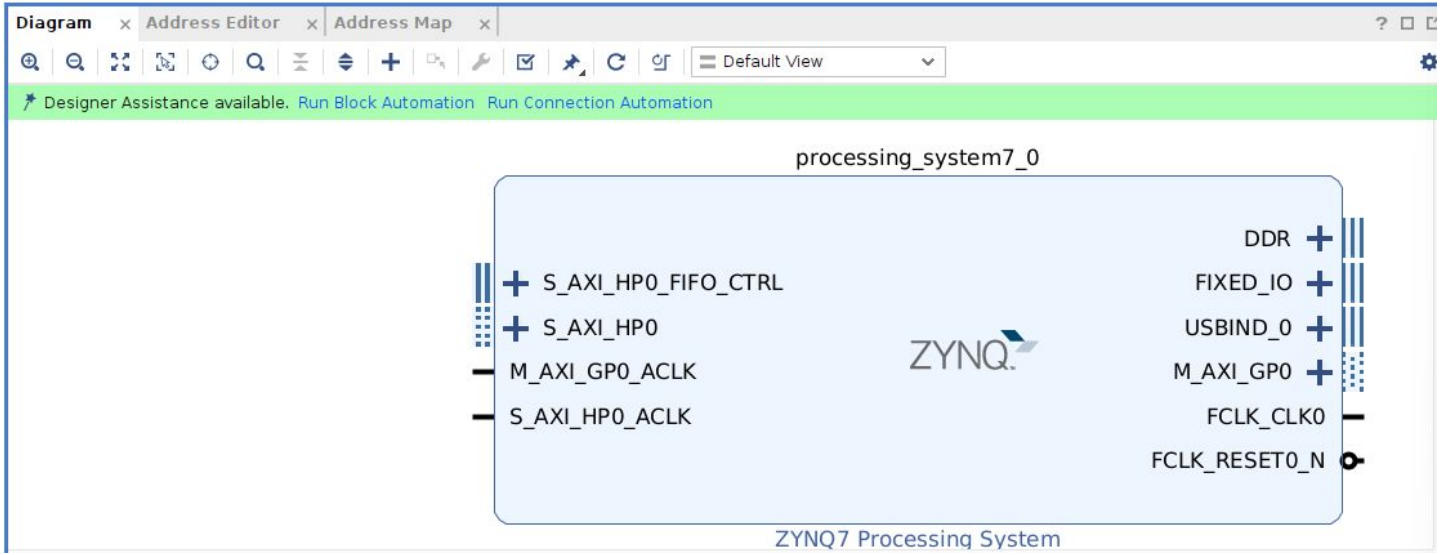
Create PS - (1)

```
set processing_system7_0 [ create_bd_cell -type ip -vlnv xilinx.com:ip:processing_system7:5.5
processing_system7_0 ]
```



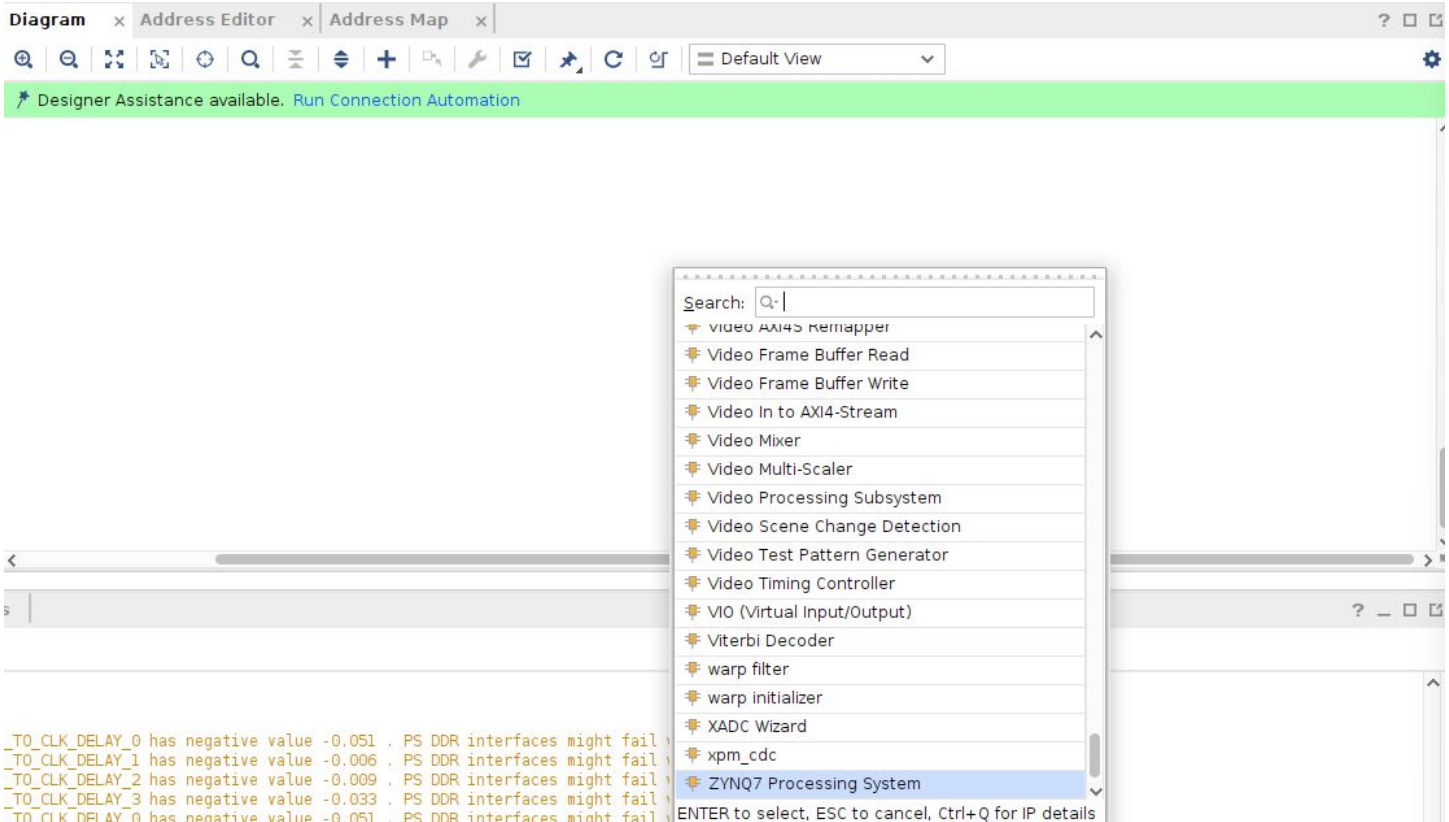
Create PS - (2)

- It has to configure lots of attributes
- Please refer to https://github.com/bol-edu/caravel-soc_fpga-lab/blob/main/lab-exmem_fir/vivado/vvd_caravel_fpga_10mhz.tcl#L408-L1184



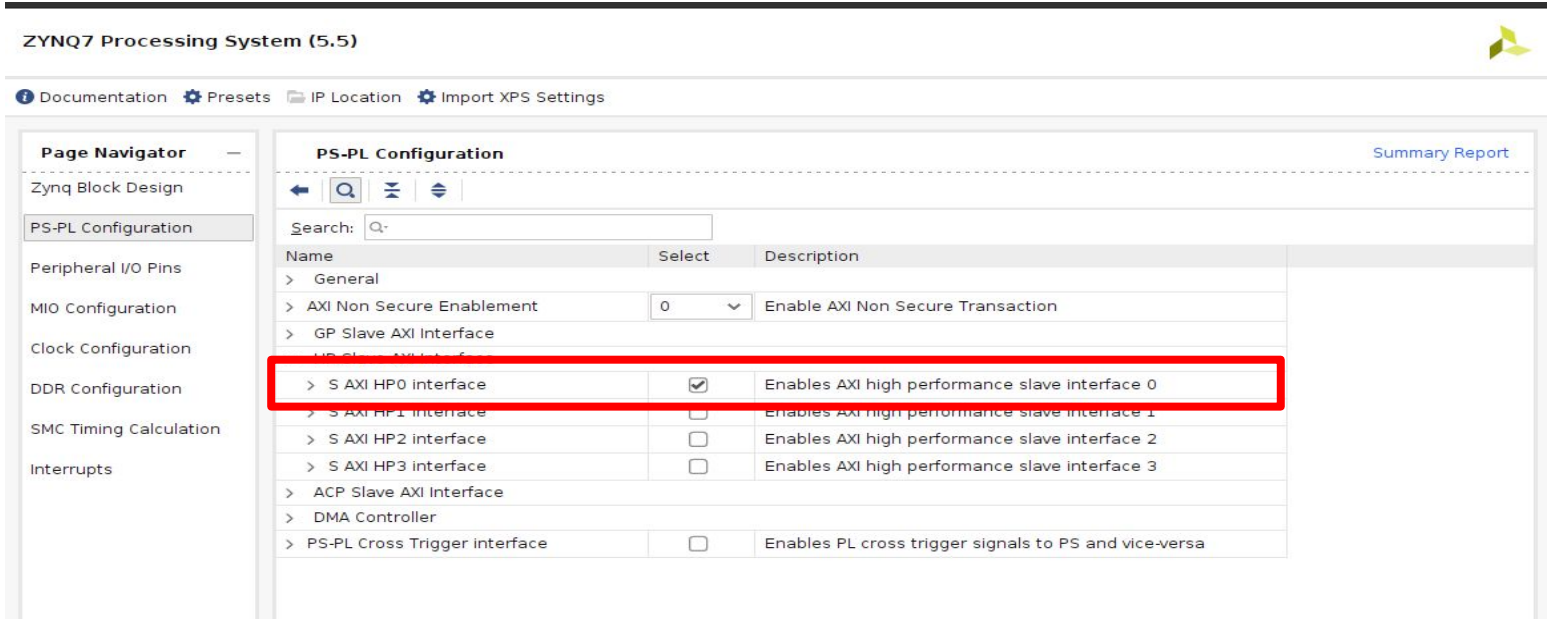
Create PS without TCL - (1)

- Add IP



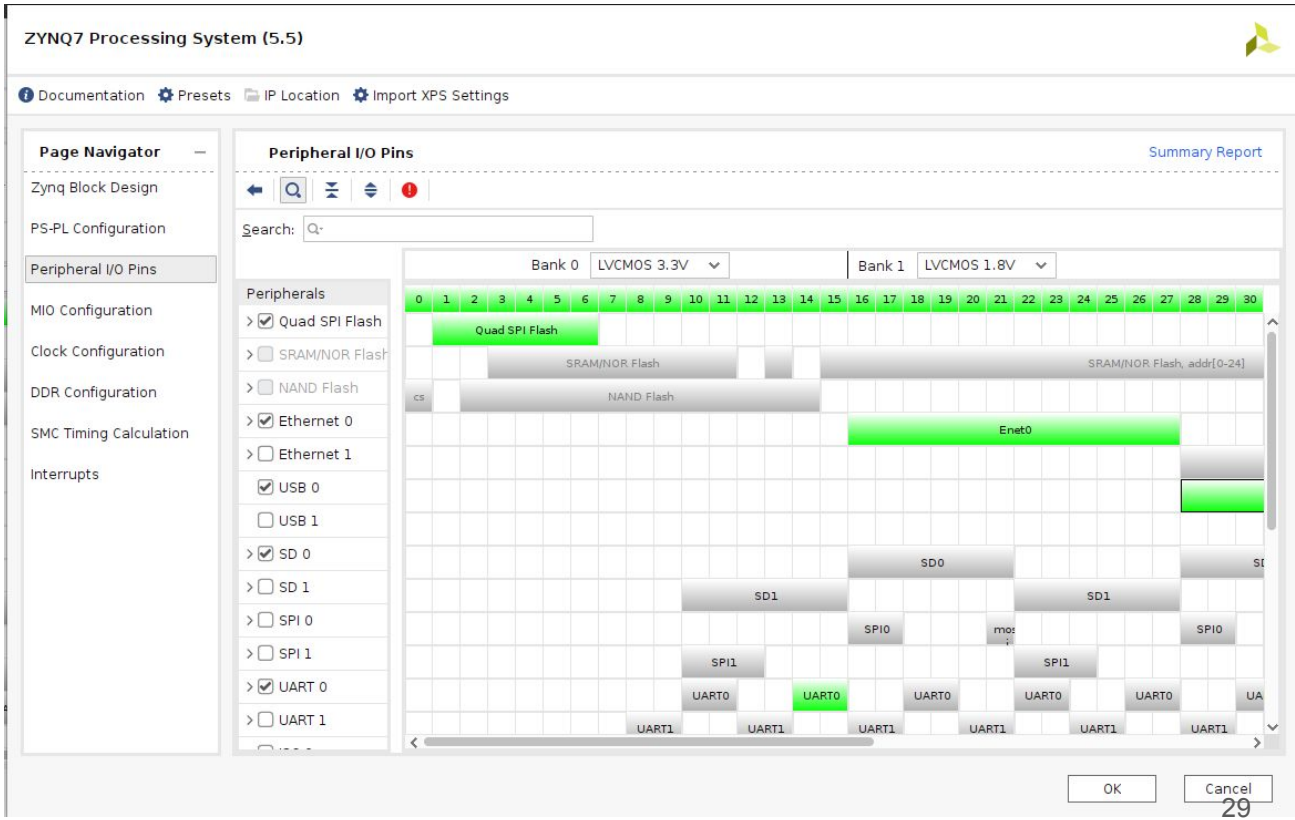
Create PS without TCL - (2)

- One HP port
- Refer to https://github.com/bol-edu/caravel-soc_fpga-lab/blob/main/lab-exmem_fir/vivado/vvd_caravel_fpga_10mhz.tcl#L1174



Create PS without TCL - (3)

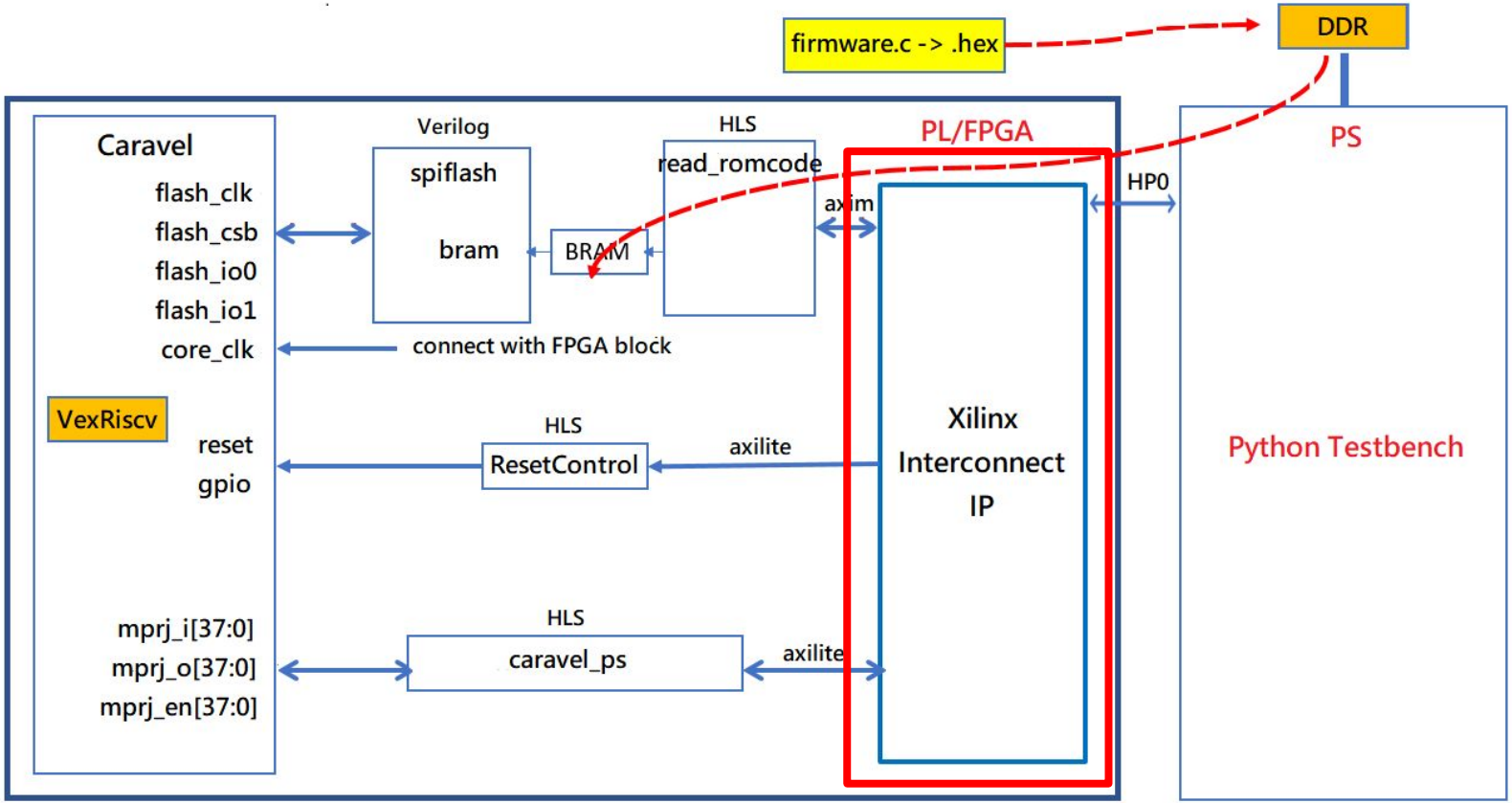
- Set Peripheral IO
- SPI flash
- Ethernet
- USB
- SD
- UART
- GPIO



Create PS without TCL - (4)

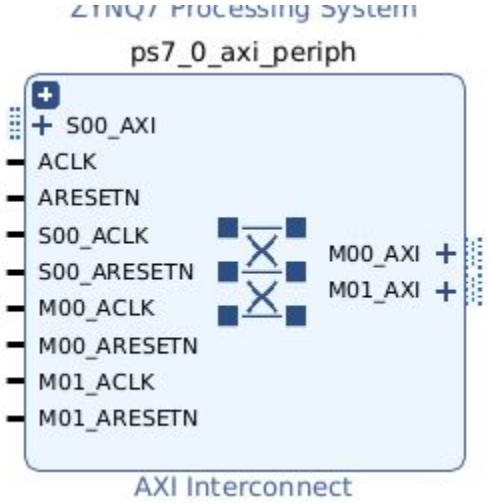
- DDR Configuration
- Memory part
  - https://github.com/bol-edu/caravel-soc_fpga-lab/blob/main/lab-exmem_fir/vivado/vvd_caravel_fpga_10mhz.tcl#L1123
- ~~DQS to Clock Delay~~
  - https://github.com/bol-edu/caravel-soc_fpga-lab/blob/main/lab-exmem_fir/vivado/vvd_caravel_fpga_10mhz.tcl#L1101-L1104
- ~~Board Delay~~
  - https://github.com/bol-edu/caravel-soc_fpga-lab/blob/main/lab-exmem_fir/vivado/vvd_caravel_fpga_10mhz.tcl#L1067-L1070

Create AXI for peripheral



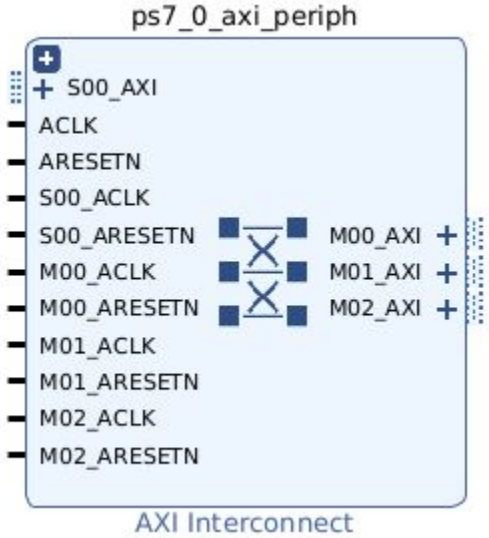
Create AXI for peripheral - (1)

```
set ps7_0_axi_periph [ create_bd_cell -type ip -vlnv xilinx.com:ip:axi_interconnect:2.1
ps7_0_axi_periph ]
```



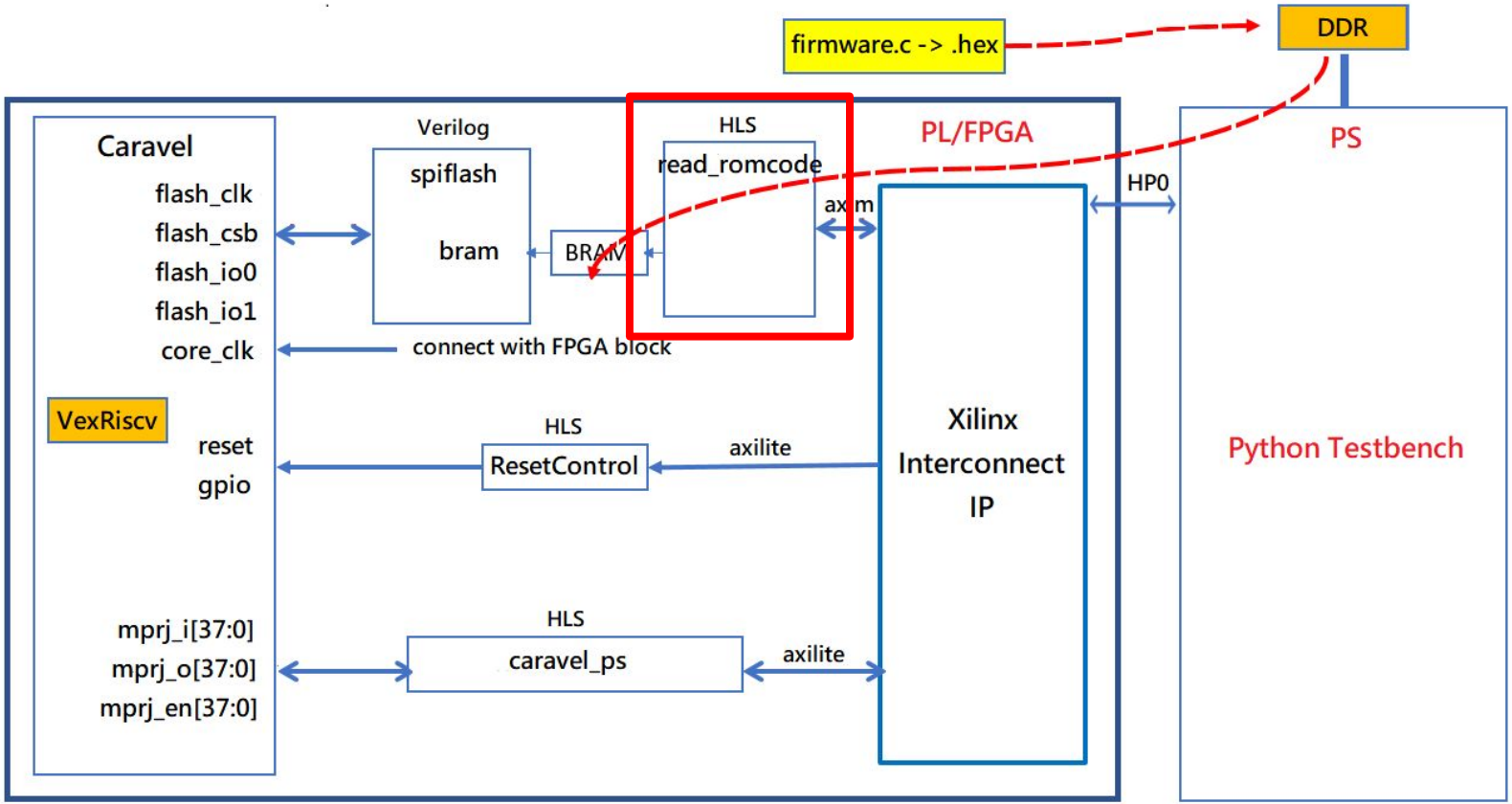
Create AXI for peripheral - (2)

```
set_property -dict [ list CONFIG.NUM_MI {3}] $ps7_0_axi_periph
```



- Without TCL, you can do the same way as page 10~13

Create Read ROM

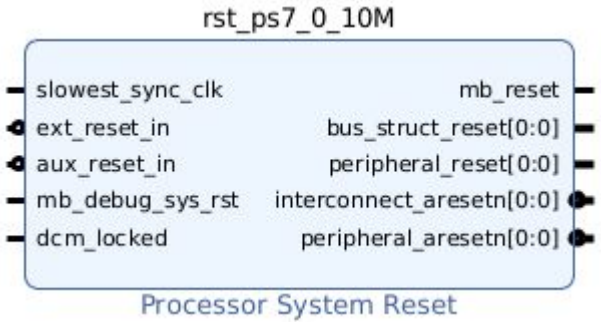


Create Read ROM

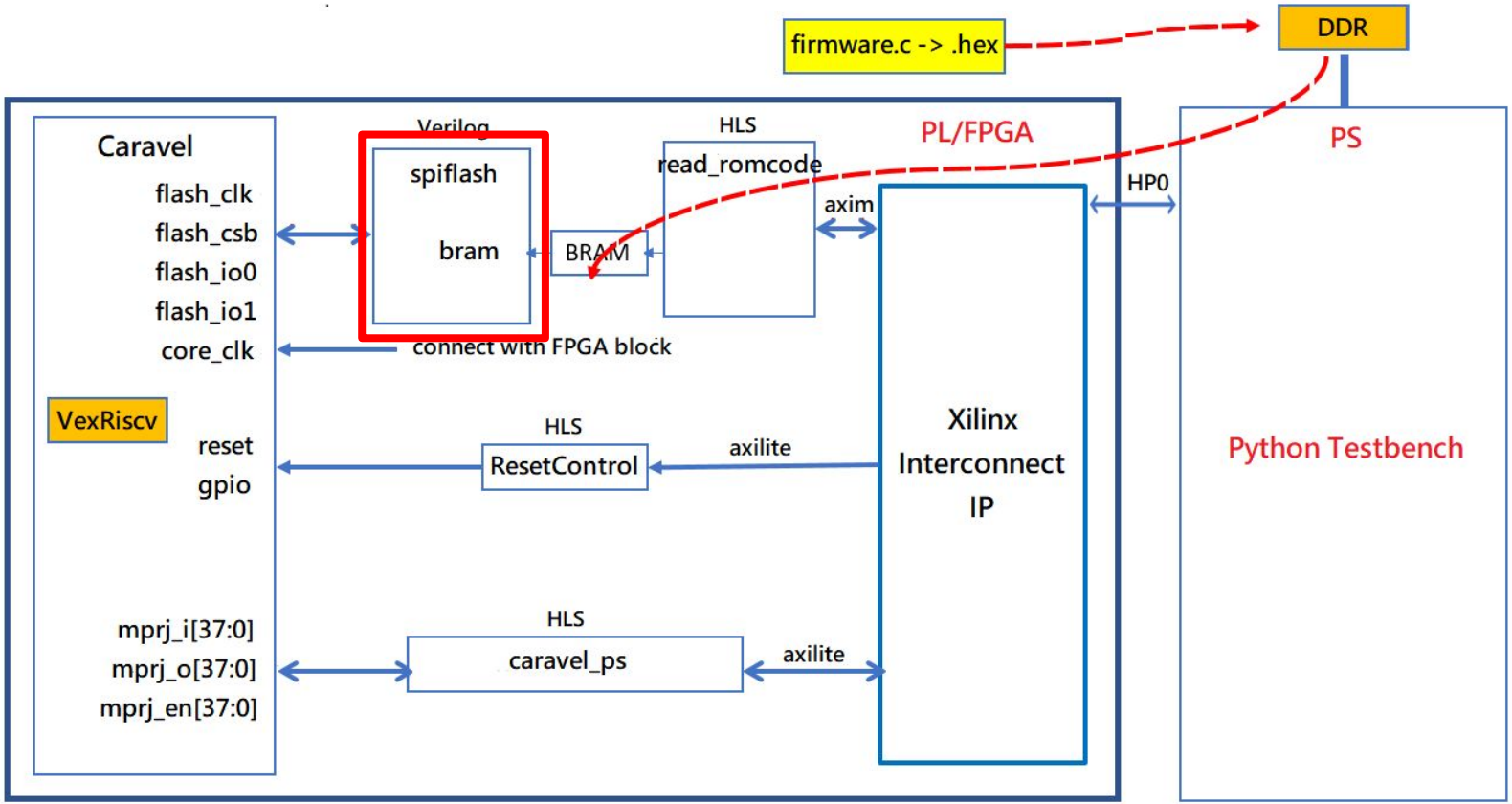
```
set read_romcode_0 [ create_bd_cell -type ip -vlnv
xilinx.com:hls:read_romcode:0.0 read_romcode_0 ]
```

Create Reset

```
set rst_ps7_0_10M [ create_bd_cell -type ip -vlnv xilinx.com:ip:proc_sys_reset:5.0
rst_ps7_0_10M ]
```

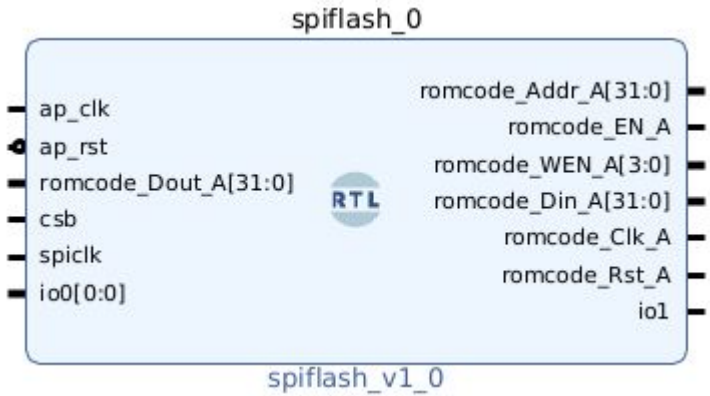


Create SPI Flash

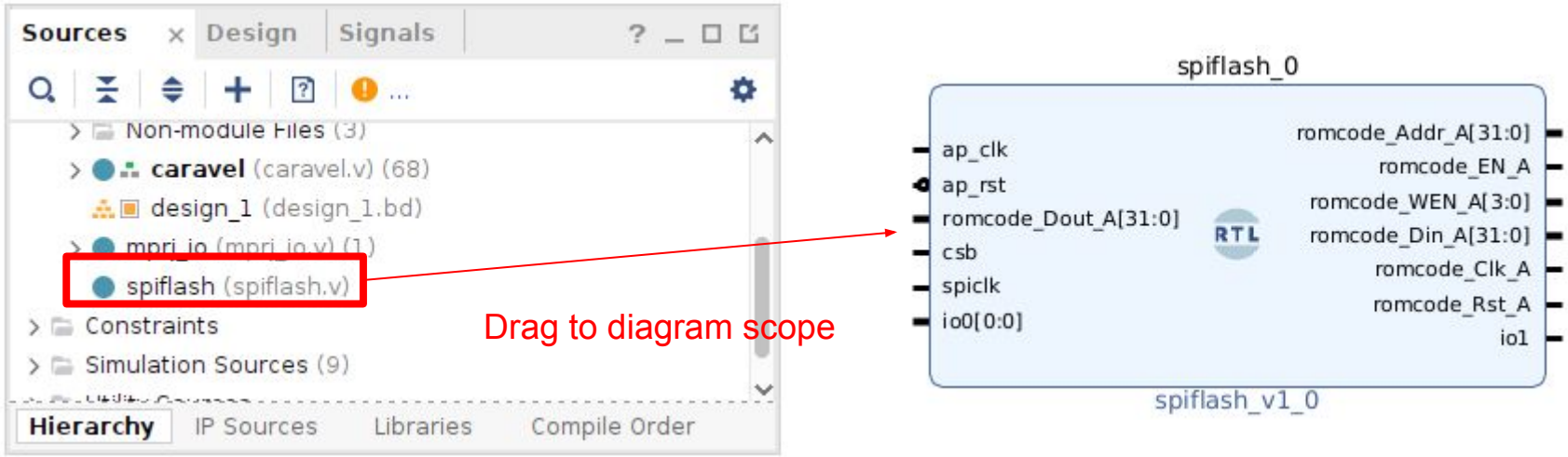


Create SPI Flash

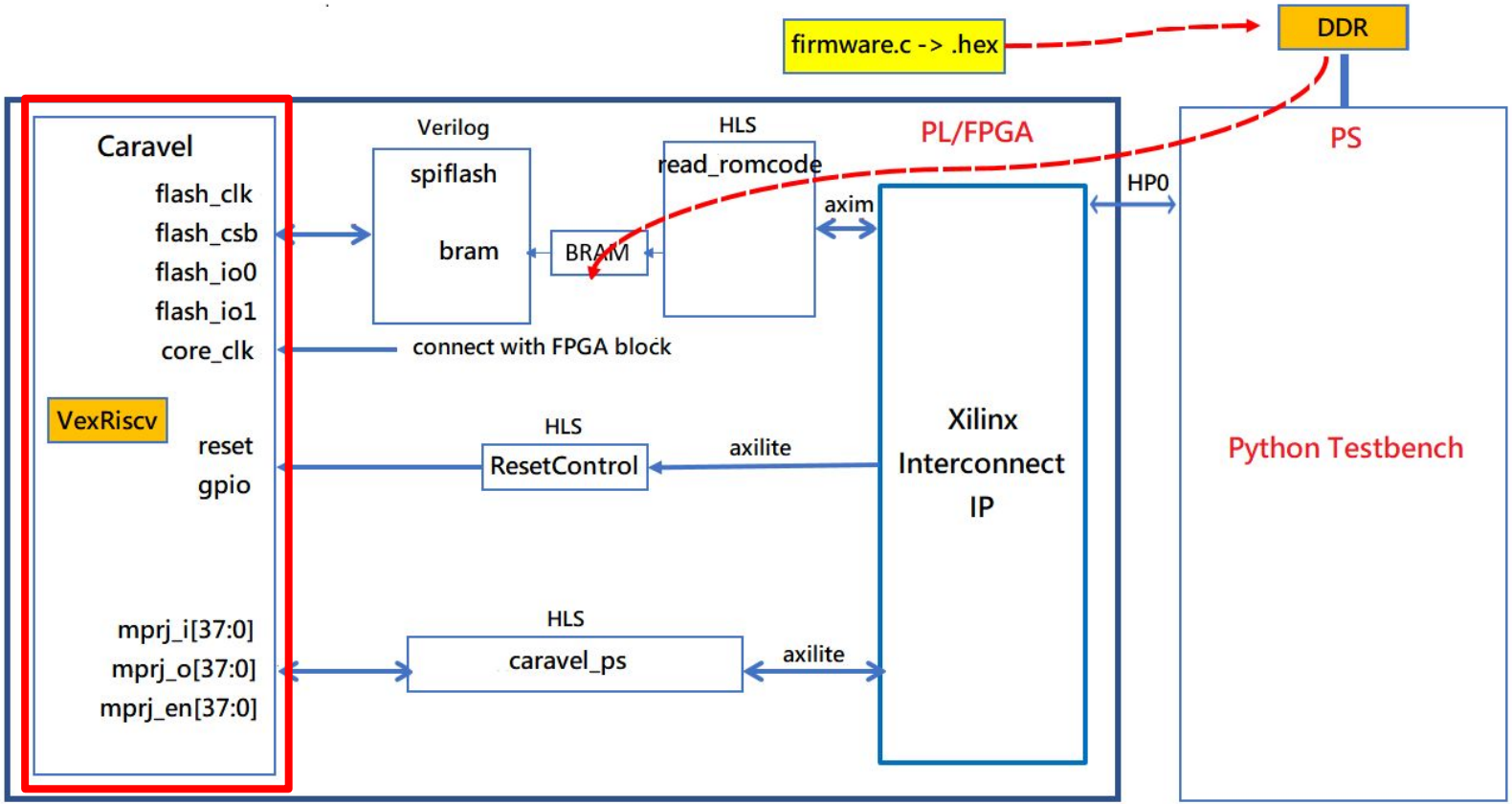
```
set block_name spiflash
set block_cell_name spiflash_0
set spiflash_0 [create_bd_cell -type module -reference $block_name $block_cell_name]
```



Create SPI Flash without TCL

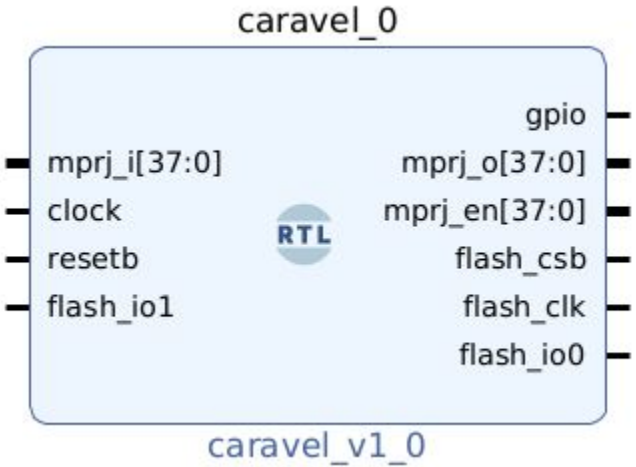


Create Caravel



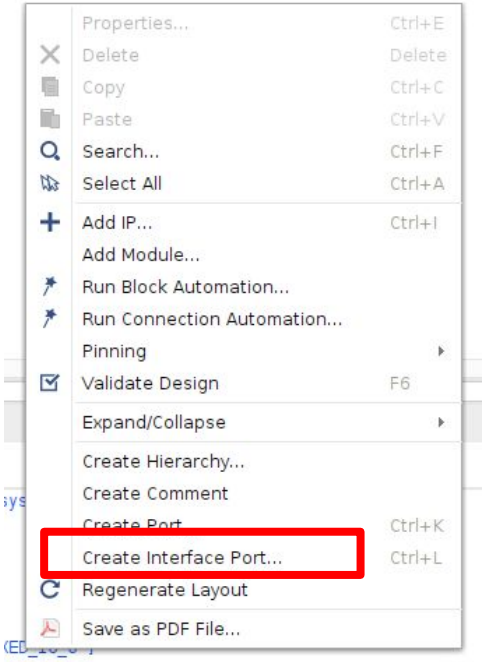
Create Caravel

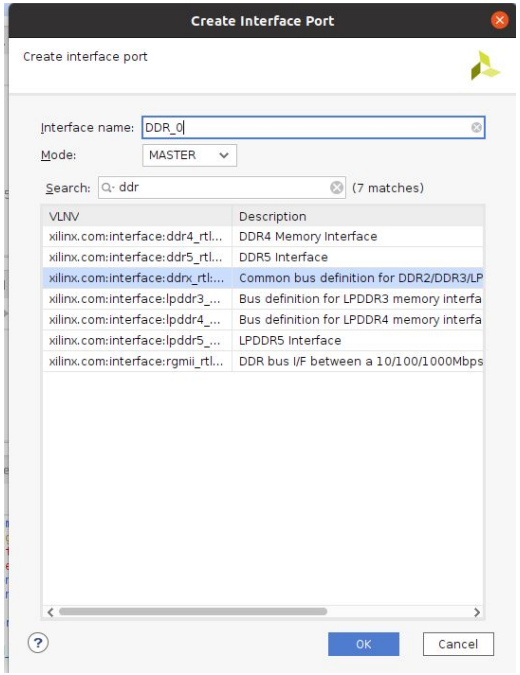
```
set block_name caravel
set block_cell_name caravel_0
set caravel_0 [create_bd_cell -type module -reference $block_name $block_cell_name]
```



Create DDR Port and IO Port for PS

```
set DDR_0 [ create_bd_intf_port -mode Master -vlnv xilinx.com:interface:ddrx_rtl:1.0 DDR_0 ]
set FIXED_IO_0 [ create_bd_intf_port -mode Master -vlnv
xilinx.com:display_processing_system7:fixedio_rtl:1.0 FIXED_IO_0 ]
```

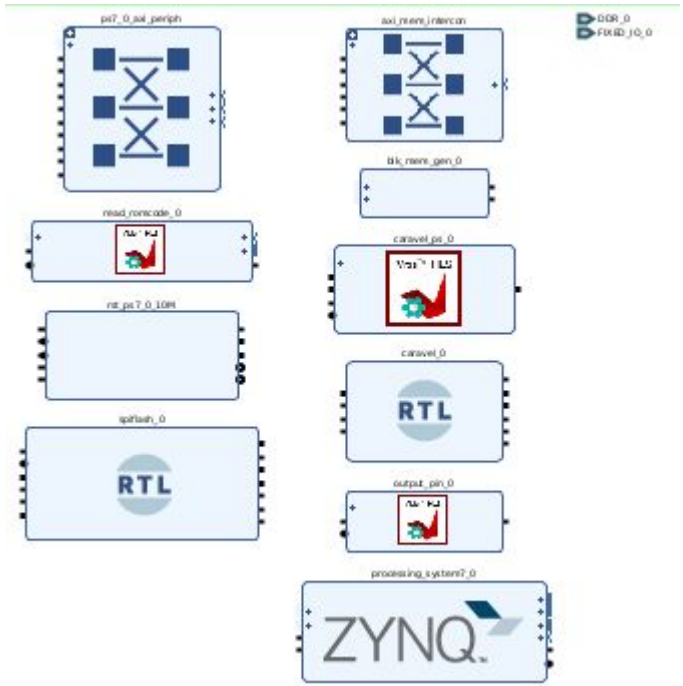


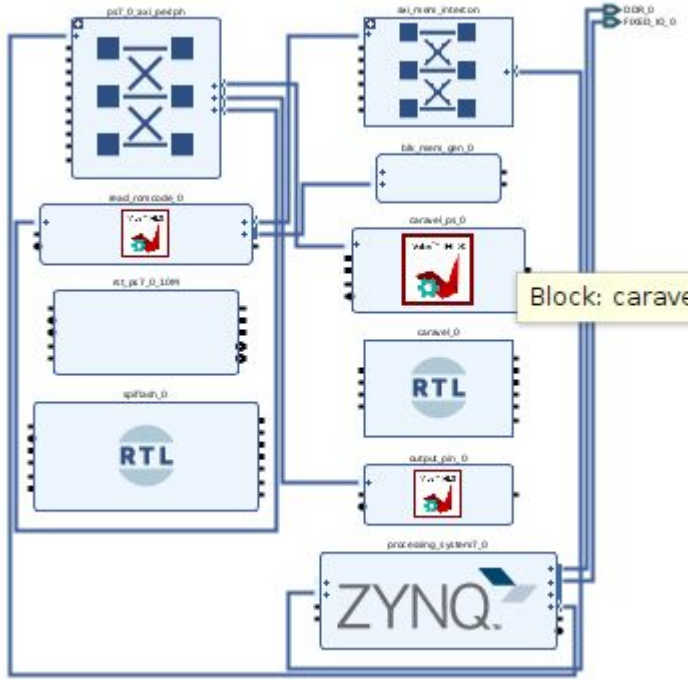


Create Interface Connection

```
connect_bd_intf_net -intf_net axi_mem_intercon_M00_AXI [get_bd_intf_pins axi_mem_intercon/M00_AXI] [get_bd_intf_pins processing_system7_0/S_AXI_HP0]
connect_bd_intf_net -intf_net processing_system7_0_DDR [get_bd_intf_ports DDR_0] [get_bd_intf_pins processing_system7_0/DDR]
connect_bd_intf_net -intf_net processing_system7_0_FIXED_IO [get_bd_intf_ports FIXED_IO_0] [get_bd_intf_pins processing_system7_0/FIXED_IO]
connect_bd_intf_net -intf_net processing_system7_0_M_AXI_GP0 [get_bd_intf_pins processing_system7_0/M_AXI_GP0] [get_bd_intf_pins ps7_0_axi_periph/S00_AXI]
connect_bd_intf_net -intf_net ps7_0_axi_periph_M00_AXI [get_bd_intf_pins caravel_ps_0/s_axi_control] [get_bd_intf_pins ps7_0_axi_periph/M00_AXI]
connect_bd_intf_net -intf_net ps7_0_axi_periph_M01_AXI [get_bd_intf_pins output_pin_0/s_axi_control] [get_bd_intf_pins ps7_0_axi_periph/M01_AXI]
connect_bd_intf_net -intf_net ps7_0_axi_periph_M02_AXI [get_bd_intf_pins ps7_0_axi_periph/M02_AXI] [get_bd_intf_pins read_romcode_0/s_axi_control]
connect_bd_intf_net -intf_net read_romcode_0_internal_bram_PORTA [get_bd_intf_pins blk_mem_gen_0/BRAM_PORTB] [get_bd_intf_pins read_romcode_0/internal_bram_PORTA]
connect_bd_intf_net -intf_net read_romcode_0_m_axi_BUS0 [get_bd_intf_pins axi_mem_intercon/S00_AXI] [get_bd_intf_pins read_romcode_0/m_axi_BUS0]
```

Create Interface Connection

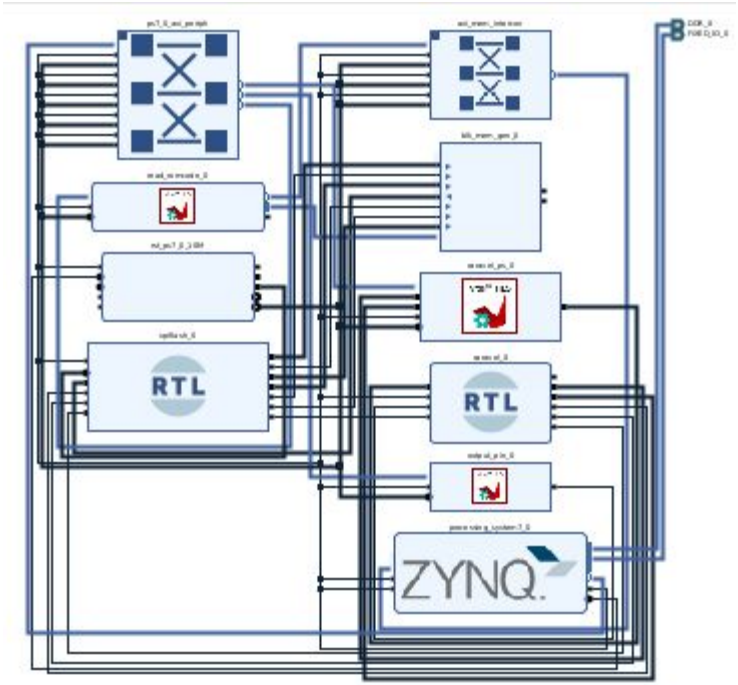




Create Port Connection

```
connect_bd_net -net blk_mem_gen_0_douta [get_bd_pins blk_mem_gen_0/douta] [get_bd_pins spiflash_0/romcode_Dout_A]
connect_bd_net -net caravel_0_flash_clk [get_bd_pins caravel_0/flash_clk] [get_bd_pins spiflash_0/spiclk]
connect_bd_net -net caravel_0_flash_csb [get_bd_pins caravel_0/flash_csb] [get_bd_pins spiflash_0/csb]
connect_bd_net -net caravel_0_flash_io0 [get_bd_pins caravel_0/flash_io0] [get_bd_pins spiflash_0/io0]
connect_bd_net -net caravel_0_mprj_en [get_bd_pins caravel_0/mprj_en] [get_bd_pins caravel_ps_0/mprj_en]
connect_bd_net -net caravel_0_mprj_o [get_bd_pins caravel_0/mprj_o] [get_bd_pins caravel_ps_0/mprj_out]
connect_bd_net -net caravel_ps_0_mprj_in [get_bd_pins caravel_0/mprj_i] [get_bd_pins caravel_ps_0/mprj_in]
connect_bd_net -net output_pin_0_outpin [get_bd_pins caravel_0/resetb] [get_bd_pins output_pin_0/outpin]
connect_bd_net -net processing_system7_0_FCLK_CLK1 [get_bd_pins axi_mem_intercon/ACLK] [get_bd_pins axi_mem_intercon/M00_ACLK] [get_bd_pins
axi_mem_intercon/S00_ACLK] [get_bd_pins caravel_0/clock] [get_bd_pins caravel_ps_0/ap_clk] [get_bd_pins output_pin_0/ap_clk] [get_bd_pins
processing_system7_0/FCLK_CLK0] [get_bd_pins processing_system7_0/M_AXI_GP0_ACLK] [get_bd_pins processing_system7_0/S_AXI_HP0_ACLK]
[get_bd_pins ps7_0_axi_periph/ACLK] [get_bd_pins ps7_0_axi_periph/M00_ACLK] [get_bd_pins ps7_0_axi_periph/M01_ACLK] [get_bd_pins
ps7_0_axi_periph/M02_ACLK] [get_bd_pins ps7_0_axi_periph/S00_ACLK] [get_bd_pins read_romcode_0/ap_clk] [get_bd_pins
rst_ps7_0_10M/slowest_sync_clk] [get_bd_pins spiflash_0/ap_clk]
connect_bd_net -net processing_system7_0_FCLK_RESET0_N [get_bd_pins processing_system7_0/FCLK_RESET0_N] [get_bd_pins
rst_ps7_0_10M/ext_reset_in]
connect_bd_net -net rst_ps7_0_100M_peripheral_aresetn [get_bd_pins axi_mem_intercon/ARESETN] [get_bd_pins axi_mem_intercon/M00_ARESETN]
[get_bd_pins axi_mem_intercon/S00_ARESETN] [get_bd_pins caravel_ps_0/ap_rst_n] [get_bd_pins output_pin_0/ap_rst_n] [get_bd_pins
ps7_0_axi_periph/ARESETN] [get_bd_pins ps7_0_axi_periph/M00_ARESETN] [get_bd_pins ps7_0_axi_periph/M01_ARESETN] [get_bd_pins
ps7_0_axi_periph/M02_ARESETN] [get_bd_pins ps7_0_axi_periph/S00_ARESETN] [get_bd_pins read_romcode_0/ap_rst_n] [get_bd_pins
rst_ps7_0_10M/peripheral_aresetn]
connect_bd_net -net rst_ps7_0_50M_peripheral_reset [get_bd_pins rst_ps7_0_10M/peripheral_reset] [get_bd_pins spiflash_0/ap_rst]
connect_bd_net -net spiflash_0_io1 [get_bd_pins caravel_0/flash_io1] [get_bd_pins spiflash_0/io1]
connect_bd_net -net spiflash_0_romcode_Addr_A [get_bd_pins blk_mem_gen_0/addra] [get_bd_pins spiflash_0/romcode_Addr_A]
connect_bd_net -net spiflash_0_romcode_Clk_A [get_bd_pins blk_mem_gen_0/clka] [get_bd_pins spiflash_0/romcode_Clk_A]
connect_bd_net -net spiflash_0_romcode_Din_A [get_bd_pins blk_mem_gen_0/dina] [get_bd_pins spiflash_0/romcode_Din_A]
connect_bd_net -net spiflash_0_romcode_EN_A [get_bd_pins blk_mem_gen_0/ena] [get_bd_pins spiflash_0/romcode_EN_A]
connect_bd_net -net spiflash_0_romcode_Rst_A [get_bd_pins blk_mem_gen_0/rsta] [get_bd_pins spiflash_0/romcode_Rst_A]
connect_bd_net -net spiflash_0_romcode_WEN_A [get_bd_pins blk_mem_gen_0/wea] [get_bd_pins spiflash_0/romcode_WEN_A]
```

Create Port Connection

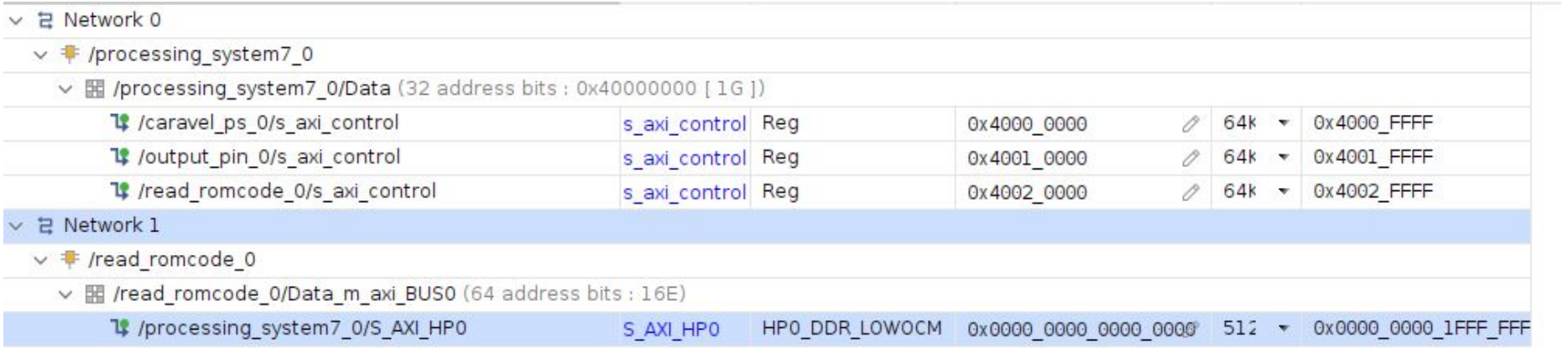


Create Address Segments

```
 1 assign_bd_address -offset 0x40000000 -range 0x00010000 -target_address_space
[get_bd_addr_spaces processing_system7_0/Data] [get_bd_addr_segs
caravel_ps_0/s_axi_control/Reg] -force
 2 assign_bd_address -offset 0x40010000 -range 0x00010000 -target_address_space
[get_bd_addr_spaces processing_system7_0/Data] [get_bd_addr_segs
output_pin_0/s_axi_control/Reg] -force
 3 assign_bd_address -offset 0x40020000 -range 0x00010000 -target_address_space
[get_bd_addr_spaces processing_system7_0/Data] [get_bd_addr_segs
read_romcode_0/s_axi_control/Reg] -force
 4 assign_bd_address -offset 0x00000000 -range 0x20000000 -target_address_space
[get_bd_addr_spaces read_romcode_0/Data_m_axi_BUS0] [get_bd_addr_segs
processing_system7_0/S_AXI_HP0/HP0_DDR_LOWOCM] -force
```

Create Address Segments

- Open address editor



Validate and Save Block Design

```
validate_bd_design
save_bd_design
close_bd_design $design_name
```

Make Wrapper

```
set_property REGISTERED_WITH_MANAGER "1" [get_files design_1.bd ]
set_property SYNTH_CHECKPOINT_MODE "Hierarchical" [get_files design_1.bd ]

#call make_wrapper to create wrapper files
if { [get_property IS_LOCKED [ get_files -norecurse design_1.bd] ] == 1  } {
  import_files -fileset sources_1 [file normalize
"${origin_dir}/vvd_caravel_fpga/vvd_caravel_fpga.gen/sources_1/bd/design_1/hdl/design_1_wrapper.v" ]
} else {
  set wrapper_path [make_wrapper -fileset sources_1 -files [ get_files -norecurse design_1.bd] -top]
  add_files -norecurse -fileset sources_1 $wrapper_path
}
```