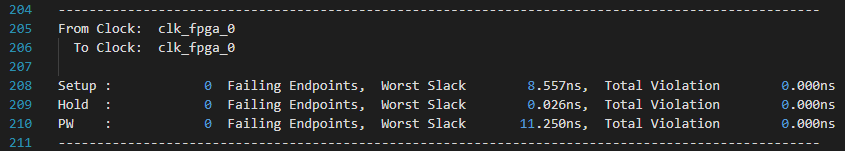
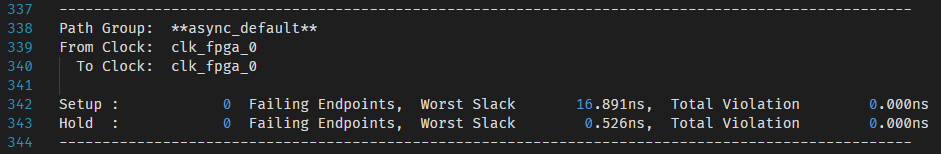
**SOC Lab6 report 第六組**

How do you verify your answer from notebook

Block design

Timing report/ resource report after synthesis





合成後的delay確實都有MET（slack > 0）

Latency for a character loop back using UART

Suggestion for improving latency for UART loop back

What else do you observe