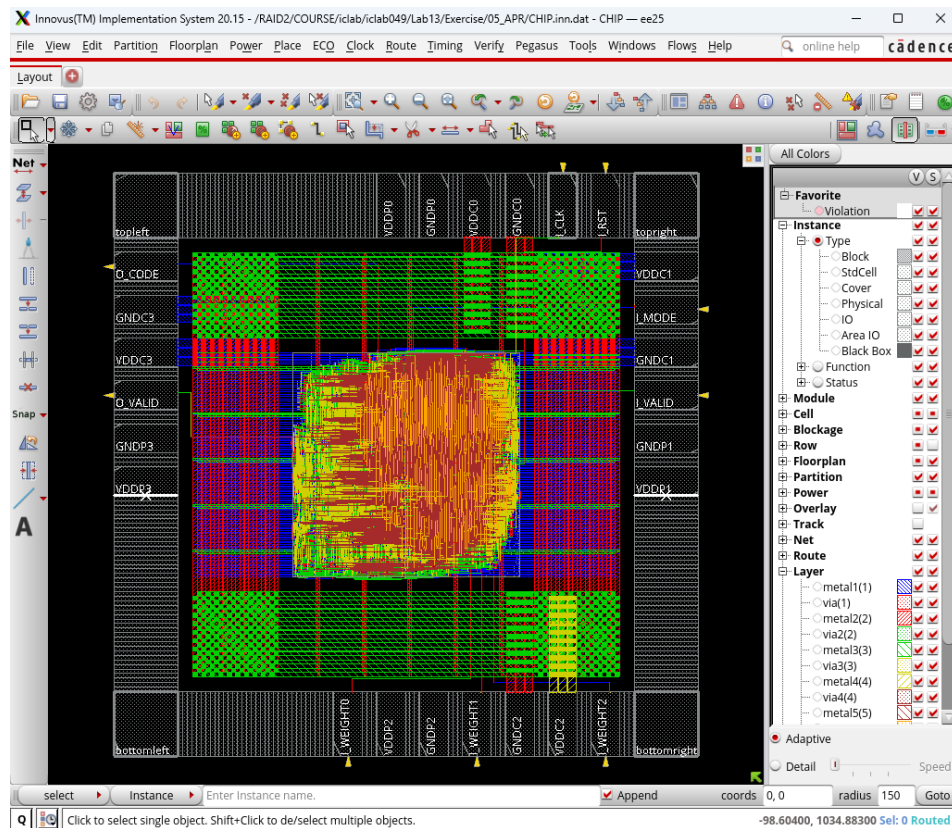
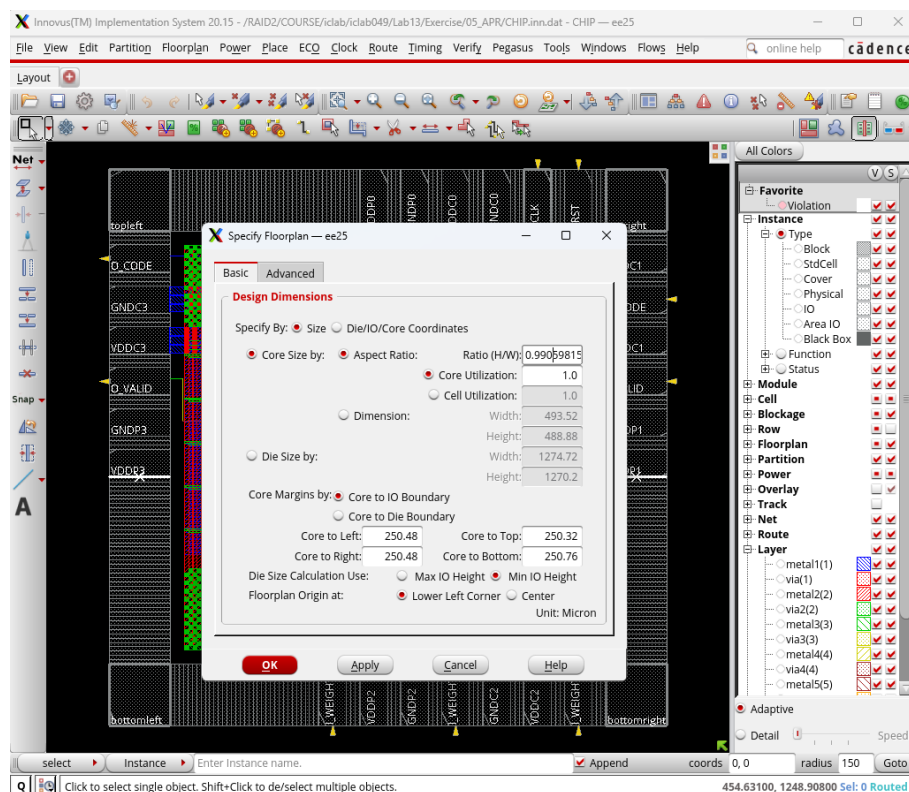


# Report

## 1. Chip Layout View :

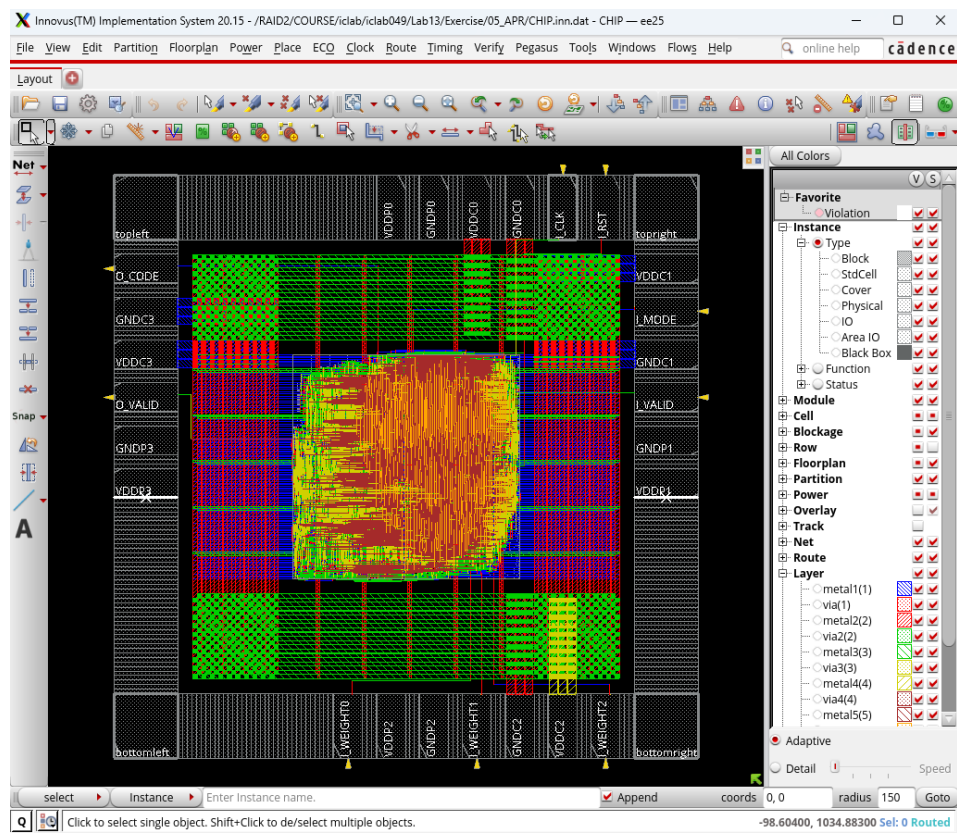


## 2. Core to IO boundary :

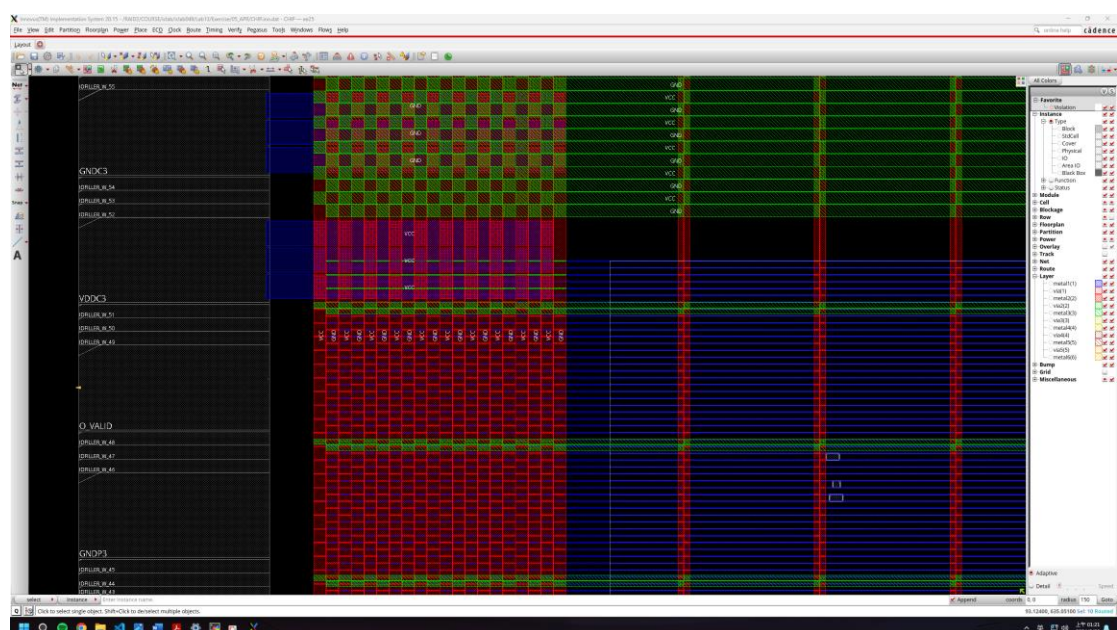


### 3. Core Ring :

#### Overall power ping

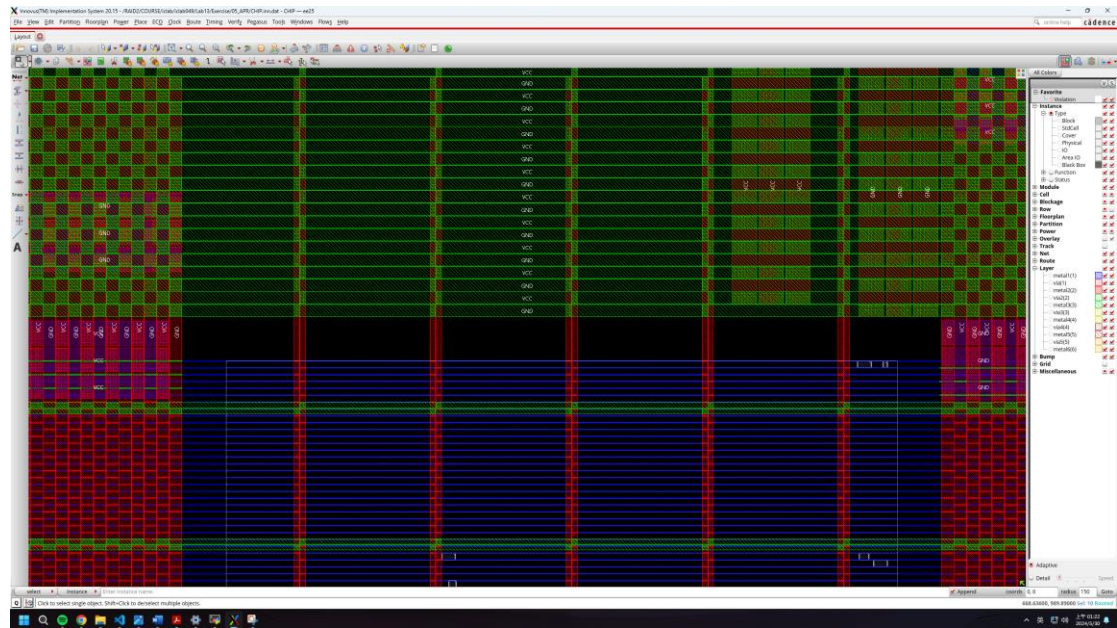


#### Left power ping

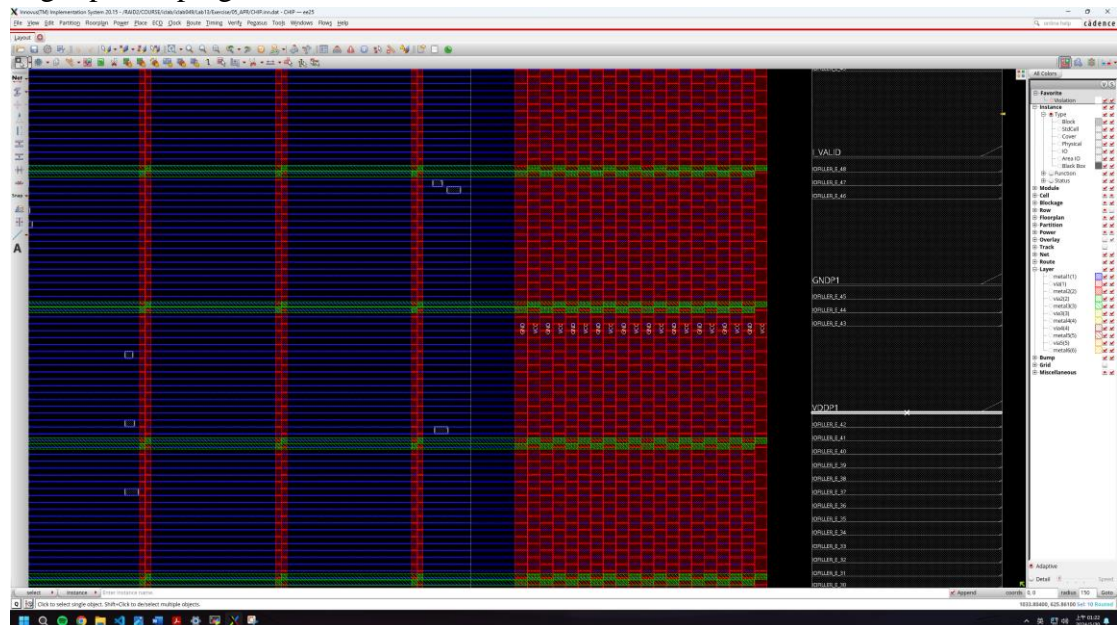




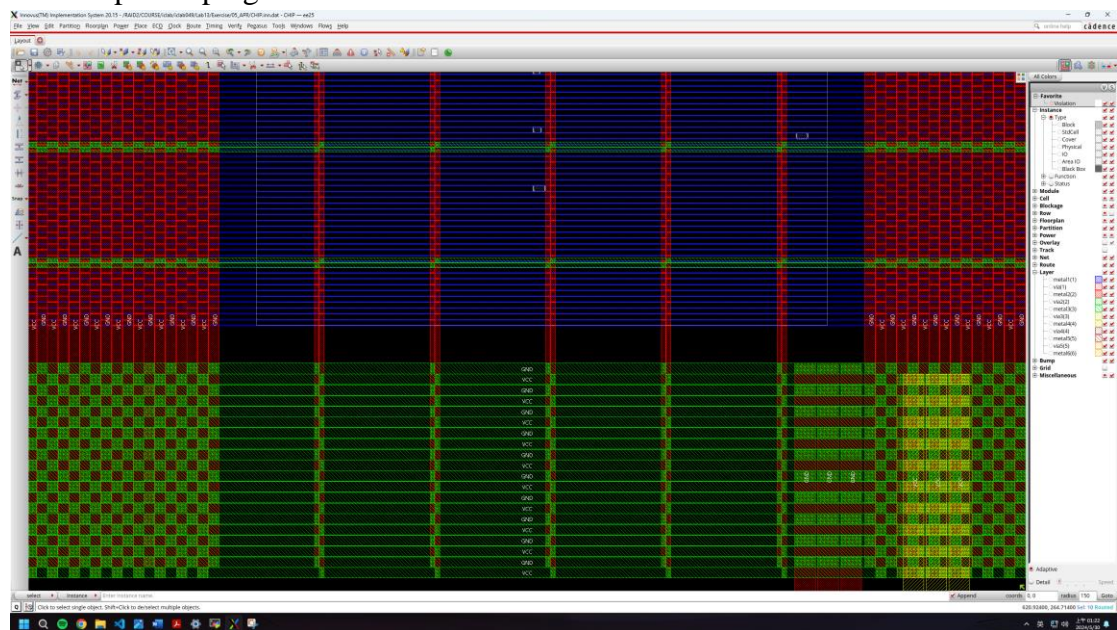
## Top power ping



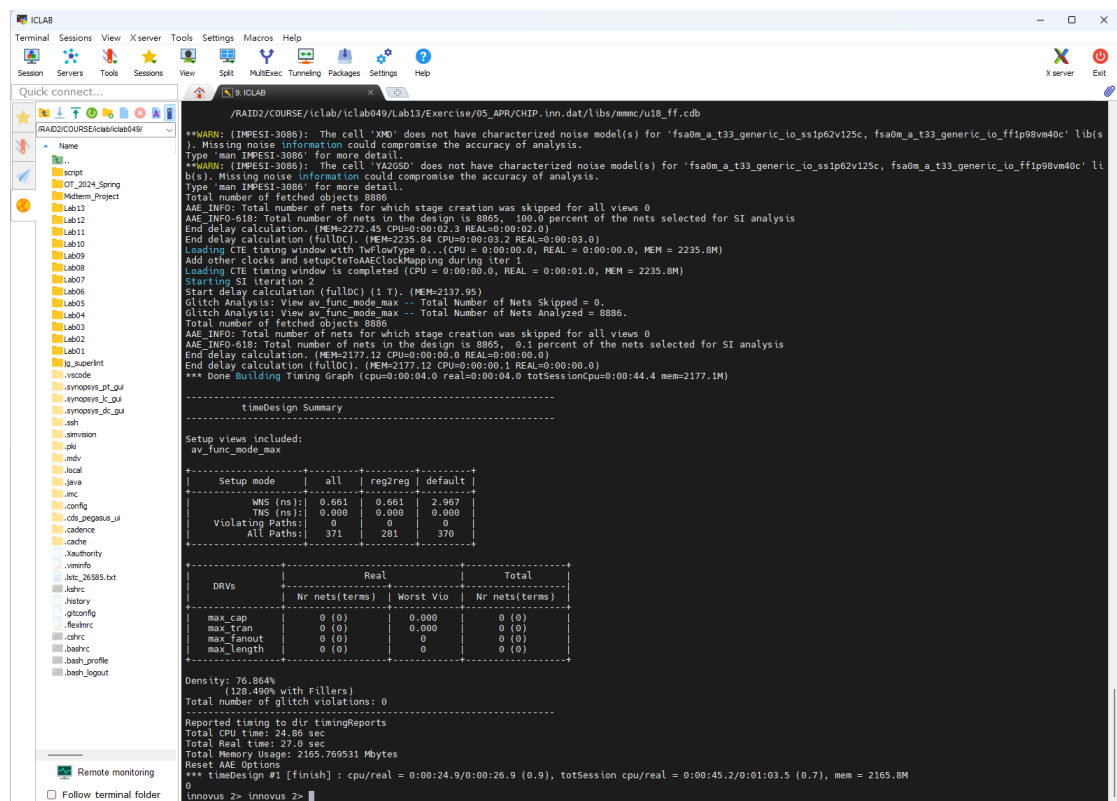
## Right power ping



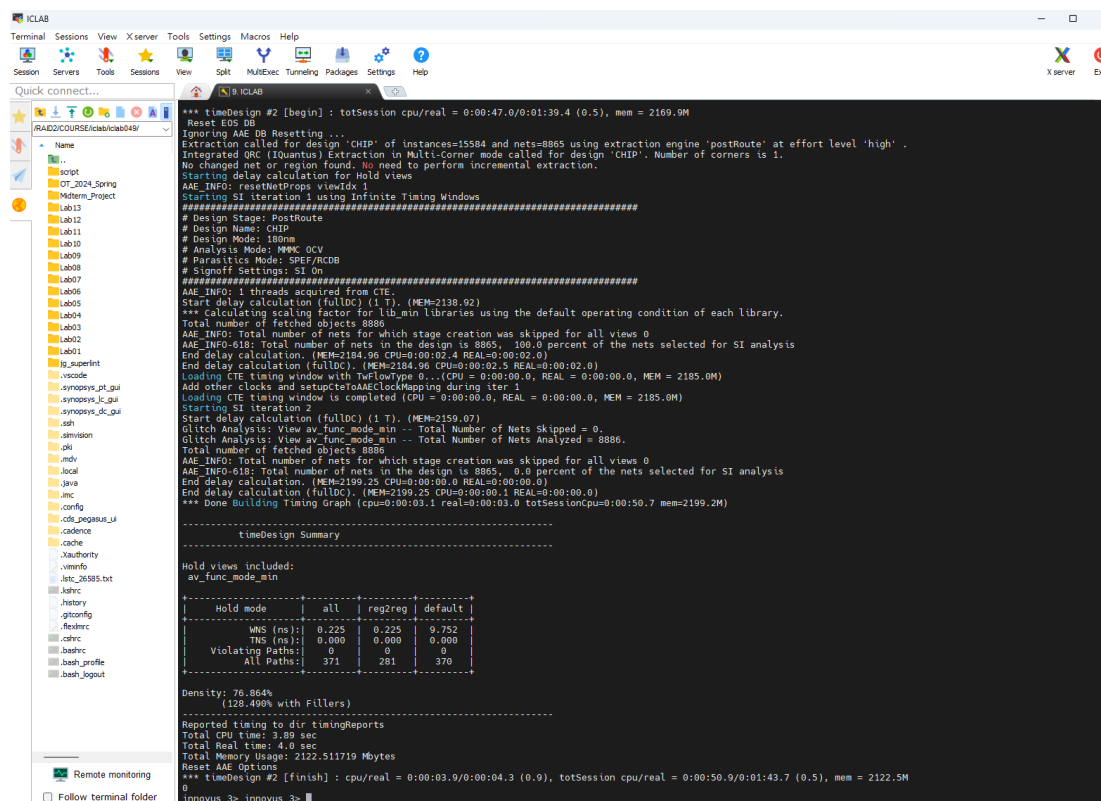
## Bottom power ping



## 4. Post-Route setup time analysis :



## 5. Post-Route hold time analysis :



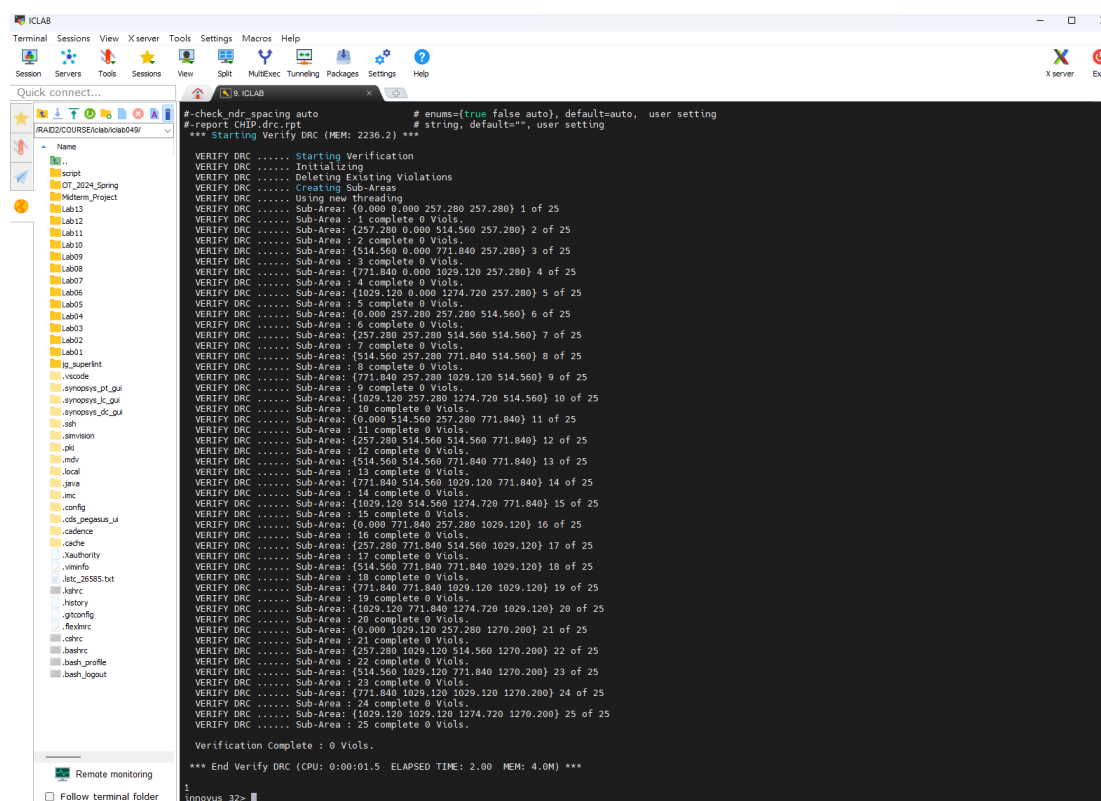
```
*** timeDesign #2 [begin] : totSession cpu/real = 0:00:47.0/0:01:39.4 (0.5), mem = 2169.9M
Reset EOS DB
Ignoring AAE DB Resetting ...
Extraction called for design 'CHIP' of instances=15594 and nets=8865 using extraction engine 'postRoute' at effort level 'high'.
Integrated QRC (IQuantus) Extraction in Multi-Corner mode called for design 'CHIP'. Number of corners is 1.
No changed net or region found. No need to perform incremental extraction.
Starting delay calculation for hold views
AAE_INFO: resetNetProps viewIdx 1
Starting SI iteration 1 using Infinite Timing Windows
=====
# Design Stage: PostRoute
# Design Name: CHIP
# Design Mode: 15nm
# Analysis Mode: MMWC QCV
# Parasitics Mode: SPEF/RCDB
# Signoff Settings: SI On
=====
AAE_INFO: 1 threads acquired from CTE
Start delay calculation (fullDC) (1.T). (MEM=2138.92)
*** Calculating scaling factor for lib_min libraries using the default operating condition of each library.
Total number of fetched objects 8866
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
AAE_INFO-618: Total number of nets in the design is 8865, 100.0 percent of the nets selected for SI analysis
End delay calculation. (MEM=2184.96 CPU=0:00:02.4 REAL=0:00:02.0)
Loading CTE timing window with TwFlowType 0. (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 2185.0M)
End delay calculation and setupTotalAAEclockSetup during iter 1
Loading CTE timing window is completed (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 2185.0M)
Starting SI iteration 2
Start delay calculation (fullDC) (1.T). (MEM=2159.07)
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Skipped = 0.
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Analyzed = 8886.
Total number of fetched Objects 8865
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
AAE_INFO-618: Total number of nets in the design is 8865, 0.0 percent of the nets selected for SI analysis
End delay calculation. (MEM=2199.25 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=2199.25 CPU=0:00:00.1 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:03.1 real=0:00:03.0 totSessionCpu=0:00:50.7 mem=2199.2M)

-----
timeDesign Summary
-----
Hold views included:
av_func_mode_min

-----
table
thead
| Hold mode | all | regreg | default |
| --- | --- | --- | --- |
|  |  |  |  |
| --- | --- | --- | --- |
| WNS (ns): | 0.225 | 0.225 | 9.752 |
| THS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 371 | 281 | 370 |


-----
Density: 76.864%
(128.490% with Fillers)
-----
Reported timing to dir: timingReports
Total CPU time: 3.89 sec
Total Real time: 4.0 sec
Total Memory Usage: 2122.511719 Mbytes
Reset AAE Options
*** timeDesign #2 [finish] : cpu/real = 0:00:03.9/0:00:04.3 (0.9), totSession cpu/real = 0:00:50.9/0:01:43.7 (0.5), mem = 2122.5M
0
Innovus 3> innovus 3> |
```

## 6. DRC result :



```
#####-check ndr spacing auto # enums={true false auto}, default=auto, user setting
#####-report CHIP.drc.rpt # string, default="", user setting
*** Starting Verify DRC (MEM: 2236.2) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: (0.000 0.000 257.280 257.280) 1 of 25
VERIFY DRC ..... Sub-Area: 1 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (257.280 0.000 514.560 257.280) 2 of 25
VERIFY DRC ..... Sub-Area: 2 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (514.560 0.000 771.840 257.280) 3 of 25
VERIFY DRC ..... Sub-Area: 3 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (771.840 0.000 1029.120 257.280) 4 of 25
VERIFY DRC ..... Sub-Area: 4 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (1029.120 0.000 1274.720 257.280) 5 of 25
VERIFY DRC ..... Sub-Area: 5 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (0.000 257.280 257.280 514.560) 6 of 25
VERIFY DRC ..... Sub-Area: 6 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (257.280 257.280 514.560 514.560) 7 of 25
VERIFY DRC ..... Sub-Area: 7 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (514.560 257.280 771.840 514.560) 8 of 25
VERIFY DRC ..... Sub-Area: 8 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (771.840 257.280 1029.120 514.560) 9 of 25
VERIFY DRC ..... Sub-Area: 9 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (1029.120 257.280 1274.720 514.560) 10 of 25
VERIFY DRC ..... Sub-Area: 10 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (0.000 514.560 257.280 771.840) 11 of 25
VERIFY DRC ..... Sub-Area: 11 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (257.280 514.560 514.560 771.840) 12 of 25
VERIFY DRC ..... Sub-Area: 12 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (514.560 514.560 771.840 771.840) 13 of 25
VERIFY DRC ..... Sub-Area: 13 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (771.840 514.560 1029.120 771.840) 14 of 25
VERIFY DRC ..... Sub-Area: 14 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (1029.120 514.560 1274.720 771.840) 15 of 25
VERIFY DRC ..... Sub-Area: 15 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (0.000 771.840 257.280 1029.120) 16 of 25
VERIFY DRC ..... Sub-Area: 16 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (257.280 771.840 514.560 1029.120) 17 of 25
VERIFY DRC ..... Sub-Area: 17 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (514.560 771.840 771.840 1029.120) 18 of 25
VERIFY DRC ..... Sub-Area: 18 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (771.840 771.840 1029.120 1029.120) 19 of 25
VERIFY DRC ..... Sub-Area: 19 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (1029.120 771.840 1274.720 1029.120) 20 of 25
VERIFY DRC ..... Sub-Area: 20 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (0.000 1029.120 257.280 1270.200) 21 of 25
VERIFY DRC ..... Sub-Area: 21 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (257.280 1029.120 514.560 1270.200) 22 of 25
VERIFY DRC ..... Sub-Area: 22 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (514.560 1029.120 771.840 1270.200) 23 of 25
VERIFY DRC ..... Sub-Area: 23 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (771.840 1029.120 1029.120 1270.200) 24 of 25
VERIFY DRC ..... Sub-Area: 24 complete 0 Viols.
VERIFY DRC ..... Sub-Area: (1029.120 1029.120 1274.720 1270.200) 25 of 25
VERIFY DRC ..... Sub-Area: 25 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:01.5 ELAPSED TIME: 2.00 MEM: 4.0M) ***
1
Innovus 32> |
```



## 7. LVS result :

```

Loading CTE timing window with TuFlowType 0... (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 2185.8M)
Add other clocks and setupCteToAAEClockMapping during iter 1
Loading CTE timing window is completed (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 2185.8M)
Starting SI iteration 2
Start delay calculation (fullDC) (1 T). (MEM=2159.87)
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Skipped = 0
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Analyzed = 8886
Total number of fetched objects 8886
AEC INFO: Total number of nets for which stage creation was skipped for all views 0
AEC INFO: Total number of nets in the design is 8865, 0.9 percent of the nets selected for SI analysis
End delay calculation. (MEM=2199.25 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=2199.25 CPU=0:00:00.1 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:03.1 real=0:00:03.0 totSessionCpu=0:00:50.7 mem=2199.2M)

-----
timeDesign Summary
-----

Hold views included:
av_func_mode_min

-----
| Hold mode | all | reg2reg | default |
-----+-----+-----+-----+
| WNS (ns): | 0.225 | 0.225 | 9.752 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 371 | 281 | 370 |
-----

Density: 76.864%
(128.490% with Fillers)

Reported timing to dir timingReports
Total CPU time: 3.89 sec
Total Real time: 4.0 sec
Total Memory Usage: 2122.511719 Mbytes
Reset AEC Options
*** timeDesign sz [finish] : cpu/real = 0:00:03.9/0:00:04.3 (0.9), totSession cpu/real = 0:00:50.9/0:01:43.7 (0.5), mem = 2122.5M
0
Unnovus > Unnovus > verifyConnectivity -type all -error 1000 -warning 50
VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Thu May 30 01:45:28 2024

Design Name: CHIP
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (1274.7200, 1270.2000)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 01:45:28 **** Processed 5000 nets.

Begin Summary
Found no problems or warnings.
End Summary

End Time: Thu May 30 01:45:28 2024
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viol. 0 Warnings.
(CPU Time: 0:00:00.4 MEM: 0.000M)

1
Unnovus 4>

```

## 8. Post Layout simulation result :

```

PASS PATTERN NO.1931
PASS PATTERN NO.1932
PASS PATTERN NO.1933
PASS PATTERN NO.1934
PASS PATTERN NO.1935
PASS PATTERN NO.1936
PASS PATTERN NO.1937
PASS PATTERN NO.1938
PASS PATTERN NO.1939
PASS PATTERN NO.1940
PASS PATTERN NO.1941
PASS PATTERN NO.1942
PASS PATTERN NO.1943
PASS PATTERN NO.1944
PASS PATTERN NO.1945
PASS PATTERN NO.1946
PASS PATTERN NO.1947
PASS PATTERN NO.1948
PASS PATTERN NO.1949
PASS PATTERN NO.1950
PASS PATTERN NO.1951
PASS PATTERN NO.1952
PASS PATTERN NO.1953
PASS PATTERN NO.1954
PASS PATTERN NO.1955
PASS PATTERN NO.1956
PASS PATTERN NO.1957
PASS PATTERN NO.1958
PASS PATTERN NO.1959
PASS PATTERN NO.1960
PASS PATTERN NO.1961
PASS PATTERN NO.1962
PASS PATTERN NO.1963
PASS PATTERN NO.1964
PASS PATTERN NO.1965
PASS PATTERN NO.1966
PASS PATTERN NO.1967
PASS PATTERN NO.1968
PASS PATTERN NO.1969
PASS PATTERN NO.1970
PASS PATTERN NO.1971
PASS PATTERN NO.1972
PASS PATTERN NO.1973
PASS PATTERN NO.1974
PASS PATTERN NO.1975
PASS PATTERN NO.1976
PASS PATTERN NO.1977
PASS PATTERN NO.1978
PASS PATTERN NO.1979
PASS PATTERN NO.1980
PASS PATTERN NO.1981
PASS PATTERN NO.1982
PASS PATTERN NO.1983
PASS PATTERN NO.1984
PASS PATTERN NO.1985
PASS PATTERN NO.1986
PASS PATTERN NO.1987
PASS PATTERN NO.1988
PASS PATTERN NO.1989
PASS PATTERN NO.1990
PASS PATTERN NO.1991
PASS PATTERN NO.1992
PASS PATTERN NO.1993
PASS PATTERN NO.1994
PASS PATTERN NO.1995
PASS PATTERN NO.1996
PASS PATTERN NO.1997
PASS PATTERN NO.1998
PASS PATTERN NO.1999

-----
Congratulations!
You have passed all patterns!
Your execution cycles = 32000 cycles
Your clock period = 20.0 ns
Total Latency = 640000.0 ns
-----

$finish called from file "PATTERN.v", line 36.
$finish at simulation time 1019630000
VCS Simulation Report
Time: 1019630000 ps
CPU Time: 29.460 seconds; Data structure size: 2.2M
Thu May 30 00:25:26 2024
CPU time: 1.538 seconds to compile + .397 seconds to elab + .003 seconds to link + 29.476 seconds in simulation
0:25 iClab49@e251~/.Lab13/Exercise/06_POST$

```

## 9. Power result :

```

ICLAB
Terminal Sessions View Xserver Tools Settings Macros Help
Session Servers Tools Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...
RAID2/COURSE/iclab/iclab049/Lab11
Name
simv.daidir
csrc
vcs.log
uci.key
TESTBED.v
simv
PATTERN.v
novas_dump.log
makefile
filelist.f
CHIP_POST.fsd
CHIP.v
CHIP.sdf
09_clean_up
09_check
05_nWave
04_verdi
03_run_post
02_run_post
01_run_vcs_post

** WARN: (VOLTUS_POWR-2152): Instance VDDC0 (VCCKD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance GNDK0 (GNDKD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance VDDC1 (VCCKD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance GNDK1 (GNDKD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance VDDC2 (VCCKD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance GNDK2 (GNDKD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance VDDC3 (VCCKD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance GNDK3 (GNDKD) has no static power.
*

Total Power
-----
Total Internal Power:      1.40782565      50.9286%
Total Switching Power:     1.34771870      48.7543%
Total Leakage Power:       0.00876541       0.3171%
Total Power:               2.76430976

** WARN: (VOLTUS_POWR-2041): There are some instances in the design which are not connected to any power or ground nets.
These instances will be added to default power/ground rail uti files.
Use 'itaputil list <uti-file>' command to get the list of instances.

** WARN: (VOLTUS_POWR-3424): Cell A0222S has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell MA0222 has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell MOAI1 has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell OAI112H has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell AN3S has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell QOFFN has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell ND2P has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell QDFFS has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell OA222S has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell ND3S has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell DFFN has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell OAI112HS has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell GNDKD has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell DFFS has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell OA13S has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell ND3P has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell MUXB2S has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell VCCKD has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell QDFFRBS has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell AN4B1S has no power pin defined in LEF/PGV.

** WARN: (EMS-27): Message (VOLTUS_POWR-3424) has exceeded the current message display limit of 20.
To increase the message display limit, refer to the product command reference manual.

Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1411.17MB/3435.32MB/1476.51MB)

Begin Creating Binary Database
Ended Creating Binary Database: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1924.27MB/4205.75MB/1924.38MB)

Output file is power_log/CHIP.rpt
  
```

Remote monitoring  
☐ Follow terminal folder

## 10. IR Drop Results :

Decrease the utilization to 60%, add a more I/O core power pad (two sets on each side, for a total of 8 sets of power pads), and increase the number of stripes.

