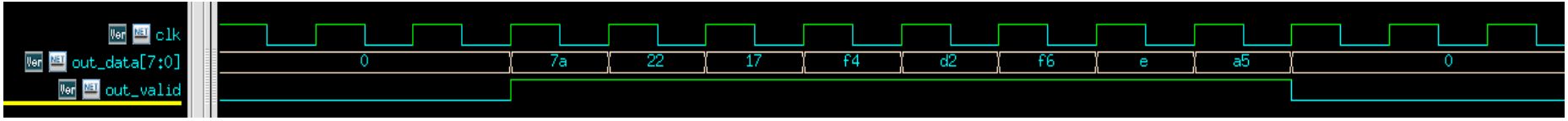
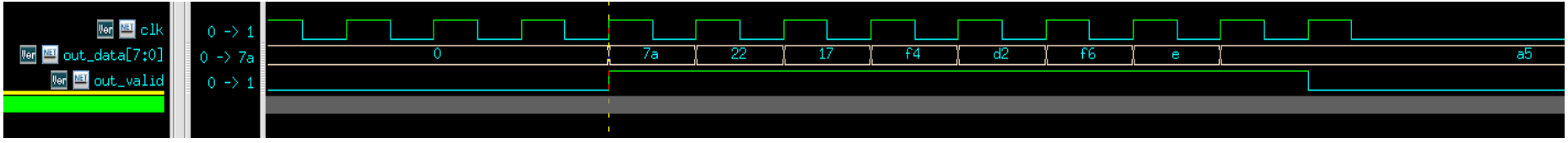
ICLAB 2024-SPRING Lab03 Error Waveform

SPEC_MAIN_2

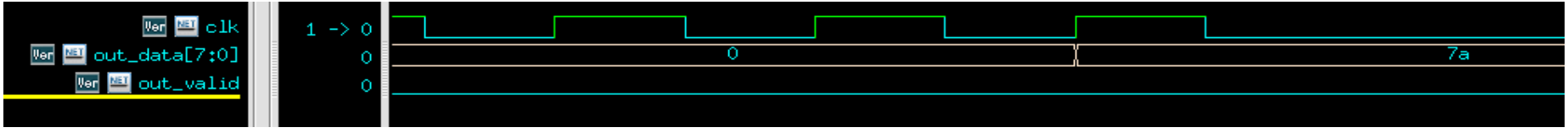
- **The output data should be reset when out_valid is low**
  - CORRECT :



  - SPEC_MAIN_2_1 :

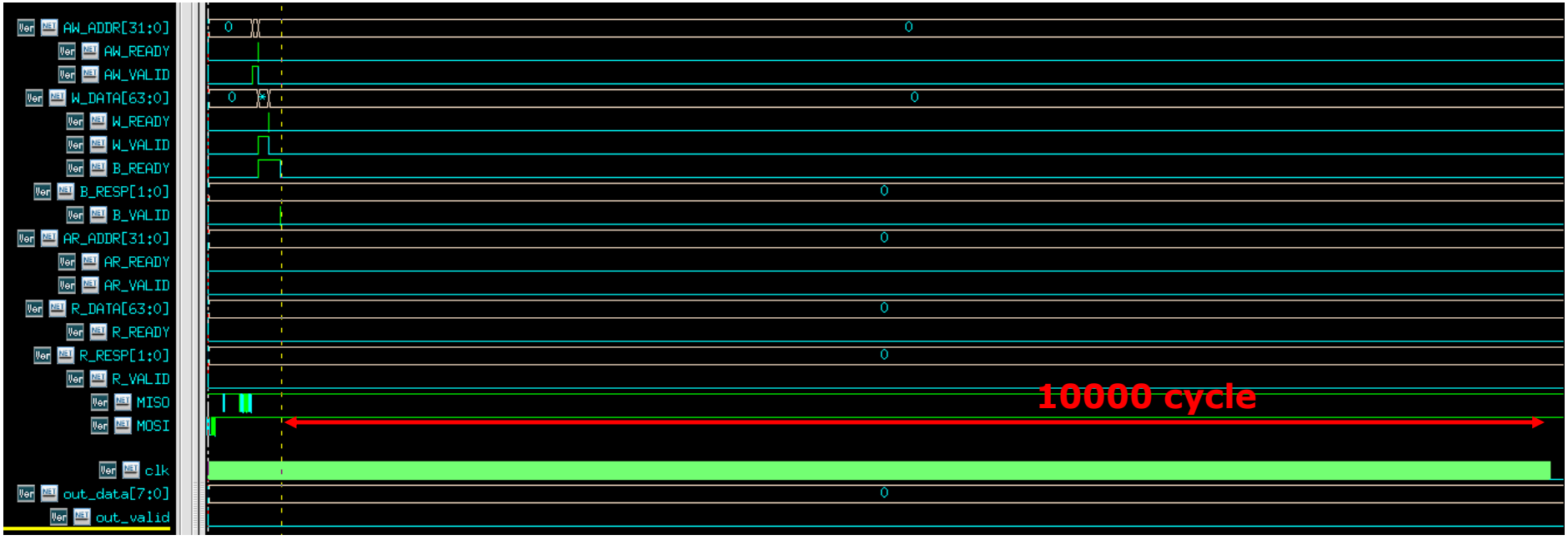


  - SPEC_MAIN_2_2 :



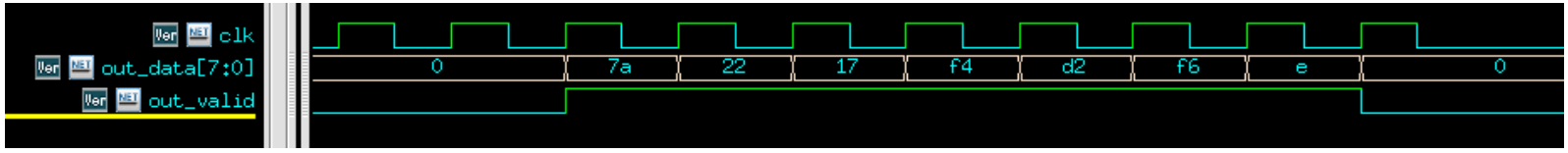
SPEC_MAIN_3

- **Latency are over 10000 cycles(No out_valid and out_data)**
  - SPEC_MAIN_3_1 :

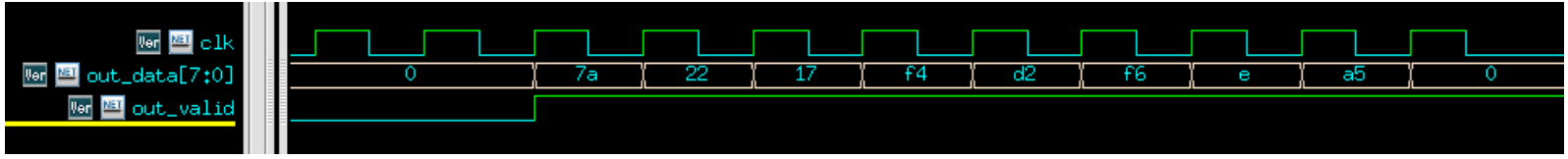


SPEC_MAIN_4

- **The out_valid and out_data must be asserted in 8 cycles.**
  - SPEC_MAIN_4_1 : asserted in 7 cycles

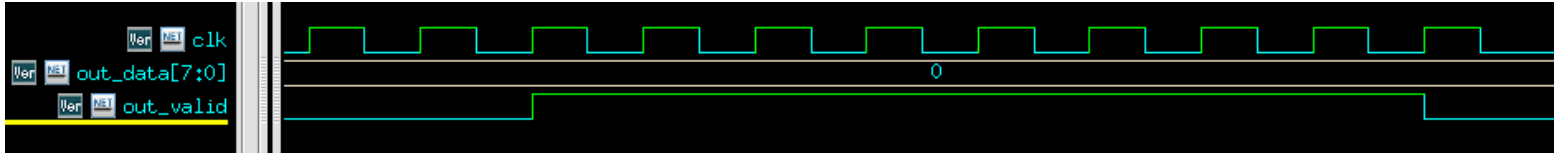


  - SPEC_MAIN_4_2 : out_valid no pull low

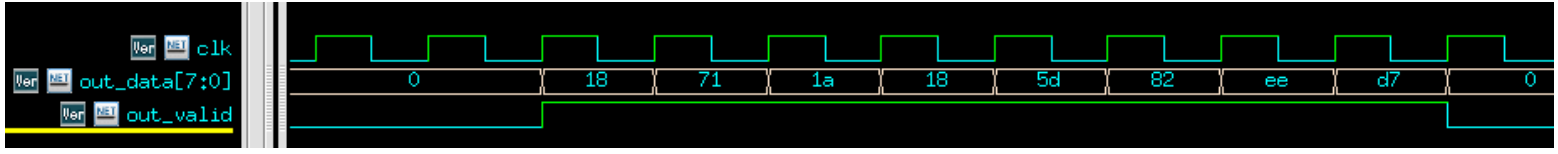


SPEC_MAIN_5

- **The out_data should be correct when out_valid is high.**
  - SPEC_MAIN_5_1 :

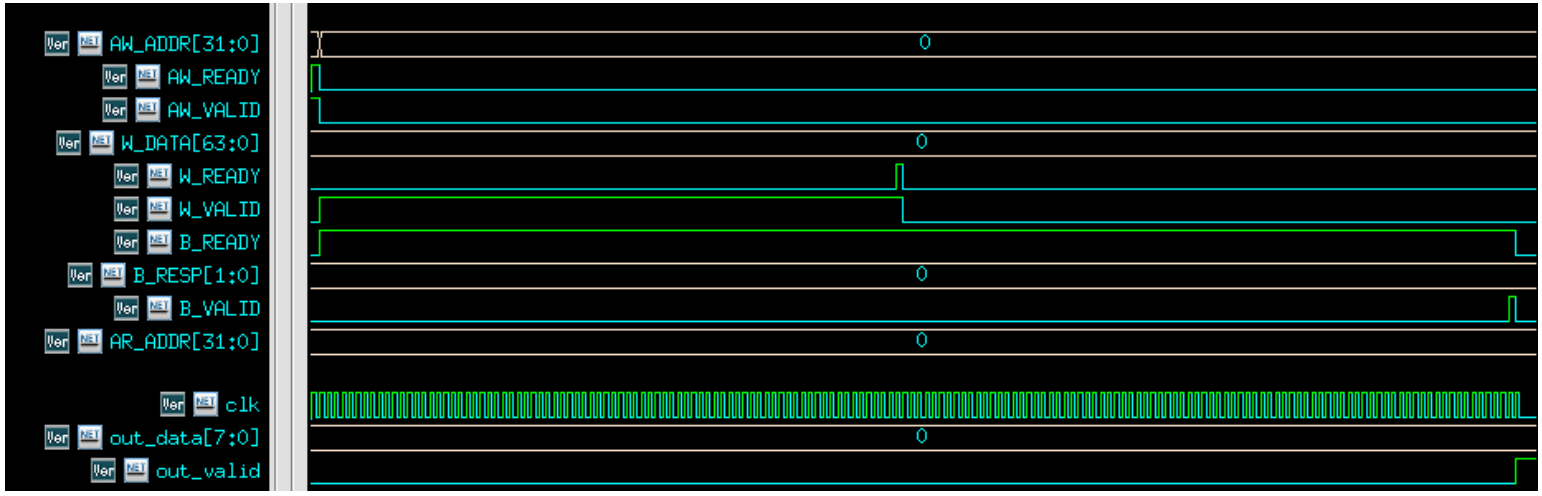


  - SPEC_MAIN_5_2 : Correct Answer should be 7a_22_17_f4_d2_f6_0e_a5



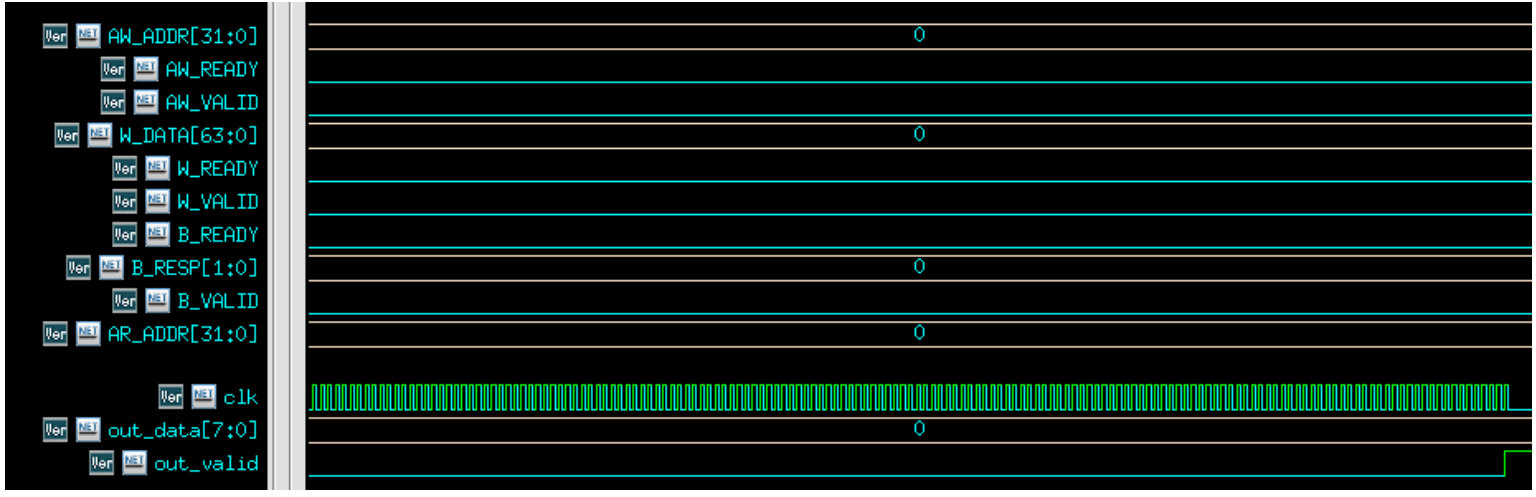
SPEC_MAIN_6

- **The data in the DRAM and SD card should be correct when out_valid is high.**
  - SPEC_MAIN_6_1：It directly write 0 to DRAM and pull high the out_valid



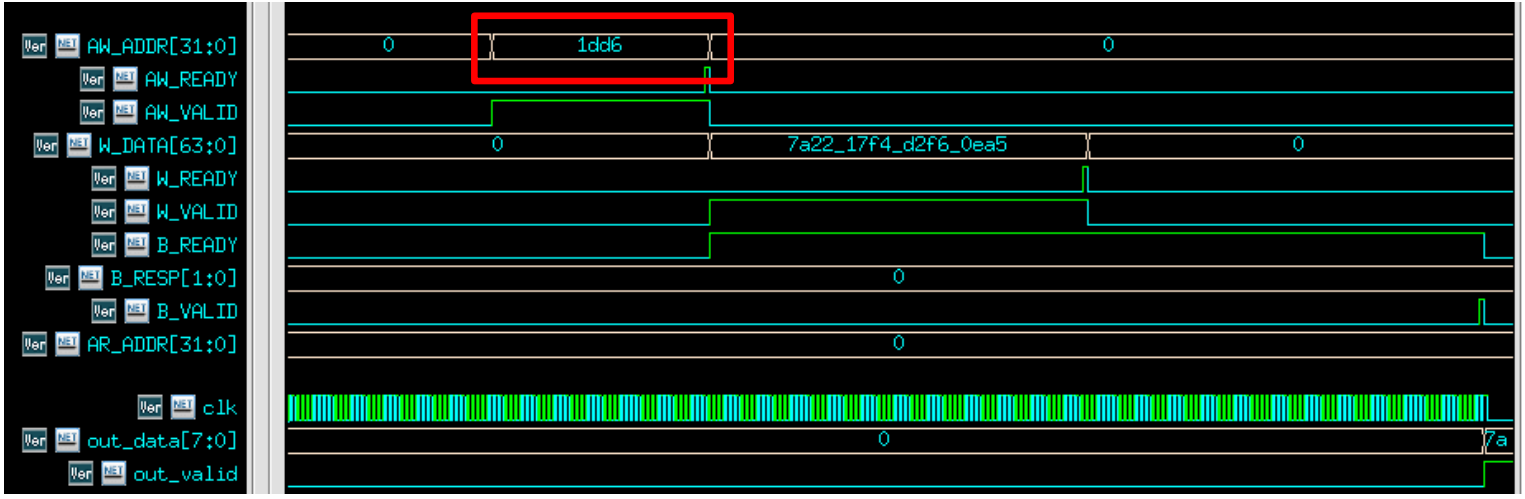
SPEC_MAIN_6

- **The data in the DRAM and SD card should be correct when out_valid is high.**
  - SPEC_MAIN_6_2：it doesn’t write data into DRAM.



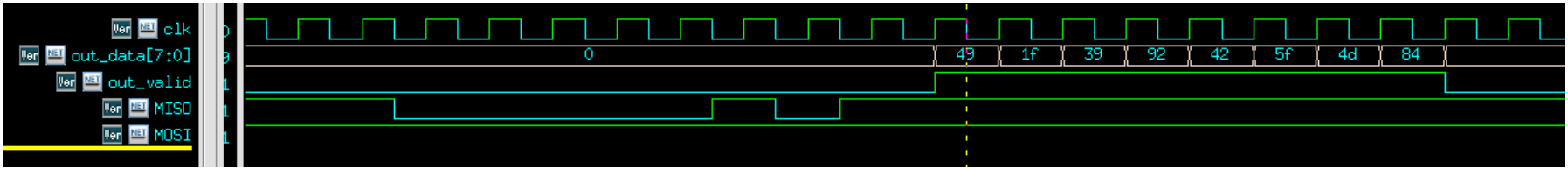
SPEC_MAIN_6

- **The data in the DRAM and SD card should be correct when out_valid is high.**
  - SPEC_MAIN_6_3 : Send wrong address to DRAM (golden address is 0x6D6)

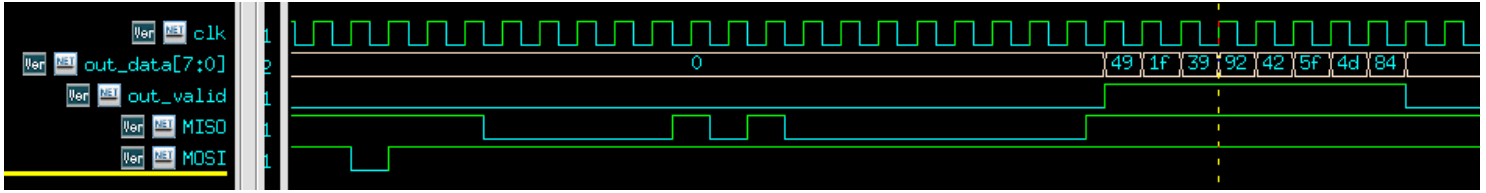


SPEC_MAIN_6

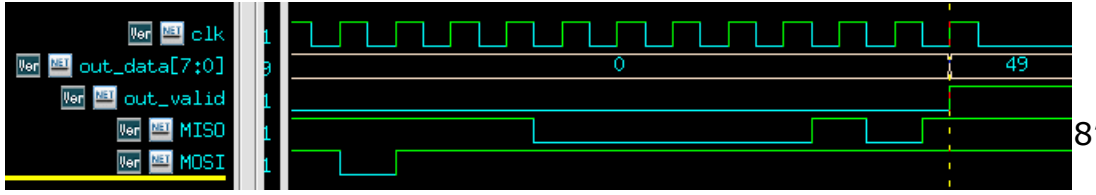
- **The data in the DRAM and SD card should be correct when out_valid is high.**
  - CORRECT 1：The Busy of the SD card Data response is 0 unit



  - CORRECT 2：The Busy of the SD card Data response is 1 unit



  - SPEC_MAIN_6_4：Bridge doesn’t wait the Busy then pull high immediately



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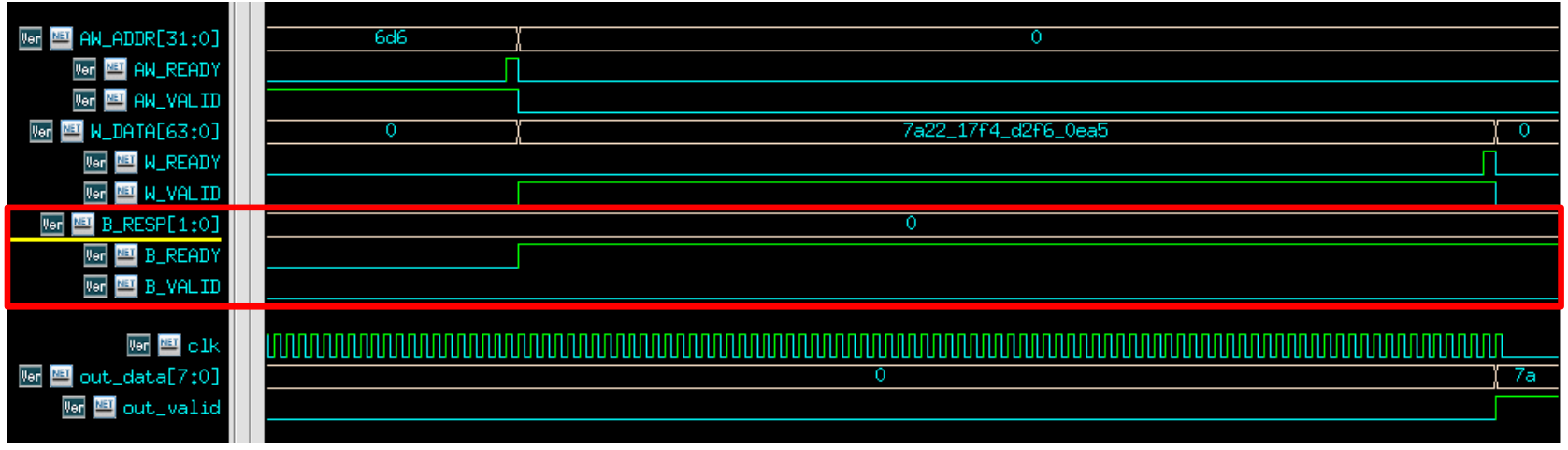
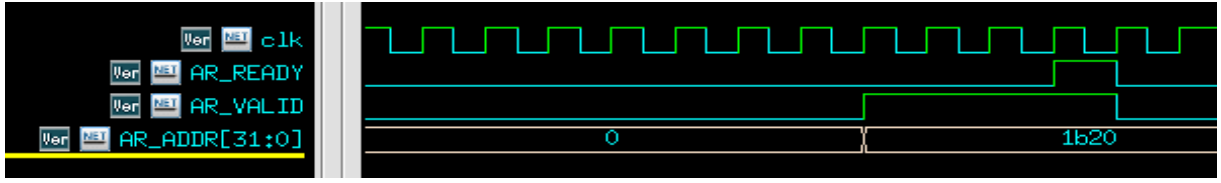
SPEC_MAIN_6

- **The data in the DRAM and SD card should be correct when out_valid is high.**
  - SPEC_MAIN_6_5：Write Response Channel (B_RADY and B_VALID) not both pull high yet

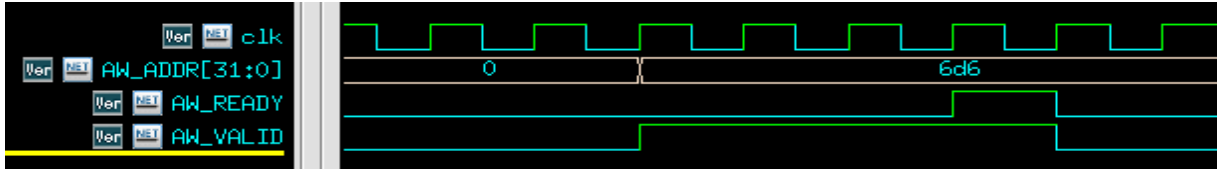


SPEC_DRAM_1

- **AR_ADDR should be reset when AR_VALID is low**
  - SPEC_DRAM_1_1 :

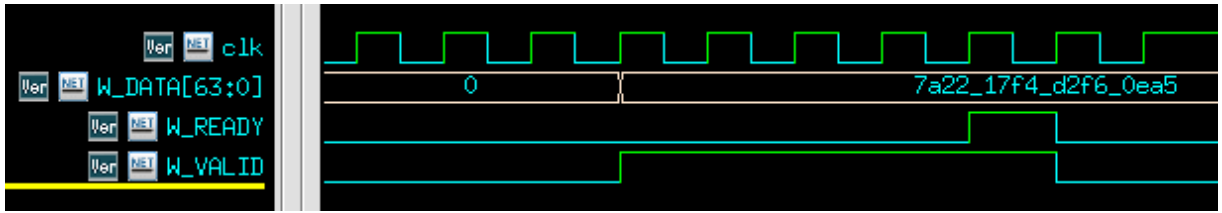


- **AW_ADDR should be reset when AW_VALID is low**
  - SPEC_DRAM_1_2 :



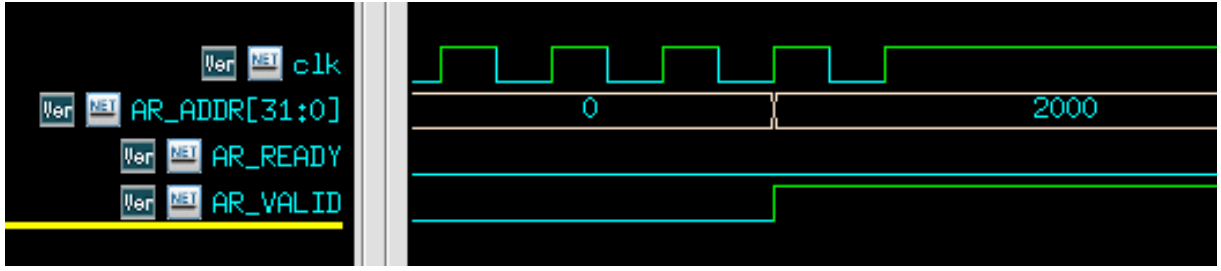
SPEC_DRAM_1

- **W_DATA should be reset when W_VALID is low.**
  - SPEC_DRAM_1_3 :

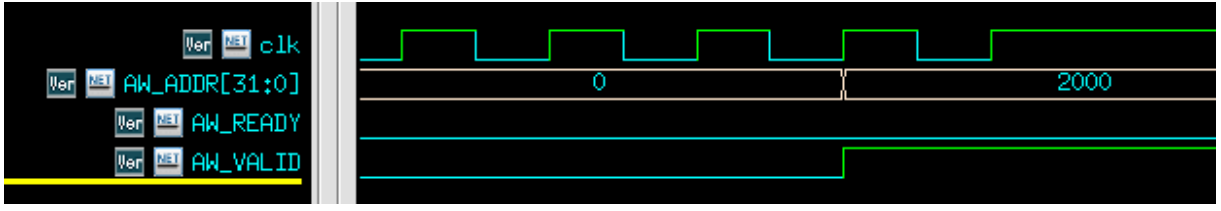


SPEC_DRAM_2

- **The DRAM address should be within the legal range (0~8191).**
  - SPEC_DRAM_2_1 : Read Address Channel

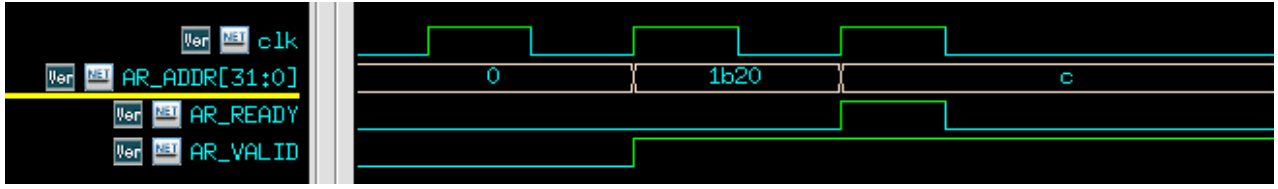


  - SPEC_DRAM_2_2 : Write Address Channel

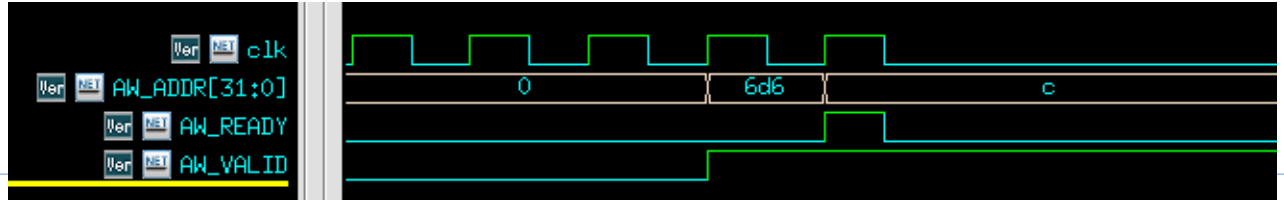


SPEC_DRAM_3

- **AR_VALID and AR_ADDR should remain stable until AR_READY goes high.**
  - SPEC_DRAM_3_1 : Please ensure that AR_READY is asserted high when AR_VALID has been asserted high for at least two cycles.(hint: use $urandom_range function to control AR_READY pull high within 0~50 cycles after AR_VALID is high)

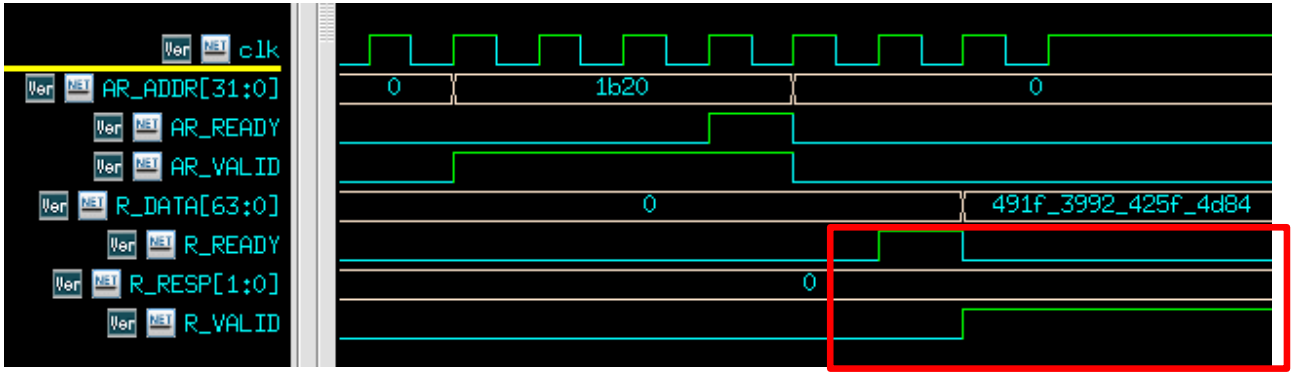


- **AW_VALID and AW_ADDR should remain stable until AW_READY goes high**
  - SPEC_DRAM_3_2 : Please ensure that AW_READY is asserted high when AW_VALID has been asserted high for at least two cycles.(hint: use $urandom_range function to control AW_READY pull high within 0~50 cycles after AW_VALID is high)



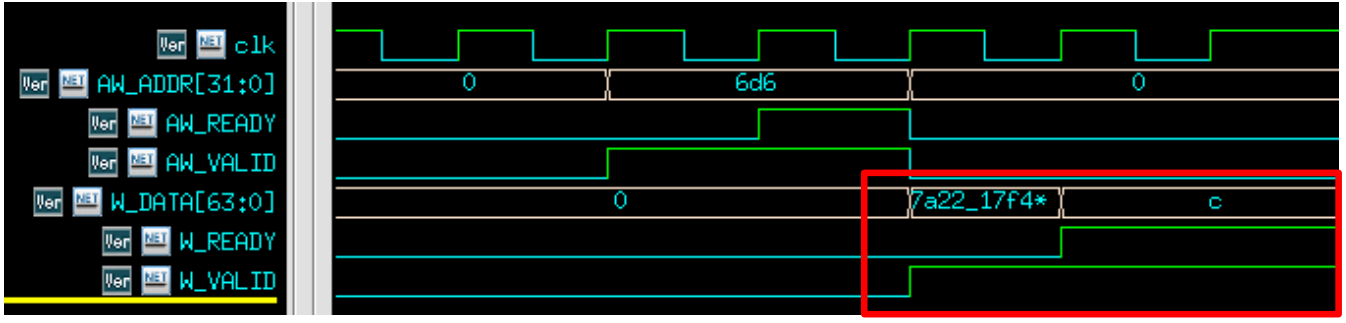
SPEC_DRAM_3

- **R_READY should remain stable until R_VALID goes high.**
  - SPEC_DRAM_3_3 : R_READY go down but R_VALID doesn't go high yet



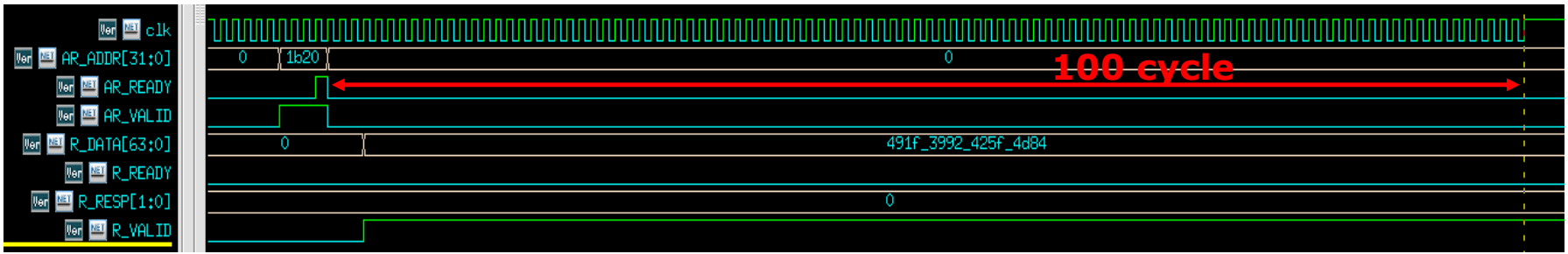
SPEC_DRAM_3

- **W_VALID and W_DATA should remain stable until W_READY goes high.**
  - SPEC_DRAM_3_4 : Please ensure that W_READY is asserted high when W_VALID has been asserted high for at least two cycles.(hint: use $urandom_range function)

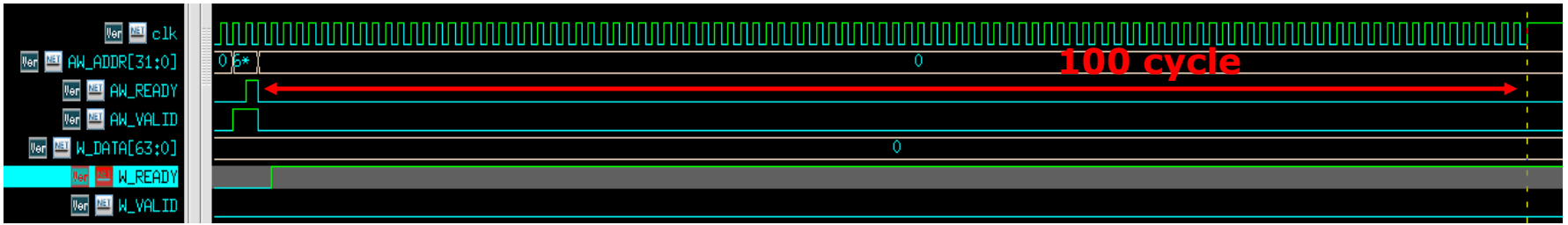


SPEC_DRAM_4

- **R_READY should be asserted within 100 cycles after AR_READY goes high.**
  - SPEC_DRAM_4_1 :

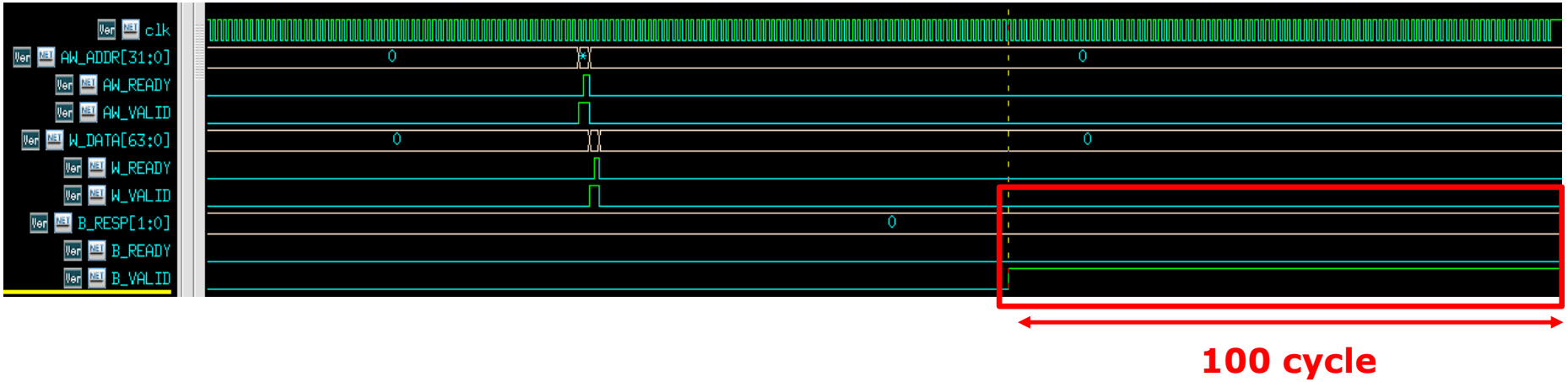


- **W_VALID should be asserted within 100 cycles after AW_READY goes high.**
  - SPEC_DRAM_4_2 :



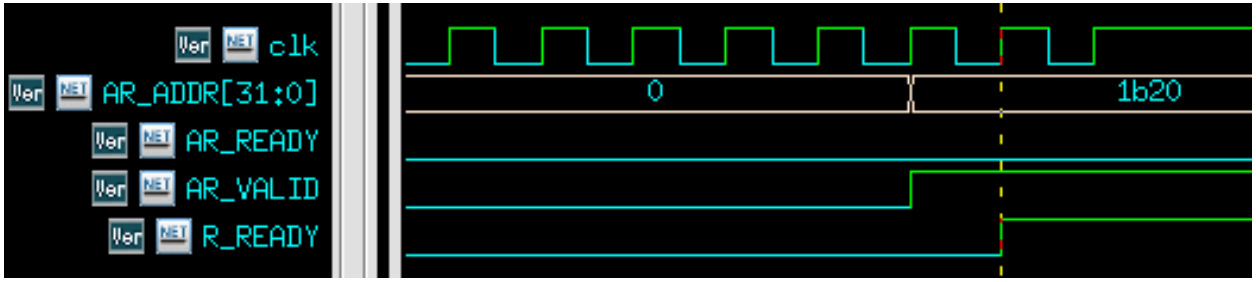
SPEC_DRAM_4

- **B_READY should be asserted within 100 cycles after B_VALID goes high.**
  - SPEC_DRAM_4_3 :



SPEC_DRAM_5

- **R_READY should not be pulled high when AR_READY or AR_WALID go high**
  - SPEC_DRAM_5_1 :



- **W_VALID should not be pulled high when AW_READY or AW_VALID goes high.**
  - SPEC_DRAM_5_2 :