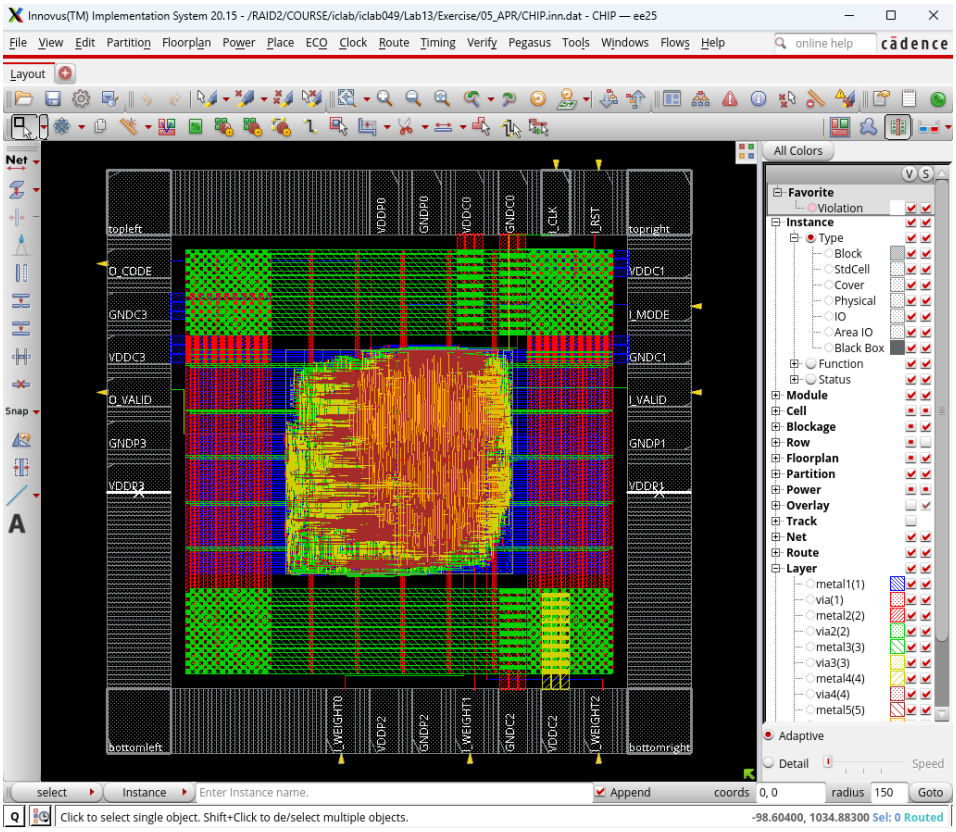
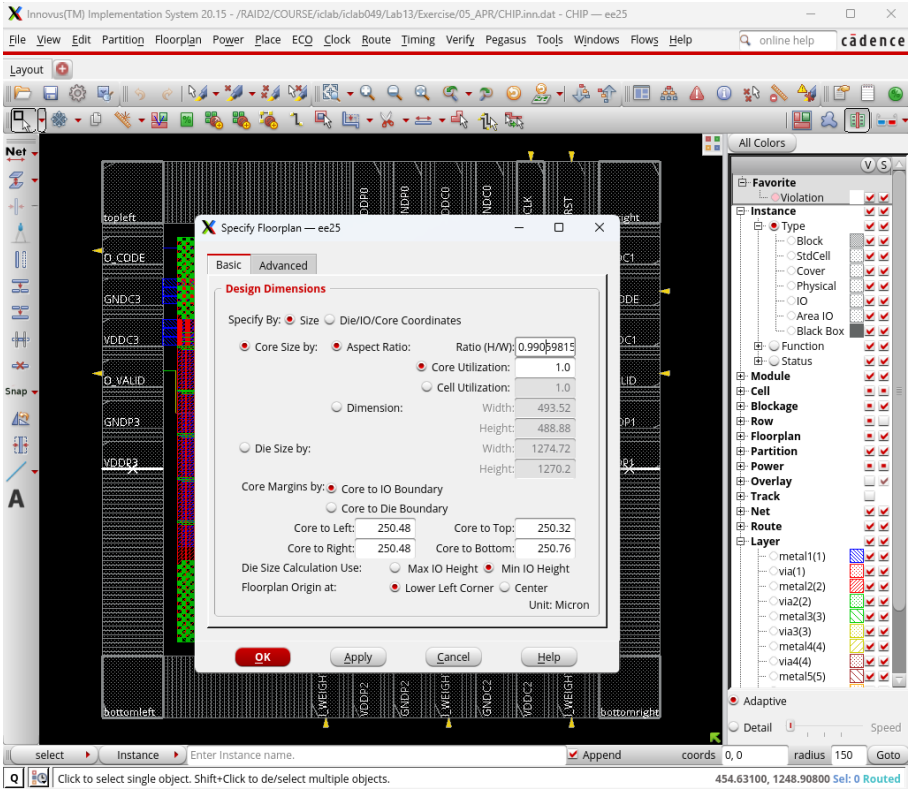
Report

1. Chip Layout View :

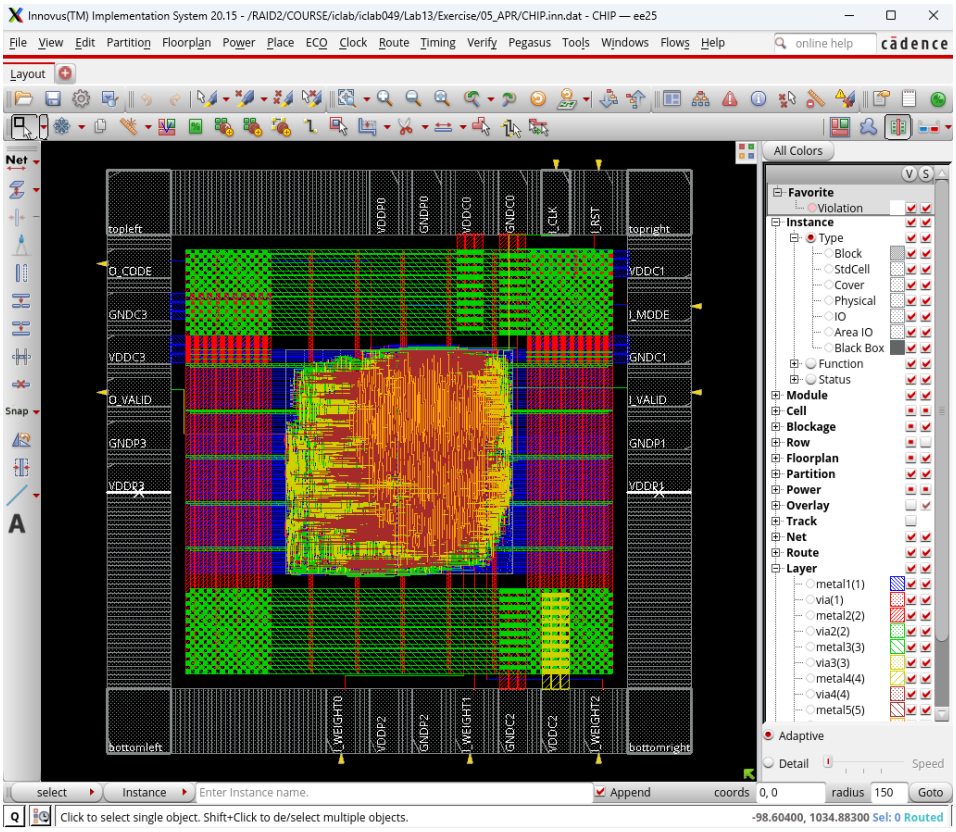


2. Core to IO boundary :

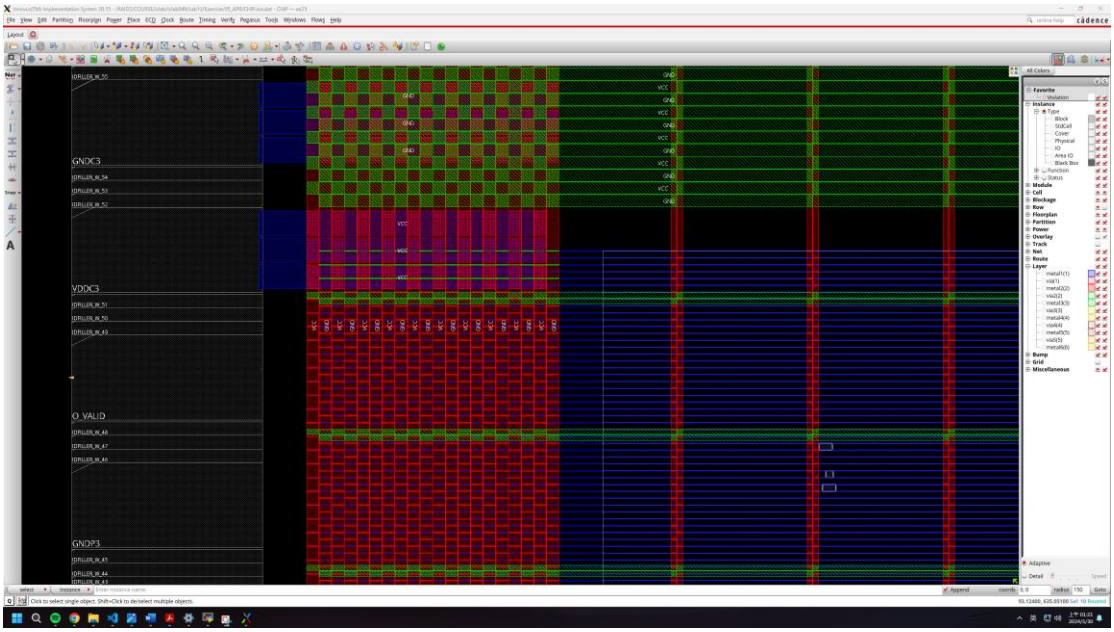


3. Core Ring :

Overall power ping

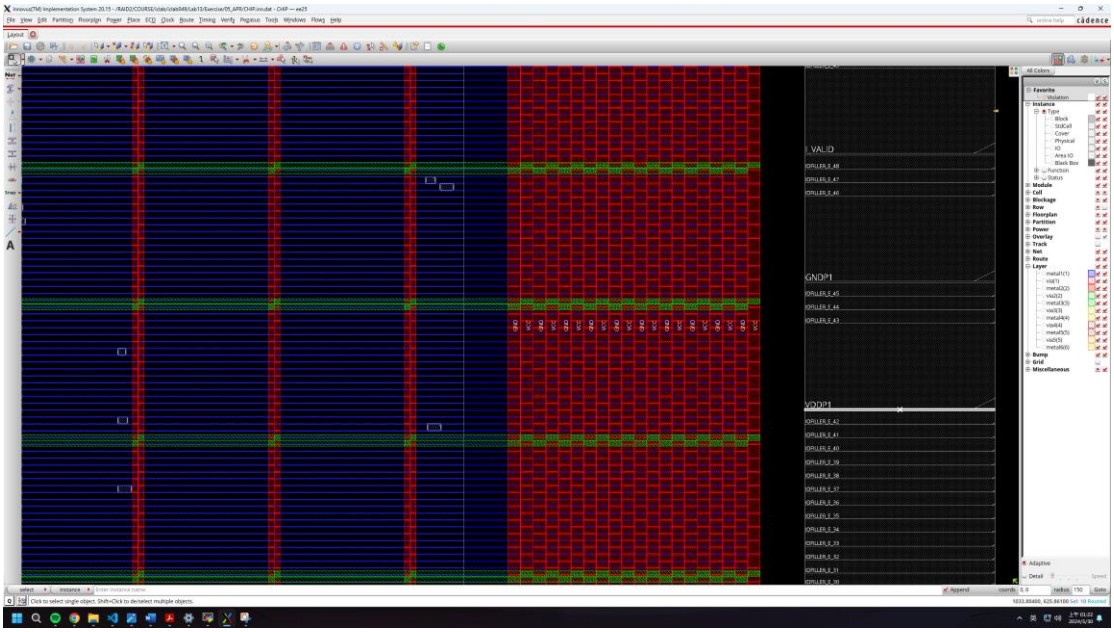


Left power ping

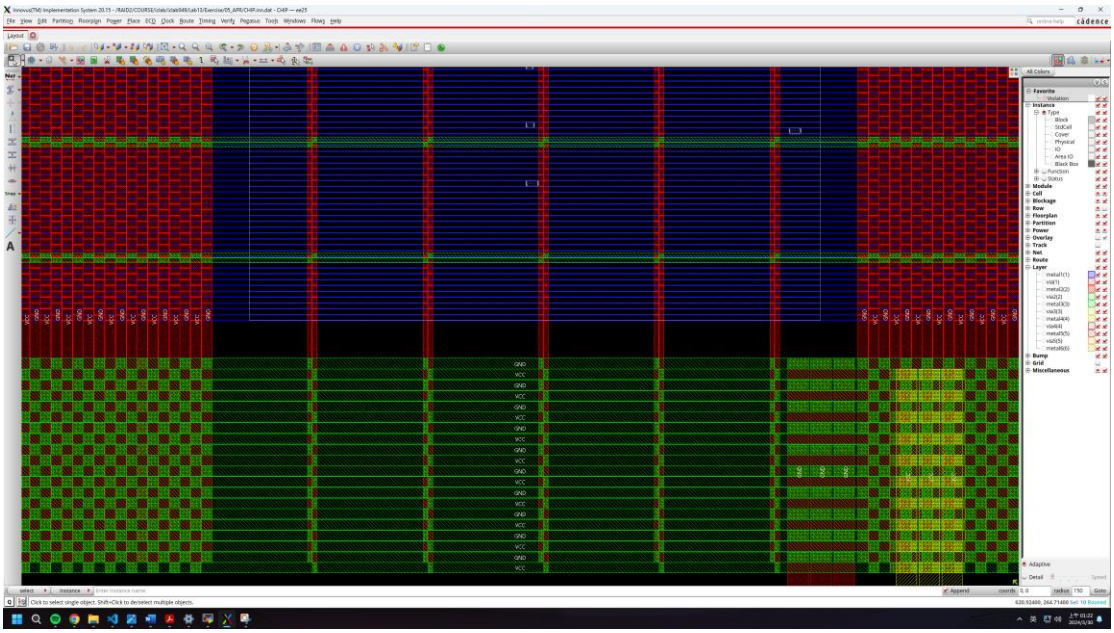


Top power ping

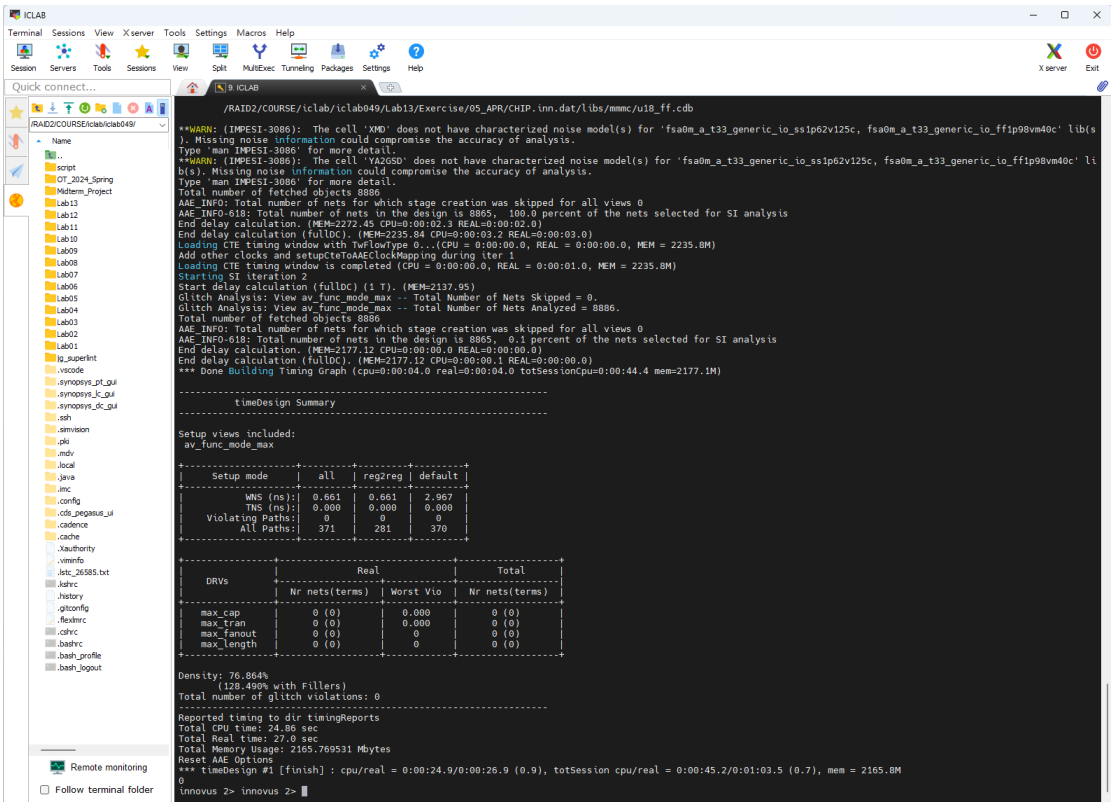
Right power ping



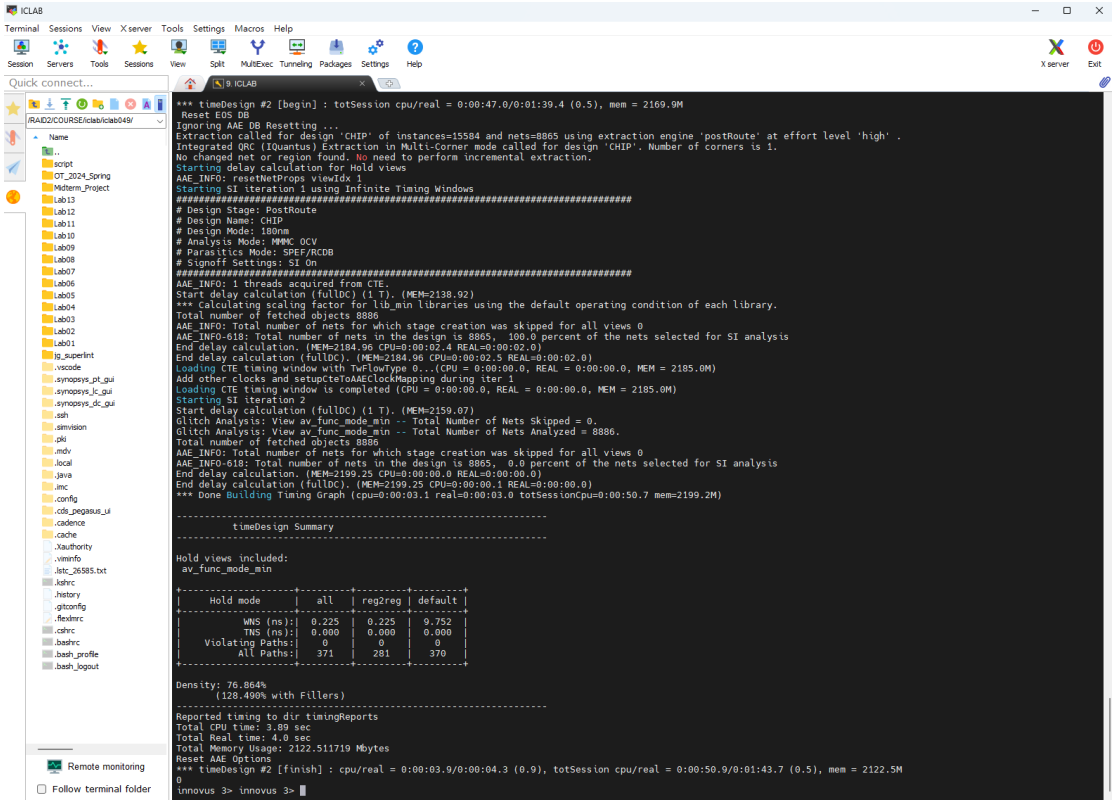
Bottom power ping



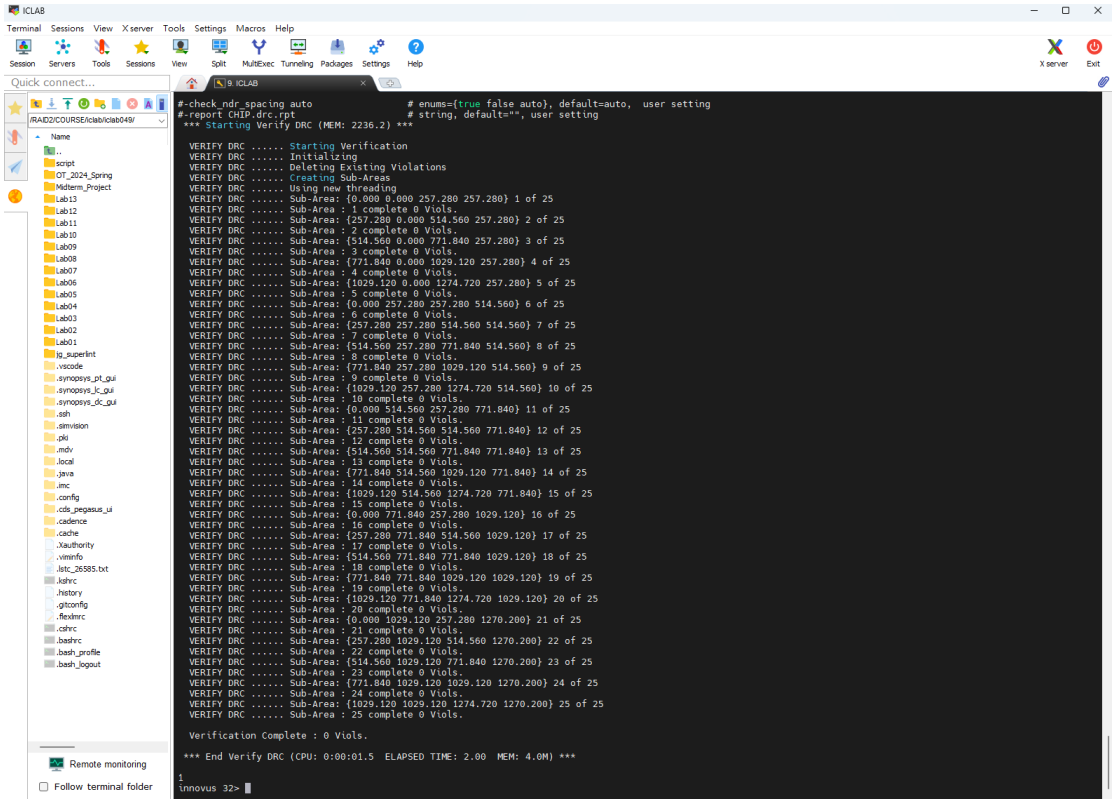
4. Post-Route setup time analysis :



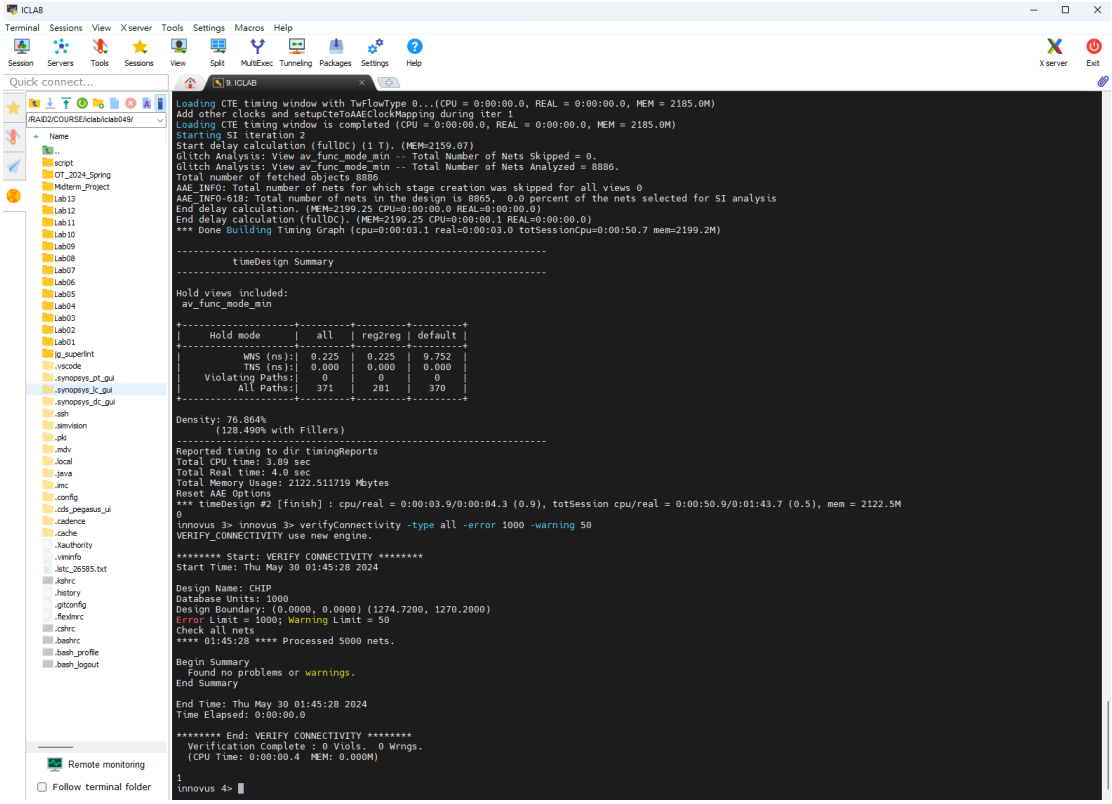
5. Post-Route hold time analysis :



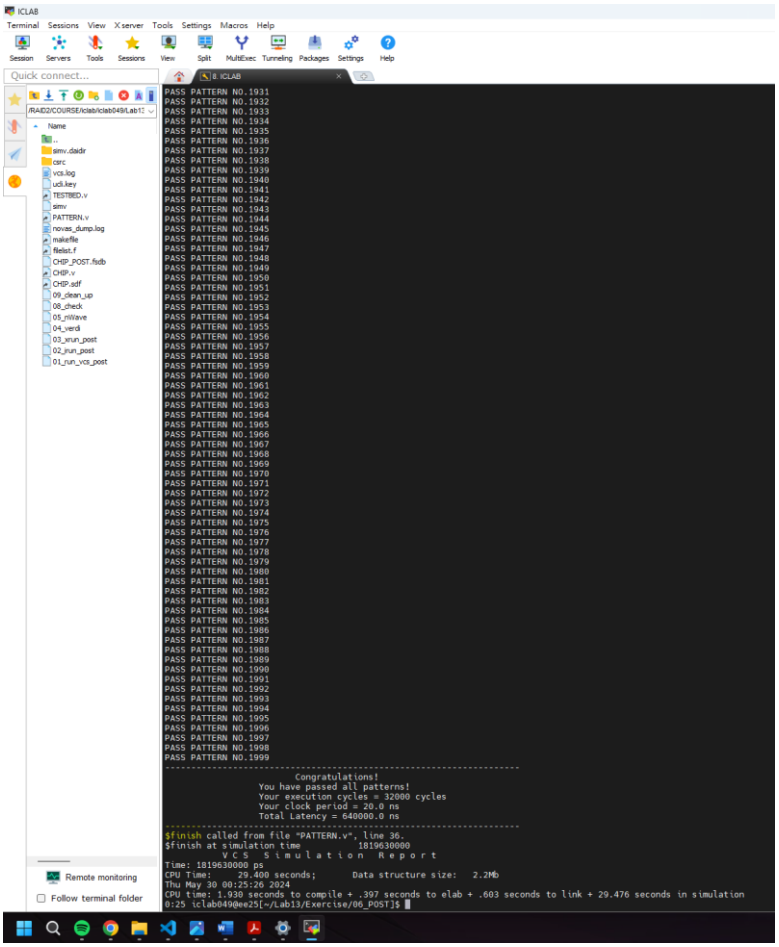
6. DRC result :



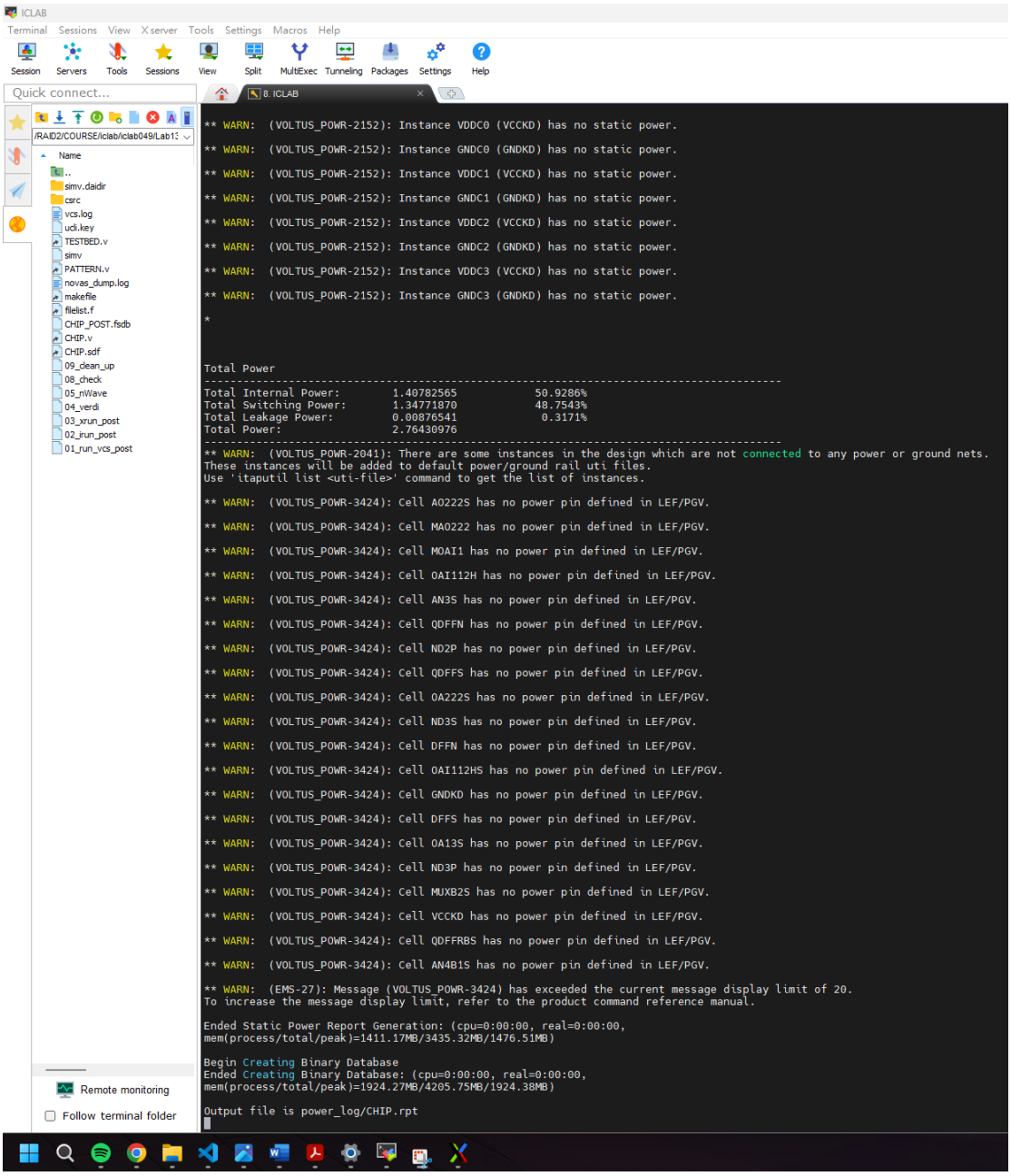
7. LVS result :



8. Post Layout simulation result :



9. Power result :



10. IR Drop Results :

Decrease the utilization to 60%, add a more I/O core power pad (two sets on each side, for a total of 8 sets of power pads), and increase the number of stripes.