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1 4-Bit Adder Subtractor

In this assignment, we had to design a 4-Bit Ripple Carry Adder-Subtractor using Structural Description in VHDL.

1.1 Structural Description

We were given the Full-Adder design as reference. I created an entity encompassing the *Full-Adder* and *XOR Gate* to perform single bit addition or subtraction. 4 such components were cascaded to generate the 4-bit result.

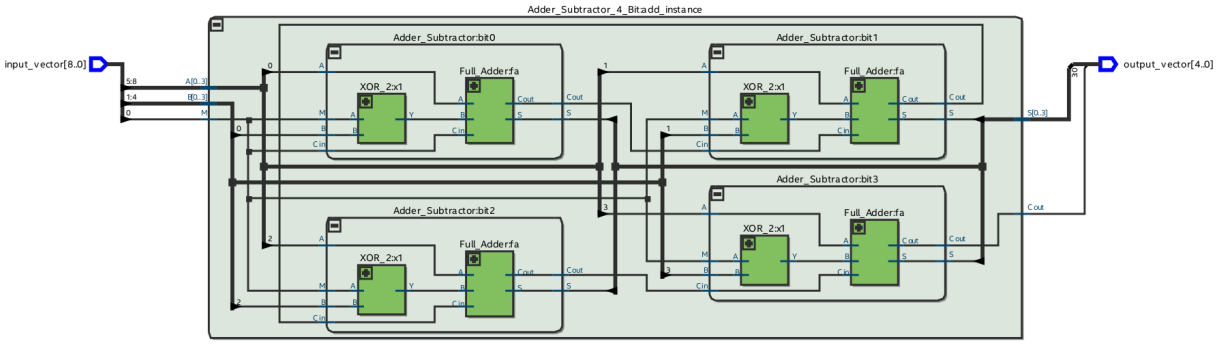

Figure 1: RTL View of Model

1.2 Circuit Functionality

The input signal *M* determines whether the circuit performs addition or subtraction. Each bit of number B is XORed with M. M is also passed as the input carry to the circuit.

1.2.1 Case I: $M = 0$

When M is equal to 0, B is passed to the Full-Adder block since $b \oplus 0 = b$. The input carry to the circuit is 0 which leads to addition.

1.2.2 Case I: $M = 1$

When M is equal to 1, ¬B is copied to the output since $b \oplus 1 = \neg b$. One's complement of B is passed to the Full-Adder Block. The input carry to the circuit is 1 which can be identified as computing the two's complement of B. Addition with two's complement is equivalent to subtraction.

1.3 Simulation

RTL and Gate Level Simulation were performed using *ModelSim*. Due to larger circuit size, I needed to increase the time for the circuit to settle down from 10ns to 20ns between test cases.

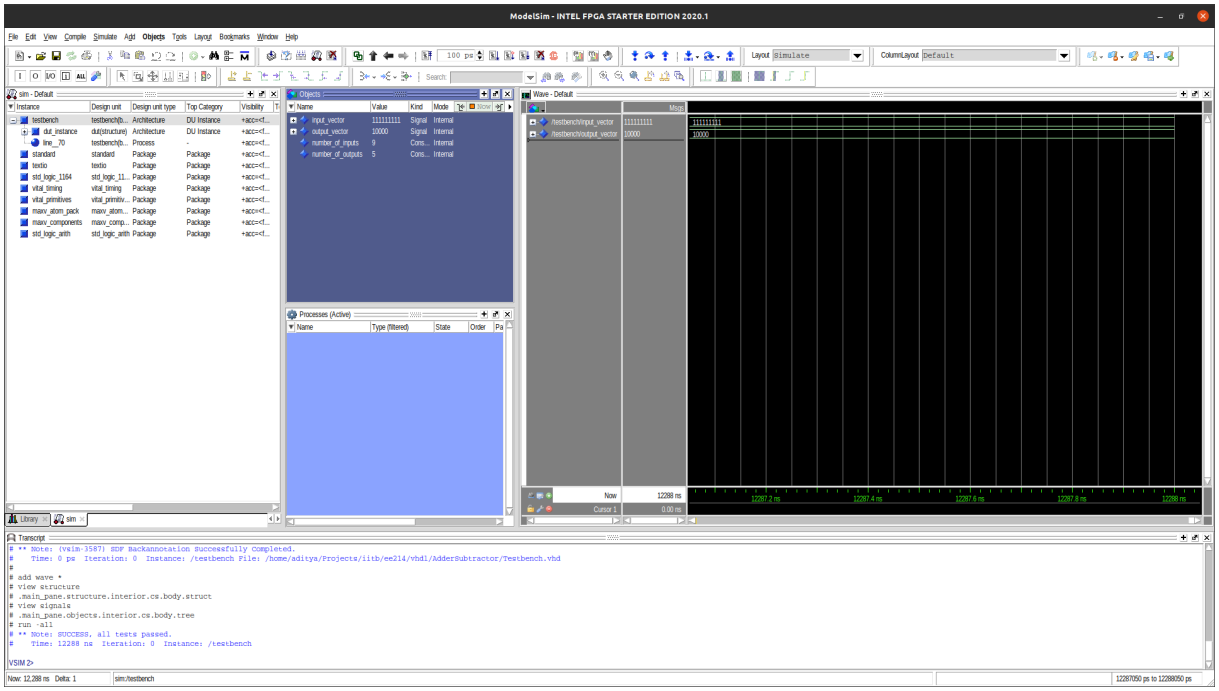

Figure 2: Gate Level Simulation