Test Planning for Honors Design Lab AHB Convolver

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Top Level Design Tests:

Module Tested	Feature Tested	Test Name	Inputs	Outputs
AHB Convolver	Reset	Power On / Reset	Reset	All zeros
AHB Convolver	Coefficient Loading	Coefficient Loading Test	Write to all three coefficient registers, then set coefficient load bit	Modwait is asserted during coefficient loading, then deasserted, and values are properly stored in coefficient register
AHB Convolver	Sample Loading	Sample Loading Test	From idle, write to sample register then set new_sample bit. Repeat two more times to complete initial load.	Modwait asserted during each load, then deasserted and sample_stream asserted to indicate ready for column streaming
AHB Convolver	Streaming / Convolution	Streaming / Convolution Test	From convolve state, repeatedly write new sample and assert new_sample bit. After many convolutions, attempt to read some results.	Alternating between sample_stream and modwait.
AHB Convolver	Sample Loading	New Sample Row Loading Test	From convolve state, assert new_row bit and follow three sample load procedure from before.	Modwait asserted during each load, then deasserted and sample_stream asserted to indicate ready for more column streaming
AHB Convolver	Sample Complete	Sample Complete Test	After max number of convolutions (with new rows at appropriate intervals), read results	Correct result values in sequence

Multiplier/Adder Tree Tests:

Module Tested	Feature Tested	Test Name	Inputs	Outputs
Mult/Add Tree	Multiply/Sum	Zeros	All zeros	All zeros
Mult/Add Tree	Multiply/Sum	Small Coefficients / Small Samples	Small coefficients, small samples	Correct sum of multiplied values
Mult/Add Tree	Multiply/Sum	Small Coefficients / Large Samples	Small coefficients, large samples	Correct sum of multiplied values
Mult/Add Tree	Multiply/Sum	Large Coefficients / Small Samples	Large coefficients, small samples	Correct sum of multiplied values
Mult/Add Tree	Multiply/Sum	Large Coefficients / Large Samples	Large coefficients, large samples	Correct sum of multiplied values
Mult/Add Tree	Multiply/Sum	Max	Max coefficients, max samples	2025
Mult/Add Tree	Result Ready	Result Ready Test	Series of calculations	Result_ready pulsed for 1 clock period 1 clock period after each calculation

Sample Shift Register Tests:

Module Tested	Feature Tested	Test Name	Inputs	Outputs
Sample Shift Register	Reset	Power On / Reset	Reset	Empty Registers (Zeros outputted)
Sample Shift Register	Shift Enable	Enable Test	No enable and various samples	Zero output steady
Sample Shift Register	Input Shifting	Single Sample Shift	Enable and one sample, followed by two zero samples	Correct sequence of values corresponding to single input
Sample Shift Register	Input Shifting	Three sample shift	Enable and three large samples	Correct sequence of values outputted corresponding to sequenced input

Coefficient Register Tests:

Module Tested	Feature Tested	Test Name	Inputs	Outputs
Coefficient Register	Reset	Power On / Reset	Reset	Empty Registers (Zeros outputted)
Coefficient Register	Coefficient Loading	Coefficient Load Enable Test	Sequence of coefficients sent to 0 index register with coeff_ld enabled and disabled	Correct sequence of values based on enable status
Coefficient Register	Coefficient Loading	Coefficient Addressing Test	Coeff_ld and various coefficient values / addresses	Correct sequence of values in corresponding 12 bit regions of output

FIFO Result Shift Register Tests:

Module Tested	Feature Tested	Test Name	Inputs	Outputs
Result FIFO	Reset	Power On / Reset	Reset	Empty Registers (Zeros outputted)
Result FIFO	Write Enable	Wenable Test	Sequence of result_in values and pulsing wenable to ensure correct operation	Correct sequence of values read out
Result FIFO	Read Enable	Renable Test	Write sequence of values first, then read by pulsing renable	Correct sequence of valued read out, after pulsing renable for one clock cycle for each value
Result FIFO	Writing / Reading	Result Writing Test	Long sequence of wenable pulses and result_in values.	Correct sequence of values when read out (FIFO order)
Result FIFO	Full	Write when Full	Write until full, then attempt to write again	Full output, then no response to write attempt
Result FIFO	Empty	Read when Empty	Attempt read after reset	Empty output, then no response to read attempt

Convolver Controller Tests:

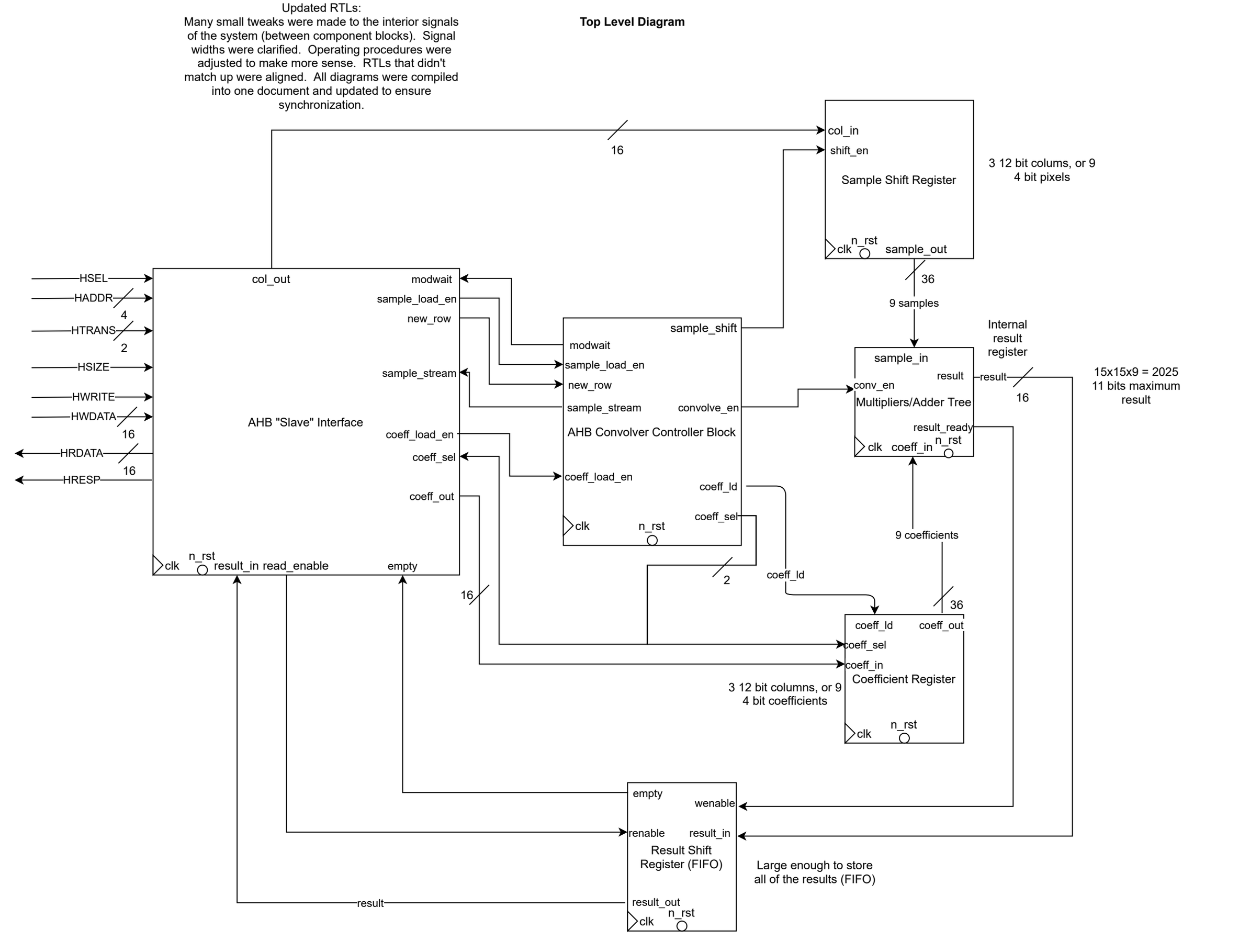
Module Tested	Feature Tested	Test Name	Inputs	Outputs
Controller	Reset	Power On / Reset	Reset	Empty Registers (Zeros outputted)
Controller	Coefficient Loading	Coefficient Load Test	coeff_load_en	Correct sequence of modwait, coeff_ld, and coeff_sel outputs to load all three coefficient columns. Also correct modwait behavior
Controller	Sample Loading	Sample Load Test	From idle, assert sample_load_en and follow procedure for initial sample load	Modwait and sample shift pulsed according to moore state transition diagram
Controller	Sample Streaming and Convolving	Sample Streaming Test	After initial sample loading, input a new sample column and assert sample_load_en repeatedly	Alternation between convolve_en/sample_stream and modwait/sample_shift
Controller	Sample Loading	New Sample Row Test	In convolve state, assert, new_row and follow procedure for initial sample load	Modwait and sample shift pulsed according to moore state transition diagram
Controller	Sample Complete	Sample Complete Test	From convolve state, assert new_row and sample_load_en	Return to idle state (no outputs)

AHB “Slave” Interface Tests:

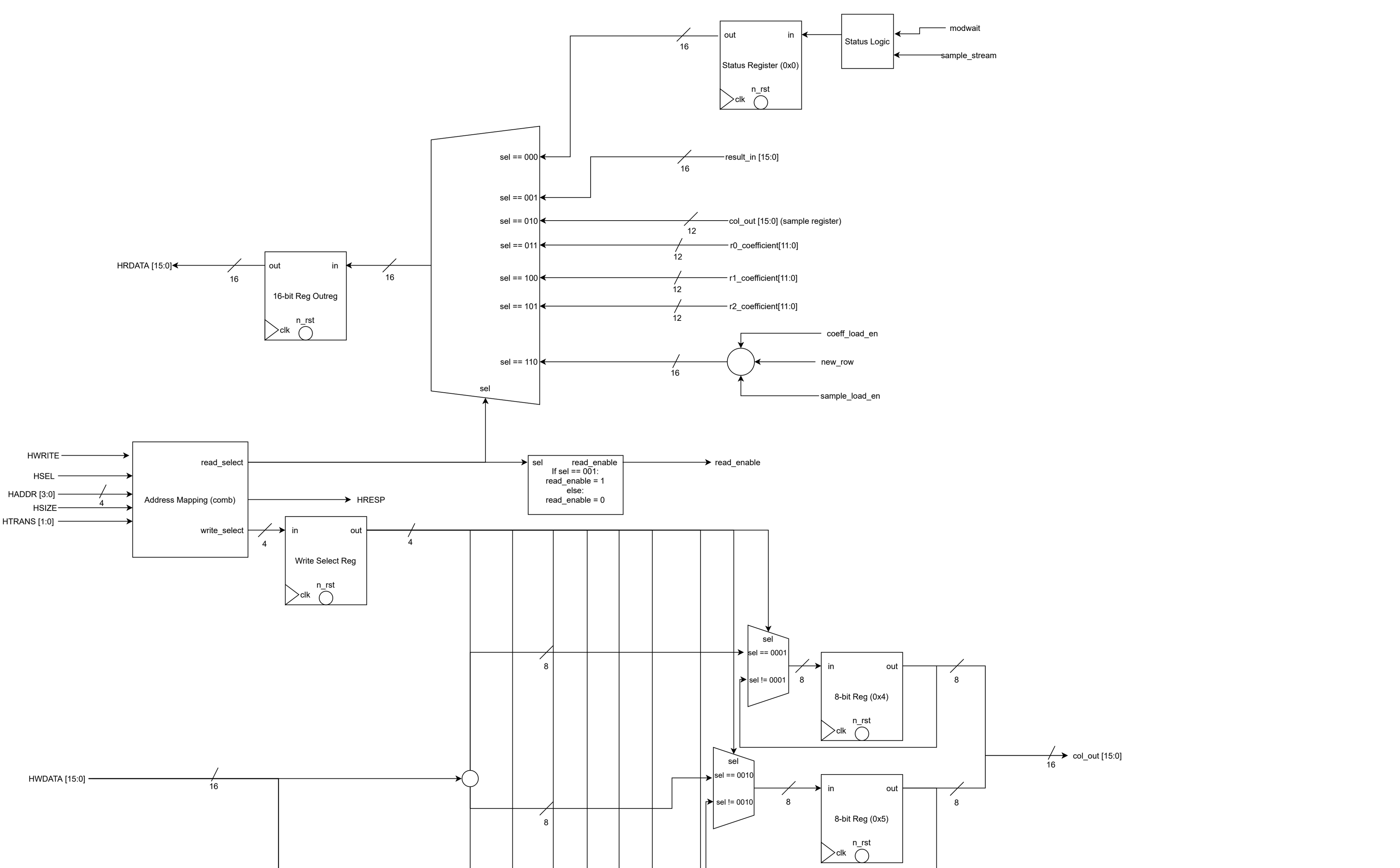
Module Tested	Feature Tested	Test Name	Inputs	Outputs
AHB “Slave”	Reset	Power On / Reset	Reset	Empty Registers (Zeros outputted)
AHB “Slave”	Status Register	Status Write Test	Attempt AHB write of value to status register	Error condition (HRESP)
AHB “Slave”	Status Register	State Read Test	Assert modwait and sample_stream high and low	Correct output from status register on HRDATA (particularly for bits 0 and 8)
AHB “Slave”	FIFO Result Register	FIFO Write Test	Attempt AHB write of value to result register	Error condition (HRESP)
AHB “Slave”	FIFO Result Register	FIFO Read Test	Attempt AHB read of value from result register while asserting a value on result_in	Read_enable followed by the value in result_in being outputted on HRDATA
AHB “Slave”	New Sample Column Register	Sample Write Test	Attempt AHB write to new sample register	Sample value written to register (no output)
AHB “Slave”	New Sample Column Register	Sample Read Test	Attempt AHB read from new sample register	Sample value outputted on HRDATA
AHB “Slave”	Coefficient Column Registers	Coefficient Write Test	Attempt AHB write to all three coefficient registers (separate transactions)	Coefficient Values written to corresponding registers (no output)
AHB “Slave”	Coefficient Column Registers	Coefficient Read Test	Attempt AHB read from all three coefficient registers (separate transactions)	Coefficient values outputted on HRDATA
AHB “Slave”	Command/Control Register	Command Write Test (Load Coefficients)	Attempt AHB write to bit 0, then manipulate coeff_sel	Coeff_load_en is asserted and coeff_out corresponds to coeff_sel input

AHB “Slave”	Command/Control Register	Command Write Test (Load New Column	Attempt AHB write to bit 1	Sample_load_en is asserted
AHB “Slave”	Command/Control Register	Command Write Test (Start New Row)	Attempt AHB write to bit 2	New_row is asserted
AHB “Slave”	Command/Control Register	Command Write Test (Sample Done)	Attempt AHB write to bits 1 and 2	Sample_load_en and new_row are asserted
AHB “Slave”	Command/Control Register	Command Read Test	Attempt AHB read from command /control register	Correct value is outputted on HRDATA

Top Level Diagram

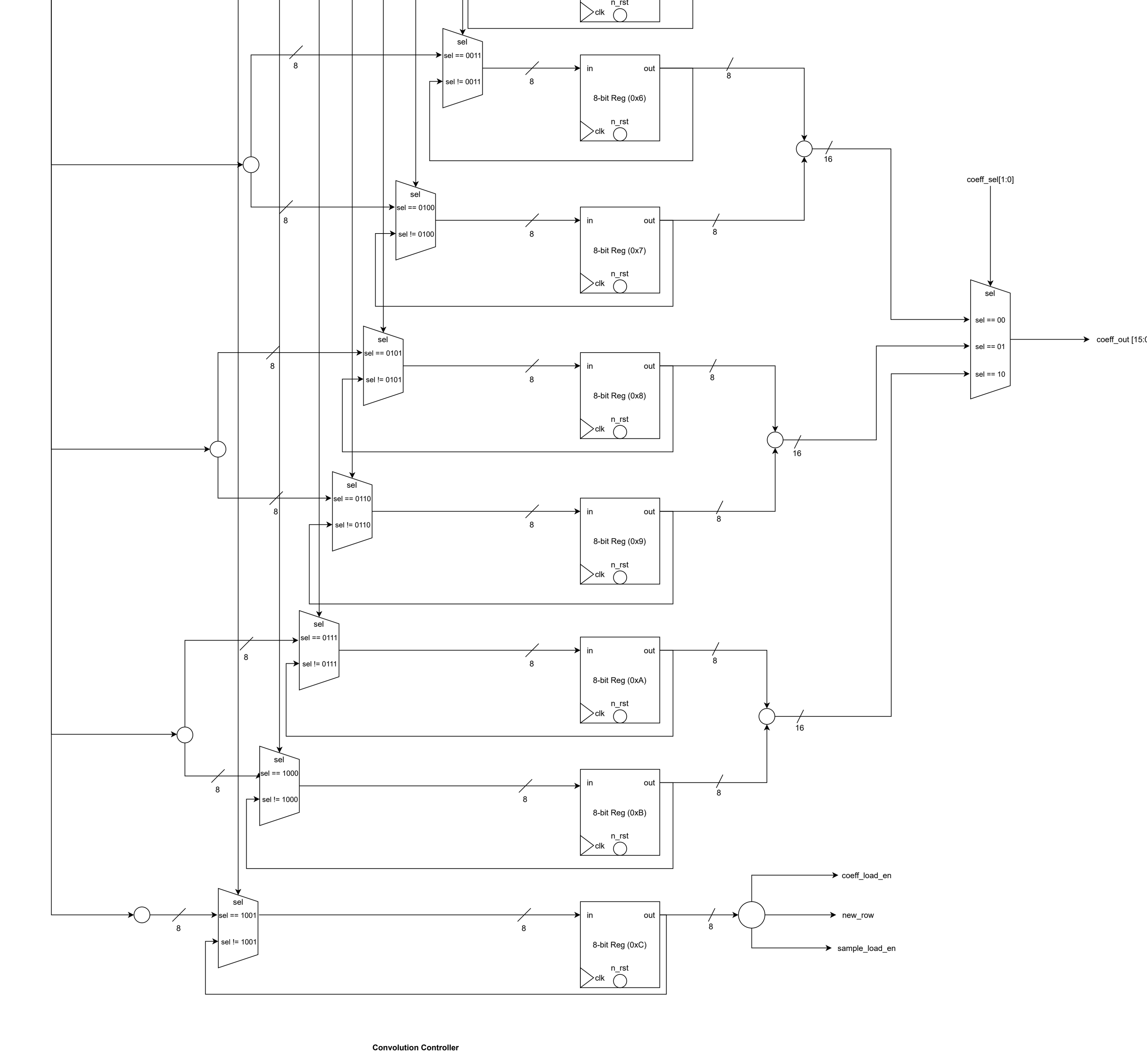


AHB "Slave" Interface

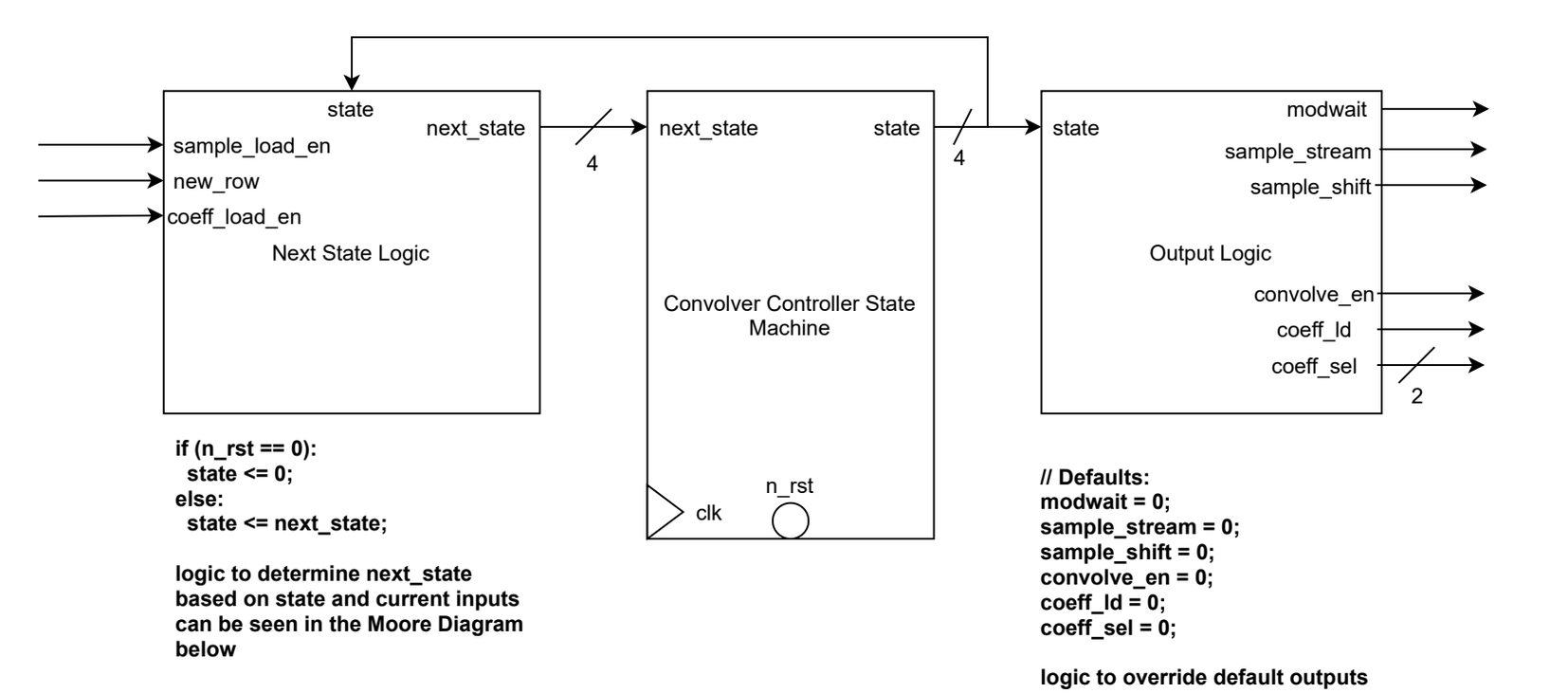


AHB "Slave" Interface Address Mapping

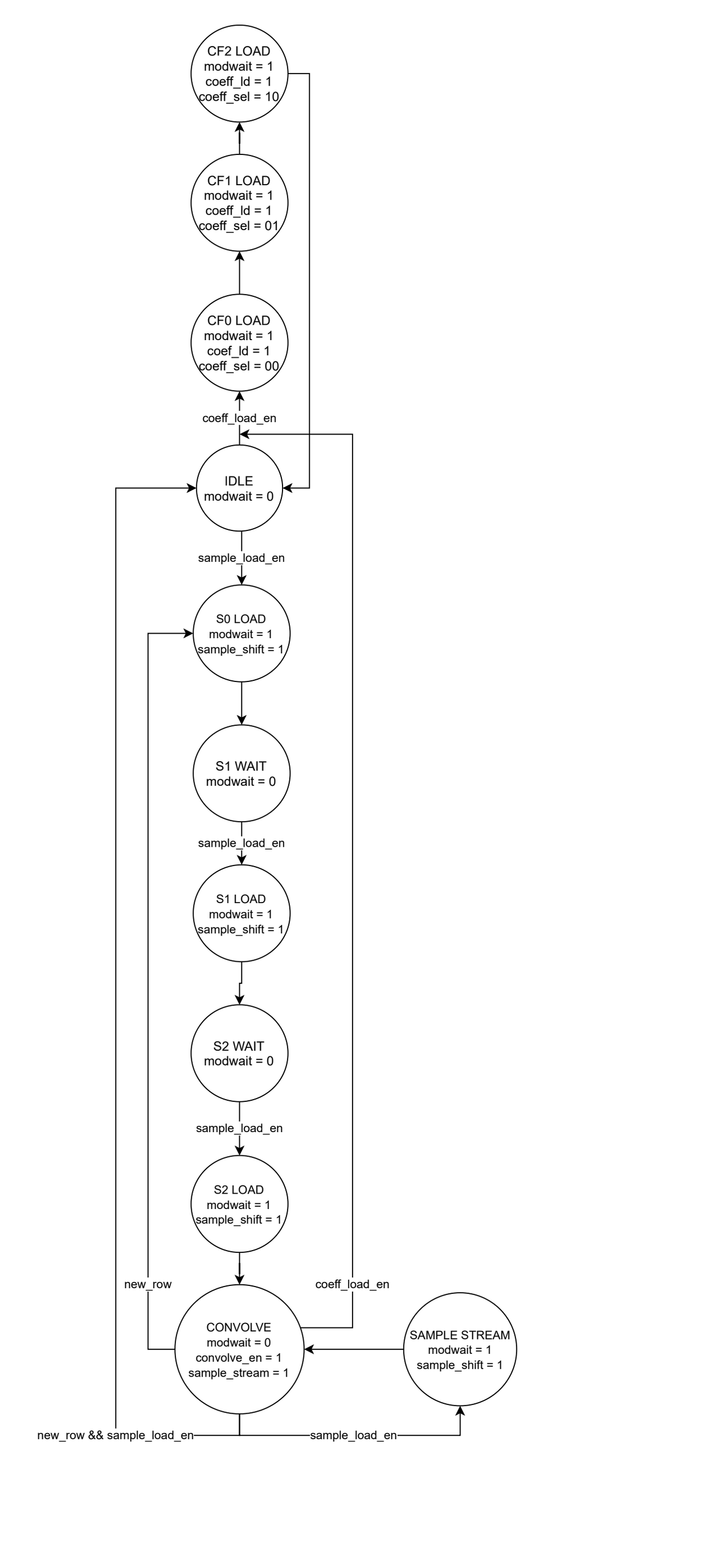
Address	Size (in Bytes)	Read/Write	Description
0x0	2	R	**Status Register:** 0: Convolver is idle 1 for bit 0: Convolver is busy 1 for bit 8: Sample streaming mode active
0x2	2	R	**FIFO Result Register:** Reading from the FIFO Result Register causes shift, so that next read is the next value and so on
0x4	2	R/W	**New Sample Column Register:** Write 12-bit sample column here (3 4-bit pixels)
0x6	2	R/W	**R0 Coefficient Column Register:** Write 1st 12-bit coeff column here (3 4-bit coeffs)
0x8	2	R/W	**R1 Coefficient Column Register:** Write 2nd 12-bit coeff column here (3 4-bit coeffs)
0xA	2	R/W	**R2 Coefficient Column Register:** Write 3rd 12-bit coeff column here (3 4-bit coeffs)
0xC	1	R/W	**Command/Control Register:** 0: Idle 1: Load Coefficients (Set bit 0 to indicate start of new convolution cycle) 2: Load New Column Only (Set bit 1 during column streaming) 4: Start Load New Row (Set bit 2 to load new three column set) 6: Sample Done (Set bits 1 and 2 to indicate end of sample)



Convolution Controller

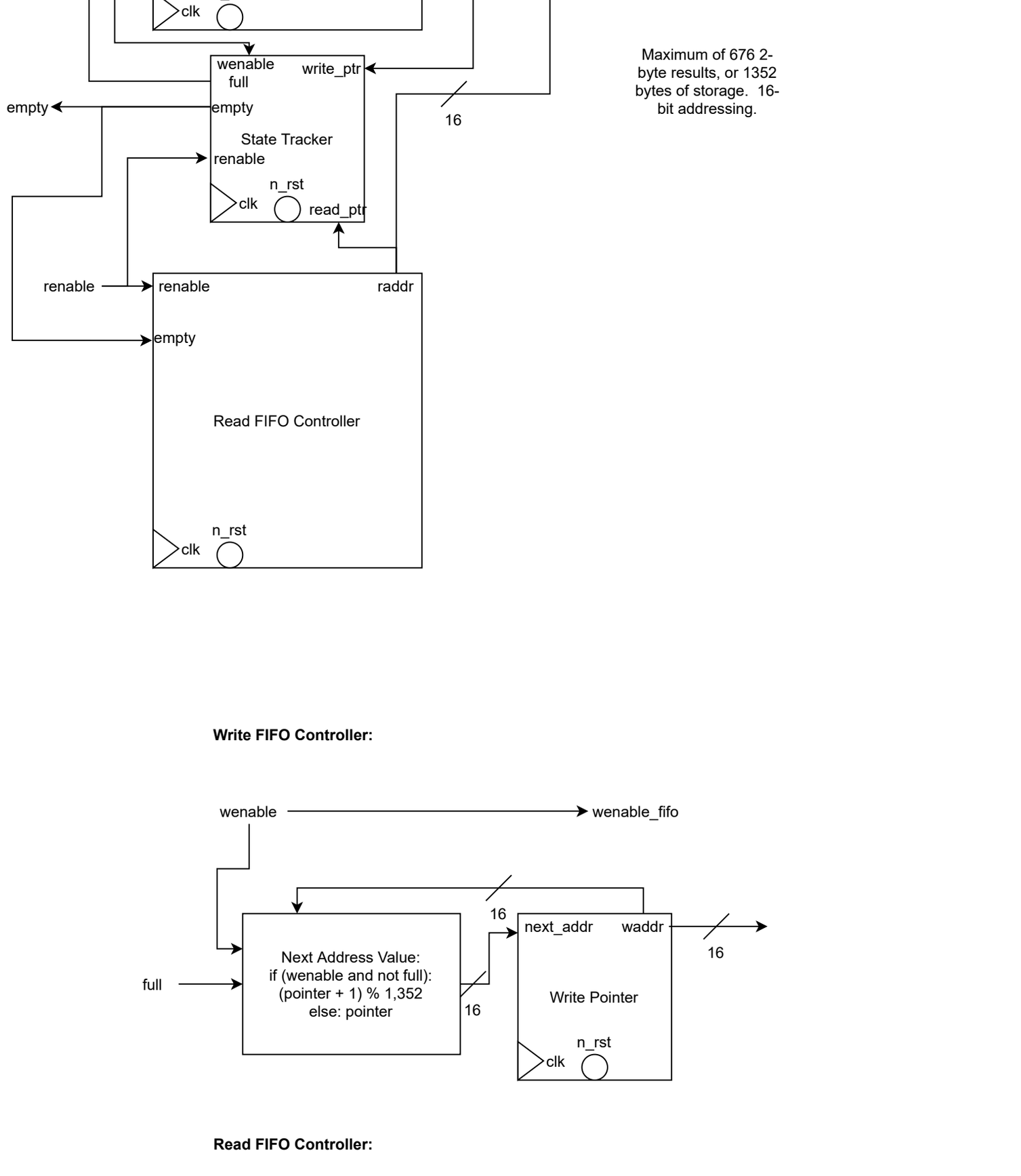


Controller Moore Diagram

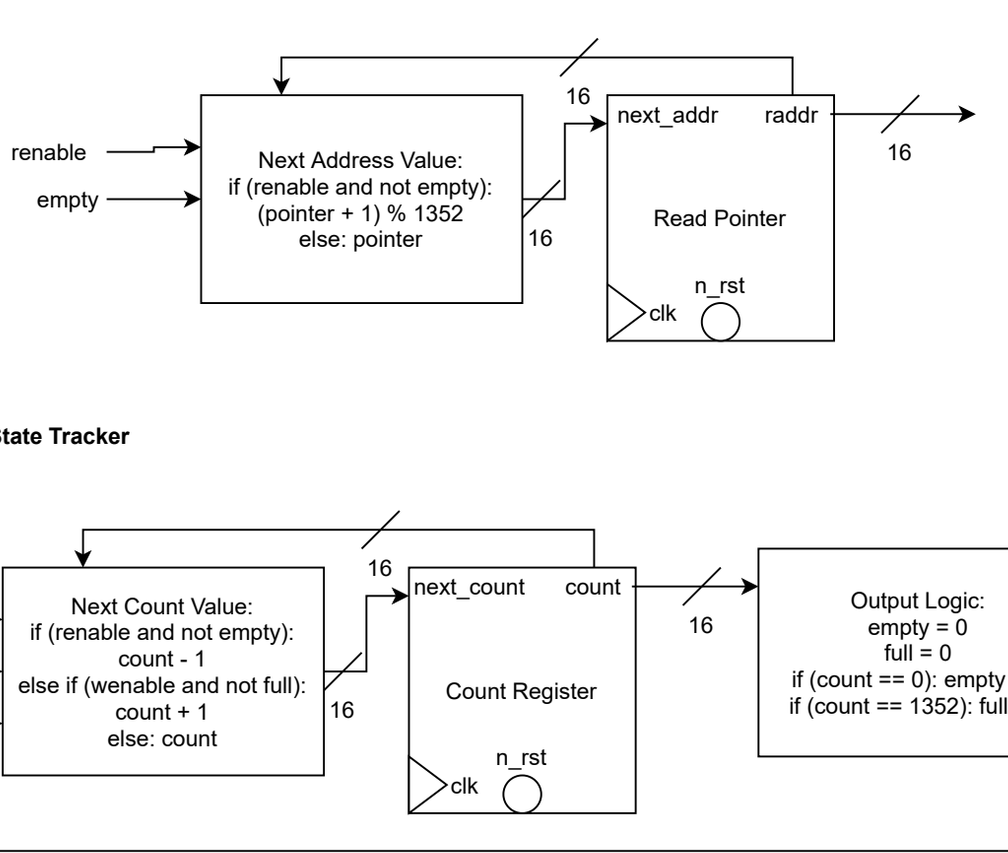


FIFO Result Buffer

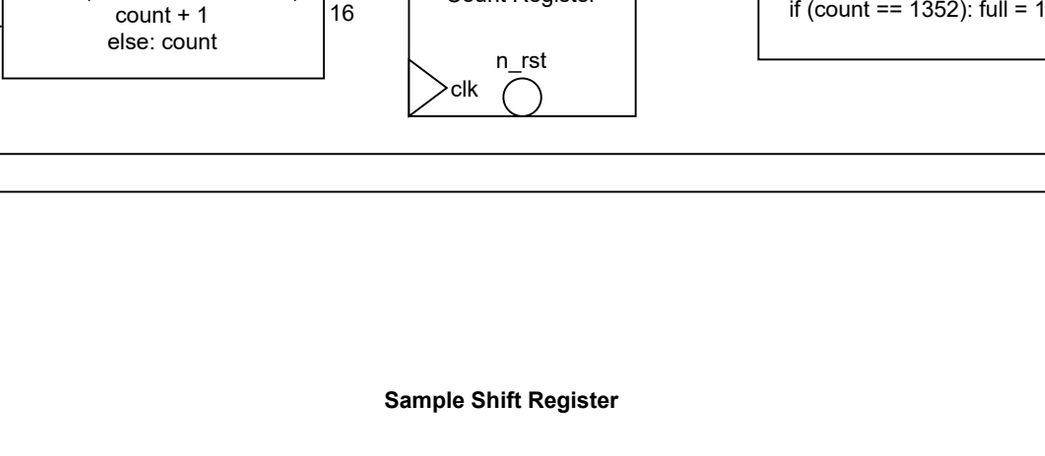
Top Level Diagram



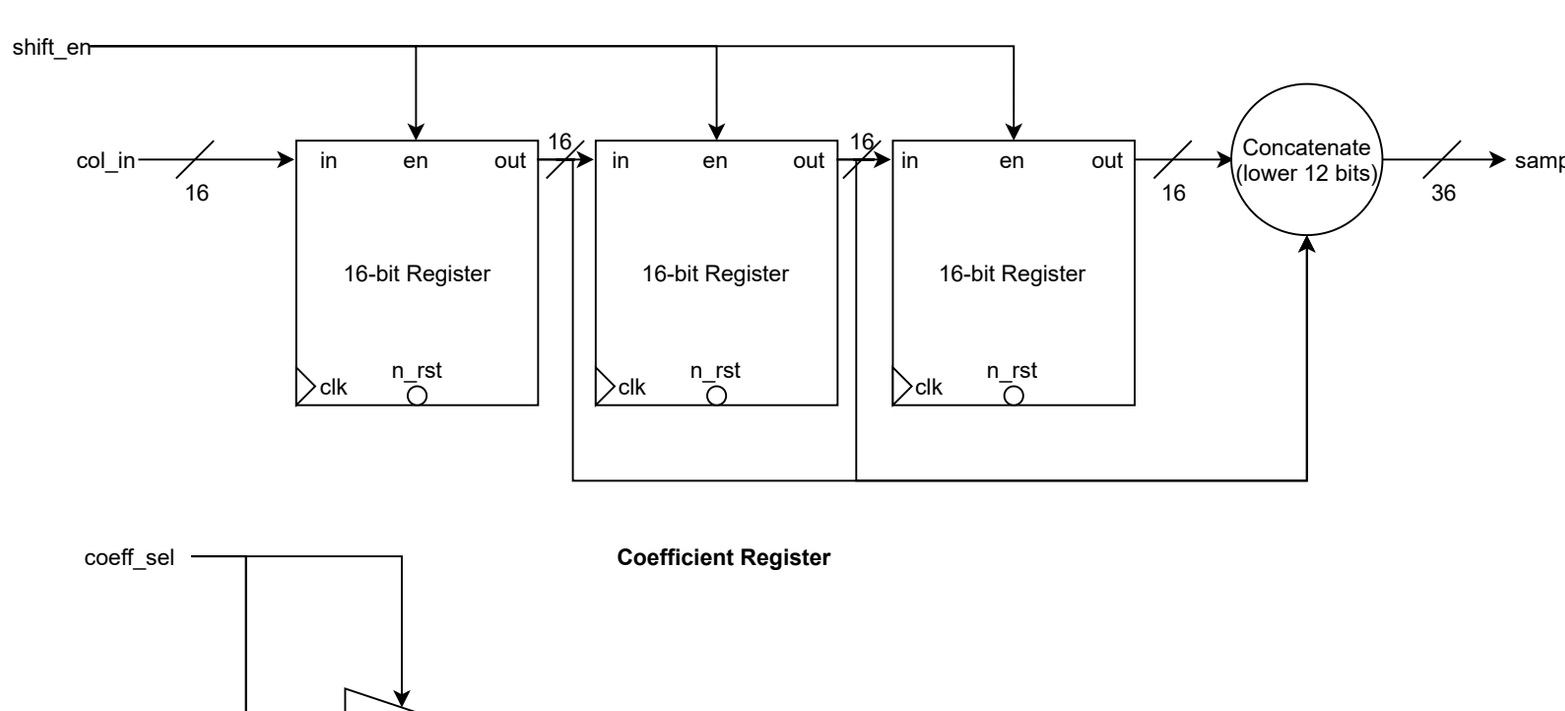
Write FIFO Controller



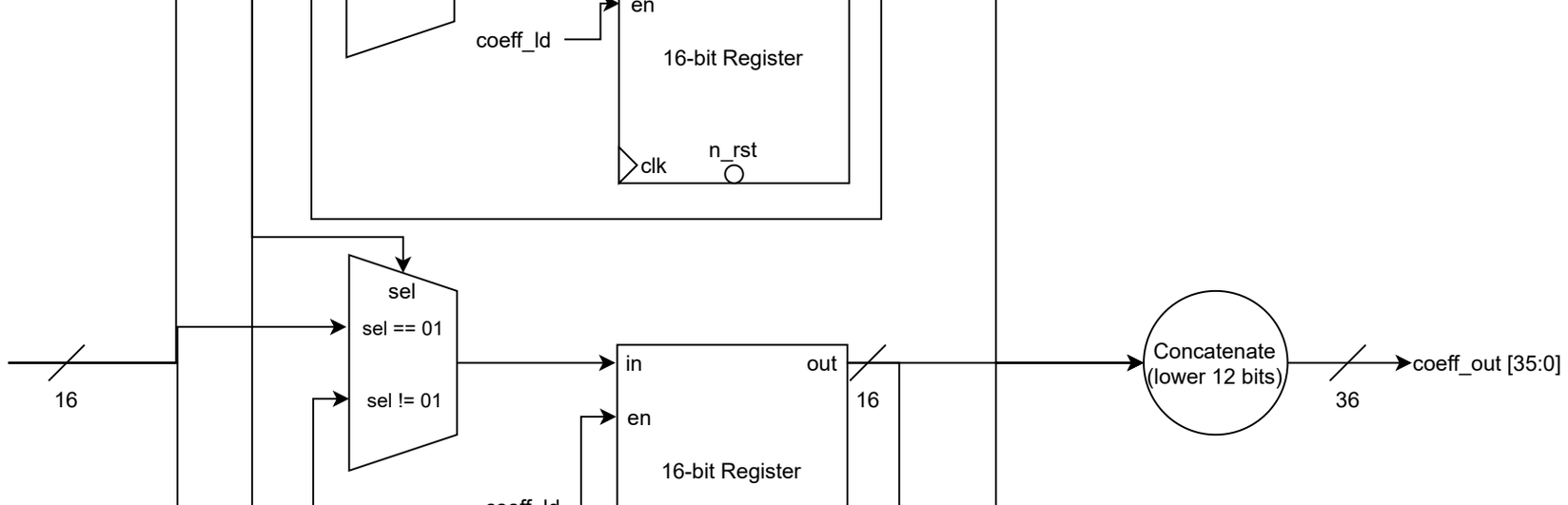
Read FIFO Controller



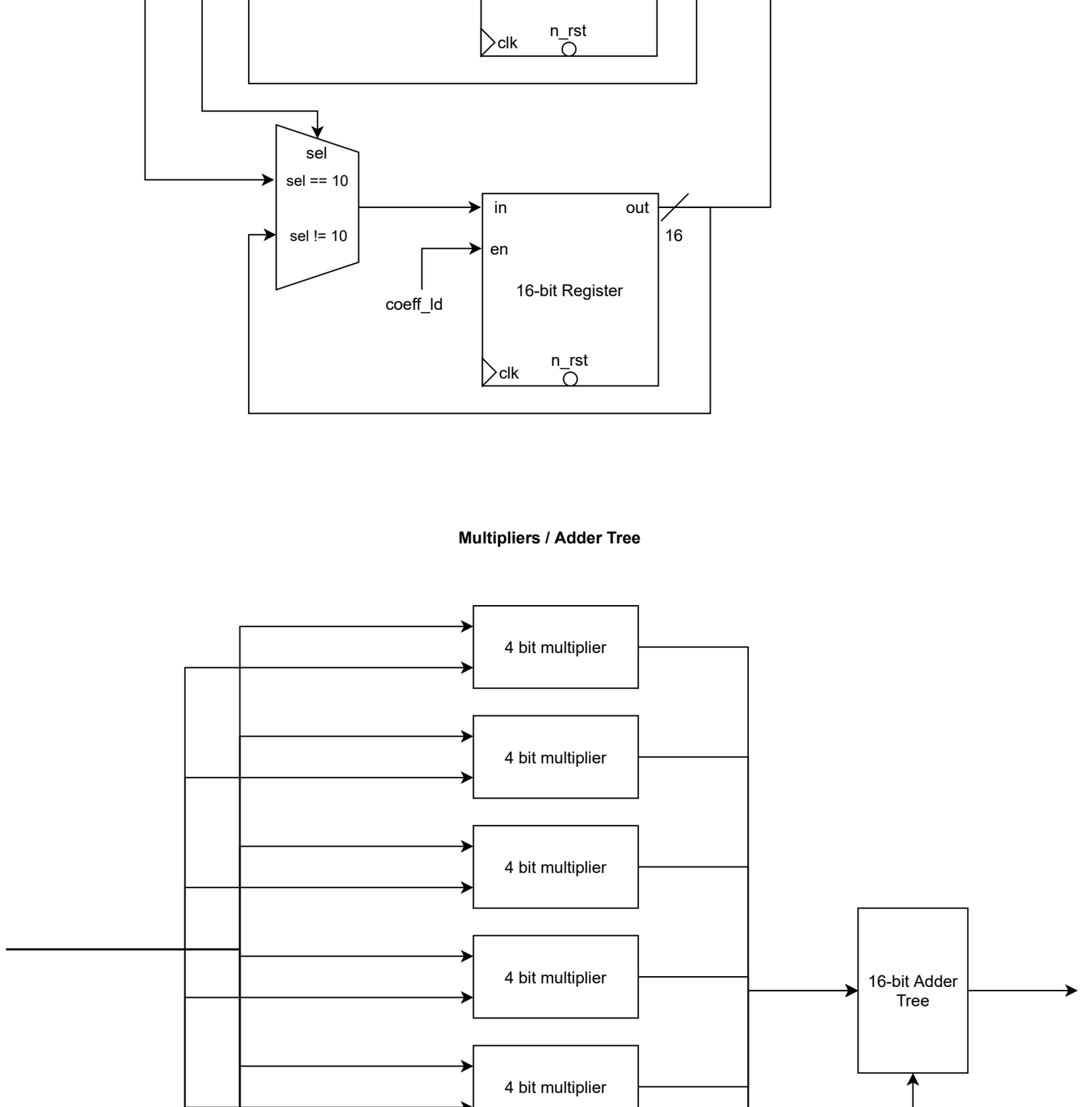
State Tracker



Sample Shift Register



Coefficient Register



Multiplier / Adder Tree