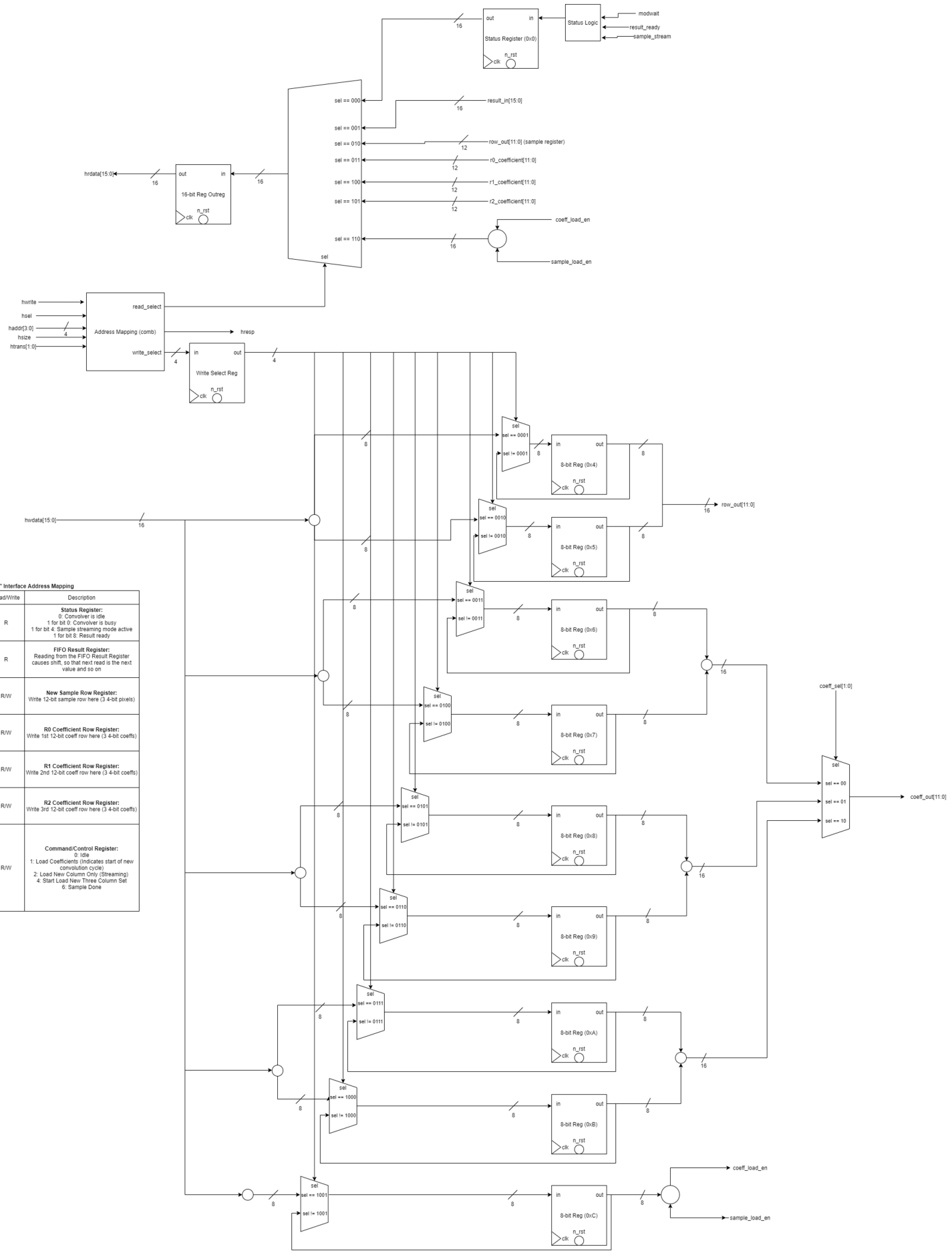
4-12 Design Submission

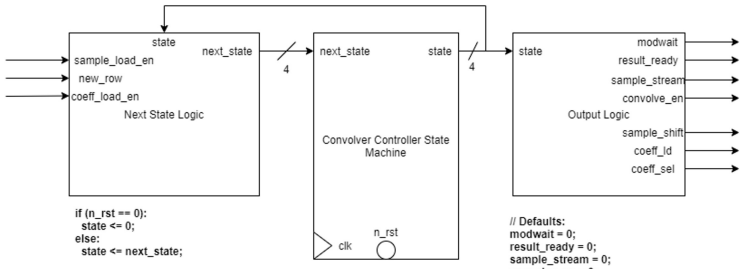
Monday, April 12, 2021 11:02 PM

Disclaimer: This project is a separate CDL conducted under an Honors contract. Please ensure it is graded by Dr. Johnson!



AHB "Slave" Interface Address Mapping

Address	Size (in Bytes)	Read/Write	Description
0x0	2	R	**Status Register:** 0: Convolver is idle 1 for bit 0: Convolver is busy 1 for bit 4: Sample streaming mode active 1 for bit 8: Result ready
0x2	2	R	**FIFO Result Register:** Reading from the FIFO Result Register causes shift, so that next read is the next value and so on
0x4	2	R/W	**New Sample Row Register:** Write 12-bit sample row here (3 4-bit pixels)
0x6	2	R/W	**R0 Coefficient Row Register:** Write 1st 12-bit coeff row here (3 4-bit coeffs)
0x8	2	R/W	**R1 Coefficient Row Register:** Write 2nd 12-bit coeff row here (3 4-bit coeffs)
0xA	2	R/W	**R2 Coefficient Row Register:** Write 3rd 12-bit coeff row here (3 4-bit coeffs)
0xC	1	R/W	**Command/Control Register:** 0: Idle 1: Load Coefficients (Indicates start of new convolution cycle) 2: Load New Column Only (Streaming) 4: Start Load New Three Column Set 6: Sample Done




```
if (n_rst == 0):
  state <= 0;
else:
  state <= next_state;
```

logic to determine next_state based on state and current inputs can be seen in the Moore Diagram below

```
// Defaults:
modwait = 0;
result_ready = 0;
sample_stream = 0;
convolve_en = 0;
sample_shift = 0;
coeff_ld = 0;
coeff_sel = 0;
```

logic to override default outputs based on state can be seen in the Moore Diagram below

Moore Diagram: