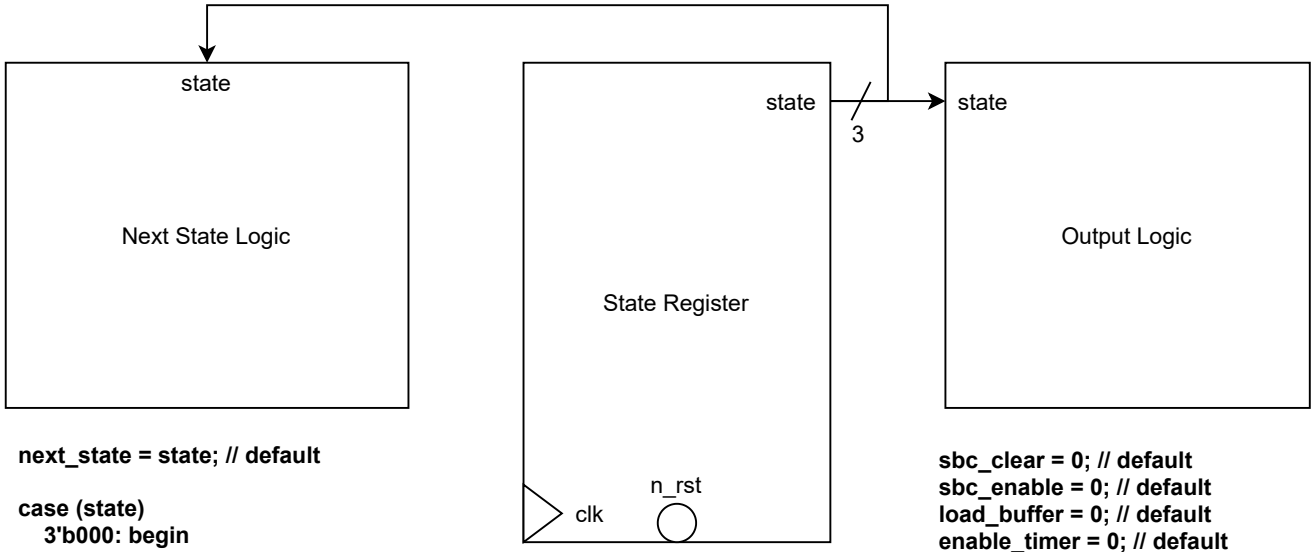


```
next_state = state; // default

case (state)
   3'b000: begin
     if (start_bit_detected == 1)
       next_state = 3'b001;
   end
   3'b001: begin
     next_state == 3'b010;
   end
   3'b010: begin
     if (packet_done == 1)
       next_state = 3'b011;
   end
   3'b011: begin
     if (if framing_error == 1)
       next_state = 3'b000;
     else
       next_state = 3'b100;
   end
   3'b100: begin
     next_state = 3'b00;
   end
 endcase
```

```
sbc_clear = 0; // default
sbc_enable = 0; // default
load_buffer = 0; // default
enable_timer = 0; // default

case (state)
   3'b001: begin
     sbc_clear = 1;
     enable_timer = 1;
   end
   3'b010: begin
     enable_timer = 1;
   end
   3'b011: begin
     sbc_enable = 1;
   end
   3'b100: begin
     load_buffer = 1;
   end
 endcase
```