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CSE 122: HW 5 Report

Characterizing the FF:

1. The ideal clock-to-q time with plenty of setup/hold time is **0.18135 ns.**
2. The shortest hold time was found while the clock-to-q time was at .199462 which is 9.98% more than the ideal. This hold time is **11.5ps**
3. The shortest setup time was found while the clock-to-q time was at .199446 which is 9.97% more than the ideal. This hold time is **41.1ps**

SRAM Cell:

1. To maximize the read SNM the sizes of the transistors are as follows:
   Access Nmos Transistor: **0.36µm**
   Inverter Nmos Transistor: **0.42µm**
   Inverter Pmos Transistor: **0.42µm**
   The corner case that maximized the SNM was the '**ss**' corner case.
   After testing with the hvt pmos transistors I gathered data which showed a smaller SNM than what I found with the regular pmos transistors.

SNM with HVT Pmos Transistor and Process Corner: ss			
inv_pmos(µm)	inv_nmos(µm)	access_nmos(µm)	SNM(V)
0.42	0.36	0.42	0.76
0.42	0.42	0.64	0.735

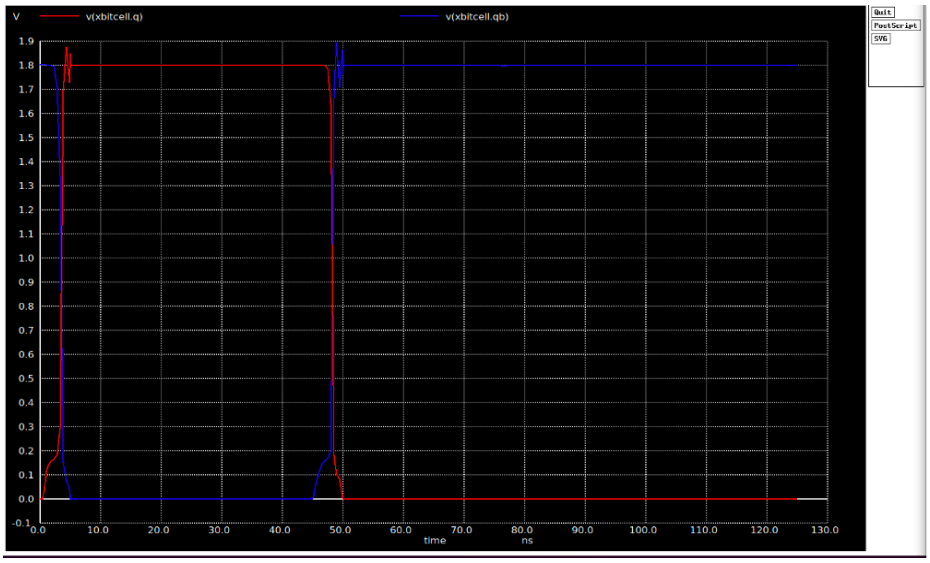
   This maximum SNM was found to be: **0.772V**
2. The Read SNM was tested at every process corner to find the best and worst Read SNM. The '**sf'** process corner gave the worst Read SNM.

Read SNM for different Process Corners	
Process Corner	SNM(V)
tt	0.718
ff	0.672
ss	0.753
fs	0.736
sf	**0.624**

3. The Hold SNM was tested at every process corner to find the best and worst Hold SNM. The **'sf'** process corner gate the worst Hold SNM.

Hold SNM for different Process Corners	
Process Corner	SNM(V)
tt	0.718
ff	0.672
ss	0.753
fs	0.736
sf	**0.624**

4. The cell **was** able to be written and is shown here in the transient analysis.



5. The bitcell width, length, and area is shown here:

```
% box
Root cell box:
          width x height  (   llx,  lly  ), (   urx,  ury  )  area (units^2)

microns:    2.12 x 3.40    ( -0.30, -3.12 ), (  1.82,  0.29 )  7.22
lambda:   212.00 x 340.50  (-30.00, -311.50), ( 182.00,  29.00)  72186.00
internal:    424 x 681     (   -60, -623  ), (   364,  58   )  288744
%
```

6. The 3x3 array width, length, and area (including taps) is shown here:

```
Root cell box:
          width x height  (   llx,  lly  ), (   urx,  ury  )  area (units^2)

microns:    6.82 x 10.22   (  0.00, -6.81 ), (  6.82,  3.40 )  69.67
lambda:   682.00 x 1021.50  (  0.00, -681.00), ( 682.00,  340.50)  696663.00
internal:   1364 x 2043    (     0, -1362 ), (  1364,  681  )  2786652
```

My Design:

For my design I tested various transistor sizes to find one with a high SNM, relatively small area, and good sizing for implementation. Here is the data I collected for the decision process. The transistor sizes I decided on is highlighted.

SNM with Regular Pmos Transistor and Process Corner: tt			
inv_pmos(µm)	inv_nmos(µm)	access_nmos(µm)	SNM(V)
0.42	0.36	0.42	0.727
0.42	**0.42**	**0.64**	**0.718**
0.42	0.54	0.61	0.709
0.42	0.54	0.61	0.708
0.42	0.54	0.64	0.718
0.64	0.42	0.64	0.709
0.64	0.42	0.84	0.704
0.84	0.54	0.84	0.699
0.58	0.84	1.26	0.696

Once my transistor sizes were set I went ahead and started building my SRAM bitcell based on a design from openRAM. As I went about placing elements, I minimized spacing between them as best I could. Once I completed my bitcell, I moved onto the tap cells which I based my design off the standard tap cells in the skywater 130 library. This is where I ran into a problem when routing my GND node to the tap cell. I solved this problem by routing all the GND nodes in my bitcells using a horizontal m2 layer. Once I finished, the 3x3 array was simple to

construct. If I did this assignment again, I would explore more compact designs like having the WL on poly and a strap cell, or strictly horizontal transistors.