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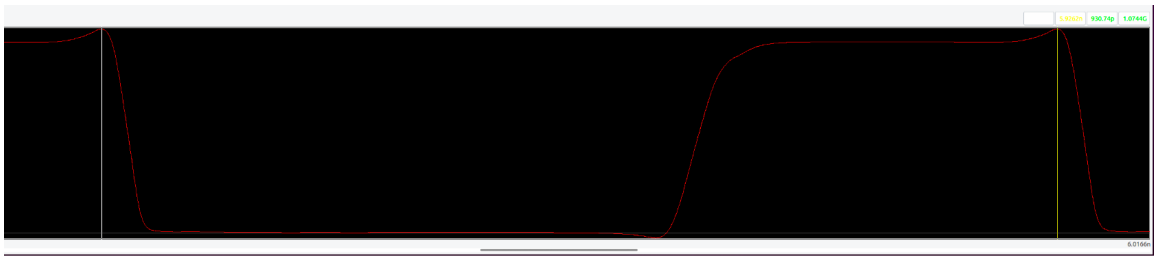
Feb 24, 2022

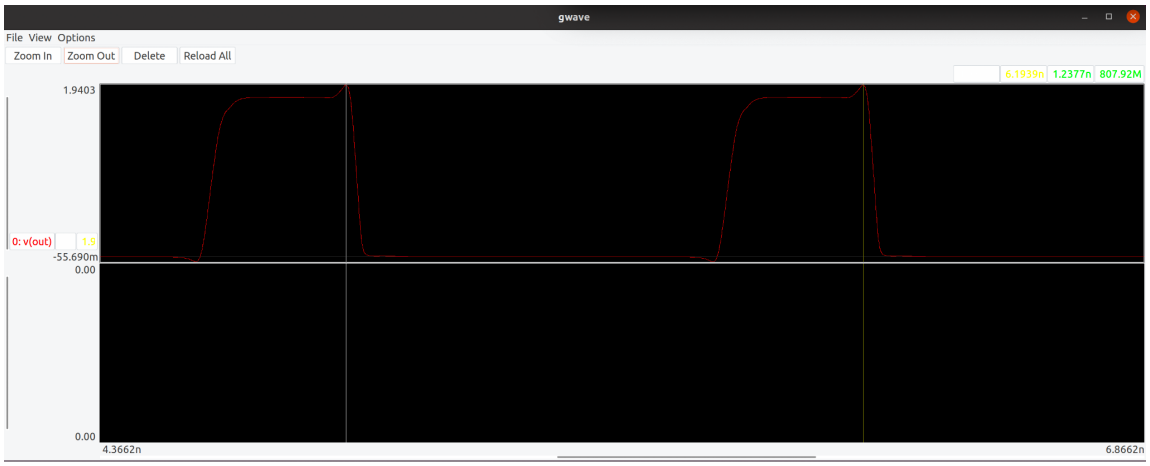
CSE 122: HW 4 Report

1. The period from the ngspice simulation with no paracitics = 930.74ps meaning the **frequency = 1.07GHz**

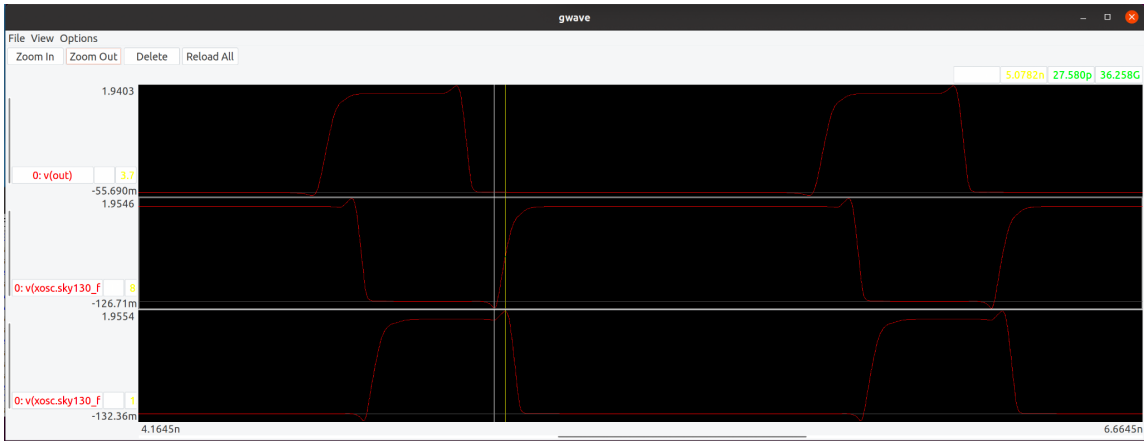


2. The stage delay of one inverter without parasitics was measured from inv_1_4/a to inv_1_5/a a. **Stage delay = 26.55ps**

3. The period from the ngspice simulation with paracitics = 1.237ns meaning the **frequency = .808GHz**



4. The stage delay of one inverter with parasitics was measured from inv_1_4/a to inv_1_5/a a. **Stage delay = 27.58ps**



5. The frequency of the ring oscillator did vary with the process corners.

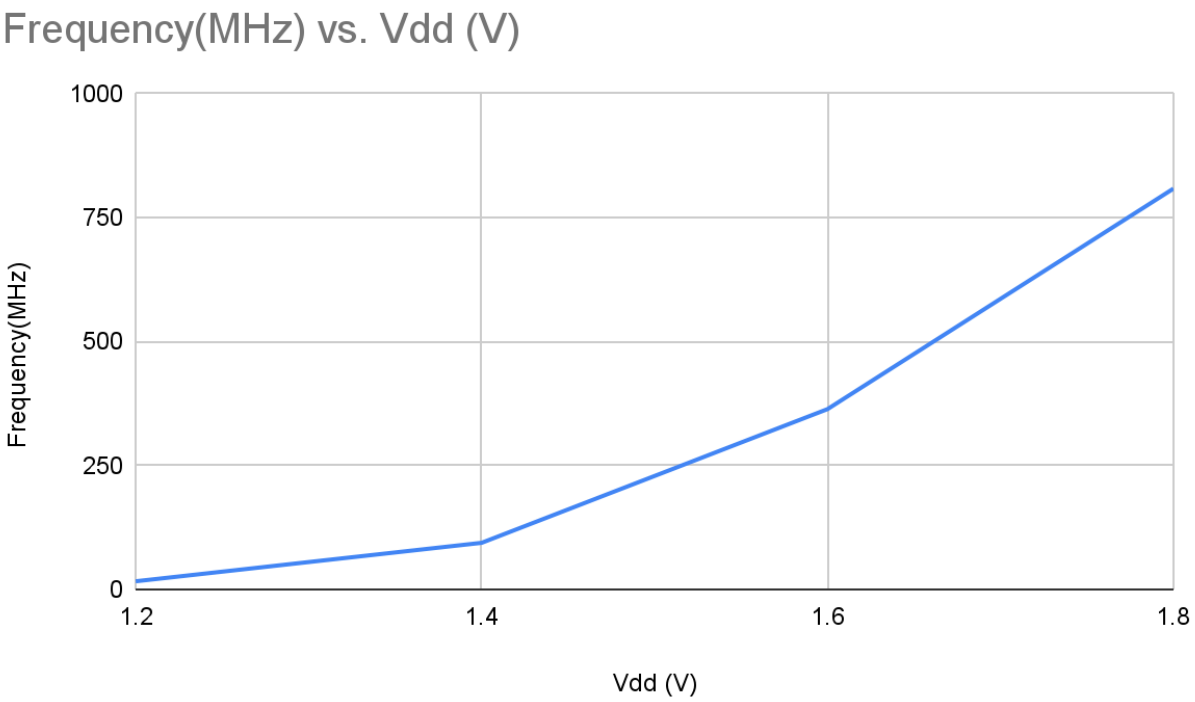
Process Corner	Period(ns)	Frequency (GHz)
tt	1.237	0.8084074373
ss	3.804	0.2628811777
fs	1.083	0.9233610342
ff	0.666	1.501501502

6. The signal slew of the NAND2 output did vary with different process corners.

Process Corner	Transition	Slew Rate (ps)
tt	Low -> High	51.3
ss	Low -> High	80.5
fs	Low -> High	40
ff	Low -> High	38.2
tt	High -> Low	23.4
ss	High -> Low	32.6
fs	High -> Low	29.3
ff	High -> Low	19.3

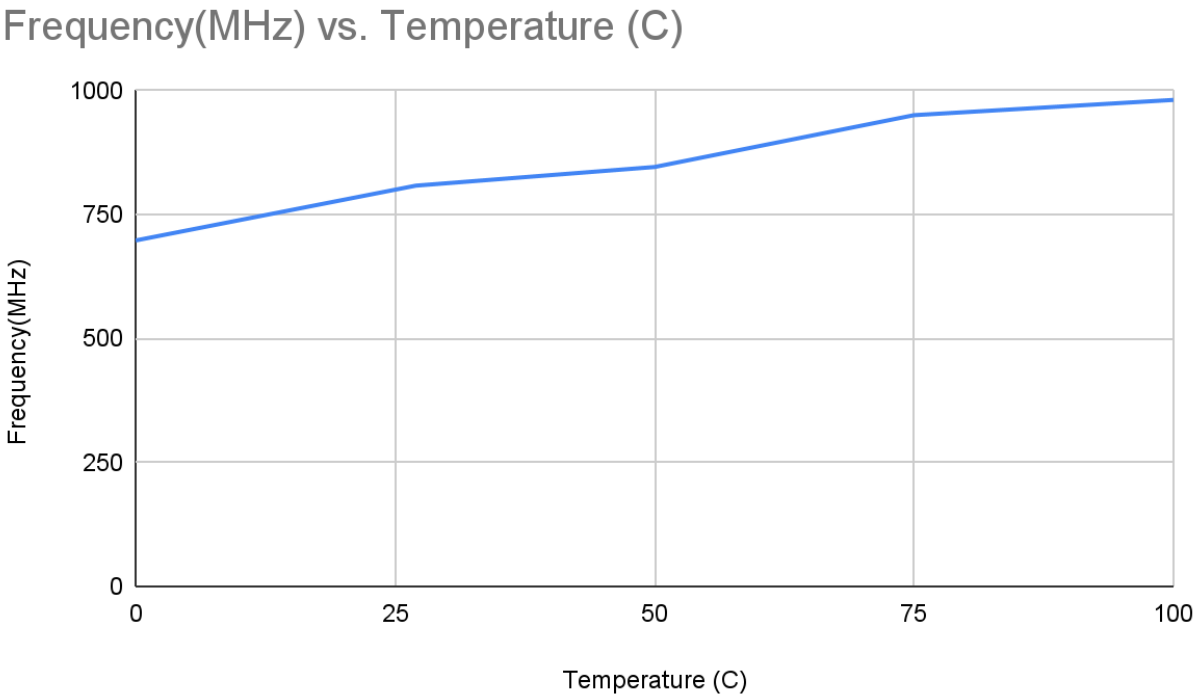
7. The ring oscillator frequency drops rapidly as Vdd decreases from 1.8. It seems to go towards zero as Vdd approaches 1V.

VDD vs. Frequency		
Vdd (V)	Frequency(MHz)	Period(ns)
1.8	808.4074373	1.237
1.6	363.6363636	2.75
1.4	93.89671362	10.65
1.2	16.34253963	61.19



8. The ring oscillator frequency increased as the temperature increased.

Temperature vs. Frequency		
Temperature (C)	Frequency(MHz)	Period (ns)
0	697.8367062	1.433
27	808.4074373	1.237
50	846.0236887	1.182
75	950.5703422	1.052
100	981.3542689	1.019



9. PDF attached at the end.
10. PDF attached at the end.

11. The calculated logical effort estimate which was computed on problem #9 was

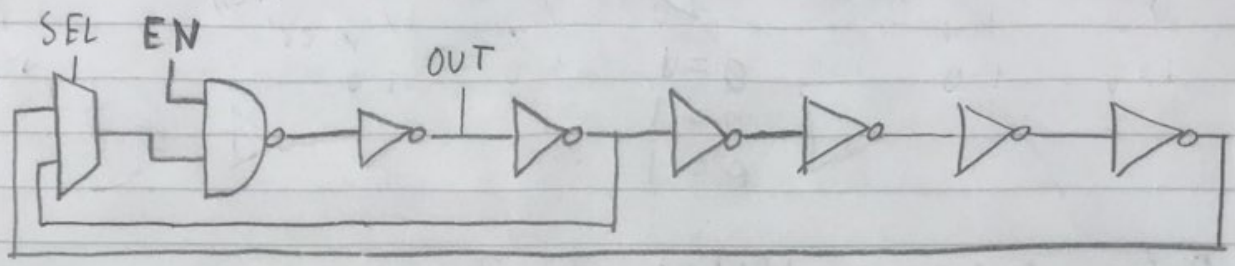
    Frequency = 4.6875GHz

    The actual estimate from ng spice (with parasitics) was

    Frequency = .808GHz

    The calculated estimate frequency and the actual estimate frequency was off by a **factor of 5.801**

9. Logical Effort:



$g=2$	$g=4/3$	$g=1$	$g=1$	$g=1$	$g=1$	$g=1$	$g=1$
$h=4/6$	$h=3/4$	$h=1$	$h=1$	$h=1$	$h=1$	$h=1$	$h=6/3$
$p=4$	$p=2$	$p=1$	$p=1$	$p=1$	$p=1$	$p=1$	$p=1$

$$D_{rel} = \left(2\left(\tfrac{4}{6}\right)+4\right) + \left(\tfrac{4}{3}\left(\tfrac{3}{4}\right)+2\right) + \left(1(1)+1\right)(5) + \left(1\left(\tfrac{6}{3}\right)+1\right)$$

$$D_{rel} = \tfrac{4}{3} + 4 + 3 + 10 + 3$$

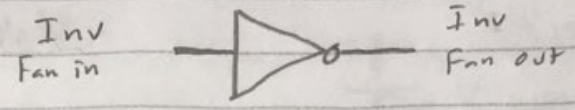
$$D_{rel} = 21.\overline{3}$$

$$D_{abs} = D_{rel} \cdot \tau \rightarrow D_{abs} = 21.\overline{3} \cdot 5ps \approx 106.67ps$$

$$\text{Frequency} = \frac{1}{2 \cdot D_{abs}} \approx \boxed{4.6875\,GHz}$$

Assumptions:
- $\tau_{130} = 5ps$
- Branch Effort <u>not</u> accounted for
- Oscillator travels through <u>all</u> gates

10.



$g = 1$
$h = 1$
$p = 1$

$$D_{rel} = g^h + p = 1(1) + 1 = 2$$

$$D_{abs} = D_{rel} \cdot \tau = 2 \cdot 5ps = \boxed{10ps}$$

Estimate Inverter stage Delay : 10 ps
ngspice Inverter stage Delay : 27.58ps

Simulation vs. Estimate off by a factor of 2.758

Assumptions :

- Fan in and Fan out of Inverter is only another Inverter
- $\tau = 5ps$
- Parasitic Delay is accounted for in both Simulation and Estimate.