SBS 1.1-COMPLIANT GAS GAUGE and PROTECTION with CEDV

Check for Samples: bq3060

FEATURES

- Advanced CEDV (Compensated End-of-Discharge Voltage) Gauging
- Fully Integrated 2, 3, and 4 Series Li-Ion or Li-Polymer Cell Battery Pack Manager
- 8-Bit RISC CPU With Ultra-Low Power Modes
- Full Array of Programmable Protection Features
  - Voltage, Current, and Temperature
- SHA-1 Authentication
- Flexible Memory Architecture With Integrated Flash Memory
- Supports Two-Wire SMBus v1.1 Interface With High-speed 400kHz Programming Option
- P-CH High Side Protection FET Drive
- Low Power Consumption Sleep Mode: < 69 µA
- High-Accuracy Analog Front End With Two Independent ADCs
  - High-Resolution, 15~22-bit Integrator for Coulomb Counting
  - 16-Bit Delta-Sigma ADC With a 16-Channel Multiplexer for Voltage, Current, and Temperature
- Ultra Compact Package: 24-Pin TSSOP PW

APPLICATIONS

- Netbook/Notebook PCs
- Medical and Test Equipment
- Portable Instruments

DESCRIPTION

The Texas Instruments bq3060 Battery Manager is a fully integrated, single-chip, pack-based solution that provides a rich array of features for gas gauging, protection, and authentication for 2, 3, or 4 series cell Li-Ion battery packs. With a footprint of merely 7.8mmx6.4mm in a compact 24-pin TSSOP package, the bq3060 maximizes functionality and safety while dramatically cutting the solution cost and size for smart batteries.

Using its integrated high-performance analog peripherals, the bq3060 measures and maintains an accurate record of available capacity, voltage, current, temperature, and other critical parameters in Li-Ion or Li-Polymer batteries, and reports the information to the system host controller over an SMBus 1.1 compatible interface.

The bq3060 provides software-1st level and 2nd level safety protection on overvoltage, undervoltage, overtemperature, and overcharge, as well as hardware-overcurrent in discharge, short circuit in charge and discharge protection.

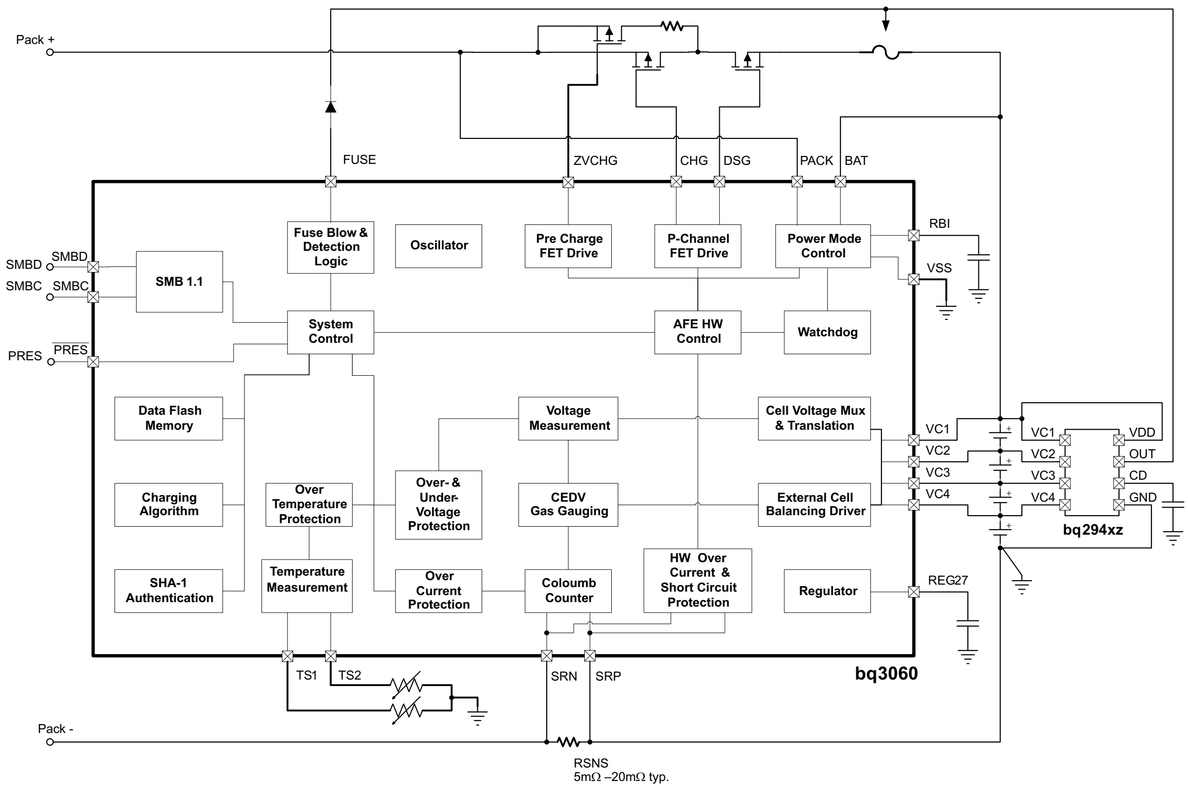
Table 1. ORDERING INFORMATION

AVAILABLE OPTIONS	PACKAGE TSSOP (PW)
Standard	bq3060PW(1)

(1) The bq3060 can be ordered in tape and reel by adding the suffix R to the orderable part number, i.e., bq3060PWR.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SYSTEM PARTITIONING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)[1]

			VALUE	UNIT
V_{MAX}	Supply voltage range	PACK w.r.t. Vss	–0.3 to 34	V
V_{IN}	Input voltage range	VC1, BAT	V_{VC2}–0.3 to V_{VC2}+8.5 or 34, whichever is lower	V
		VC2	V_{VC3}–0.3 to V_{VC3}+8.5	V
		VC3	V_{VC4}–0.3 to V_{VC4}+8.5	V
		VC4	V_{SRP}–0.3 to V_{SRP}+8.5	V
		SRP, SRN	–0.3 to V_{REG27}	V
		SMBD, SMBC	–0.3 to 6.0	V
		TS1, TS2, /PRES	–0.3 to V_{REG27} + 0.3	V
V_O	Output voltage range	CHG, DSG, ZVCHG, FUSE	–0.3 to BAT	V
		RBI, REG27	–0.3 to 2.75	V
I_{SS}	Maximum combined sink current for input pins		50	mA
T_{FUNC}	Functional temperature		–40 to 110	°C
T_{STG}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
	Supply voltage	PACK			25	V
		BAT	3.8		V_{VC2}+5	
$V_{STARTUP}$		Start up voltage at PACK		5.2	5.5	V
$V_{shutdown}$		VPACK or VBAT, whichever is higher	3	3.2	3.3	V
V_{IN}	Input voltage range	VC1, BAT	V_{VC2}		V_{VC2}+5	V
		VC2	V_{VC3}		V_{VC3}+5	
		VC3	V_{VC4}		V_{VC4}+5	
		VC4	V_{SRP}		V_{SRP}+5	
		VCn – VC(n+1), (n=1, 2, 3, 4)	0		5	
		PACK			25	
		SRP to SRN	–0.3		1	V
C_{REG27}	External 2.7V REG capacitor		1			μF
T_{OPR}	Operating temperature		–40		85	°C

PIN DETAILS

TSSOP (PW)
(TOP VIEW)

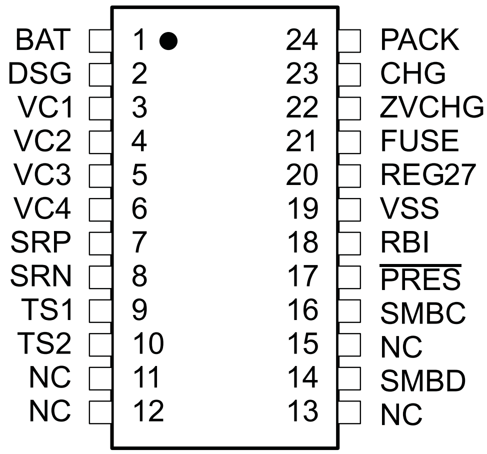


Table 2. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BAT	1	P	Power input from battery
DSG	2	O	P-CH FET Drive controlling discharge
VC1	3	IA	Sense voltage input terminal and external cell balancing drive output for most positive cell, and battery stack measurement input.
VC2	4	IA	Sense voltage input terminal and external cell balancing drive output for second most positive cell.
VC3	5	IA	Sense voltage input terminal and external cell balancing drive output for third most positive cell.
VC4	6	IA	Sense voltage input terminal and external cell balancing drive output for least positive cell.
SRP	7	IA	Analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between SRP and SRN where SRP is the top of the sense resistor.
SRN	8	IA	Analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between SRP and SRN where SRN is the bottom of the sense resistor.
TS1	9	I/O,IA	Thermistor input TS1
TS2	10	I/O,IA	Thermistor input TS2
NC	11	-	Keep this pin floating
NC	12	-	Keep this pin floating
NC	13	-	Keep this pin floating
SMBD	14	I/OD	SMBus data pin
NC	15	-	Keep this pin floating
SMBC	16	I/OD	SMBus clock pin
$\overline{\text{PRES}}$	17	I/OD	Active low input to sense system insertion and typically requires additional ESD protection
RBI	18	P	RAM backup pin to provide backup potential to the internal DATA RAM if power is momentarily lost by using a capacitor attached between RBI and VSS
VSS	19	P	Device ground
REG27	20	P	Internal power supply 2.7V bias output
FUSE	21	I/OD	Push-pull fuse drive and secondary protector activation input sensing
ZVCHG	22	O	P-CH precharge FET Drive controlling pre-charge and zero-volt charge
CHG	23	O	P-CH FET Drive controlling charge
PACK	24	P	PACK positive terminal and alternative power source

ELECTRICAL SPECIFICATIONS

GENERAL PURPOSE I/O

Typical values stated where T_A = 25°C and VBAT=VPACK= 14.4V, Min/Max values stated where T_A = –40°C to 85°C and VBAT=VPACK= 3.8V to 25V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	/PRES, SMBD, SMBC, TS1, TS2	2			V
V_{IL}	Low-level input voltage	/PRES, SMBD, SMBC, TS1, TS2			0.8	V
V_{OH}	Output voltage high	/PRES, SMBD, SMBC, TS1, TS2, I_L = –0.5 mA	V_{REG27}–0.5			V
$V_{OH(FUSE)}$	High level fuse output	V_{BAT} = 3.8 V to 9 V, C_L = 1 nF	3	V_{BAT}–0.3	8.6	V
		V_{BAT} = 9 V to 25 V, C_L = 1nF	7.5	8	9	
$t_{R(FUSE)}$	FUSE output rise time	C_L = 1 nF, $V_{OH(FUSE)}$ = 0 V to 5 V			10	µs
$Z_{O(FUSE)}$	FUSE output impedance			2	6	kΩ
V_{FUSE_DET}	FUSE detect input voltage		0.8	2	3.2	V
V_{OL}	Low-level output voltage	/PRES, SMBD, SMBC, TS1, TS2, I_L = 7 mA			0.4	V
C_{IN}	Input capacitance			5		pF
I_{lkg}	Input leakage current	/PRES, SMBD, SMBC, TS1, TS2 SMBD and SMBC pull-down disabled			1	µA
$R_{PD(SMBx)}$	SMBD and SMBC pull-down	T_A = –40°C to 100°C	600	950	1300	kΩ
R_{PAD}	Pad resistance	TS1, TS2		87	110	Ω

SUPPLY CURRENT

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{CC}	Normal mode	Firmware running, no flash writes		441		µA
I_{SLEEP}	Sleep mode	Discharge FET ON, Charge FET ON ([NR]=1, [NRCHG]=1)		69		µA
		Discharge FET ON, Charge FET OFF ([NR]=1, [NRCHG]=0)		66		µA
		Discharge FET OFF, Charge FET OFF ([NR]=0, System not present)		61		µA
$I_{SHUTDOWN}$	Shutdown mode	T_A = –40°C to 110°C		0.5	1	µA

REG27 POWER ON RESET

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{REG27IT–}$	Negative-going voltage input	At REG27	2.22	2.35	2.34	V
$V_{REG27IT+}$	Positive-going voltage input	At REG27	2.25	2.5	2.6	V

INTERNAL LDO

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REG}	Regulator output voltage	I_{REG27} = 10 mA	T_A = –40°C to 85°C	2.5	2.7	2.75	V
$\Delta V_{(REGTEMP)}$	Regulator output change with temperature	I_{REG} = 10 mA	T_A = –40°C to 85°C		±0.5%		
$\Delta V_{(REGLINE)}$	Line regulation	I_{REG} = 10 mA			±2	±4	mV
$\Delta V_{(REGLOAD)}$	Load regulation	I_{REG} = 0.2 to 10 mA			±20	±40	mV
$I_{(REGMAX)}$	Current limit			25		50	mA

SRx WAKE FROM SLEEP

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{WAKE_ACR}	Accuracy of V_{WAKE}	V_{WAKE} = 1.2 mV	0.2	1.2	2	mV
		V_{WAKE} = 2.4 mV	0.4	2.4	3.6	
		V_{WAKE} = 5 mV	2	5	6.8	
		V_{WAKE} = 10 mV	5.3	10	13	
V_{WAKE_TCO}	Temperature drift of VWAKE accuracy			0.5		%/°C
t_{WAKE}	Time from application of current and wake of bq3060			0.2	1	ms

COULOMB COUNTER

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input voltage range		-0.20		0.25	V
Conversion time	Single conversion		250		ms
Effective resolution	Single conversion	15			Bits
Integral nonlinearity	T_A = –25°C to 85°C		±0.007	±0.034	%FSR
Offset error (1)	T_A = –25°C to 85°C		10		µV
Offset error drift			0.3	0.5	µV/°C
Full-scale error (2)		–0.8%	0.2%	0.8%	
Full-scale error drift				150	PPM/°C
Effective input resistance		2.5			MΩ

(1) Post Calibration Performance
(2) Uncalibrated performance. This gain error can be eliminated with external calibration.

ADC

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input voltage range		–0.2		0.8×V_{REG27}	V
Conversion time			31.5		ms
Resolution (no missing codes)		16			Bits
Effective resolution		14	15		Bits
Integral nonlinearity				±0.020	%FSR
Offset error (1)			70	160	µV
Offset error drift			1		µV/°C
Full-scale error	V_{IN} = 1 V	–0.8%	±0.2%	0.4%	
Full –scale error drift				150	PPM/°C
Effective input resistance		8			MΩ

(1) Channel to channel offset

EXTERNAL CELL BALANCE DRIVE

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{BAL_drive}	Internal pull-down resistance for external cell balance	Cell balance ON for VC1, VCi-VCi+1 = 4V, where i = 1~4		5.7		kΩ
		Cell balance ON for VC2, VCi-VCi+1 = 4V, where = i = 1~4		3.7		
		Cell balance ON for VC3, VCi-VCi+1 = 4V, where = i = 1~4		1.75		
		Cell balance ON for VC4, VCi-VCi+1 = 4V, where = i = 1~4		0.85		

CELL VOLTAGE MONITOR

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CELL Voltage Measurement Accuracy(1)	T_A = –10°C to 60°C		±10	±20	mV
	T_A = –40°C to 85°C		±10	±35	

(1) This is the performance expected for non-calibrated device.

INTERNAL TEMPERATURE SENSOR

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{(TEMP)}$	Temperature sensor accuracy			±3%		°C

THERMISTOR MEASUREMENT SUPPORT

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ERR}	Internal resistor drift			–230		ppm/°C
R	Internal resistor	TS1, TS2		17	20	kΩ

INTERNAL THERMAL SHUTDOWN

PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{MAX}	Maximum REG27 temperature		125		175	°C
$T_{RECOVER}$	Recovery hysteresis temperature			10		°C

(1) Parameters assured by design. Not production tested.

HIGH FREQUENCY OSCILLATOR

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(OSC)}$	Operating frequency of CPU clock			2.097		MHz
$f_{(EIO)}$	Frequency error(1)	T_A = –20°C to 70°C	–2%	±0.25%	2%	
		T_A = –40°C to 85°C	–3%	±0.25%	3%	
$t_{(SXO)}$	Start-up time(2)	T_A = –25°C to 85°C		3	6	ms

(1) The frequency drift is included and measured from the trimmed frequency at VBAT = VPACK = 14.4 V, T_A = 25°C
(2) The startup time is defined as the time it takes for the oscillator output frequency to be ±3% when the device is already powered.

LOW FREQUENCY OSCILLATOR

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(LOSC)}$	Operating frequency			32.768		MHz
$f_{(LEIO)}$	Frequency error(1)	T_A = –20°C to 70°C	–1.5%	±0.25%	1.5%	
		T_A = –40°C to 85°C	–2.5%	±0.25%	2.5%	
$t_{(LSXO)}$	Start-up time(2)	T_A = –25°C to 85°C			100	ms

(1) The frequency drift is included and measured from the trimmed frequency at VBAT = VPACK = 14.4 V, T_A = 25°C.
(2) The startup time is defined as the time it takes for the oscillator output frequency to be ±3%.

FLASH

PARAMETER (1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Data retention		10			Years
	Flash programming write-cycles		20k			Cycles
$t_{(ROWPROG)}$	Row programming time				2	ms
$t_{(MASSERASE)}$	Mass-erase time				250	ms
$t_{(PAGEERASE)}$	Page-erase time				25	ms
$I_{CC(PROG)}$	Flash-write supply current			4	6	mA
$I_{CC(ERASE)}$	Flash-erase supply current	TA = –40°C to 0°C		8	22	mA
		T_A = 0°C to 85°C		3	15	

(1) Specified by design. Not production tested

RAM BACKUP

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(RBI)}$	RBI data-retention input current	$V_{RBI} > V_{(RBI)MIN}$, $V_{REG27} < V_{REG27IT-}$, T_A = 70°C to 110°C		20	1500	nA
		$V_{RBI} > V_{(RBI)MIN}$, $V_{REG27} < V_{REG27IT-}$, T_A = –40°C to 70°C			500	
$V_{(RBI)}$	RBI data-retention voltage (1)		1			V

(1) Specified by design. Not production tested.

CURRENT PROTECTION THRESHOLDS

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(OCD)}$	OCD detection threshold voltage range, typical	RSNS = 0	RSNS is set in STATE_CTL register	50		200	mV
		RSNS = 1		25		100	
$\Delta V_{(OCDT)}$	OCD detection threshold voltage program step	RSNS = 0			10		mV
		RSNS = 1			5		
$V_{(SCCT)}$	SCC detection threshold voltage range, typical	RSNS = 0		–100		–300	mV
		RSNS = 1		–50		–225	
$\Delta V_{(SCCT)}$	SCC detection threshold voltage program step	RSNS = 0			-50		mV
		RSNS = 1			-25		
$V_{(SCDT)}$	SCD detection threshold voltage range, typical	RSNS = 0		100		450	mV
		RSNS = 1		50		225	
$\Delta V_{(SCDT)}$	SCD detection threshold voltage program step	RSNS = 0			50		mV
		RSNS = 1			25		
$V_{(OFFSET)}$	SCD, SCC and OCD offset			–10		10	mV
$V_{(Scale\_Err)}$	SCD, SCC and OCD scale error			–10%		10%	

CURRENT PROTECTION TIMING

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(OCDD)}$	Overcurrent in discharge delay		1		31	ms
$t_{(OCDD\_STEP)}$	OCDD step options			2		ms
$t_{(SCDD)}$	Short circuit in discharge delay	AFE.STATE_CNTL[SCDDx2] = 0	0		915	µs
		AFE.STATE_CNTL[SCDDx2] = 1	0		1830	
$t_{(SCDD\_STEP)}$	SCDD step options	AFE.STATE_CNTL[SCDDx2] = 0		61		µs
		AFE.STATE_CNTL[SCDDx2] = 1		122		
$t_{(SCCD)}$	Short circuit in charge delay		0		915	µs
$t_{(SCCD\_STEP)}$	SCCD step options			61		µs
$t_{(DETECT)}$	Current fault detect time	$V_{SRP-SRN} = V_{THRESH}$ + 12.5 mV, T_A = –40°C to 85°C		35	160	µs
t_{ACC}	Overcurrent and short circuit delay time accuracy	Accuracy of typical delay time with WDI active	–20%		20%	
		Accuracy of typical delay time with no WDI input	–50%		50%	

P-CH FET DRIVE

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{O(FETON)}$	Output voltage, charge and discharge FETs on	$V_{O(FETONDSG)} = V_{(BAT)}–V_{(DSG)}$, R_{GS} = 1MΩ, T_A = –40°C to 110°C, BAT = 20 V (1)		12	15	18	V
		$V_{O(FETONCHG)} = V_{(PACK)}–V_{(CHG)}$, R_{GS} =1MΩ, T_A = –40°C to 110°C, PACK = 20 V (1)		12	15	18	
$V_{O(FETOFF)}$	Output voltage, charge and discharge FETs off	$V_{O(FETOFFDSG)} = V_{(BAT)}–V_{(DSG)}$, T_A = –40°C to 110°C, BAT = 16 V				0.2	V
		$V_{O(FETOFFCHG)} = V_{(PACK)}–V_{(CHG)}$, T_A = –40°C to 110°C, PACK = 16 V				0.2	
t_r	Rise time	C_L = 4700 pF	V_{DSG}: 10% to 90%		70	200	µs
			V_{CHG}: 10% to 90%		70	200	
t_f	Fall time	C_L = 4700 pF	V_{DSG} : 90% to 10%		70	200	µs
			V_{CHG}: 90% to 10%		70	200	

(1) For a VBAT or VPACK input range of 3.8 V to 25 V, MIN $V_{O(FETON)}$ voltage is 12V or $V_{(BAT)}$–1V, whichever is less.

PRE-CHARGE/ZVCHG FET DRIVE

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(PreCHGON)}$	$V_{O(PreCHGON)} = V_{(PACK)}–V_{(ZVCHG)}$, pre-charge FET on (1)	R_{GS} =1 MΩ, T_A = –40°C to 110°C		12	15	18	V
$V_{(PreCHGOFF)}$	Output voltage, pre-charge FET off (1)	R_{GS} =1 MΩ, T_A = –40°C to 110°C				VBAT–0.5	V
t_r	Rise time	C_L = 4700 pF, R_G = 5.1 kΩ	V_{ZVCHG}: 10% to 90%		80	200	µs
t_f	Fall time	C_L = 4700 pF, R_G = 5.1 kΩ	V_{ZVCHG} : 90% to 10%		1.7		ms

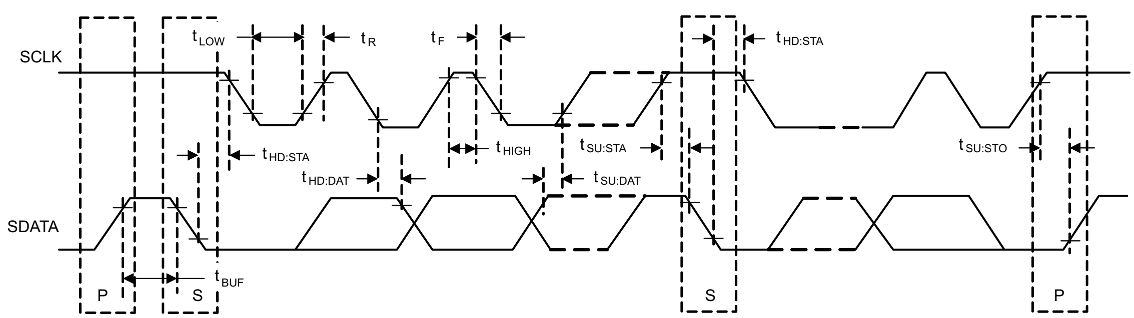
(1) For a VBAT or VPACK input range of 3.8 V to 25 V, MIN $V_{(PreCHGON)}$ voltage is 12 V or $V_{(BAT)}$–1V, whichever is less.

SMBus

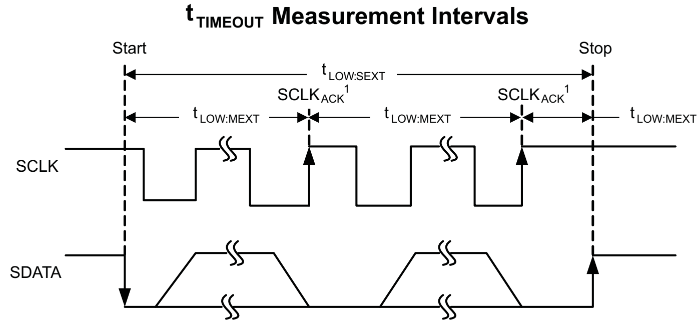
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SMB}	SMBus operating frequency	Slave mode, SMBC 50% duty cycle	10		100	kHz
f_{MAS}	SMBus master clock frequency	Master mode, no clock low slave extend		51.2		kHz
t_{BUF}	Bus free time between start and stop		4.7			µs
$t_{HD:STA}$	Hold time after (repeated) start		4.0			µs
$t_{SU:STA}$	Repeated start setup time		4.7			µs
$t_{SU:STO}$	Stop setup time		4.0			µs
$t_{HD:DAT}$	Data hold time	Receive mode	0			ns
		Transmit mode	300			
$t_{SU:DAT}$	Data setup time		250			ns
$t_{TIMEOUT}$	Error signal/detect	See (1)	25		35	ms
t_{LOW}	Clock low period		4.7			µs
t_{HIGH}	Clock high period	See (2)	4.0		50	µs
$t_{LOW:SEXT}$	Cumulative clock low slave extend time	See (3)			25	ms
$t_{LOW:MEXT}$	Cumulative clock low master extend time	See (4)			10	ms
t_F	Clock/data fall time	See (5)			300	ns
t_R	Clock/data rise time	See (6)			1000	ns

(1) The bq3060 times out when any clock low exceeds $t_{TIMEOUT}$
(2) t_{HIGH}, Max, is the minimum bus idle time. SMBC = SMBD = 1 for t > 50 µs causes reset of any transaction involving bq3060 that is in progress. This specification is valid when the NC_SMB control bit remains in the default cleared state (CLK[0]=0). If NC_SMB is set then the timeout is disabled.
(3) $t_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
(4) $t_{LOW:MEXT}$ is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to the stop.
(5) Rise time $t_R = V_{ILMAX} – 0.15$) to ($V_{IHMIN} + 0.15$)
(6) Fall time $t_F = 0.9V_{DD}$ to ($V_{ILMAX} – 0.15$)

Timing Measurement Intervals



$t_{TIMEOUT}$ Measurement Intervals



(1) $SCLK_{ACK}$ is the acknowledge-related clock pulse generated by the master.

SMBus XL

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SMBXL}	SMBus XL operating frequency	Slave mode	40		400	kHz
t_{BUF}	Bus free time between start and stop		4.7			μs
$t_{HD:STA}$	Hold time after (repeated) start		4			μs
$t_{SU:STA}$	Repeated start setup time		4.7			μs
$t_{SU:STO}$	Stop setup time		4			μs
$t_{TIMEOUT}$	Error signal/detect	See (1)	25		35	ms
t_{LOW}	Clock low period		1		1	μs
t_{HIGH}	Clock high period	See (2)	1		2	μs

(1) The bq3060 times out when any clock low exceeds $t_{TIMEOUT}$
(2) t_{HIGH}, Max, is the minimum bus idle time. SMBC = SMBD = 1 for t > 50 μs causes reset of any transaction involving bq3060 that is in progress. This specification is valid when the NC_SMB control bit remains in the default cleared state (CLK[0]=0). If NC_SMB is set then the timeout is disabled.

FEATURE SET

Primary (1st Level) Safety Features

The bq3060 supports a wide range of battery and system protection features that can easily be configured. The primary safety features include:

- Cell over/undervoltage protection
- Charge and discharge overcurrent
- Short circuit
- Charge and discharge overtemperature
- AFE Watchdog

Secondary (2nd Level) Safety Features

The secondary safety features of the bq3060 can be used to indicate more serious faults via the FUSE (pin 21). This pin can be used to blow an in-line fuse to permanently disable the battery pack from charging and discharging. This pin is also used as an input to sense the state of the fuse. The secondary safety protection features include:

- Safety overvoltage
- Safety overcurrent in charge and discharge
- Safety overtemperature in charge and discharge
- Charge FET and Zero-Volt Charge FET fault
- Discharge FET fault
- Cell imbalance detection
- Fuse blow by a secondary voltage protection IC
- AFE register integrity fault (AFE_P)
- AFE communication fault (AFE_C)

Charge Control Features

The bq3060 charge control features include:

- Supports JEITA temperature ranges. Reports charging voltage and charging current according to the active temperature range.
- Handles more complex charging profiles. Allows for splitting the standard temperature range into 2 sub-ranges and allows for varying the charging current according to the cell voltage.
- Reports the appropriate charging current needed for constant current charging and the appropriate charging voltage needed for constant voltage charging to a smart charger using SMBus broadcasts.
- Reduce the charge difference of the battery cells in fully charged state of the battery pack gradually using a voltage-based cell balancing algorithm during charging. A voltage threshold can be set up for cell balancing to be active. This prevents fully charged cells from overcharging and causing excessive degradation and also increases the usable pack energy by preventing premature charge termination
- Supports pre-charging/zero-volt charging
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range
- Reports charging fault and also indicate charge status via charge and discharge alarms.

Gas Gauging

The bq3060 uses advanced CEDV (Compensated End-of-Discharge Voltage) technology to measure and calculate the available capacity in battery cells. The bq3060 accumulates a measure of charge and discharge currents and compensates the charge current measurement for temperature and state-of-charge of the battery. The bq3060 estimates self-discharge of the battery and also adjusts the self-discharge estimation based on temperature.

See *bq3060 Technical Reference*(SLUU319) for further details.

Lifetime Data Logging Features

The bq3060 offers limited lifetime data logging for the following critical battery parameters for analysis purposes:

- Lifetime maximum temperature
- Lifetime minimum temperature
- Lifetime maximum battery cell voltage
- Lifetime minimum battery cell voltage

Authentication

The bq3060 supports authentication by the host using SHA-1.

Power Modes

The bq3060 supports 3 different power modes to reduce power consumption:

- In Normal Mode, the bq3060 performs measurements, calculations, protection decisions and data updates in 1 second intervals. Between these intervals, the bq3060 is in a reduced power stage.
- In Sleep Mode, the bq3060 performs measurements, calculations, protection decisions and data update in adjustable time intervals. Between these intervals, the bq3060 is in a reduced power stage. The bq3060 has a wake function that enables exit from Sleep mode, when current flow or failure is detected.
- In Shutdown Mode the bq3060 is completely disabled.

Configuration

Oscillator Function

The bq3060 fully integrates the system oscillators. Therefore the bq3060 requires no external components for this feature.

System Present Operation

The bq3060 checks the $\overline{\text{PRES}}$ pin periodically (1 second). If $\overline{\text{PRES}}$ input is pulled to ground by external system, the bq3060 detects the presence of the system.

2-, 3-, or 4-Cell Configuration

In a 2-cell configuration, VC1 is shorted to VC2 and VC3. In a 3-cell configuration, VC1 is shorted to VC2.

Cell Balance Control

If cell balancing is required, the bq3060 cell balance control allows a weak, internal pull-down for each VCx pin. The purpose of this weak pull-down is to enable an external FET for current bypass. Series resistors placed between the input VCx pins and the positive battery cell terminals control the VGS of the external FET. See *bq3060 Cell balancing using external MOSFET* (SLUA509) for more details.

Battery Parameter Measurements

The bq3060 uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell and battery voltage, and temperature measurement.

Charge and Discharge Counting

The integrating delta-sigma ADC measures the charge/discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SR1 and SR2 pins. The integrating ADC measures bipolar signals from -0.20 V to 0.25 V. The bq3060 detects charge activity when $V_{SR} = V_{(SRP)} - V_{(SRN)}$ is positive, and discharge activity when $V_{SR} = V_{(SRP)} - V_{(SRN)}$ is negative. The bq3060 continuously integrates the signal over time, using an internal counter. The fundamental rate of the counter is 0.65 nVh.

Voltage

The bq3060 updates the individual series cell voltages at one second intervals. The internal ADC of the bq3060 measures the voltage, scales, and offsets, and calibrates it appropriately. To ensure an accurate differential voltage sensing, the IC ground should be connected directly to the most negative terminal of the battery stack, not to the positive side of the sense resistor. This minimizes the voltage drop across the PCB trace.

Voltage Calibration and Accuracy

The bq3060 is calibrated for voltage prior to shipping from TI. The bq3060 voltage measurement signal chain (ADC, high voltage translation, circuit interconnect) will be calibrated for each cell. The external filter resistors, connected from each cell to the VCx input of the bq3060, are required to be 1kΩ. The accuracy of the factory-calibrated devices is +/- 10mV per cell at room temperature at 4V cell voltage. Without any customer voltage calibration, this is the level of accuracy expected as long as the filter resistor value is 1kΩ. If better voltage accuracy is desired, customer voltage calibration is required. An application note on calibrating and programming the bq3060 is available in the product web folder. See *Data Flash Programming and Calibrating the bq3060 Gas Gauge*(SLUA502) for more details.

Current

The bq3060 uses the SRP and SRN inputs to measure and calculate the battery charge and discharge current using a 5 mΩ to 20 mΩ typ. sense resistor.

Auto Calibration

The bq3060 can automatically calibrate its offset between the A to D converter and the output of the high voltage translation circuit. Also, the bq3060 provides an auto-calibration for the coulomb counter to cancel the voltage offset error across SRN and SRP for maximum charge measurement accuracy. The bq3060 performs auto-calibration when the SMBus lines stay low continuously for a minimum of 5 s.

Temperature

The bq3060 has an internal temperature sensor and inputs for 2 external temperature sensor inputs TS1 and TS2 used in conjunction with two identical NTC thermistors (default is Semitec 103AT) to sense the battery cell temperature. The bq3060 can be configured to use internal or up to 2 external temperature sensors.

Communications

The bq3060 uses SMBus v1.1 with Master Mode and package error checking (PEC) options per the SBS specification.

SMBus On and Off State

The bq3060 detects an SMBus off state when SMBC and SMBD are logic-low for ≥ 2 seconds. Clearing this state requires either SMBC or SMBD to transition high. Within 1 ms, the communication bus is available.

SBS Commands

See *bq3060 Technical Reference*(SLUU319) for further details.

REVISION HISTORY

Changes from Original (March 2009) to Revision A	Page
• Changed Device From: Product Preview To: Production	1

PACKAGING INFORMATION

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/Ball Finish	MSL Peak Temp [(3)]
BQ3060PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ3060PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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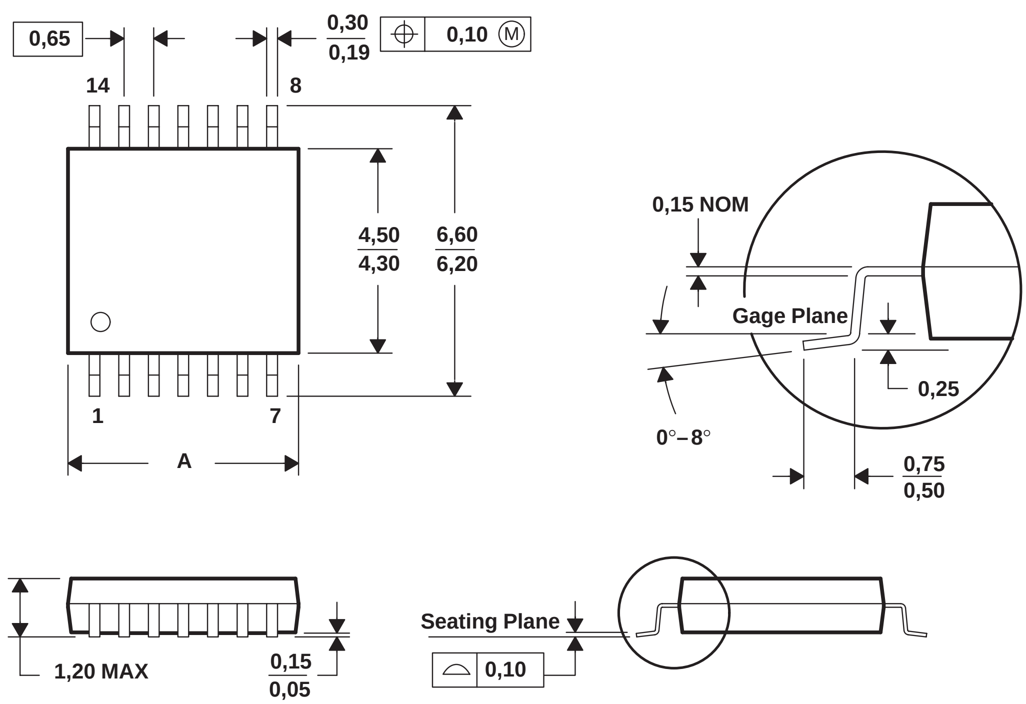
PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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