3-V to 20-V High-Current Load Switch with Programmable Inrush Slew Rate

Check for Samples: TPS25910

FEATURES

- **3-V to 20-V Bus Operation**
- **Integrated 30-mΩ Pass MOSFET**
- **Programmable Current Limit from: 0.83 A to 6.5 A**
- **Programmable Inrush Current Slew Rate**
- **Thermal Shutdown and fault alert**
- **4-mm x 4-mm QFN16**
- **-40°C to 125°C Junction Temperature Range**

APPLICATIONS

- **Solid State Drive (SSD)**
- **Hard Disk Drive (HDD)**
- **RAID Arrays**
- **Telecommunications**
- **Plug-In Circuit Boards**
- **Notebooks and Netbooks**

DESCRIPTION

The TPS25910 provides highly integrated hot-swap power management and superior protection in applications where the load is powered by voltages between 3 V and 20 V. This device is intended for systems where a voltage bus must be protected from undesired permanent and transient overload.

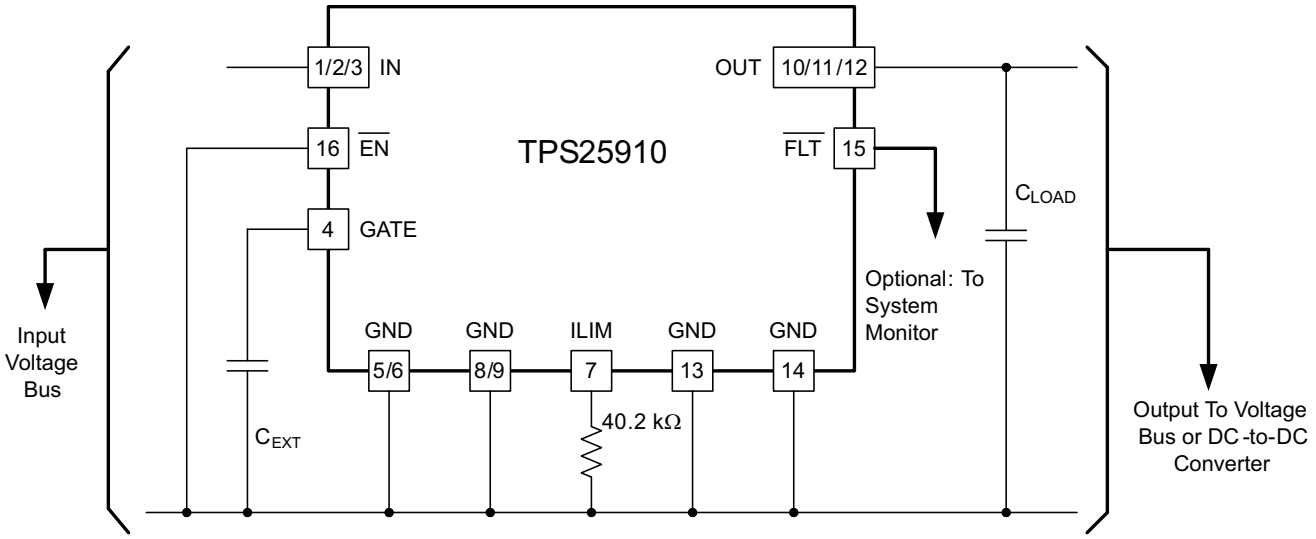
At start up or when hot plugging into the system bus, the TPS25910 limits the inrush current by controlling the ramp rate of the output voltage, V_{OUT}. The slew rate of V_{OUT} can be adjusted with a capacitor between the GATE pin and the GND pin.

Built in SOA protection ensures that the internal MOSFET operates inside a safe operating area (SOA) under the harshest operating conditions. In addition, the current limit threshold, which is independent of the power limit, can be adjusted with a resistor between the ILIM pin and the GND pin.

The TPS25910 provides a fault indicator output when in thermal fault.

The TPS25910 is in a 16-pin QFN package.

12-V, 4.75-A APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

DEVICE	JUNCTION TEMPERATURE	PACKAGE	ORDERING CODE	MARKING
TPS25910	-40°C to 125°C	RSA (4-mm x 4-mm QFN)	TPS25910RSAR	TPS25910
			TPS25910RSAT	

ABSOLUTE MAXIMUM RATINGS

over device junction temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Input voltage range IN, OUT	-0.3	22	V
Voltage range, GATE	-0.3	30	
Voltage range $\overline{FLT}$	-0.3	20	V
Voltage ILIM		1.75	
Output sink current $\overline{FLT}$		10	mA
Input voltage range, $\overline{EN}$	-0.3	6	
Voltage range ILIM(3)	-0.3	3	V
ESD rating, HBM		2 .5 k	
ESD rating, CDM		500	
Operating junction temperature range, T_J	Internally Limited		°C
Storage temperature range, T_{stg}	-65	150	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Do not apply voltage to pin.

RECOMMENDED OPERATING CONDITIONS

over device junction temperature range (unless otherwise noted)

PARAMETER	MIN	NOM	MAX	UNIT
Input voltage range IN, OUT	3		20	V
Voltage range $\overline{EN}$	0		5	
Voltage range $\overline{FLT}$	0		20	
Continuous output current I_{OUT}	0		5	A
Output sink current $\overline{FLT}$	0		1	mA
External Capacitor, GATE	1		47	nF
dv/dt, V_{IN} (1)			12	V/µS
R_{LIM} (2)	0		237k	Ω
Junction temperature	-40		125	°C

(1) dV/dt, V_{IN} should be limited to 12 V/µS to confine the shoot-through current to the load.
(2) When R_{LIM} value is beyond this range, I_{LIM} will not be as accurate as within this range.

THERMAL INFORMATION

THERMAL METRIC (1)		TPS25910 RSA (QFN) 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance (2)	34.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance (3)	35.3	
θ_{JB}	Junction-to-board thermal resistance (4)	11.9	
ψ_{JT}	Junction-to-top characterization parameter (5)	0.4	
ψ_{JB}	Junction-to-board characterization parameter (6)	12.0	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance (7)	3.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

Over operating free-air temperature range, V_{IN} = 3 V – 20 V, $\overline{EN}$ = 0 V, $\overline{FLT}$ = open, $R_{(RLIM)}$ = 40.2 kΩ, No external capacitors are connected to either GATE or OUT, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IN						
	UVLO	V_{IN} ↑	2.60	2.75	2.90	V
		Hysteresis		100		mV
	Bias current	$\overline{EN}$ = 2.4 V		2.5	4	mA
		$\overline{EN}$ = 0 V		3.3	5	
OUT						
	RON	$R_{(VIN-VOUT)}$, $I_{(VOUT)} < I_{(RLIM)}$, 1 A ≤ $I_{(VOUT)}$ ≤ 4.5 A		29.5	42	mΩ
	Power limit	V_{IN}: 12 V, C_{OUT} = 1000 µF, $\overline{EN}$: 3 V → 0 V	3	5	7.5	W
	Reverse diode voltage	$V_{OUT} > V_{IN}$, $\overline{EN}$ = 5 V, I_{IN} = - 1 A		0.77	1	V
ILIM						
	Current limit program I_{VOUT}, $V_{(VIN - OUT)}$ = 0.3 V, pulsed test	$R_{(RLIM)}$ = 237 kΩ	0.50	0.82	1.1	A
		$R_{(RLIM)}$ = 200 kΩ	0.75	1	1.25	
		$R_{(RLIM)}$ = 100 kΩ	1.75	2	2.25	
		$R_{(RLIM)}$ = 66.5 kΩ	2.65	3	3.3	
		$R_{(RLIM)}$ = 40.2 kΩ	4.50	5	5.5	
		$R_{(RLIM)}$ = 29.4 kΩ	5.70	6.50	7.3	
$\overline{EN}$						
	Threshold voltage	$V_{(\overline{EN})}$ falling	1.10	1.35		V
		$V_{(\overline{EN})}$rising		1.50	1.75	
		Hysteresis		150		mV
	Input bias current	$V_{(\overline{EN})}$ = 2.4 V (sinking)	-1.5	-1	0.5	µA
		$V_{(\overline{EN})}$ = 0.2 V (sourcing)	-2	-1	0.5	
	Turn on propagation delay	V_{IN} = 3.3 V, I_{LOAD} = 1 A, $V_{(\overline{EN})}$: 2.4 V → 0.2 V, till I_{GATE} changes direction.		10		µs
	Turn off propagation delay	V_{IN} = 3.3 V, I_{LOAD} = 1 A, $V_{(\overline{EN})}$: 0.2 V → 2.4 V, till I_{GATE} changes direction.		2.5		
$\overline{FLT}$						
	V_{OL}	$I_{(\overline{FLT})}$ = 1 mA, Fault active (Over Temperature)		0.2	0.4	V
	Leakage current	$V_{(\overline{FLT})}$ = 18 V			1	µA
THERMAL SHUTDOWN						
	Thermal shutdown	T_J		160		°C
		Hysteresis		20		
GATE						
	Sourcing current	$V_{(GATE-OUT)}$ = 3.5 V, $V_{(\overline{EN})}$ = Low	8	11	15	µA
	Strong pull down resistor	$V_{(\overline{EN})}$ = Low	10	40	80	Ω
	Weak pull down current	$V_{(\overline{EN})}$ = Low	250	500	750	µA
	Output Voltage, $V_{(GATE-OUT)}$		5.5	6.6	7.5	V

DEVICE INFORMATION

TPS25910 FUNCTIONAL BLOCK DIAGRAM

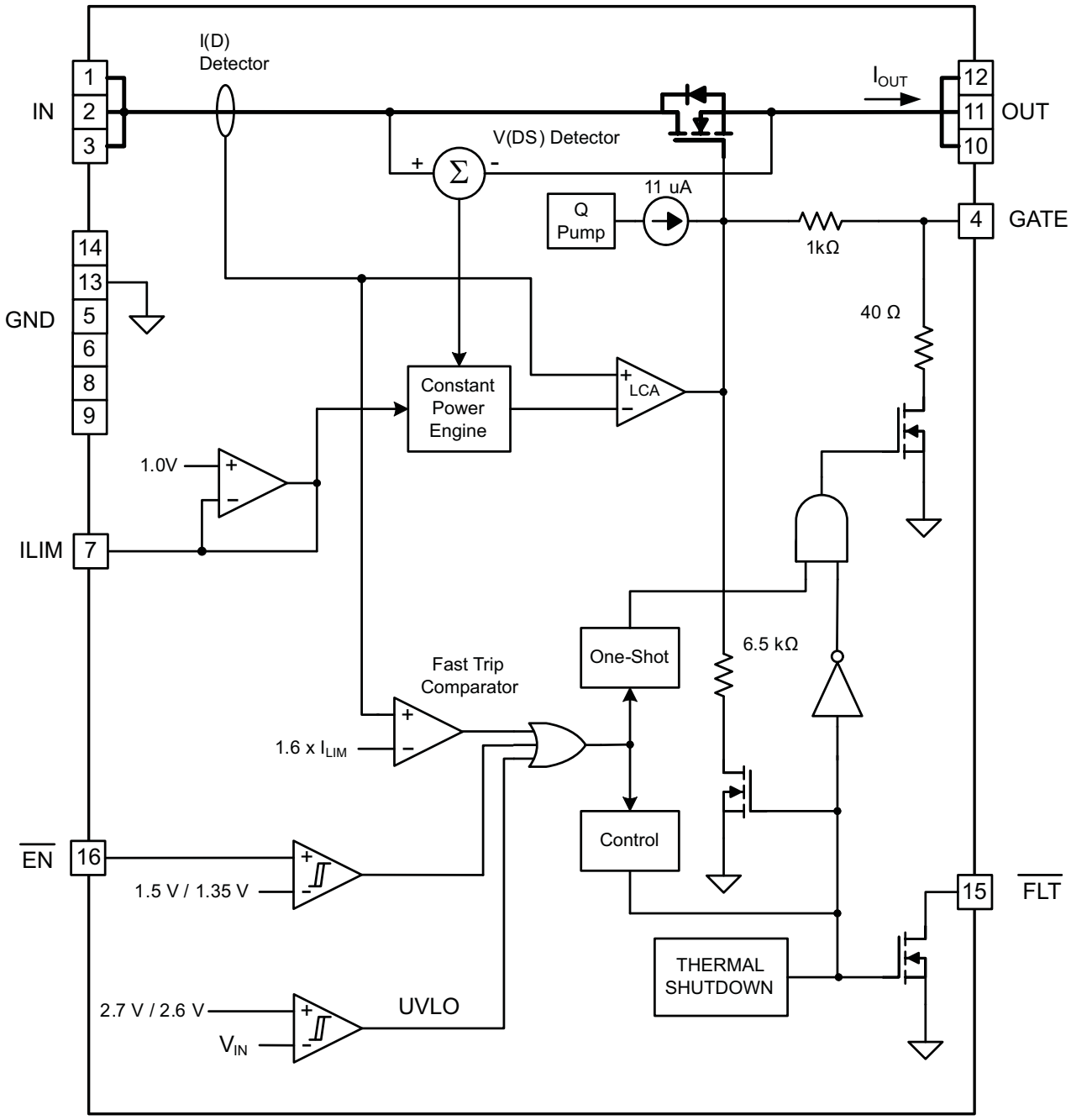
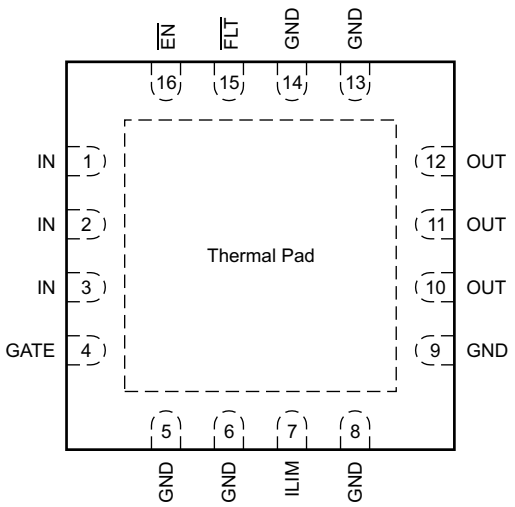


Figure 1. Functional Block Diagram

TPS25910 PIN ASSIGNMENT

RSA-16 Package
(Top View)



PIN FUNCTIONS

PIN NAME	PIN NUMBER	DESCRIPTION
$\overline{EN}$	16	Device is enabled when this pin is pulled low.
IN	1, 2, 3	Power In and control supply voltage.
GATE	4	If the chip die temperature exceeds the OTSD rising threshold, GATE is pulled down to GND by a 7.5KOhm resistor.
ILIM	7	A resistor to ground sets the current limit level.
GND	5, 6, 8, 9, 13, 14	GND
OUT	10, 11, 12	Output to the load.
$\overline{FLT}$	15	Fault low indicates that the internal pass FET junction temperature exceeds the thermal shutdown threshold

PIN DESCRIPTION

$\overline{\text{FLT}}$: Open-drain output that pulls low during thermal shutdown. $\overline{\text{FLT}}$ activates when device thermally shuts down and deactivates when die temperature cools down below the device thermal protection threshold and the device ends thermal shutdown cycle. $\overline{\text{FLT}}$ becomes operational before UV, when V_{IN} is greater than 1V.

GND: This is the most negative voltage in the circuit and is used as reference for all voltage measurements unless otherwise specified. All the GND pins must be connected to system power supply negative return point

GATE: Output that provides gate drive for the internal pass FET. Its sourcing current is about 11 µA. An internal clamp prevents GATE from rising 6.6 V above OUT. C_{INT} is 200 pF.

The GATE pin is disabled by the following mechanisms:

1. When $\overline{\text{EN}}$ is above its rising threshold, GATE is pulled down by a 40-Ω resistor connecting to GND for approximately 50 µs. Then, a 7.5-kΩ resistor ties GATE to GND to ensure the GATE is off.
2. When V_{IN} drops below the UVLO threshold, GATE is pulled down by a 40-Ω resistor connecting to GND for approximately 50 µs. Then, a 7.5-kΩ resistor ties GATE to GND to ensure the GATE is off.
3. When short circuit fault occurs, GATE is pulled down by a 40-Ω resistor connecting to GND for approximately 50 µs. Then, a 500 µA current source continues to pull down on the GATE.
4. If the chip die temperature exceeds the OTSD rising threshold, GATE is pulled down to GND by a 7.5-kΩ resistor.

An external capacitor can be connected from GATE pin to GND pin to create linear inrush profile. The slew rate of the inrush can be controlled by a different capacitor value.

$$I_{CHARGE} = (C_{EXT} + C_{INT})\frac{dV_{OUT}}{dt} \quad (1)$$

Where:

I_{CHARGE} is 11 µA (typical)

C_{INT}, the equivalent gate input capacitance of the internal FET (200 pF typical).

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ILIM: A resistor connected from this pin to ground sets $I_{(LIM)}$. R_{LIM} is set by the formula:

$$R_{LIM} = \frac{197.388}{I_{LIM}^{0.976944}} \text{ for currents below 2 A where } R_{LIM} \text{ is in k}\Omega. \quad (2)$$

$$R_{LIM} = \frac{205.62}{I_{LIM}^{1.02912}} \text{ for currents above 2 A where } R_{LIM} \text{ is in k}\Omega. \quad (3)$$

$\overline{\text{EN}}$: When this pin is pulled low, the device is enabled. The input threshold is hysteretic, allowing the user to program a startup delay with an external RC circuit. $\overline{\text{EN}}$ is pulled to VIN by a 10-MΩ resistor, pulled to GND by 16.8 MΩ and is clamped to ground by a 7-V Zener diode. Because high impedance pullup and or down resistors are used to reduce current draw, any external FET controlling this pin should be low leakage.

IN: Input voltage to the TPS25910. The recommended operating voltage range is 3 V to 20 V. All VIN pins should be connected together and to the power source.

OUT: Output connection for the TPS25910. When switched on, the output voltage is approximately:

$$V_{OUT} = V_{IN} - 0.04 \times I_{OUT} \quad (4)$$

All OUT pins should be connected together and to the load.

TYPICAL CHARACTERISTICS

CURRENT LIMIT vs JUNCTION TEMPERATURE

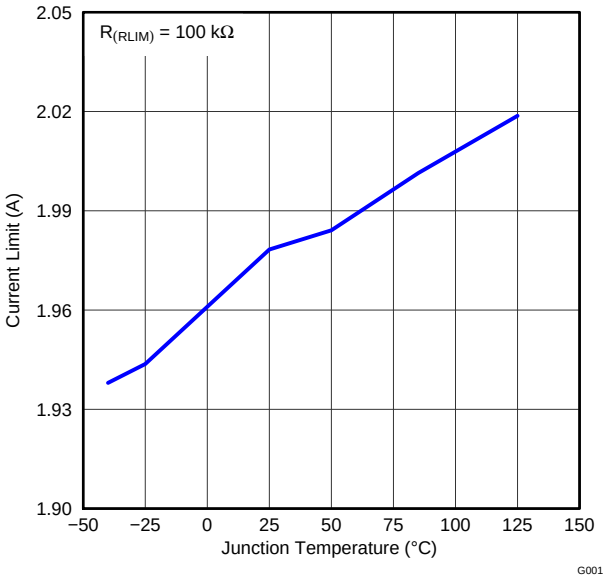


Figure 2.

POWER LIMIT vs JUNCTION TEMPERATURE

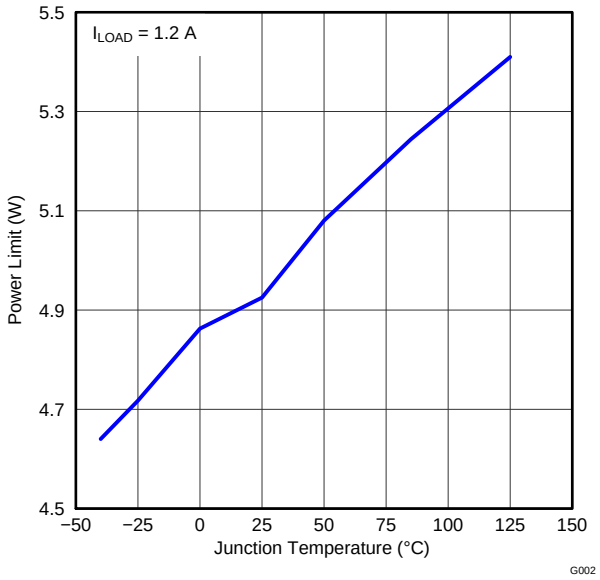


Figure 3.

ON-STATE SUPPLY CURRENT vs JUNCTION TEMPERATURE

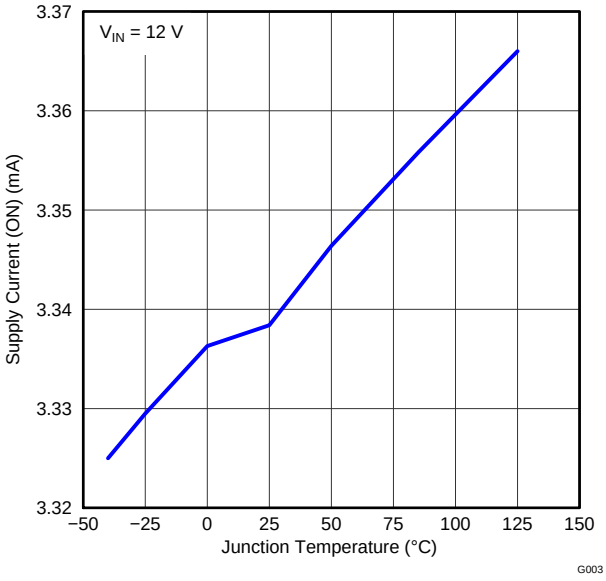


Figure 4.

OFF-STATE SUPPLY CURRENT vs JUNCTION TEMPERATURE

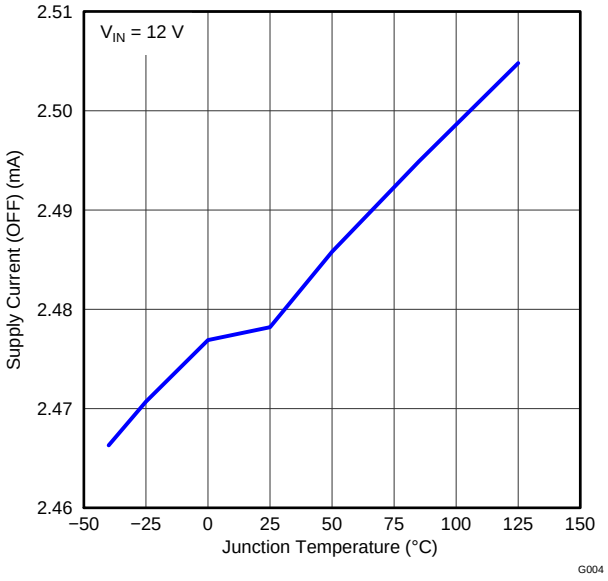


Figure 5.

APPLICATION INFORMATION

Programming the Current-Limit Threshold

The over-current threshold is user programmable via an external resistor. The TPS25910 uses an internal regulation loop to provide a regulated voltage on the ILIM pin. The current-limit threshold is proportional to the current sourced out of ILIM. The recommended 1% resistor range for R_{ILIM} is 0 kΩ ≤ R_{ILIM} ≤ 237 kΩ to ensure stability of the internal regulation loop. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the over-current threshold when selecting a value for R_{ILIM}. Consult the Electrical Characteristics table for specific current limit settings. The traces routing the R_{ILIM} resistor to the TPS25910 should be as short as possible to reduce parasitic effects on the current-limit accuracy.

Equation 5 through Equation 7 can be used to estimate current limit below 2 A:

$$I_{LIM(min)} = \frac{1051.9}{R_{LIM(max)}^{1.3854}} \quad (5)$$

$$I_{LIM(typ)} = \frac{223.61}{R_{LIM(typ)}^{1.0236}} \quad (6)$$

$$I_{LIM(max)} = \frac{104.95}{R_{LIM(min)}^{0.8347}} \quad (7)$$

Equation 8 through Equation 10 can be used to estimate current limit above 2 A:

$$I_{LIM(min)} = \frac{161.24}{R_{LIM(max)}^{0.9796}} \quad (8)$$

$$I_{LIM(typ)} = \frac{176.85}{R_{LIM(typ)}^{0.9717}} \quad (9)$$

$$I_{LIM(max)} = \frac{194.81}{R_{LIM(min)}^{0.9694}} \quad (10)$$

where $R_{LIM(max)}$ is the maximum resistor value in factoring in error, $R_{LIM(typ)}$ is the typical resistor value, and $R_{LIM(min)}$ is the minimum resistor value factoring in error. All resistor values are represented in kΩ. For example, a 100-kΩ, 1% resistor would have the following values:

- $R_{LIM(min)}$ = 99 kΩ
- $R_{LIM(typ)}$ = 100 kΩ
- $R_{LIM(max)}$ = 101 kΩ

A plot of the current limit threshold vs. RLIM using equations Equation 5 through Equation 10 above is shown in Figure 6.

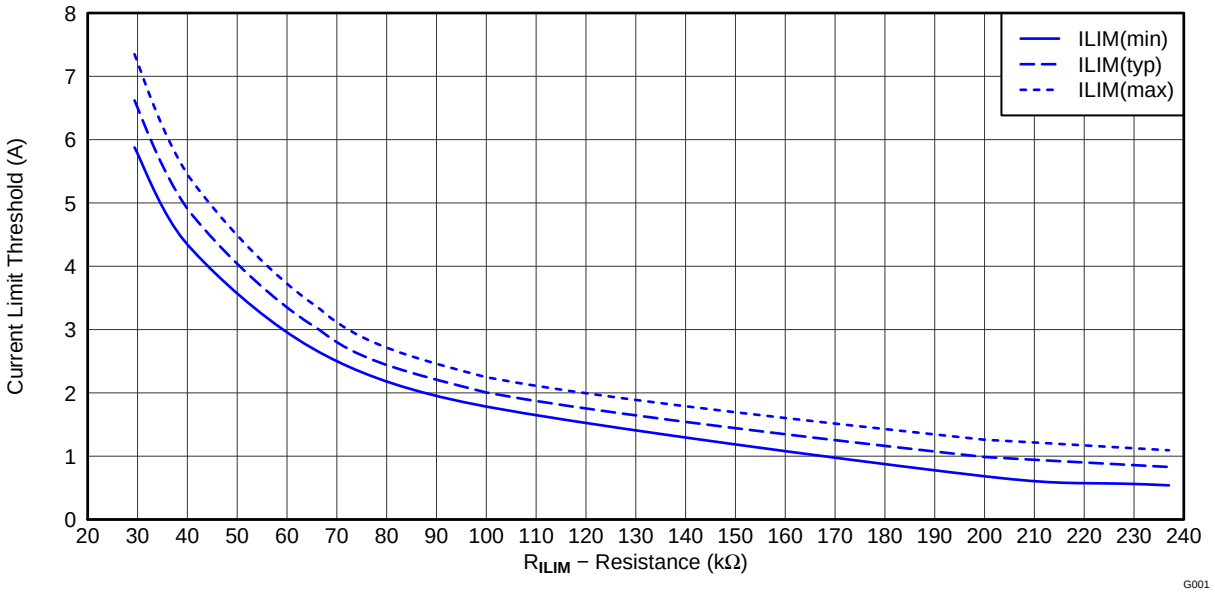


Figure 6. Current Limit Threshold vs. R_{ILIM}

Slew Rate Control Using C_{GATE}

The TPS25910 can be used with applications that require constant turn-on currents. The current is controlled by a single capacitor from the GATE terminal to ground. The TPS25910 internal MOSFET appears to operate as a source follower (following the gate voltage) in this implementation. Choose a time to charge, Δt, based on the output capacitor, input voltage VI, and desired charge current, I_{CHARGE}. Select the device load to be less than 5 W ÷ VIN.

$$\Delta t = \frac{C_{LOAD} \times V_{IN}}{I_{C-LOAD}} \tag{11}$$

To select the gate capacitance:

$$C_{EXT} = I_{CHARGE} \times \frac{\Delta t}{V_{IN}} - C_{INT} \tag{12}$$

- I_{CHARGE} = 11 µA
- C_{INT} = 200 pF (typical)

Figure 7 and Figure 8 illustrate the effects of C_{EXT} = 0.1 µF on inrush current using TPS25910EVM-088.

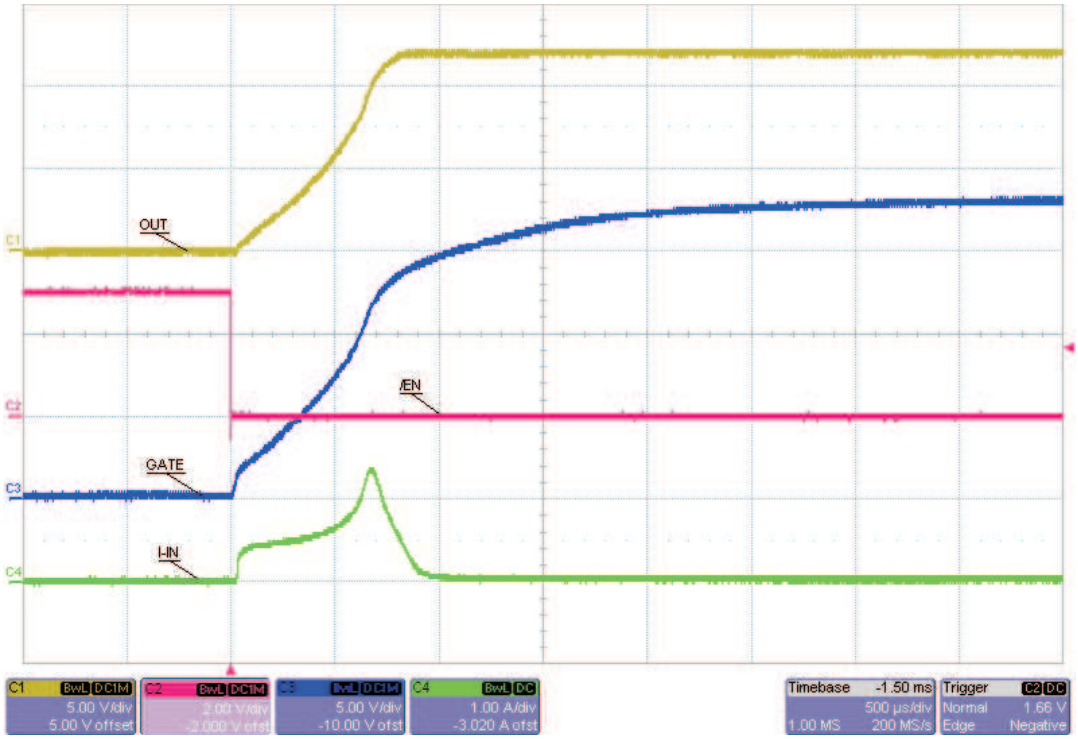


Figure 7. Typical Power Limited Inrush Start Up (no C_{EXT})

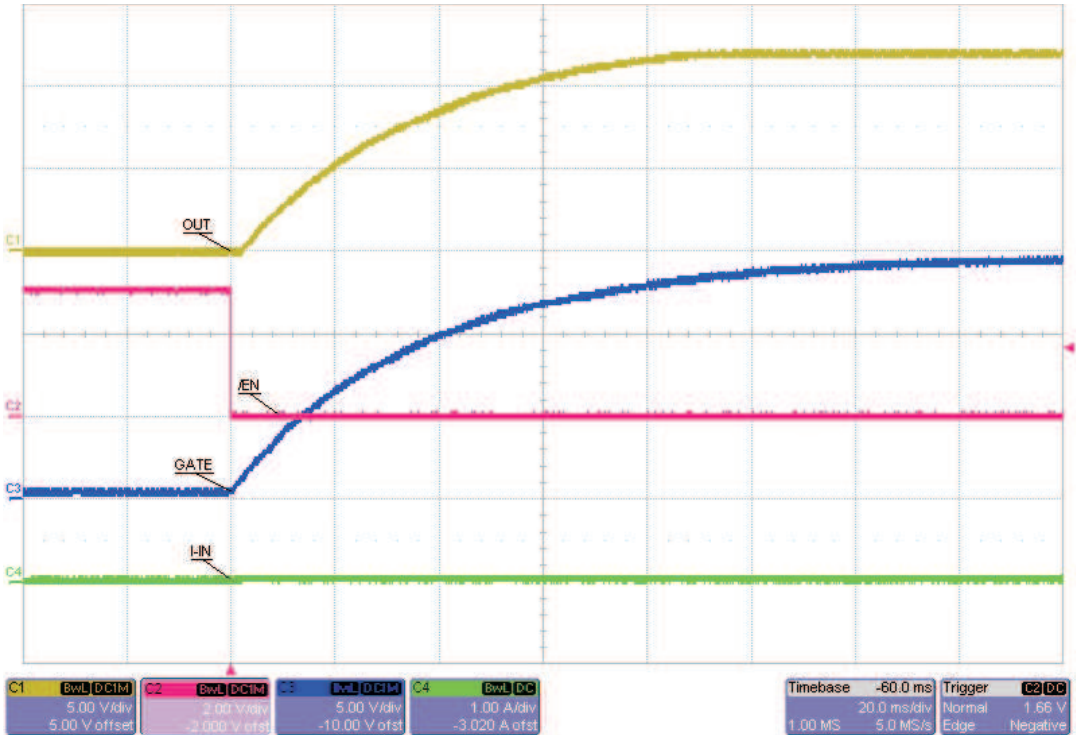


Figure 8. Start Up With Slew Rate Control (C_{EXT} = 0.1 µF)

Thermal Sense

The TPS25910 self protects by using a thermal sensing circuit that monitors the operating temperature of the power switch and disables operation if the temperature exceeds the thermal shutdown condition (160°C typical). The TPS25910 device operates in power-limit mode during an overload condition and increases the voltage drop across power switch. The thermal sensor turns off the power switch when the die temperature exceeds 160°C. Hysteresis is built into the thermal sensor, and the switch turns on after the device has cooled approximately 20°C. Figure 9 below illustrates the thermal behavior during output overload.

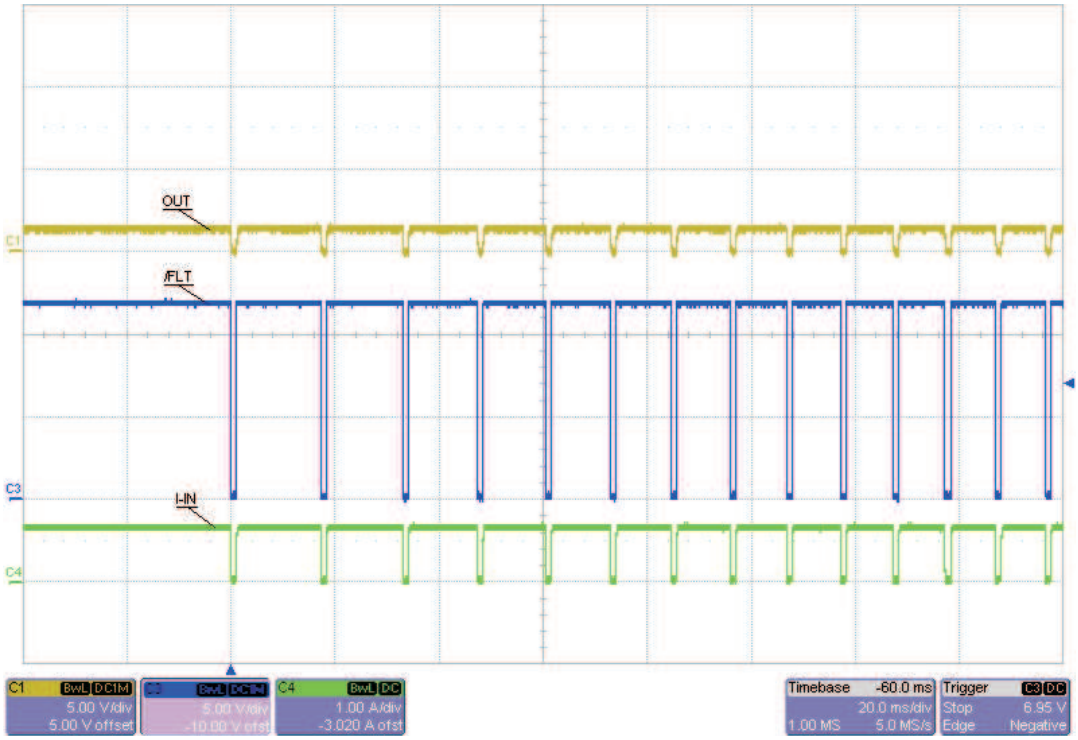


Figure 9. Thermal Sense Behavior

Back-to-Back (B2B) FET Operation

Many applications require reverse current blocking (from load to input source) so that pending system activities can be completed (such as writing important data to non-volatile memory) prior to power down or during brown out. TPS25910 provides the GATE pin externally for slew rate control, but this external connection can also be used to control an external blocking MOSFET, Q1 as shown in Figure 10.

As VIN drops during input power removal, the comparator circuit de-asserts ENb, GATE falls, and both the TPS25910 internal MOSFET and Q1 is turned off and block any current flow from V_{LOAD} to V_{IN}. C_{LOAD} can then be chosen to furnish the required load current for long enough to complete the required power down system activities.

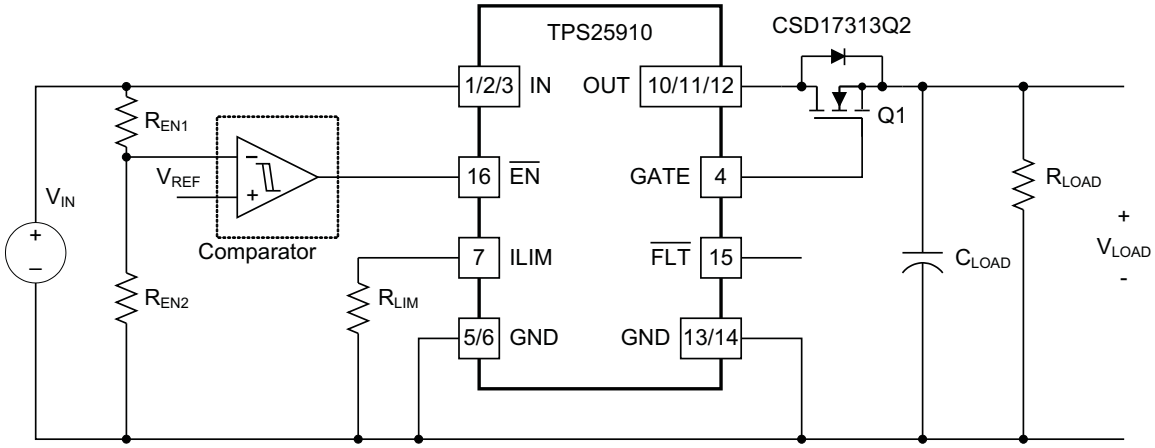


Figure 10. B2B Implementation

NOTE

Connecting the load voltage to the non-inverting input of the external comparator can provide a simple ORing function that prevents holdup energy in C_{LOAD} from discharging through the TPS25910 to $V_{IN(source)}$ when $V_{IN(source)}$ droops or collapses.

Circuit operation is illustrated in Figure 11 and Figure 12. Figure 11 shows the power down event with no load at the output. When V_{IN} drops to approximately 10 V (threshold of comparator circuit), ENb is de-asserted and GATE falls and enables reverse current blocking. The voltage on C_{LOAD} then stops following VIN and remains flat for a long duration.

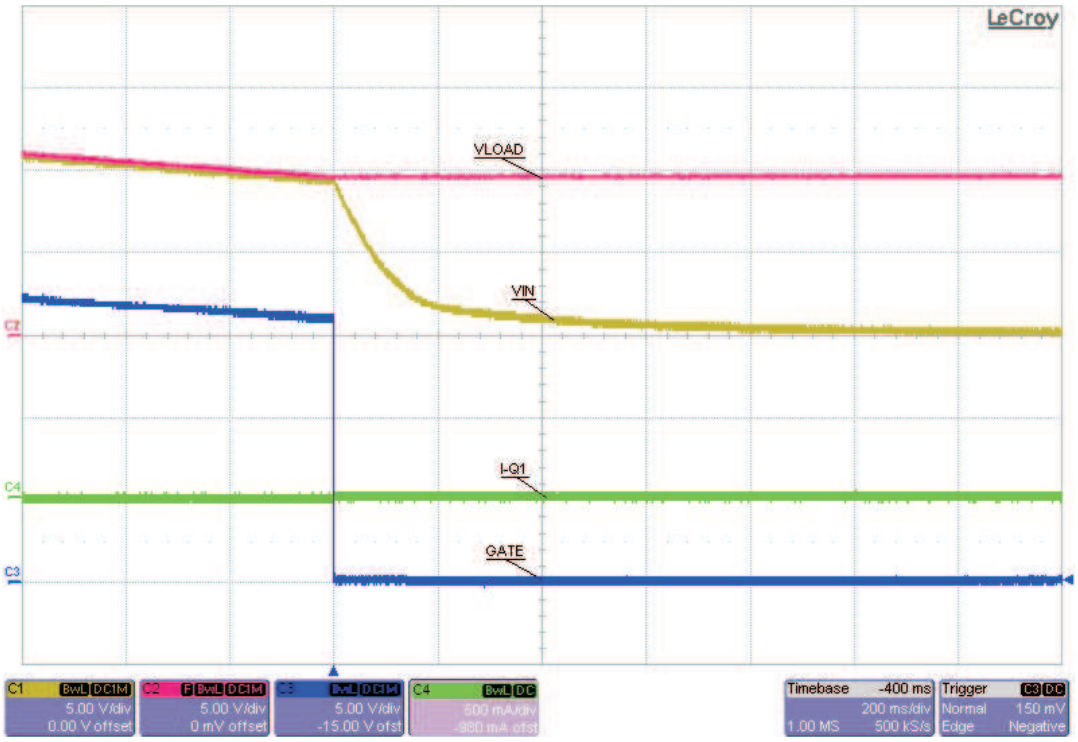


Figure 11. B2B Performance with No-Load

Figure 12 illustrates the power down event with a 200-mA load. As V_{IN} starts to fall, the output load is supplied by C_{LOAD}. C_{LOAD} must be large enough to support V_{LOAD} for long enough for the power down activities to complete. For the case shown in Figure 12, C_{LOAD} is a 3900-µF capacitor and can support a droop from approximately 10 V to approximately 5 V for approximately 170 ms.

TPS3700DDC (dual comparator with wide input voltage range) can be used for the B2B comparator circuit shown in Figure 10. Only one comparator is needed, but the second comparator can be utilized as either a power good flag or as a notification to the system load that a brownout or power down event is about to occur.

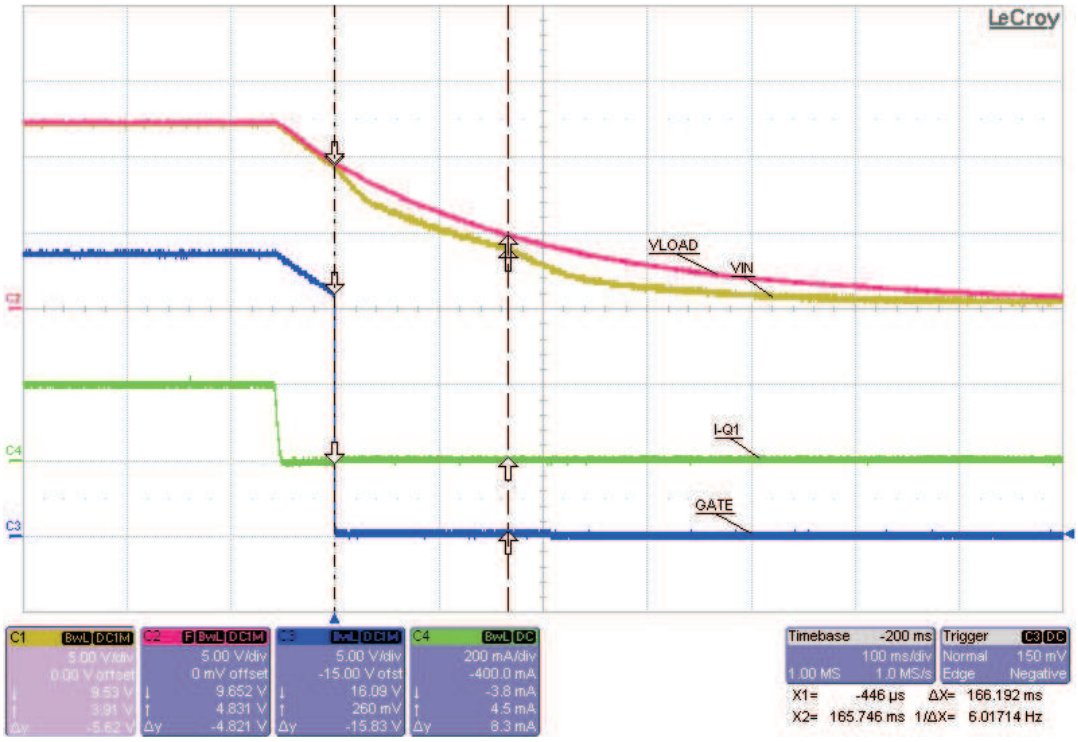


Figure 12. B2B Performance with 200-mA Load

Maximum Load at Startup

The power limiting function of the TPS25910 provides effective protection for the internal FET. Expectedly, there is a supply voltage dependent maximum load which the device is able to power up. Loads above this level may cause the device to shut off current before startup is complete. Neglecting any load capacitance, the maximum load (minimum load resistance) is calculated using Equation 13;

$$R_{MIN} = \frac{V_{IN}^2}{12} \tag{13}$$

Adding load capacitance may reduce the maximum load which can be present at start up.

If $\overline{EN}$ is tied to GND at startup and IN does not ramp quickly, the TPS25910 may momentarily turn off then on during startup. This can happen if a capacitive load pulls down the input voltage below the UV threshold. If necessary, this can be avoided by delaying the $\overline{EN}$ assertion until VIN is fully up.

Transient Protection

The need for transient protection in conjunction with hot-swap controllers should always be considered. When the TPS25910 interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. Such transients can easily exceed twice the supply voltage if steps are not taken to address the issue. Typical methods for addressing transients include;

- Minimizing lead length/inductance into and out of the device.
- Transient Voltage Suppressors (TVS) on the input to absorb inductive spikes.
- Shottky diode across the output to absorb negative spikes.
- A combination of ceramic and electrolytic capacitors on the input and output to absorb energy.

The following equation estimates the magnitude of these voltage spikes:

Where;

$$V_{SPIKE(absolute)} = V_{NOM} + I_{LOAD} \times \sqrt{L/C} \tag{14}$$

- V_{NOM} equals the nominal supply voltage.
- I_{LOAD} equals the load current.
- C equals the capacitance present at the input or output of the TPS25910.
- L equals the effective inductance seen looking into the source or the load.

The inductance due to a straight length of wire equals approximately.

Where;

$$L_{straightwire} \approx 0.2 \times L \times \ln\left(\frac{4 \times L}{D} - 0.75\right) (nH) \tag{15}$$

- L equals the length of the wire.
- D equals wire diameter.

Some applications may require the addition of a TVS to prevent transients from exceeding the absolute ratings if sufficient capacitance cannot be included.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS25910RSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS25910RSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

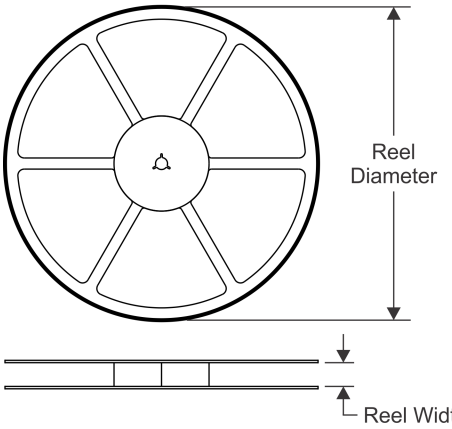
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

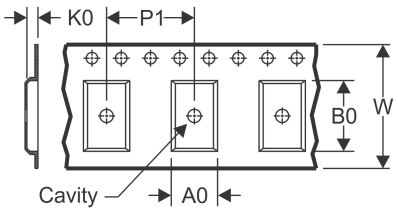
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

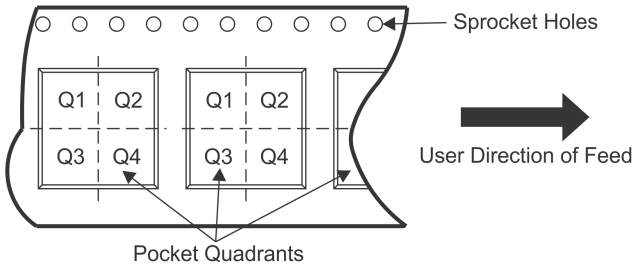


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

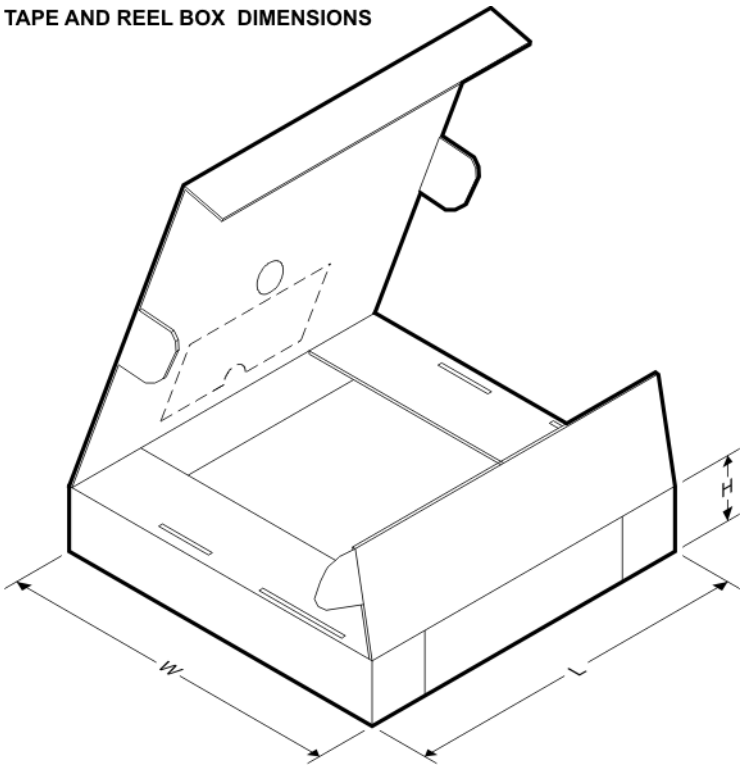
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25910RSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS25910RSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

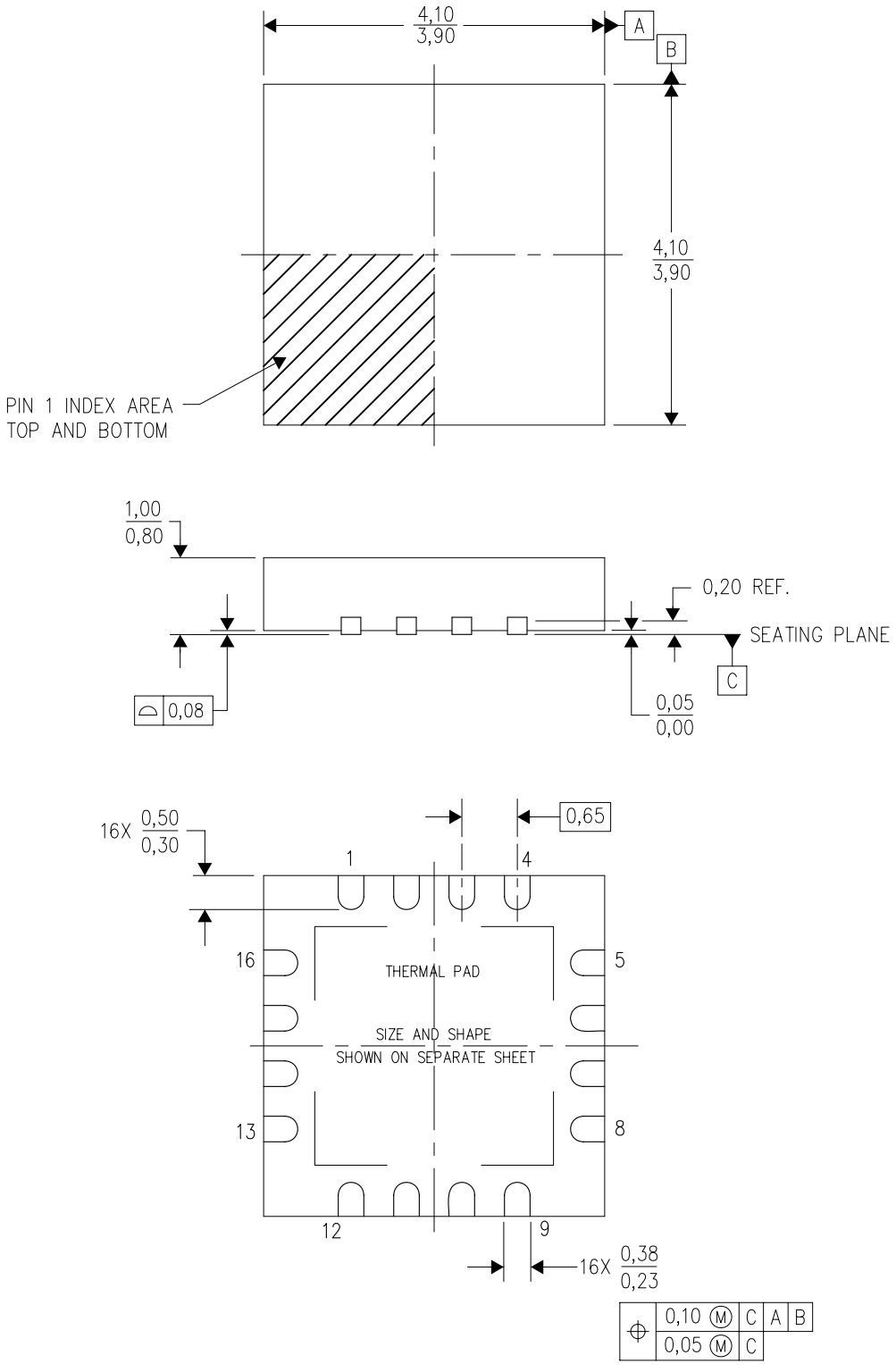
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25910RSAR	QFN	RSA	16	3000	367.0	367.0	35.0
TPS25910RSAT	QFN	RSA	16	250	210.0	185.0	35.0

RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

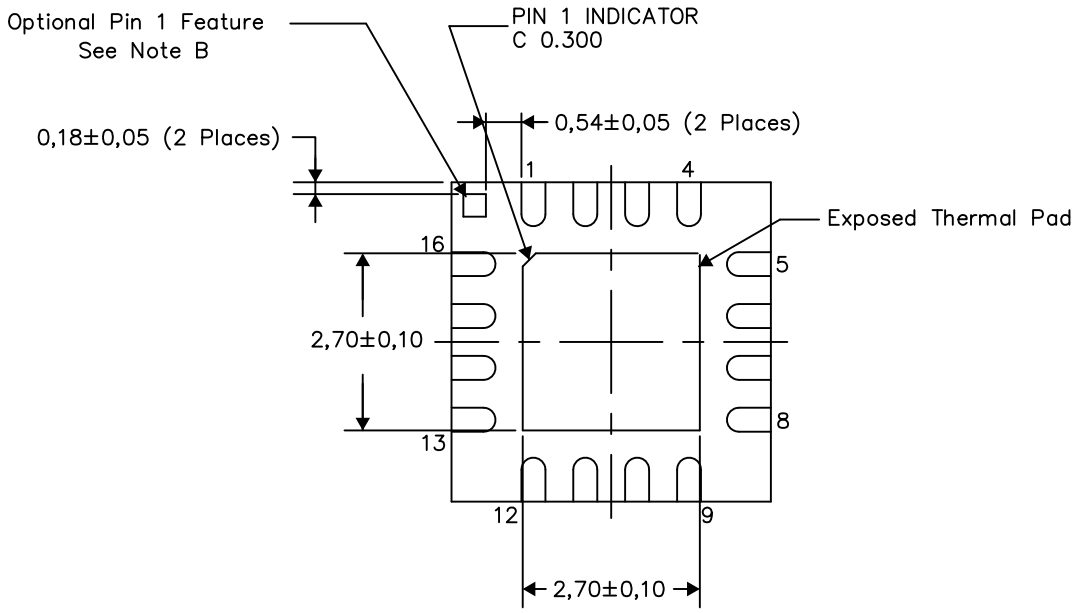
RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

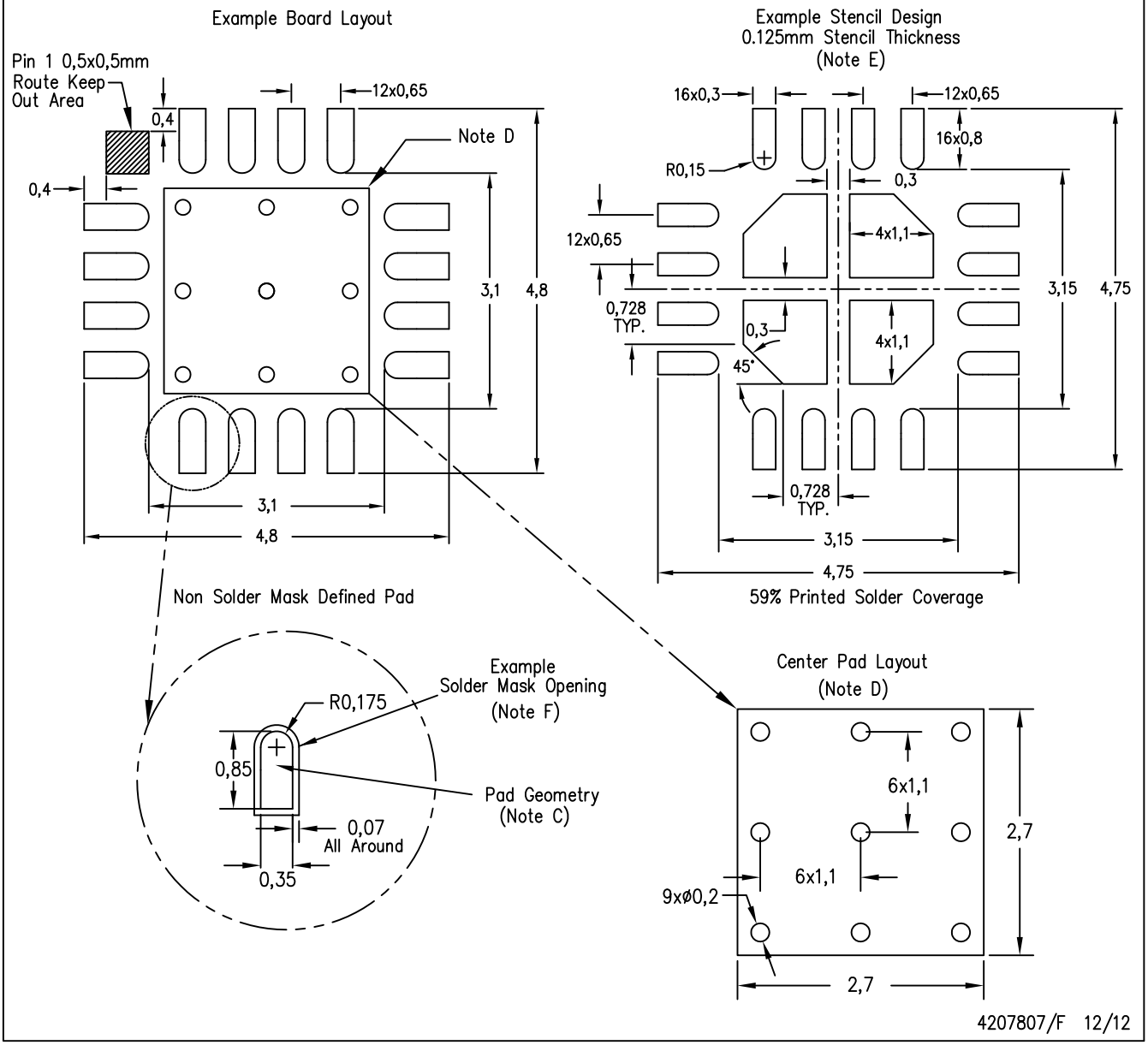
4206364/M 12/12

NOTES:

A. All linear dimensions are in millimeters

B. The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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