CISC 341 - Spring 2015

Assignment #4

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5. How many bits are required to address a 4M × 16 main memory if

a) Main memory is byte-addressable? 23 bytes
b) Main memory is word-addressable? 20 bytes

9. How many 256x8 RAM chips are needed to provide a memory capacity of 4096 bytes? 2

a) How many bits will each address contain? 16
b) How many lines must go to each chip? 8
c) How many lines must be decoded for the chip select inputs? Specify the size of the decoder.
2, one for each chip.

11. Redo Exercise 10 assuming a 16M × 16 memory built using 512K × 8 RAM chips.

12. Suppose we have 1Gx16 RAM chips that make up a 32Gx64 memory that uses high interleaving. (Note: This means that each word is 64 bits in size and there are 32G of these words.)

3600x3 10800
128x2 256
16 16
11072
385r2

a) How many RAM chips are necessary? 385 chips are necessary
b) Assuming 4 chips per bang, how many banks are required? 97 banks
c) How many lines must go to each chip? 16 lines
d) How many bits are needed for a memory address, assuming it is word addressable? 815
e) For the bits in part ?
d), draw a diagram indicating how many and which bits are used for chip select, and how many and which bits are used for the address on the chip.
you did not teach this.
f) Redo this problem assuming low order interleaving is being used instead.

25. Consider the MARIE program below.
a) List the hexadecimal code for each instruction.
b) Draw the symbol table.
c) What is the value stored in the AC when the program terminates? 0x2203

Hex Address	Label	Instruction	
200	Begin,	LOAD Base	0x1200
201		ADD Offs	0x3201
202	Loop,	SUBT One	
203		STORE Addr	0x2203
204		SKIPCOND 800	
205		JUMP Done	
206		JUMPI Addr	
207		CLEAR	
208	Done,	HALT	0x7000
209	Base,	HEX 200	
20A	Offs,	DEC 9	0x0009
20B	One,	HEX 0001	
20C	Addr,	HEX 0000	

43. Suppose we add the following instruction to MARIE's ISA:

IncSZ Operand http://www.cse.wustl.edu/~jbf/cse362.d/cse362.slides.d/Ch2.b.pdf

This instruction increments the value with effective address "Operand," and if this newly incremented value is equal to 0, the program counter is incremented by 1. Basically, we are incrementing the operand, and if this new value is equal to 0, we skip the next instruction. Show how this instruction would be executed using RTN.

ld (:= op= 1) → R[ra] ← M[disp]: c3⟨2..0⟩=2 → R[rc]=0:la (:= op= 5) → R[ra] ← disp:1

50. Suppose some hypothetical system's control unit has a ring (cycle) counter consisting of some number of D flip-flops. This system runs at 1 GHz and has a maximum of 10 microoperations/instruction.

a) What is the maximum frequency of the output (number of signal pulses) output by each flip-flop? 100Mhz

b) How long does it take to execute an instruction that requires only 4 microoperations? 250 nano seconds

It depends on the number of hertz per each microoperation.
http://meseec.ce.rit.edu/eecc550-winter2010/550-12-7-2010.pdf