SOC Dual Channel, Wide Voltage Pin Electronics Solution

ISL55188-AS

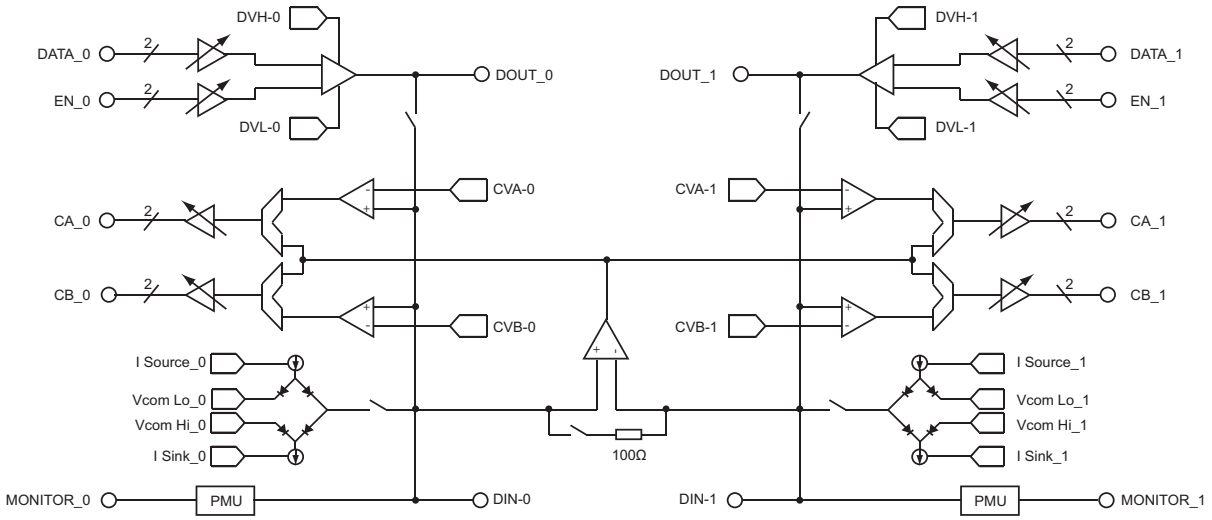
The ISL55188-AS is a highly integrated System-on-a-Chip (SOC) pin electronics solution aimed at incorporating every analog function, along with some digital support functionality, required on a per channel basis for Automated Test Equipment. The interface, control and I/O of the chip are all digital; all analog circuitry is inside the chip. Two complete tester channels are integrated into each ISL55188-AS.

Features

- Pin Electronics Driver
  - 75MHz Fmax
  - 2 Level Driver (DVH/DVL)
  - DC Level Generators On-Chip
  - 24V Driver Output Swings
  - Adjustable Output Voltage Range (–15V to +24V)
  - Programmable Slew Rates (1V/ns to .1V/ns)
  - Iout = 200mA (DC)
  - Extremely Low Leakage Over the Operating Range
- Pin Electronics Comparator
  - Threshold Level Generators On-Chip
  - Extremely Low Leakage over a 32V Range
  - 32V Comparator Input Compliance Range
  - Differential Comparator
- Load
  - 24mA Source/Sink Capability
  - Split Load Configuration
  - Resistive Load Capability
- Deskew
  - Propagation Delay Adjustment
  - Falling Edge Adjustment
  - Delay Range Set by PLL Clock
- PMU
  - 5 Current Ranges (20µA, 200µA, 2mA, 20mA, 200mA)
  - FV/MI
  - FI/MV
  - Imax = 200mA
- On-Chip DC Levels
  - 10 Levels/Channel; 16-bit Levels
  - 16-Bit Gain and 16-Bit Offset Correction/Level
  - DUT Ground Sensing and Correction
- 3-Bit Serial CPU Port
  - 2 Control Bits per Channel (for Ext Relay Support)
- Flexible Real Time Digital Inputs and Outputs
  - 50Ω Serial Terminations for Comparator Outputs
  - Selectable On-Chip Terminations for Inputs
- Package/Power Dissipation
  - Lead-Free
  - 128-Lead, 14mm x 20mm TQFP with Heat Slug
  - Pdq < 1.5 Watts/Channel; Pdq < 3.0 Watts/Chip

Applications

- Automated Test Equipment
- Instrumentation
- ASIC Verifiers



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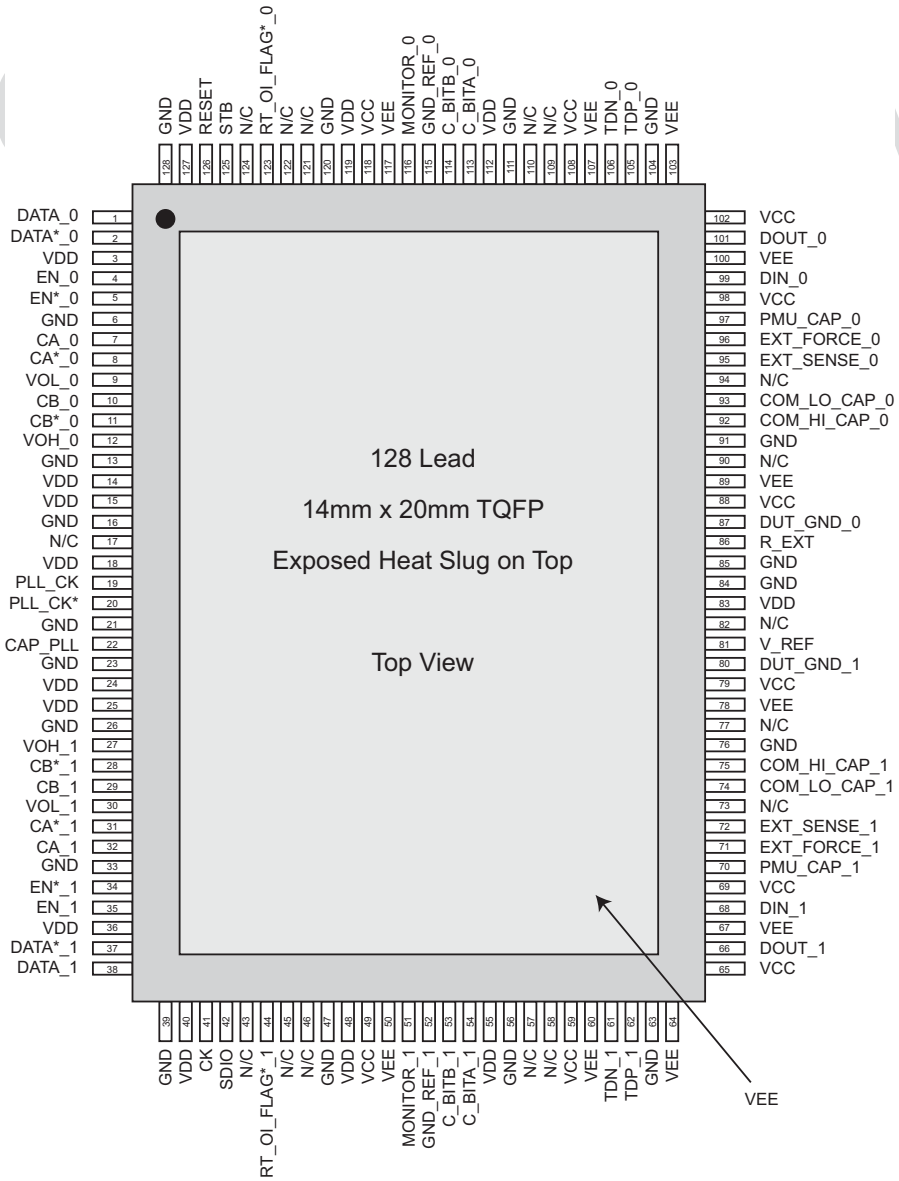
Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
DIGITAL INPUTS		
1, 2	DATA_0, DATA*_0	Channel 0 driver data
4, 5	EN_0, EN*_0	Channel 0 driver enable
38, 37	DATA_1, DATA*_1	Channel 1 driver data
35, 34	EN_1, EN*_1	Channel 1 driver enable
19, 20	PLL_CK, PLL_CK*	Differential PLL reference signal
DIGITAL OUTPUTS		
7, 8	CA_0, CA*_0	Channel 0, comparator A output
10, 11	CB_0, CB*_0	Channel 0, comparator B output
32, 31	CA_1, CA*_1	Channel 1, comparator A output
29, 28	CB_1, CB*_1	Channel 1, comparator B output
113, 114	C_BITA_0, C_BITB_0	Channel 0 control bits
54, 53	C_BITA_1, C_BITB_1	Channel 1 control bits
123, 44	RT_OI_FLAG*_0, RT_OI_FLAG*_1	Open drain output indicating an over-current flag
DUT PINS		
101, 66	DOUT_0, DOUT_1	Analog I/O pin that connects to Device Under Test
99, 68	DIN_0, DIN_1	Analog input pin that connects to the window comparator and load
ANALOG PINS		
81, 22, 86	V_REF, CAP_PLL, R_EXT	External reference pins
97, 70	PMU_CAP_0, PMU_CAP_1	External compensation pins
87, 80	DUT_GND_0, DUT_GND_1	Analog voltage input used to track GND at the DUT
96, 95	EXT_FORCE_0, EXT_SENSE_0	Channel 0 external PMU connection pins
71, 72	EXT_FORCE_1, EXT_SENSE_1	Channel 1 external PMU connection pins
92, 93	COM_HI_CAP_0, COM_LO_CAP_0	Channel 0 output of the load high commutating buffers
75, 74	COM_HI_CAP_1, COM_LO_CAP_1	Channel 1 output of the load high commutating buffers
116, 115	MONITOR_0, GND_REF_0	Analog voltage pins used to track channel 0 parameters
51, 52	MONITOR_1, GND_REF_1	Analog voltage pins used to track channel 1 parameters
105, 106	TPD_0, TDN_0	Channel 0 thermal diodes
62, 61	TDP_1, TDN_1	Channel 1 thermal diodes
CPU INTERFACE		
41, 42, 125	CK, SDIO, STB	3-bit serial port (Clock, Data, Strobe)
126	RESET	Chip reset
POWER SUPPLIES		
3, 14, 15, 18, 24, 25, 36, 40, 48, 55, 83, 112, 119, 127	VDD	Digital power supply
6, 13, 16, 21, 23, 26, 33, 39, 47, 56, 63, 76, 84, 85, 91, 104, 111, 120, 128	GND	Device ground

Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
49, 59, 65, 69, 79, 88, 98, 102, 108, 118	VCC	Positive analog voltage supply
50, 60, 64, 67, 78, 89, 100, 103, 107, 117	VEE	Negative analog voltage supply
12, 9	VOH_0, VOL_0	Channel 0 comparator output levels supplies
27, 30	VOH_1, VOL_1	Channel 1 comparator output level supplies
MISCELLANEOUS		
17, 43, 45, 46, 57, 58, 73, 77, 82, 90, 94, 109, 110, 121, 122, 124	N/C	No connection

Pin Configuration



Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Power Supplies				
VCC	**VDD – 0.4**		**+30**	**V**
VEE	**–20**		**+0.4**	**V**
VCC – VEE	**0**		**+34**	**V**
VDD	**–0.4**		**+5**	**V**
VOH			**VDD + 0.5**	**V**
VOL	**GND – 0.5**			**V**
Input/Output HiZ Compliance				
DOUT	**VEE – 0.5**		**VCC + 0.5**	**V**
DIN	**VEE – 0.5**		**VCC + 0.5**	**V**
Monitor				
MONITOR Output Compliance	**VEE – 0.5**		**VCC + 0.5**	**V**
Flags, Control Bits				
RT-OI_FLAG*_#	**GND – 0.5**		**VDD + 0.5**	**V**
C_BIT_A_#, C_BIT_B_#	**GND – 0.5**		**VCC + 0.5**	**V**
Output Currents				
CA, CB	**–80**		**80**	**mA**
SDIO	**–20**		**20**	**mA**
External References				
V_REF	**GND – 0.25V**		**VCC + 0.25**	**V**
EXT_SENSE	**VEE – 0.5**		**VCC + 0.5**	**V**
EXT_FORCE	**VEE – 0.5**		**VCC + 0.5**	**V**
Thermal Information				
Junction Temperature	**–55**		**150**	**°C**

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Power Supplies				
VCC	+10		+29	V
VEE	–18		–3	V
VDD	+3.25	+3.3	+3.5	V
GND		0		V
VCC – VEE	+13		+32	V
Comparator Output Supplies				
VOH			VDD	V
VOL	GND			V
VOH – VOL	0.4		VDD – GND	V
Digital Inputs				
CK, SDIO, STB, RESET	GND		VDD	V
Driver				
DVH (in Drive Mode)	VEE + 5		VCC – 3	V
DVH (in PMU Mode)	VEE + 4		VCC – 3	V
DVL	VEE + 4		VCC – 7	V
DVH – DVL	0.5			V
DOUT (in HiZ)	VEE		VCC	V
DC Output Current	–200		+200	mA
Comparator				
CVA, CVB	VEE + 2		VCC – 7	V
DIN	VEE		VCC	V
Load				
Vcom Lo, Vcom Hi	VEE + 2		VCC – 7	V
Load Voltage Compliance (in HiZ)	VEE		VCC	V
Monitor				
Monitor Output Operating Range	VEE + 1		VCC – 3	V
Monitor Output Compliance	VEE		VCC	V
Flags, Control Bits				
RT_OI_FLAG*_#	GND		VDD	V
C_BIT_A_#, C_BIT_B_#	GND		VCC	V
External References				
V_REF	+2.99	+3.0	+3.01	V
PLL_CK	50		100	MHz
EXT_SENSE	VEE		VCC	V
EXT_FORCE	VEE		VCC	V
DUT_GND	–3		+3	V
R_EXT		10		KΩ
Miscellaneous				
Junction Temperature	25		100	°C
CPU Port Frequency	10		25	MHz

DC Characteristics

NOTE: For all of the following DC Electrical Specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

DC Characteristics - Power Supplies and Junction Temperature

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	Pd (TYP)
Positive Supply; Static; PLL_CK = 50MHz							
11120	VCC	VCC = +27V, VEE = –5V, VDD = +3.3V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0. All deskew elements bypassed, no elements selected. Isource, Isink = 0. Driver in HiZ. Slew Rate = 01111; Drv-Bias = 000	90	130	180	mA	3.5W
11220	VEE		100	150	200	mA	750mW
11320	VDD		160	200	240	mA	660mW
							4.9W/Chip 2.5W/Chan
Positive Supply; No Load; Dynamic; PLL_CK = 100MHz							
11130	VCC	VCC = +27.5V, VEE = –5.5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0. All deskew elements selected. Channel 0 and Channel 1 configured as ring oscillators. Isource, Isink = 0. Slew Rate = 0111; Drv-Bias = 000; DVH = +14V, DVL = –2V	120	170	220	mA	4.6W
11230	VEE		140	185	235	mA	925mW
11330	VDD		200	250	300	mA	825mW
							6.34W/Chip 3.2W/Chan
Positive Supply; With Load; Dynamic; PLL_CK = 100MHz							
11100	VCC	VCC = +27.5V, ,VEE = –5.5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0. All deskew elements selected. Channel 0 and Channel 1 configured as ring oscillators. Isource, Isink = 12mA. Slew Rate = 0111; Drv-Bias = 000; DVH = +14V, DVL = –2V	160	200	250	mA	5.4W
11200	VEE		170	215	270	mA	1.075W
11300	VDD		200	250	300	mA	825mW
							7.3W/Chip 3.65W/Chan
Negative Supply; With Load; Dynamic; PLL_CK = 100MHz							
11110	VCC	VCC = +16.5V, ,VEE = –16.5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0. All deskew elements selected. Channel 0 and Channel 1 configured as ring oscillators. Isource, Isink = 12mA. Slew Rate = 0111; Drv-Bias = 000; DVH = +8V, DVL = –8V	160	205	250	mA	3.4W
11210	VEE		170	220	275	mA	3.63W
11310	VDD		200	250	300	mA	825mW
							7.8W/Chip 3.9W/Chan
Junction Temperature							
11000	Junction Temperature	VCC = +27.5V, VEE = –5.5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0. All deskew elements selected. Channel 0 and Channel 1 configured as ring oscillators. Isource, Isink = 0. DVH = +14V, DVL = –2V	45		115	°C	

DC Electrical Specifications – CPU Port

VCC = +27V, VEE = –5V, VDD = +3.3V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0 unless otherwise noted.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SDIO, CK, STB, RESET						
17100	VIH		2.0			V
17110	VIL				0.8	V
17120	Iin (Input Leakage Current)	Tested at 0V, VDD. VCC = +27.5V, VEE = –5.5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0.	–100	0	+100	nA
17200	VOH (SDIO only)	Output Current = 2mA sourcing	2.4			V
17210	VOL (SDIO Only)	Input Current = 2mA sinking			0.8	V

DC Electrical Specifications – Control Bits

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
C_BIT_A, C_BIT_B						
17300	VOL (sinking 20mA)	VCC = +27V, VEE = –5V, VDD = +3.3V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0			0.5	V
17310	IOH (HiZ Leakage)	Tested at 0V, VDD. VCC = +27.5V, VEE = –5.5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0	–100		+100	nA

DC Electrical Specifications – Analog Pins

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
10999	V_REF Input Current	Note 1	–1	0	+1	µA
10998	GND_REF#, DUT_GND_# Input Current	Tested at 0V, VDD. Note 1.	–25	0	+25	nA
10996	PMU_CAP_# Leakage	Tested at (VCC + VEE) / 2. Notes 1 and 2	–5	0	+5	nA
10997	PMU_CAP_# Leakage	Tested at VCC and VEE + 0.25V. Notes 1 and 2	–10	0	+10	nA
10996	EXT_FORCE_# HiZ Leakage	Tested at (VCC + VEE) / 2. Notes 1 and 2	–5	0	+5	nA
10997	EXT_FORCE_# HiZ Leakage	Tested at VCC and VEE + 0.25V. Notes 1 and 2	–10	0	+10	nA
10996	EXT_SENSE_# HiZ Leakage	Tested at (VCC + VEE) / 2. Notes 1 and 2	–5	0	+5	nA
10997	EXT_SENSE_# HiZ Leakage	Tested at VCC and VEE + 0.25V. Notes 1 and 2	–10	0	+10	nA
	Capacitance on EXT_FORCE_#	Limits established by characterization and are not production tested. All other switches open.		10		pF
	Capacitance on EXT_SENSE_#			5		pF

NOTES:

1. VCC = +27.5V, VEE = –5.5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0.
2. VCC = +16.5V, VEE = –16.5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0.

DC Electrical Specifications – PLL

VCC = +27V, VEE = –5V, VDD = +3.3V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0 unless otherwise indicated.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Differential Inputs PLL_CK/PLL_CK#						
	Differential Input Swing - VIH	PLL_CK = 50MHz; VIH = 2.1V, VIL = 1.9V; VIH = 1.1V, VIL = 0.9V; Note 6	0.2		VDD	V
	Differential Input Swing - VIL		0		VDD	V
	Differential Input Swing - Crossing Voltage		0.5		2.25	V
18100	Input Leakage Current	Tested @ 0V, VDD. PLL-ZA = 0, PLL-ZB = 0; 1.5V @ 6mA. Note 3	–100	0	+100	nA
18110	Differential Input Resistance	Notes 4 and 5		105		Ω

NOTES:

3. VCC = +27.5V, VEE = –5.5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0.
4. PLL-ZA = 1; PLL-ZB = 0; 1.5V @ 6mA.
5. PLL-ZA = 0; PLL-ZB = 1; 1.5V @ 6mA.
6. Limits established by characterization and are not production tested.

DC Electrical Specifications – Level DAC Calibration

VCC = +26.9V, VEE = –4.9V, VDD = +3.25V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0. All DC tests are performed after the DAC is first calibrated. The upper 5 bits of the Level DAC are calibrated in the sequence D11 to D15. the DAC Cal bits are adjusted to make the major carries as small as possible.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
16150	Level DAC D15 Step Error	Code 8000 – Code 7FFF – LSB; VR1. Note 7	–5		5	mV
16160	Level DAC D14 Step Error	Code 4000 – Code 3FFF – LSB; VR1. Note 8	–5		5	mV
16170	Level DAC D13 Step Error	Code 6000 – Code 5FFF – LSB; VR1. Note 9	–5		5	mV
16180	Level DAC D12 Step Error	Code 7000 – Code 6FFF – LSB; VR1. Note 10	–5		5	mV
16190	Level DAC D11 Step Error	Code 7800 – Code 77FF – LSB; VR1. Note 11	–5		5	mV

NOTES:

7. (DAC @ 8000 – DAC @ 7FFF) / (8000 – 7FFF) – DAC LSB; VR1
8. (DAC @ 7000 – DAC @ 3000) / (7000 – 3000) – DAC LSB; VR1
9. (DAC @ 7000 – DAC @ 5000) / (7000 – 8000) – DAC LSB; VR1
10. (DAC @ 7000 – DAC @ 6000) / (7000 – 6000) – DAC LSB; VR1
11. (DAC @ 7800 – DAC @ 7000) / (7800 – 7000) – DAC LSB; VR1

DAC

There are 3 on-chip internal DACs per channel used for:

1. DC Level
2. DC Level Offset Correction
3. DC Level Gain Correction

These on-chip DACs are not used off-chip explicitly as stand-alone outputs. Rather, they are internal resources that are used by every functional block. The DACs are tested many times over by the DC tests for driver and comparator. However, the DACs are specifically tested independently from all other functional blocks to verify basic functionality.

DC Electrical Specifications – DAC

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Level DAC						
16100	Span	DVH in VR1 via Diag Mux (Monitor); Span = DAC(FFFF) – DAC(0000); Notes 12, 13	7.5	8.0	8.7	V
16110	Linearity	DVH in VR1 via Diag Mux (Monitor); Notes 12, 13, 16	–10	0	+10	mV
16120	Bit Test	DVH in VR1 via Diag Mux (Monitor); Notes 12, 13, 17	–10	0	+10	mV
16400	DAC Noise Test	Notes 12, 18			+1	mV
16190	Droop Test	Notes 12, 19			3	mV/ms
Offset DAC Test						
16200	+Adjustment Range	DVH in VR1 via Diag Mux (Monitor); Code 0000, FFFF relative to mid-scale (8000); Notes 12, 14	+4.5	+5.4	+6.0	% of Span
16210	–Adjustment Range	DVH in VR1 via Diag Mux (Monitor); Code 0000, FFFF relative to mid-scale (8000); Notes 12, 14	–6.0	–5.4	–4.5	% of Span
16220	Linearity	DVH in VR1 via Diag Mux (Monitor); Notes 12, 14, 16	–10	0	+10	mV
16230	Bit Test	DVH in VR1 via Diag Mux (Monitor); Notes 12, 14, 17	–10	0	+10	mV
16250	Major Carry Error	DVH in VR1 via Diag Mux (Monitor); DAC Code 8000 – 7FFF – 1LSB; Notes 12, 15	–20	0	+5	mV
Gain DAC Test						
16300	+Adjustment Range	DVH in VR1 via Diag Mux (Monitor); Notes 12, 15	1.07	1.125	1.15	V/V
16310	–Adjustment Range	DVH in VR1 via Diag Mux (Monitor); Notes 12, 15	.850	.875	.922	V/V
16320	Linearity	DVH in VR1 via Diag Mux (Monitor); Notes 12, 15, 16	–5	0	+5	mV
16330	Bit Test	DVH in VR1 via Diag Mux (Monitor); Notes 12, 15, 17	–5	0	+5	mV
16350	Major Carry Error	DVH in VR1 via Diag Mux (Monitor); DAC Code 8000 – 7FFF – 1LSB; Notes 12, 15	–20	0	+5	mV
16360	Gain DAC Calibration	Excludes DVH and DVL in VR0; Note 12	.875		1.125	V/V
Offset DAC Calibration						
16260	DAC in VR0	Excludes DVH and DVL in VR0; Note 12	–200		+200	mV
16270	DAC in VR1	Excludes DVH and DVL in VR0; Note 12	–400		+400	mV
16280	DAC in VR2	Excludes DVH and DVL in VR0; Note 12	–800		+800	mV
16290	DAC in VR3	Excludes DVH and DVL in VR0; Note 12	–1,600		+1,600	mV
Vmid DAC						
16440	Linearity	DVH in VR1 via Diag Mux (Monitor); Notes 12, 20	–20		+20	mV

DC Electrical Specifications – DAC

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS

NOTES:

12. VCC = +26.9V, VEE = –4.9V, VDD = +3.25V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.
13. Offset and Gain DACs both programmed to midscale (Code 7FFF).
14. Level and Offset DACs both programmed to midscale (Code 7FFF).
15. Level DAC = FFFF, Offset DAC = 7FFF.
16. Linearity Test: 16 equal spaced codes relative to a straight line determined by 1/8 and 7/8 measurement points: 0000, 0FFF, **1FFF**, 2FFF, 3FFF, 4FFF, 5FFF, 6FFF, 7FFF, 8FFF, 9FFF, AFFF, BFFF, CFFF, **DFFF**, EFFF, FFFF.
17. Bit Test: Walking 1 and walking 0 to determine the correct bit weight — 1's: 8000, 4000, 2000, 1000, 0800, 0400, 0200, 0100, 0080, 0040, 0020, 0010, 0000; 0's — 7FFF, BFFF, DFFF, EFFF, F7FF, FBFF, FDFF, FEFF, FF7F, FFBF, FFDF, FFEF, FFF7, FFFB, FFFD, FFFE.
18. Measured @ DOUT_0; RMS measurement, DVH = 0V, VR3.
19. CPU CK turned off. 256ms between measurements. Each DC level checked one at a time.
20. Linearity Test — 16 all codes relative to a straight line determined by 2/15 and 13/15 measurement points: 0000, 0001, **0010**, 0011 ... 1100, **1101**, 1110, 1111; DAC Code = 7FFF, FV Mode, VR1

DC Electrical Specificatons – Driver

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
13300	DOUT HiZ Leakage	Tested @ DOUT = (VCC + VEE) / 2; Notes 21, 22	–25		+25	nA
13310	DOUT HiZ Leakage	Tested @ DOUT = VCC – 2, VEE + 3; Notes 21, 22	–25		+25	nA
13110	DVH, DVL Post Cal Error (Range 1)	VR1 Test Points, IR3; TP1; Note 23	–30		+30	mV
13120	DVH, DVL Post Cal Error (Range 2)	VR2 Test Points, IR3; TP2; Note 23	–40		+40	mV
13130	DVH, DVL Post Cal Error (Range 3)	VR3 Test Points, IR3; TP3; Note 23	–50		+50	mV
13140	DVH, DVL Post Cal Error (Range 3)	VR3 Test Points, IR3; TP4; Notes 23 and SP1	–50		+50	mV
13320	DOUT Output Impedance	IR4; Notes 24, 25		11		Ω
13321	DVH, DVL DC Output Current	IR4; Notes 24, 26	±200			mA
Differential Inputs DATA and EN						
	VIH (DATA – DATA*; EN – EN*)	Notes 27, 28, 29			VDD	V
	VIL (DATA* – DATA; EN* – EN)	Notes 27, 28, 29	0			V
13210	Input Leakage Current	Tested @ VDD, 0V; Notes 22, 30	–100	0	+100	nA
13220	Differential Input Resistance	Note 31 or 32		105		Ω

NOTES:

21. VCC = +16.5V, VEE = –16.5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.
22. VCC = +27.5V, VEE = –5.5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.
23. VCC = +26.9V, VEE = –4.9V, VDD = +3.25V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.
24. VCC = +27V, VEE = –5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.
25. Output impedance test conditions; DVH = 3V @ 100mA; DVL = 0V @ 100mA.
26. DOUT forcing +5V and shorted to GND, forcing 0V and shorted to +5V, I-Limit-Dis = 0.
27. Limits established by characterization and are not production tested.
28. DATA, EN = 2.1V, DATA*, EN* = 1.9V.
29. DATA, EN = 1.9V, DATA*, EN* = 2.1V.
30. DZ#<1:0> = 00, EZ#<1:0> = 00; 1.5V @ 6mA.
31. DZ#<1:0> = 01, EZ#<1:0> = 01; 1.5V @ 6mA.
32. DZ#<1:0> = 10, EZ#<1:0> = 10; 1.5V @ 6mA.

SP1: Calibrated and tested with slew rate = 31, DrBias = 1. The DVH/DVL tests are performed with a separation voltage of 0.75V. (DVH – DVL = 0.75). DVH is always greater than DVL.

TABLE 1. Test and Cal Points

Test Point	Voltage Range	Vmid	Cal Points	DVL Test Points	DVH Test Points
TP1	VR1	+3V	0V, +5V	–1V, +3V, +6V	0V, +3V, +7V
TP2	VR2	+4.5V	0V, +10V	–1V, +5V, +11.5V	0V, +5V, +12.5V
TP3	VR3	+9.0	0V, +20V (DVH), +15V (DVL)	–1V, +10V, +20V	0V, +10V, +24V
TP4	VR3	+9.0	0V, +20V (DVH), +15V (DVL)	+19V, +19.5V, +20V	+19.75V, +20V, +25V, +20.75V

DC Electrical Specifications – Comparator

Window comparator thresholds are tested using a binary search algorithm at the digital outputs COMP_A and COMP_B.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
14400	DIN Input Leakage Current	Tested at DIN = (VCC + VEE) / 2; Notes 33, 34	–10	0	+10	nA
14420	DIN Input Leakage Current	Tested @ DIN = VCC, VEE; Notes 33, 34	–15	0	+15	nA
14500	Post Calibration Threshold Error, VR0	Notes 35, 37	–15		+15	mV
14501	Post Calibration Threshold Error, VR1	Notes 35, 38	–20		+20	mV
14502	Post Calibration Threshold Error, VR2	Notes 35, 39	–30		+30	mV
14503	Post Calibration Threshold Error, VR3	Notes 35, 40	–50		+50	mV
13360	Comparator Output Impedance	VOH = +3V, sourcing 20mA; VOL = 0V, sinking 20mA; Note 36		40		Ω
13361	Differential Comparator Input Impedance	Tested at 6mA @ 1.5V; Note 36		100		Ω

NOTES:

33. VCC = +16.5V, VEE = –16.5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.
34. VCC = +27.5V, VEE = –5.5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.
35. VCC = +26.9V, VEE = –4.9V, VDD = +3.25V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.
36. VCC = +27V, VEE = –5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.
37. Comparator threshold test points, VR0, test the internal references via Test & Cal Mux.
38. Comparator threshold test points, VR1, test the internal references via Test & Cal Mux.
39. Comparator threshold test points, VR2, test the internal references via Test & Cal Mux.
40. Comparator threshold test points, VR3, test the comparator outputs using a binary search.

TABLE 2. COMPARATOR THRESHOLD

V Range	Cal Points	Test Points
VR0	0V +3V (Vmid = +1.5V)	–0.5V +1.5V +3.5V
VR1	0V +5V (Vmid = +3.0V)	–1V +3V +7V
VR2	0V +10V (Vmid = +4.5V)	–3V +5V +12.5V
VR3	0V +20V (Vmid = +9V)	–3V +10V +20V

DC Electrical Specifications – Load

VCC = +26.9V, VEE = –4.9V, VDD = +3.25V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V. Load currents calibrated using a 4-segment calibration at the 20% and 80% points within each segment, tested at 0%, 25%, 50%, 75% and 100% Imax.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
10900	Sink Current Post Cal Error	Note 41.	–1		+1	% Imax
10900	Source Current Post Cal Error	Note 41	–1		+1	% Imax
Vcom Lo/Vcom Hi						
10920	VR0	Vcom in bypass mode. Source and sink = 0. No external current load. Rload = 250Ω	–15		+15	mV
10930	VR1		–20		+20	mV
10940	VR2		–25		+25	mV
10950	VR3		–50		+50	mV

NOTES:

41. Source and sink current calibrated using a 4-setment software calibration at the 20% and 80% points within each segment. Vcom = +11V. Force output pin to 8V, 14V.

TABLE 3. VCOM CALIBRATION TABLE

V Range	Cal Points	Test Points
VR0	0V +3V (Vmid = +1.5V)	–0.5V +1.5V +3.5V
VR1	0V +5V (Vmid = +3.0V)	–1V +3V +7V
VR2	0V +10V (Vmid = +4.5V)	–3.0V +5V +12.5V
VR3	0V +15V (Vmid = +9V)	–3V +10V +20V

DC Electrical Specifications – Current Alarms

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Alarm Errors						
14510	IR0	Notes 42, 45	0X0000		0XFFFF	
14520	IR1	Notes 42, 45	0X0000		0XFFFF	
14530	IR2	Notes 42, 45	0X0000		0XFFFF	
14540	IR3	Notes 42, 45	0X0000		0XFFFF	
14550	IR4	FS = 800mA, Imax = 200mA; Notes 42, 45	0X0000		0XFFFF	
RT_OI_FLAG*_#						
14570	VOL (sinking 8mA)	Note 43			0.4	V
14571	IOH (HiZ Leakage)	Tested @ 0V, VDD; Note 44	–100		+100	nA

NOTES:

42. VCC = +26.9V, VEE = –4.9V, VDD = +3.25V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.
43. VCC = +27V, VEE = –5V, VDD = +3.45V, R_EXT = 10kΩ V_REF = 3V, DUT_GND = 0V.
44. VCC = +27.5V, VEE = –5.5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.
45. Tested in FV/MI Mode @ +11V. Cal at ±80%. Offset is adjusted for least error at 0 current. Gain is set to maximum. Binary search using the comparators @ –Imax, 0, + Imax. Binary search must return a level DAC code value > 0x0000 and <0xFFFF at each test point for the part to pass. This guarantees that the alarms can be calibrated in software.

DC Electrical Specifications – Measure Voltage

MONITOR is tested post 2-point software calibration.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
10996	Monitor HiZ Leakage Current	Tested at MONITOR = (VCC + VEE) / 2; Notes 46, 47	–5	0	+5	nA
10997	Monitor HiZ Leakage Current	Tested at MONITOR = VCC, VEE + 0.25V; Notes 46, 47	–10	0	+10	nA
14700	Monitor Output Impedance	Tested at +2V, Iout = 0µA, 1mA; Note 48		.6	1	kΩ
14701	Ground Reference Output Impedance	Tested at +0V, Iout = 0µA, 1mA; Note 48		.750	1	kΩ
14720	Voltage Error	Monitor Test Points; Note 49	–5		+5	mV
	MV Temperature Coefficient	Notes 49, 50		+50		µV/°CV
14741	GND_REF_#Error	DUT_GND = ±1V, Measure GND_REF w/Sel-Gnd-Ref# = 1; Note 49	–5		+5	mV
14742	DUT_GND_#Error	DUT_GND = ±1V, FV Mode, DVH = +3V, Measured at Test & Cal relative to GND; Note 49	–15		+15	

NOTES:

46. VCC = +16.5V, VEE = –16.5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.
47. VCC = +27.5V, VEE = –5.5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.
48. VCC = +27V, VEE = –5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.
49. VCC = +26.9V, VEE = –4.9V, VDD = +3.25V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.
50. Limits established by characterization and are not production tested.

TABLE 4. Measure Voltage Cal & Test Points

MV Cal Points	MV Test Pionts
0V/0µA	–3V/0µA
+20V/0µA	+10V/0µA
	+24V/0µA

DC Electrical Specifications – Measure Current

MI tested in VR3, IR0 – IR4. MI is calibrated separately for sourcing and sinking current. 2-point calibration plus 4-point CMRR calibration.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MI (Post Calibration)						
14100	MI Accuracy	IR0; Slew Rate = 00100; Drv-Bias = 000; Note 51	–1		+1	% Imax
14101	MI Accuracy	IR1; Slew Rate = 00100; Drv-Bias = 000; Note 51	–0.5		+0.5	% Imax
14102	MI Accuracy	IR2; Slew Rate = 00100; Drv-Bias = 000; Note 51	–0.5		+0.5	% Imax
14103	MI Accuracy	IR3; Slew Rate = 00100; Drv-Bias = 000; Note 51	–0.5		+0.5	% Imax
14104	MI Accuracy	In current range IR4, Imax = 200mA, FS = 925mA; Slew Rate = 00100; Drv-Bias = 000; Note 51	–1		+1	% FS
MI Common Mode						
14110	MI Accuracy	IR0; Slew Rate = 00100; Drv-Bias = 000; Note 51	–1.5		+1.5	% Imax
14111	MI Accuracy	IR1; Slew Rate = 00100; Drv-Bias = 000; Note 51	–1		+1	% Imax
14112	MI Accuracy	IR2; Slew Rate = 00100; Drv-Bias = 000; Note 51	–1		+1	% Imax
14113	MI Accuracy	IR3; Slew Rate = 00100; Drv-Bias = 000; Note 51	–1		+1	% Imax
14114	MI Accuracy	In current range IR4, Imax = 200mA, FS = 925mA; Slew Rate = 00100; Drv-Bias = 000; Note 51	–1		+1	% FS
MI Temperature Coefficient						
	IR0	Note 52		.002		%FS / °C
	IR1	Note 52		.002		%FS / °C
	IR2	Note 52		.002		%FS / °C
	IR3	Note 52		.003		%FS / °C
	IR4	Note 52		.003		%FS / °C

NOTES:

51. VCC = +26.9V, VEE = –4.9V, VDD = +3.25V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.
52. VCC = +27V, VEE = –5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.

TABLE 5.

Range	Cal Points	Test Points
MI Post Calibration Sourcing		
IR0 – IR4	((VCC + VEE) / 2)V / (0.2 • Imax) ((VCC + VEE) / 2)V / (0.8 • Imax)	((VCC + VEE) / 2)V / 0mA ((VCC + VEE) / 2)V / 0.5 • Imax ((VCC + VEE) / 2)V / 1.0 • Imax
MI Post Calibration Sinking		
IR0 – IR4	((VCC + VEE) / 2)V / (–0.2 • Imax) ((VCC + VEE) / 2)V / (–0.8 • Imax)	((VCC + VEE) / 2)V / 0mA ((VCC + VEE) / 2)V / –0.5 • Imax ((VCC + VEE) / 2)V /– 1.0 • Imax
MI Common Mode		
IR0 – IR4	((VCC + VEE) / 2)V / (0.2 • Imax) ((VCC + VEE) / 2)V / (0.8 • Imax)	(VCC – 5)V / 0µA (VEE + 5)V / 0µA

Force Current

The sequence of events performed for FI Testing is:

1. Program FI to the desired current
2. Force Voltage with external PMU and FORCE
3. Measure the current at FORCE.

FI is tested in all current ranges.

DC Electrical Specifications – Force Current

VCC = +26.9V, VEE = –4.9V, VDD = +3.25V, R_EXT = 10kΩ, V_REf = 3V, DUT_GND = 0.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
FI Accuracy						
14800	Force Current Error	IR0; Slew Rate = 00100; Drv-Bias = 000.	–1		+1	% Imax
14801	Force Current Error	IR1; Slew Rate = 00100; Drv-Bias = 000.	–0.5		+0.5	% Imax
14802	Force Current Error	IR2; Slew Rate = 00100; Drv-Bias = 000.	–0.5		+0.5	% Imax
14803	Force Current Error	IR3; Slew Rate = 00100; Drv-Bias = 000.	–0.5		+0.5	% Imax
14804	Force Current Error	Slew Rate = 00100; Drv-Bias = 000. In current range IR4, Imax = 200mA, FS = 925mA.	–1		+1	% FS

TABLE 6.

Range	Cal Points	Test Points
IR0 – IR4	((VCC + VEE) / 2)V / (0.8 • Imax) ((VCC + VEE) / 2)V / – (0.8 • Imax)	(VCC – 5)V / 0mA (VEE + 5)V / 0mA ((VCC + VEE) / 2)V / 1.0 • Imax ((VCC + VEE) / 2)V / – 1.0 • Imax

Force Voltage

The sequence of events performed for FV Testing is:

1. Program FV
2. Force current at DOUT
3. Measure the voltage at DOUT

FV Tests:

1. VR0 calibrated and tested in IR4
2. VR1 calibrated and tested in IR4
3. VR2 calibrated and tested in IR4
4. VR3 calibrated and tested in all current ranges.

DC Electrical Specifications – Force Voltage

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
FV (Post Calibration)						
14200	Output Force Error	VR0; Cal0; Force Voltage Test Points, Voltage Range = VR0; Note 53	–10		+10	mV
14201	Output Force Error	VR1; Cal1; Force Voltage Test Points, Voltage Range = VR1; Note 53	–15		+15	mV
14202	Output Force Error	VR2; Cal2; Force Voltage Test Points, Voltage Range = VR2; Note 53	–25		+25	mV
14203	Output Force Error	VR3; Cal 3; Force Voltage Test Points, Voltage Range = VR3; Note 53	–50		+50	mV
FV Temperature Coefficient						
	@ DAC Code 0000	VR0, Note 54		+150		µV/°C
	@ DAC Code 7FFF	VR0, Note 54		+100		µV/°C
	@ DAC Code FFFF	VR0, Note 54		0		µV/°C
	@ DAC Code 0000	VR1, Note 54		+500		µV/°C
	@ DAC Code 7FFF	VR1, Note 54		+200		µV/°C
	@ DAC Code FFFF	VR1, Note 54		0		µV/°C
	@ DAC Code 0000	VR2, Note 54		+600		µV/°C
	@ DAC Code 7FFF	VR2, Note 54		+400		µV/°C
	@ DAC Code FFFF	VR2, Note 54		0		µV/°C
	@ DAC Code 0000	VR3, Note 54		+1200		µV/°C
	@ DAC Code 7FFF	VR3, Note 54		+400		µV/°C
	@ DAC Code FFFF	VR3, Note 54		–400		µV/°C

NOTES:
53. VCC = +26.9V, VEE = –4.9V, VDD = +3.25V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.
54. VCC = +27V, VEE = –5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.

TABLE 7. Force Voltage

Range	Cal Points	FV Test Points
VR0 IR4 (Vmid = +1.5V)	0V/0µA +3V/0µA	0.0V/0µA +1.5V/0µA +3.5V/0µA
VR1 IR4 (Vmid = +3V)	0V/0µA +5V/0µA	0.0V/0µA +3V/0µA +7V/0µA
VR2 IR4 (Vmid = +4.5V)	0V/0µA +10V/0µA	–1V/0µA +5V/0µA +12.5V/0µA
VR3 IR0 (Vmid = +9V)	0V/0µA +20V/0µA	–1V/0µA +24V/0µA +0.5V/–Imax +23V/+Imax

TABLE 7. Force Voltage

Range	Cal Points	FV Test Points
VR3 IR1 (Vmid = +9V)	0V/0µA +20V/0µA	–1V/0µA +24V/0µA +0.5V/–Imax +23V/+Imax
VR3 IR2 (Vmid = +9V)	0V/0µA +20V/0µA	–1V/0µA +24V/0µA +0.5V/–Imax +22.5V/+Imax
VR3 IR3 (Vmid = +9V)	0V/0µA +20V/0µA	–1V/0µA +24V/0µA +0V/–Imax +22V/+Imax
VR3 IR4 (Vmid = +9V)	0V/0µA +20V/0µA	–1V/0µA +24V/0µA +1.0V/–200mA +21V/+200mA

DC Electrical Specifications – Resistor Values

VCC = +27V, VEE = –5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
On-Chip FET Switches						
19130	Diff-Z			100		Ω
19131	Ld-E#			60		Ω
19132	Con-EF-DIN#			50		Ω
19133	Con-ES-DIN#			1		kΩ
19134	RLoad Lo#<01>			250		Ω
19135	RLoad Lo#<10>			1		kΩ
19134	RLoad Hi#<01>			250		Ω
19135	RLoad Hi#<10>			1		kΩ
19138	Rsense IR4			1.08		Ω
19139	Rsense IR2			500		Ω
19140	Rsense IR1			5		kΩ
19141	Rsense IR0			50		kΩ
19142	IR<0> Connect Switch			1.2		kΩ
19143	IR<1> Connect Switch			.6		kΩ
19144	IR<2> Connect Switch			160		Ω
19145	IR<1:0> Connect Switch)			.6		kΩ

AC Characteristics

NOTE: For all of the following AC Electrical Specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

AC Electrical Specifications – CPU Port

VCC = +26.9V, VEE = –4.9V, VDD = +3.25V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Set-Up Time						
27100	SDIO to Rising CK		10			ns
27110	STB to Rising CK		10			ns
Hold Time						
27120	SDIO to Rising CK		10			ns
27130	STB to Rising CK		10			ns
27140	CK Minimum Pulse Width High		18			ns
27150	CK Minimum Pulse Width Low		18			ns
27160	CK Period		40		100	ns
Propagation Delay						
27180	Rising CK to SDIO Out				10	ns
27170	Reset Minimum Pulse Width		100			ns

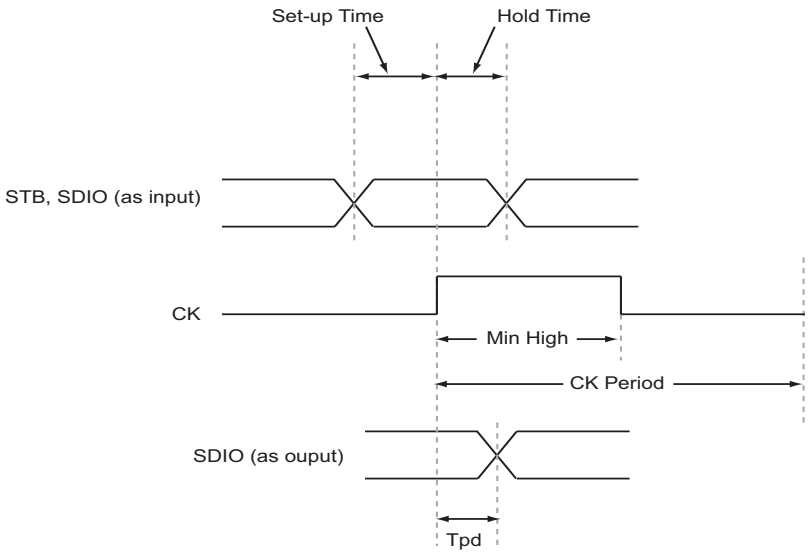


FIGURE 1.

AC Electrical Specifications – Driver

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
22230	Minimum Pulse Width (2V)	Notes 1, 2		8		ns
22230	Minimum Pulse Width (12V)	Notes 1, 2		20		ns
22230	Minimum Pulse Width (24V)	Notes 1, 2		40		ns
Propagation Delay						
	DATA to DOUT	All deskew elements bypassed. No elements selected. Drv-Bias = 000; Slew Rate = 011111; Notes 1, 2, 3.		11.5		ns
	EN to DOUT – HiZ to Enable	All deskew elements bypassed. No elements selected. Drv-Bias = 000; Slew Rate = 011111; Notes 1, 2, 4		20.5		ns
	EN to DOUT – Enable to HiZ	All deskew elements bypassed. No elements selected. Drv-Bias = 000; Slew Rate = 011111; Notes 1, 2, 4		14.5		ns
	Output Capacitance in HiZ	Note 1		15		pF
Driver Slew Rates						
22240	Median Slew Rate	Post slew rate calibration. Notes 5, 6	0.75		1.5	V/ns
22250	Maximum Slew Rate	Post slew rate calibration. Notes 5, 7	1.0			V/ns

NOTES:
1. Limits guaranteed by characterization and are not production tested.
2. Drv-Bias = 000 (mid-point), SR-Adj = 01111 (mid-point). 3' cable into 1MΩ//18pF, measured to full amplitude.
3. DATA to DOUT. Tested at DOUT = 1.5V, DVH = 3V, DVL = 0V.
4. EN to DOUT. DVH = 3V, DVL = 0V, tested at DOUT = 0.75V (terminated through 50Ω to ground).
5. VCC = +26.9V, VEE = –4.9V, VDD = +3.25V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.
6. Tr/f# = 01111, No Load, Dr-Bias#<2:0> = 000, tested @ 20% and 80%.
7. Tr/f# = 11111, No Load, Dr-Bias#<2:0> = 011, tested @ 20% and 80%.

AC Electrical Specifications – Comparator

Limits guaranteed by characterization and are not production tested.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
	Minimum Pulse Width	No deskew elements. All bypassed. Minimum pulse width conditions; Note 8.		4	5	ns
	Input Tracking Rate		1.0			V/ns
	DIN Input Capacitance			15		pF
	Propagation Delay (DOUT to COMP_A, _B)	No deskew elements. All bypassed.		15		ns
	Output Rise Time (COMP_A, _B)			1.0		ns

NOTES:
8. VOH = 3V, VOL = 0V, DIN = 0V to 3V. CVA, CVB = 1.5V.

AC Electrical Specifications – Load

VCC = +27V, VEE = –5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V. Limits guaranateed by characterization and are not production tested.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay						
	EN to LOAD (HiZ to On)	Note 9		25		ns
	EN to LOAD (On to HiZ)	Note 9		19		ns

NOTES:
9. VCOM = 3V, ISRC = ISNK = 12mA. Tested at DOUT = 0.75V (DOUT terminated through 50Ω to GND).

Ring Oscillator

All loop delay measurements are taken with:

- driver and comparator configured as a ring
- channels tested in pairs

AC Electrical Specifications – Ring Oscillator

VCC = +27V, VEE = –5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.
The loop time measured when the channel is configured as a ring oscillator does NOT indicate the total round-trip time of the pin electronics as some circuitry in the driver signal paths are bypassed, and the circuitry of the ring oscillator control logic is inserted into the overall loop. The total delay measured in this configuration is used as a figure of merit to verify part-to-part AC performance.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
20000	Ring Oscillator Loop Delay (Max Loop Time, PLL_CK = 50MHz)	All deskew elements selected. Channel 0 and Channel 1 configured as ring oscillators. Notes 10, 11, 12.	70	95	110	ns
20020	Ring Oscillator Loop Delay (Max Loop Time, PLL_CK =100MHz)	All deskew elements selected. Channel 0 and Channel 1 configured as ring oscillators. Notes 10, 11, 12.	50	68	80	ns
20100	PLL Lock Test at 50MHz	PLL_CK = 50MHz. PLL voltage measured @ CAP_PLL pin.	.85	1.1	1.35	V
20120	PLL Lock Test at 100MHz	PLL_CK = 100MHz. PLL voltage measured @ CAP_PLL pin.	1.3	1.6	1.9	V

NOTES:
10. Ring triggered on a rising edge.
11. Ring configured DATA through Comp A.
12. Delay elements programmed to maximum delay. FEA elements programmed to mid code.

AC Electrical Specifications – Coarse Delay

Channel 0 and Channel 1 configured as ring oscillators.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DATA, EN, COMP A, B; PLL_CK = 50MHz						
25100	Tmin (Tpd+, Tpd– with CD = 0)	Notes 13, 15		2.9		ns
25110	Full Scale Delay (Tpd+, Tpd–)	Notes 13, 15		19.375		ns
25115	Resolution (step size over all codes)	Notes 13, 15		625		ps
DATA, EN, COMP A, B; PLL_CK = 100MHz						
25120	Tmin (Tpd+, Tpd– with CD = 0)	Note 14	1.5	2.2	3.0	ns
25130	Full Scale Delay (Tpd+, Tpd–)	Note 14	6.0	9.6875	16.0	ns
25140	Resolution (step size over all codes)	Note 14		312.5		ps

NOTES:
13. Limits guaranteed by characterization and are not production tested.
14. VCC = +26.9V, VEE = –4.9V, VDD = +3.25V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.
15. VCC = +27V, VEE = –5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.

AC Electrical Specifications – Coarse Falling Edge Adjust

Channel 0 and Channel 1 configured as ring oscillators.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PLL_CK = 50MHz						
25200	Tmin (Tpd+, Tpd–; Sel-XX-CFEA = 0; (Code = 1000)	Notes 16, 17		10.5		ns
25210	ΔTpd– Full Scale Acceleration (Code 0000 relative to 1000)	Notes 16, 17		–5.3		ns
25220	ΔTpd– Full Scale Delay (Code 1111 relative to 1000)	Notes 16, 17		4.5		ns
25215	Resolution (step size over all codes)	Notes 16, 17		625		ps
PLL_CK = 100MHz						
25230	Tmin (Tpd+, Tpd–; Sel-XX-CFEA = 0; (Code = 1000)	Note 18	4.0	6.1	10.0	ns
25240	ΔTpd– Full Scale Acceleration (Code 0000 relative to 1000)	Note 18	–4.0	–2.5	–1.0	ns
25250	ΔTpd– Full Scale Delay (Code 1111 relative to 1000)	Note 18	0.5	2.3	4.0	ns
25260	Resolution (step size over all codes)	Note 18		312.5	1,000	ps
25270	ΔTpd+ vs. all CFEA codes	Note 18	–1000		+1000	ps

NOTES:
16. Limits guaranteed by characterization and are not production tested.
17. VCC = +27V, VEE = –5V, VDD = +3.45V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.
18. VCC = +26.9V, VEE = –4.9V, VDD = +3.25V, R_EXT = 10kΩ, V_REF = 3V, DUT_GND = 0V.

Chip Overview

The ISL55188-AS is a highly integrated "System on a Chip" (SOC) pin electronics solution aimed at incorporating every analog function, along with some digital support circuitry, required on a per-channel basis for Automatic Test Equipment (see picture below). The interface, control and I/O of the chip are digital; all analog circuitry is inside the chip. Two complete tester channels are integrated into each Saturn.

CPU Control

All chip set up, configuration control, the writing to and reading back of the internal registers and memory are controlled through the 3-bit serial data CPU port. The CPU port is typically used to set up the operating mode of the chip prior to executing a test, or to change modes during a test.

An internal register chart (Memory Map - listed later in the datasheet) documents all programmable control signals and their addresses, and shows how to program each internal signal.

Real Time Control

All real time control and observation are accomplished via the real time input and output signals:

- DATA_0, DATA_1 (Differential Inputs)
- EN_0, EN_1 (Differential Inputs)
- CA_0, CB_0 (Differential Outputs)
- CA_1, CB_1 (Differential Outputs

Analog Reference

All on-chip analog functions are related to one of several off-chip precision reference inputs:

- PLL_CK
- V_REF
- R_EXT

These external references are used to provide accurate and stable analog circuit performance that does not vary over time, temperature, supply voltage, or process changes.

External Signal Nomenclature

All input and output pins, when referred to in the data sheet or in any circuit diagram, use the following naming conventions:

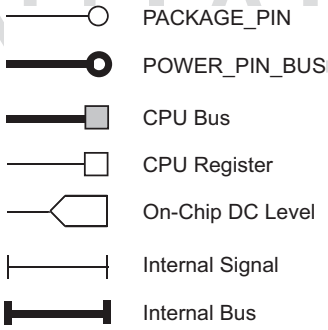
1. all capital letters (i.e. DATA, CK, SDIO)
2. underscores for clarity (i.e. EXT_SENSE, EN_0)
3. shown next to an I/O circle in any schematic.

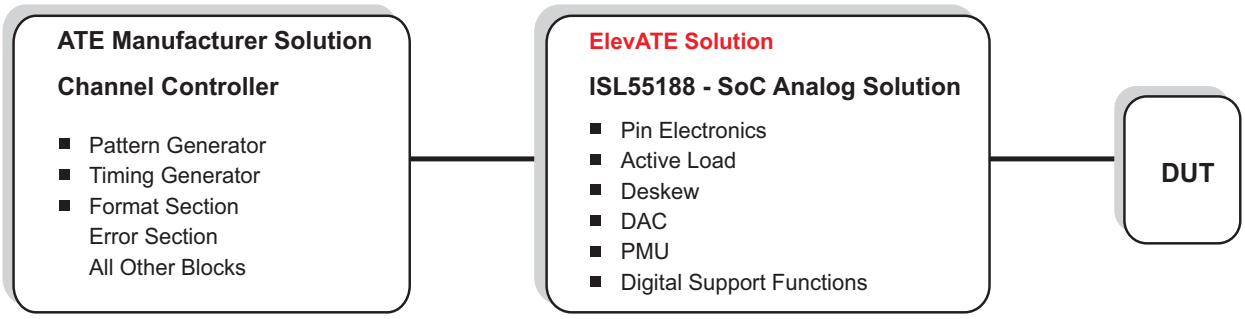
CPU Programmed Control Line Nomenclature

Any internal signal, DAC level, or control signal which is programmed via the CPU port uses a different nomenclature:

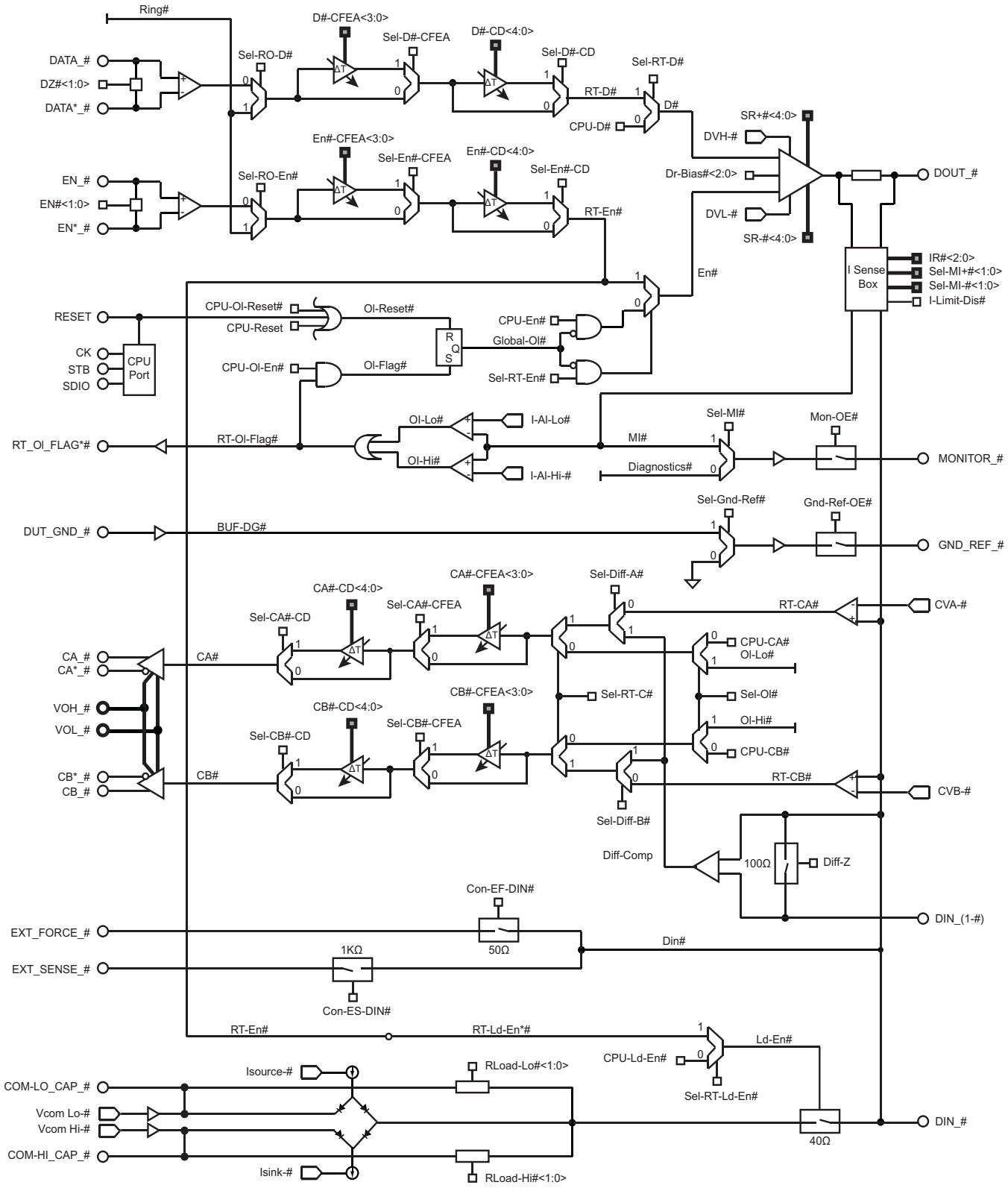
1. the first letter in a word is always a capital letter
2. subsequent letters within the same word are small
3. dashes (but never an underscore) for clarity
4. NOT shown with an I/O circle in any schematic.

Control lines, internal registers, and other internal signals which are programmable by the CPU port are listed in the Memory Map table.





Detailed Chip Diagram



PLL

The on-chip PLL is used to establish and maintain the range and resolution of all coarse delay and coarse falling edge adjust delay circuitry automatically.

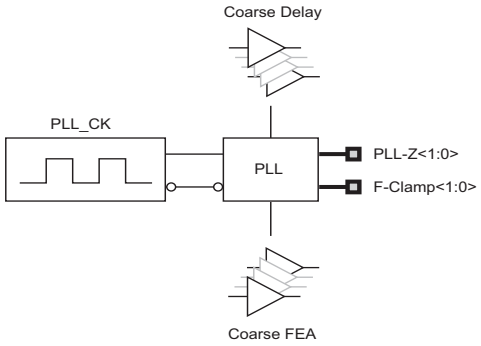


FIGURE 2.

PLL Range

For the purpose of setting the range of the deskew elements, the PLL_CK is allowed to vary between 50MHz and 100MHz.

$$50MHz \leq PLL\_CK \leq 100MHz$$

Frequency Clamps

There are internal clamps which help guarantee that the PLL locks to the PLL_CK signal. The setting of the frequency clamps depends upon the PLL_CK frequency. If there is no input PLL_CK, the PLL will attempt to lock at the lower limit of the frequency clamps.

TABLE 8.

F-Clamp<1:0>	PLL_CK Frequency
00	<70MHz
01	70MHz – 105MHz
10	Reserved (do not use)
11	Reserved (do not use)

Default condition upon power-up or reset is 00.

PLL Disable

The CPU port can connect the PLL output voltage to ground through an on-chip switch. This connection may be used to place the PLL in a known state prior to locking.

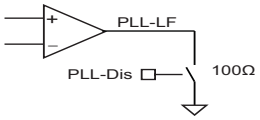


FIGURE 3.

TABLE 9.

PLL-Dis	PLL-LF
0	Active
1	Disabled (100Ω to ground)

PLL Input Terminations

PLL_CK / PLL_CK* inputs have on-chip termination options which support 3 different termination schemes:

1. No termination (open circuit)
2. 100Ω across the differential inputs
3. 50Ω single-ended termination.

All of these termination schemes may be realized without requiring any external resistors.

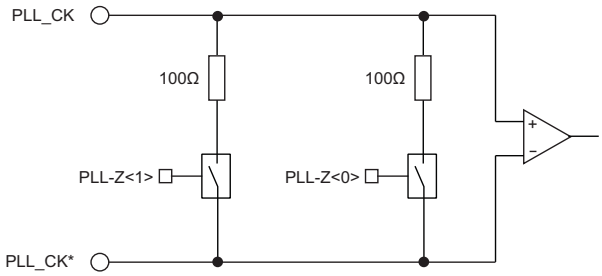


FIGURE 4.

The selection of any on-chip termination is made through the CPU port. PLL-ZA and PLL-ZB are the internal control bits that select the termination option. Their addresses are listed in the memory map tables.

TABLE 10.

PLL-Z<1:0>	Termination Option
00	No Termination
01	100Ω Differential
10	100Ω Differential
11	50Ω Single-Ended

Default condition upon power-up or reset is"No Termination."

For applications that do not use the deskew elements and do not have a PLL_CK input, PLL_CK/PLL_CK* should be tied to a digital low/high state and not left floating.

100Ω DIFFERENTIAL TERMINATION

By selecting either (but not both) 100Ω terminators, a 100Ω resistance is connected between the differential inputs, thus cleanly terminating 50Ω transmission lines on the PCB without any external components.

50Ω SINGLE ENDED TERMINATION

Selecting both 100Ω terminators creates a single-ended 50Ω termination. The inverting input then becomes the termination voltage for the input signal, and the appropriate termination voltage level must be applied to this pin.

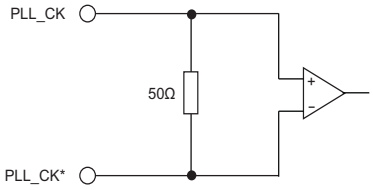


FIGURE 5.

Driver

Real Time Inputs

Each driver has two real-time control inputs, DATA and EN, that determine the driver operation.

TABLE 11.

EN	DATA	Driver Output
0	X	HiZ
1	0	DVL
1	1	DVH

When placed in HiZ, the driver maintains a low leakage input current when the output is between the supply levels VCC and VEE, minus the headroom.

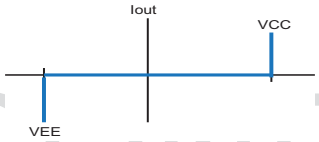


FIGURE 6.

Flexible Inputs

DATA and EN are differential inputs that accept most standard technologies.

On-Chip Terminations

Each channel's DATA and EN inputs have independent on-chip termination options that support 3 different termination schemes:

1. No termination (open circuit)
2. 100Ω across the differential input
3. 50Ω single ended termination.

TABLE 12.

EZ#<1:0> DZ#<1:0>	Input Termination
00	No Termination
01	100Ω
10	100Ω
11	50Ω

CPU Control

After all driver signal processing and timing adjust are performed, data and enable enter one last stage where the real time signals may be bypassed and the CPU port can take direct control over the driver. This final logic stage allows the CPU port to exercise driver control regardless of any real-time inputs.

TABLE 13.

Sel-RT-D#	Data# Source
0	CPU-D#
1	RT-D#

Sel-RT-En#	Enable# Source
0	CPU-En#
1	RT-En#

Driver Control Read Back

The status of the internal nodes D# and En# may be read back directly via the CPU port. This read only function is useful for a tester to be able to go out and check the driver inputs at any time.

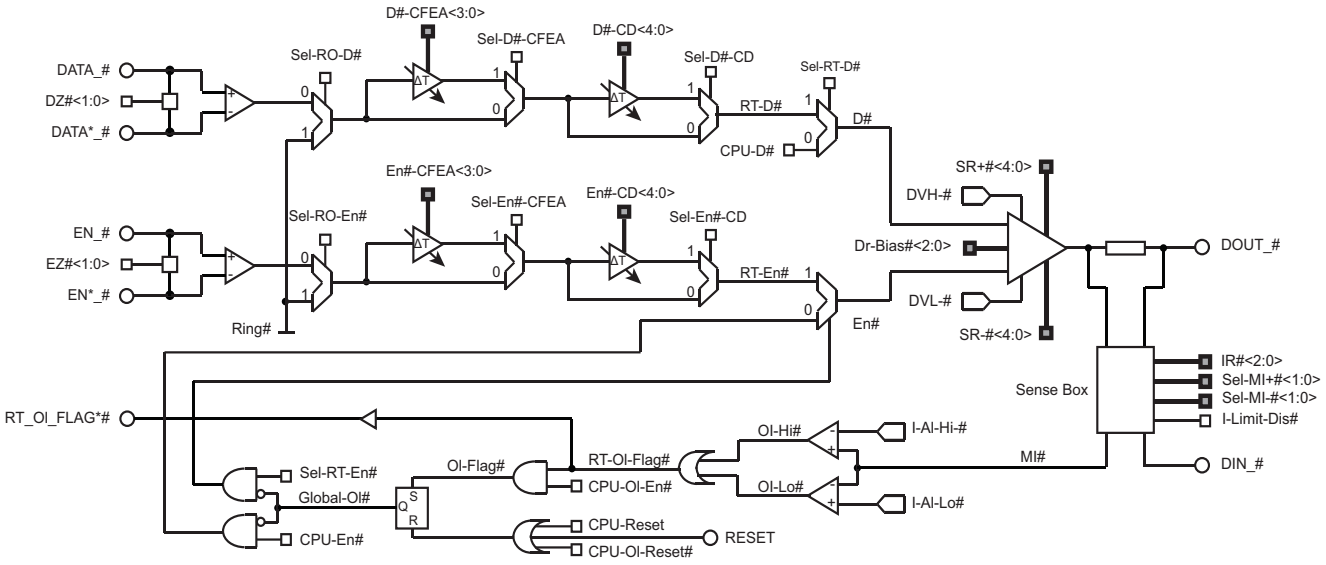


FIGURE 7.

Timing Adjust

Each channel's high-speed DATA and EN inputs have timing adjustment capability with the following characteristics:

1. Separate and independent delay circuitry for the DATA and EN paths
2. Separate and independent delay circuitry for each channel
3. Propagation delay adjust (both rising and falling edge Tpd are delayed equally)
4. Falling edge adjust (falling edge adjusted while the rising edge remains unchanged)
5. Timing delay range and resolution established by an external frequency (PLL_CK).

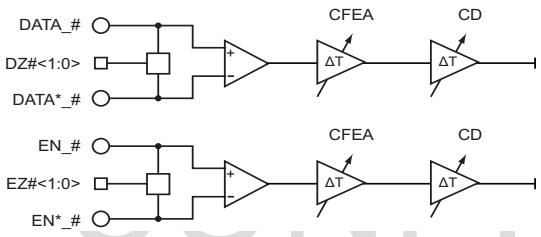


FIGURE 8.

Data and Enable Propagation Delay Adjust

The propagation delay circuitry adds timing delay to the rising edge (Tpd+) and the falling edge (Tpd-) in equal amounts. Propagation delay adjustment is typically used for aligning the timing of multiple channels inside a tester.

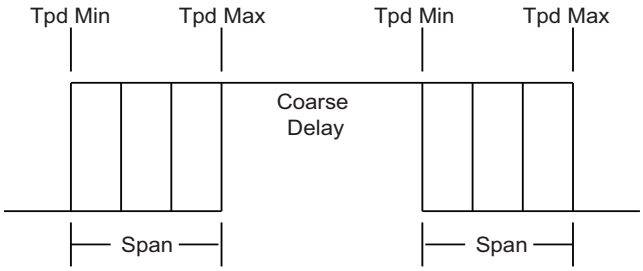


FIGURE 9.

Coarse Delay Adjust

The coarse delay circuitry divides the overall delay range (span) into 32 equal segments, and then selects one of those delays. The delay section may be bypassed via the CPU port.

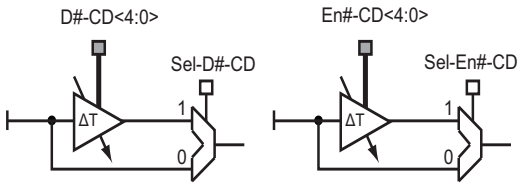


FIGURE 10.

TABLE 14.

CD<4:0>	PLL_CK	ΔTpd+, –
00000	X	ΔTpd+, – = 0
11111	T = 10ns	ΔTpd+, – +9.6875ns Resolution = 312.5ps
11111	T = 20ns	ΔTpd+, –, = +19.375ns Resolution = 625ps

TABLE 15.

Sel-D#-CD	Data Coarse Delay
0	Coarse Delay Bypassed, Powered Down
1	Coarse Delay Active, Powered Up

Sel-En#-CD	Enable Coarse Delay
0	Coarse Delay Bypassed, Powered Down
1	Coarse Delay Active, Powered Up

Power Reduction Mode

If the coarse delay is completely bypassed, the power to the delay cells is shut off and the total chip power consumption is reduced. This feature is useful in applications that do not require the coarse delay function.

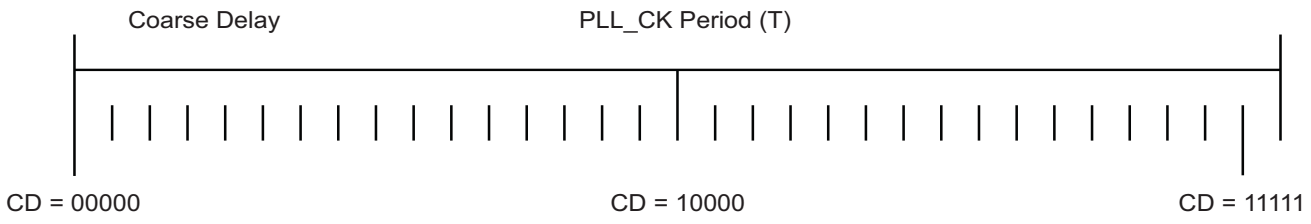


FIGURE 11.

Coarse Falling Edge Delay Adjust

The falling edge delay circuitry adds or subtracts timing delay to or from the falling edge (Tpd-) while having no effect on the rising edge (Tpd+). Propagation delay adjustment is typically used for removing any pulse width distortion inside a tester.

Coarse falling edge adjust divides the overall delay range (span) set by the period of PLL_CK into 16 equal segments, and allows the falling edge propagation delay of the signal to be modified from -8 to +7 segments.

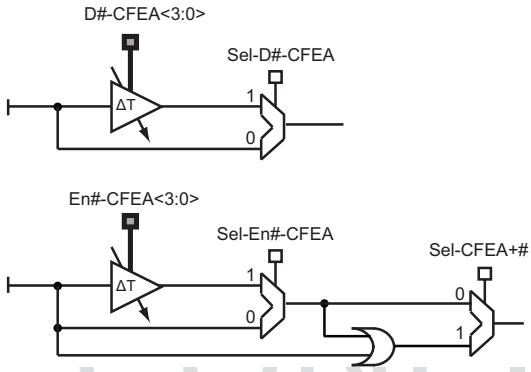


FIGURE 12.

Power Reduction Mode

If the coarse falling edge adjust section is completely bypassed, the power to the delay cells is shut off and the total chip power consumption is reduced. This feature is useful in applications that do not require the coarse FEA function.

The CFEA section may be bypassed by the select bit, which is set by the CPU port. The address of each select bit is listed in the memory map tables.

TABLE 16.

CFEA<3:0>	PLL_CK	ΔTpd –
0000 1000 1111	T = 10ns	Resolution = 312.5ps ΔTpd– = –2.5ns ΔTpd– = 0ns ΔTpd– = +2.1875ns
0000 1000 1111	T = 20ns	Resolution = 625ps ΔTpd– = –5.0ns ΔTpd– = 0ns ΔTpd– = +4.375ns

TABLE 17.

Sel-D#-CFEA	Data Coarse Falling Edge Adjust
0	Coarse FEA Bypassed, Powered Down
1	Coarse FEA Active, Powered Up

Sel-En#-CFEA	Enable Coarse Falling Edge Adjust
0	Coarse FEA Bypassed, Powered Down
1	Coarse FEA Active, Powered Up

CFEA Rising Edge Select

The CPU port can select an earlier version of the rising edge to expand the enable pulse.

TABLE 18.

Sel-CFEA+#	Sel-En#-CFEA	CFEA Operation
0	0	Coarse FEA Bypassed
1	0	Not Recommended
0	1	Normal CFEA Operation
1	1	Rising Edge Accelerated

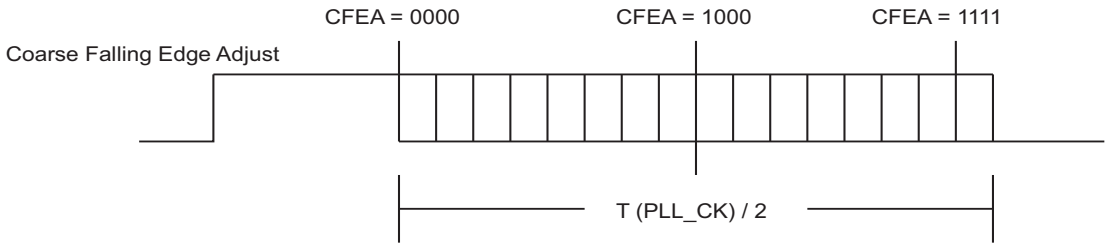


FIGURE 13.

Slew Rate Adjust

The driver has independent adjustments for the rising and falling edge slew rates.

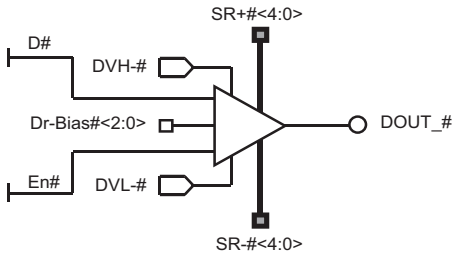


FIGURE 14.

TABLE 19.

SR+(-)#<4:0>	Driver Slew Rate
00000 • • 00100	Not recommended for use as a driver or PMU • • Not recommended for use as a driver or PMU
00101 • • 10001	Not recommended for use as a driver, but ok for PMU • • Not recommended for use as a driver, but ok for PMU
10010 • • 11111	Minimum slew rate for driver (slowest) and ok for PMU • • Maximum slew rate for driver (fastest) and ok for PMU

.

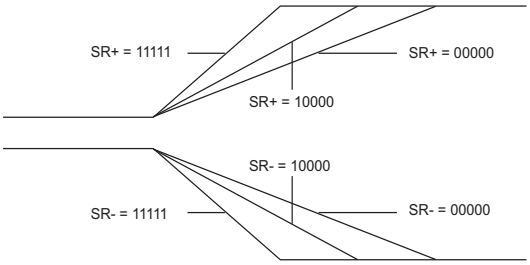


FIGURE 15.

Driver Bias

The driver output stage has a programmable bias current to allow applications that require slower edge rates to consume less power.

TABLE 20.

Dr-Bias#<2:0>	Maximum Driver Slew Rate
100	Slowest (<.3V/ns). Ok for PMU or driver with appropriate termination resistor*.
101	•
110	•
111	Ok for PMU or driver with appropriate termination resistor*
000	Ok for PMU or driver
001	•
010	•
011	Fastest (>1/ns), Ok for PMU or driver

*See Driver Output Impedance Section for selection of Termination Resistor.

Driver Output Impedance

The driver output impedance changes from roughly 8Ω to 20Ω as a function of the driver bias setting. It is recommended that the driver bias setting be determined for an application and then fixed at that setting. Once set, a suitable series termination resistor may be selected to support a 50Ω output impedance.

Driver Bias and Slew Rate Settings

There are many possible combinations between slew rate and driver bias settings. The exact setting should be determined for each application.

However, some convenient settings are:

TABLE 21.

Dr-Bias#<2:0>	SR+(-)#<4:0>	Slew Rate	Pdq (@32V)
111	11111	1V/ns	~2.5W/Ch
110	01110	.5V/ns	~1.9W/Ch
011	11111	>1.25V/ns	~4W/Ch

PMU

Measure Current

Each driver has the ability to sense the amount of current flow (MI# is an analog voltage proportional to the current).

TABLE 22.

MI#	Iout
+1V	+Imax
0V	0
–1V	–Imax

Current Ranges

There are 5 current ranges.

TABLE 23.

Current Range	Imax	Rsense
IR0	20µA	50kΩ
IR1	200µA	5kΩ
IR2	2mA	500Ω
IR3	1/(1/2 + Rterm)	1.08 + Rterm
IR4	925mA	1.08Ω

In IR4, the output buffer is current limited to ~200 mA and therefore the corresponding MI voltage is limited to ~± 200 mV. IR3 is created by sensing across the series combination of the on-chip resistor and the off-chip series termination resistor. Different values of the series termination resistor translate to different maximum currents.

MI# is created by connecting various sense points to the positive and inverting inputs of an amplifier. Different current ranges require different combinations of inputs.

TABLE 24.

Current Range	Sel-MI+#<1:0>	Sel-MI–#<1:0>	IR#<2:0>
IR0	00	00	001
IR1	01	01	010
IR2	10	10	100
IR3	11	10	000
IR4	11	11	000

In ranges IR0, IR1 and IR2 the actual current path is through the DIN_# pin, not the DOUT_# pin. Relay 2 must be open for these ranges to function properly.

MI# is routed to two destinations:

1. MONITOR_# output
2. On-chip over-current detect window comparator.

MI# is routed to two destinations:

1. MONITOR_# output
2. On-chip over-current detect window comparator.

If MI# is connected to the MONITOR_# pin it can be connected to an off-chip ADC that can measure the actual value. The window comparator converts MI# into two digital signals using the on-chip level generators as the thresholds.

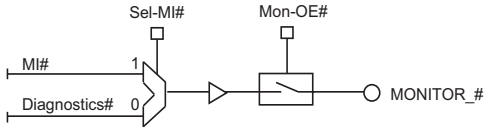


FIGURE 17.

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TABLE 25.

Sel-MI#	Monitor Mode
1	MI
0	Diagnostics

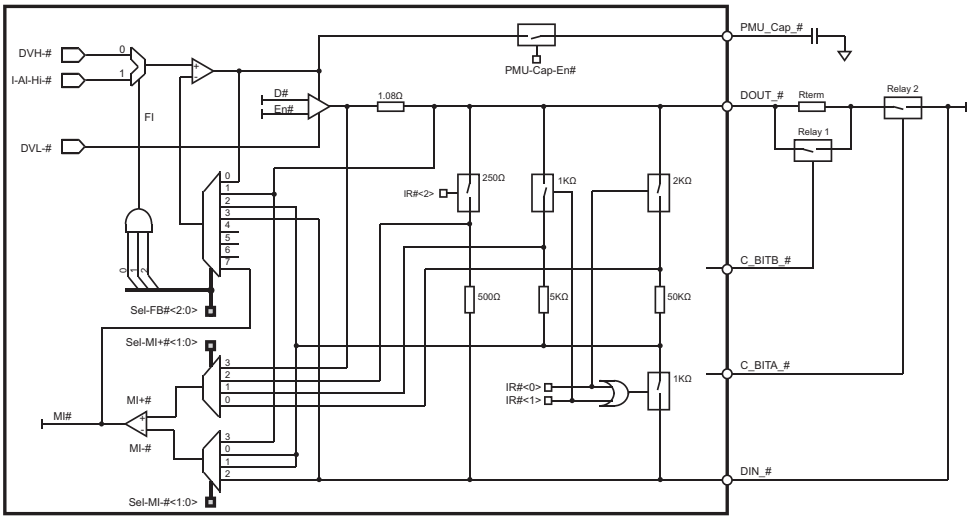


FIGURE 16.

Programmable Over-Current Protection

MI# may be compared against static limits for over-current protection and the driver may be programmed to automatically go to a high impedance condition if the current exceeds the maximum limits.

TABLE 26.

Output State	OI-Lo#	Condition
MI# > I-AI-Lo	0	OK
MI# < I-AI-Lo	1	OI Condition

Output State	OI-Hi#	Condition
MI# < I-AI-Hi	0	OK
MI# > I-AI-Hi	1	OI Condition

The individual flags are then combined into one over-current flag. OI-HI# and OI-Lo# may be read back through the CPU port.

TABLE 27.

OI-Lo#	OI-Hi#	RT-OI-Flag#	Condition
0	0	0	OK
1	X	1	OI Condition
X	1	1	OI Condition

The CPU port can enable or disable the over-current flag from taking any action. If enabled, OI-Flag# is active high any time the current exceeds the limits.

TABLE 28.

CPU-OI-En#	RT-OI-Flag#	OI-Flag#
0	X	0
1	0	0
1	1	1

OI-Flag# sets a global register (Global-OI#) that records whether any over current condition has occurred. Global-OI# is cleared with a hardware reset, CPU-Reset or a CPU-OI-Reset#. Once a global OI condition has been detected the driver is placed in HiZ until the flag is cleared. CPU-OI-Reset# is a write-only register.

TABLE 29.

I-AI-Lo-#<15:0> I-AI-Hi-#<15:0>	Alarm Level	DAC Level
0000 Hex	–Imax (Sinking)	–1V
7FFF Hex	0µA	0V
FFFF Hex	+Imax (Sourcing)	+1V

Current Alarm Full Scale Range Adjust

The current alarms may be adjusted upward or downward by the CPU port. This adjustment is linked with the active load current adjustment.

TABLE 30.

IL-Adj#<1:0>	I Alarm Level
00	Nominal
01	0.8 • Nominal
10	1.2 • Nominal
11	N/A

Over Current Flag

RT_OI_FLAG*_# is an open drain output that is active low and indicates a real time over-current condition on one or both channels. Global-OI# may be read back through the CPU port to determine which channel experienced an over current situation.

Default condition upon power up or reset is RT-OI-Flag# disabled, Global-OI# cleared and OI_FLAG* high.

Over Current Shut Down

It can be difficult to discern between an over current situation due to a short circuit at the DUT vs. a high transient current situation due to a large voltage swing and long transmission line. Therefore, there are several methods to make an over current determination.

Automatic "On-Chip" Control

By setting CPU-OI-En# high any occurrence of an over-current situation will directly place the driver into a HiZ state.

CPU Control

The CPU port can activate or bypass the over current shut down circuitry. When activated, an over-current event will trigger a flag and place the driver into HiZ until the flag is cleared.

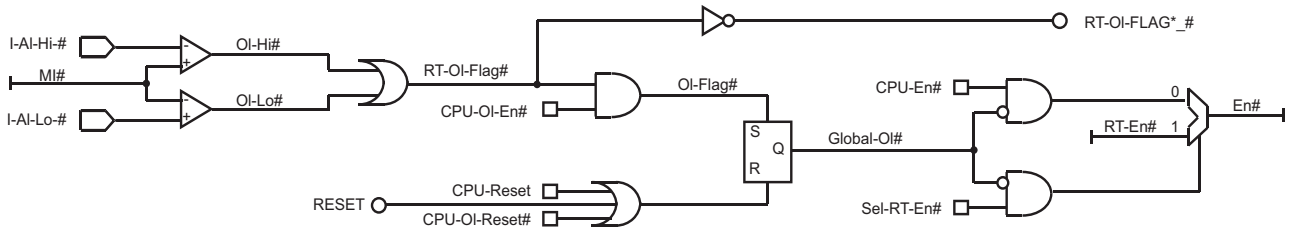


FIGURE 18. OVER-CURRENT PROTECTION

External Control

The channel timing generator can process the RT_OI_FLAG*_# signal in real time and make a determination whether or not to place the driver into HiZ. The off-chip controller can pass judgment on both the timing and the duration of the RT_OI_FLAG*_# when making an over-current failure determination.

MI "Go / No Go" Testing

The over-current window comparator may be used as a real time current monitor with the levels I-AI-Lo-# and I-AI-Hi-# setting the upper and lower bounds of the acceptable current range. The over-current comparators may then be routed off chip through CA_# and CB_# and be treated like real time pattern information.

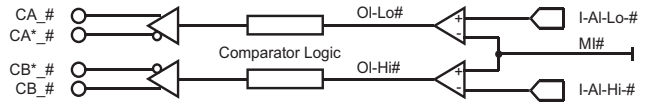


FIGURE 19.

In this mode it is important that the over-current flags be disabled so the driver is not placed in a HiZ state when the current exceeds the threshold limits.

MV

The voltage at DOUT_# and DIN_# may be brought out on the MONITOR_# pin by selecting the diagnostic option for the monitor and selection DOUT_# or DIN_# for the diagnostic path.

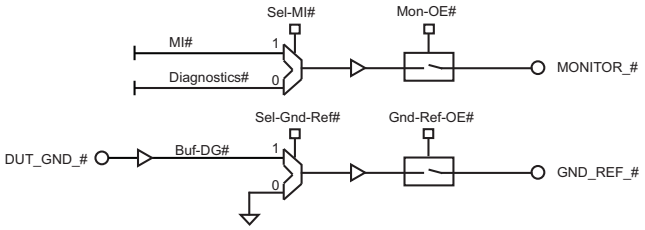


FIGURE 20.

TABLE 31.

Sel-MI#	Monitor Mode
1	MI
0	MV/Diagnostics

Differential Monitor

The monitor may be referenced to either chip ground or DUT_GND.

TABLE 32.

Gnd-Ref-OE#	Sel-Gnd-Ref#	GND_REF_#
1	0	Chip GND
1	1	BUF-DG#
0	X	HiZ

DUT_GND is used when measuring voltages, and Chip GND is used when measuring currents. Chip GND is also used when measuring diagnostic voltages.

Force Voltage

In FV/MI mode the driver is configured as a PMU with DVH-# as the forcing voltage. There are several different feedback points to the DVH-# buffer to support different driver modes and current sense ranges.

TABLE 33.

Sel-FB#<2:0>	Feedback Point	Driver Configuration
000	Op Amp Output	Driver
001	DOUT_#	PMU
010	IR0, IR1 Sense Point	PMU
011	DIN_#	PMU
100	Not Used	-
101	Not Used	-
110	Not Used	-
111	MI#	FI

Force Current

The driver may be configured as a PMU in FI mode by feeding back the MI# signal to the inverting input of the forcing op amp. The I-AI-Hi# DC level is used as the input to the forcing op amp in FI mode.

PMU Compensation

In PMU mode each channel may connect an external compensation capacitor for stability purposes.

TABLE 34.

PMU_Cap-En#	External Capacitor
0	Disconnected
1	Connected

PMU Calibration

The driver calibration values for PMU operation are different than those used in pin electronics mode.

Short Current Protection

Each driver has built-in current limiting that can be activated or bypassed by the CPU port. If active and this limit is exceeded the driver will automatically current limit. The short-circuit current limit is not programmable.

TABLE 35.

I-Limit-Dis#	Short Circuit Current Limit
0	Active, 250mA Imax.
1	Bypassed. No current limiting.

Comparator

Overview

The comparator is used to track all real-time activity on the DIN pin. Each channel has a high-speed functional dual comparator (CA# and CB#) with its own independent on-chip threshold generation (CVA-# and CVB-#).

TABLE 36.

Input Condition	Output Condition
DIN_# > CVA(B)-#	CA(B)_# = 1
DIN_# < CVA(B)-#	CA(B)_# = 0

The functional comparator maintains extremely low input leakage currentwhen DIN_# is between the power supply rails VEE and VCC.

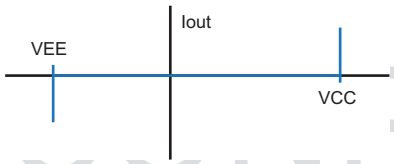


FIGURE 21.

Internal State Read Back

Direct access to the internal comparator states RT-CA#, RT-CB# and Diff-Comp is provided via the CPU port. This access is useful for diagnostic purposes and for any application where DUT status is required without using any error processing circuitry.

Output Source Options

CA_# and CB_# have a variety of sources that may be selected under CPU control.

TABLE 37.

Sel-RT-C#	Sel-Diff-A(B)#	Sel-OI#	CA_#	CB_#
1	0	X	RT-CA#	RT-CB#
1	1	X	Diff-Comp	Diff-Comp
0	X	1	OI-Lo#	OI-Hi#
0	X	0	CPU-CA#	CPU-CB#

Differential Comparator

The two independent channels may be combined into one differential comparator using the DIN_# inputs from each channel.

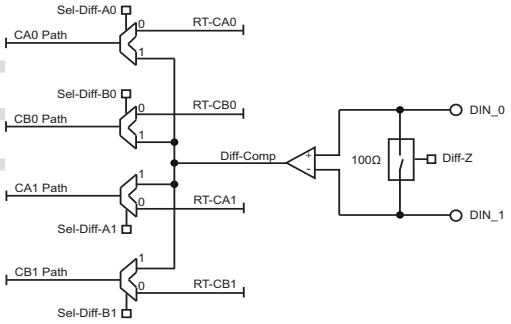


FIGURE 22.

TABLE 38.

Input Condition	Diff-Comp
DIN_0 > DIN_1	1
DIN_0 < DIN_1	0

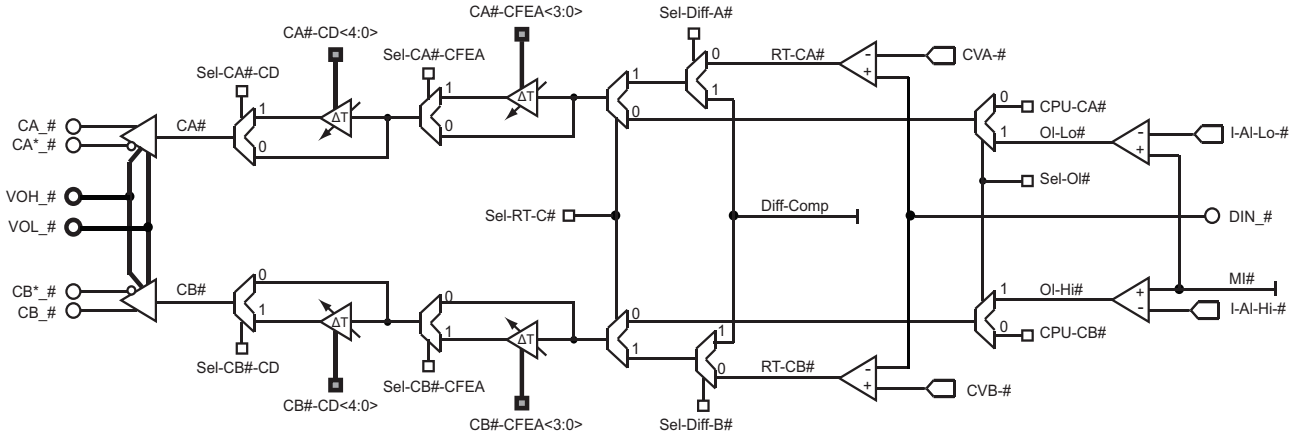


FIGURE 23. COMPARATOR

Differential Comparator Termination

The differential comparator supports an on-chip termination under CPU control.

TABLE 39.

Diff-Z	Differential Termination
0	None
1	100Ω

Timing Adjust

Each channel's CA and CB outputs have timing adjustment capability with the following characteristics:

1. Separate and independent delay circuitry for the CA and CB paths
2. Separate and independent delay circuitry for each channel
3. Propagation delay adjust (both rising and falling edge Tpd are delayed equally)
4. Falling edge adjust (falling edge adjusted while the rising edge remains unchanged)
5. Timing delay range and resolution established by an external frequency (PLL_CK).

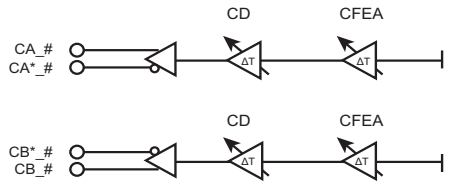


FIGURE 24.

Coarse Delay Adjust

The propagation delay circuitry adds timing delay to the rising edge (Tpd+) and the falling edge (Tpd-) in equal amounts. Propagation delay adjustment is typically used for aligning the timing of multiple channels inside a tester.

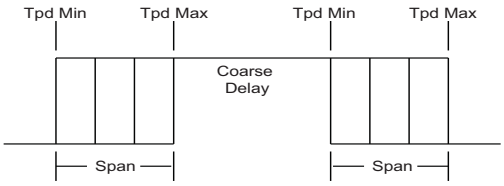


FIGURE 25.

The coarse delay circuitry divides the overall delay range (span) into 32 equal segments, then selects one of those delays. The delay section may be bypassed via the CPU port.

.

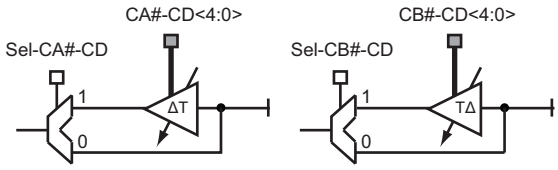


FIGURE 26.

TABLE 40.

CD<4:0>	PLL_CK	ΔTpd+,–
00000	X	ΔTpd+,– = 0
11111	T = 10ns	ΔTpd+,– = +9.6875ns Resolution = 312.5ps
11111	T = 20ns	ΔTpd+,– = +19.375ns Resolution = 625ps

TABLE 41.

Sel-CA#-CD	Comp A Coarse Delay
0	Coarse Delay Bypassed, Powered Down
1	Coarse Delay Active, Powered Up
Sel-CB#-CD	**Comp B Coarse Delay**
0	Coarse Delay Bypassed, Powered Down
1	Coarse Delay Active, Powered Up

Power Reduction Mode

If the coarse delay section is completely bypassed, the power to the delay cells is shut off and the total chip power consumption is reduced. This feature is useful in applications that do not require the coarse delay function.

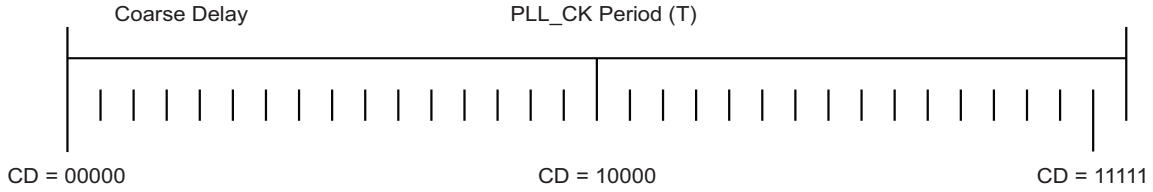


FIGURE 27. Coarse Delay

Coarse Falling Edge Delay Adjust

The falling edge delay circuitry adds or subtracts timing delay to or from the falling edge (Tpd–) while having no effect on the rising edge (Tpd+). Propagation delay adjustment is typically used for removing any pulse width distortion inside a tester.

Coarse falling edge adjust divides the overall delay range (span), set by the period of PLL_CK, into 16 equal segments, and allows the falling edge propagation delay of the signal to be modified from –8 to +7 segments.

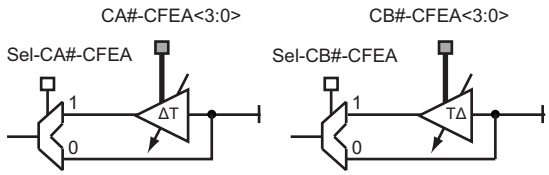


FIGURE 28.

The CFEA section may be bypassed by the select bit, which is set by the CPU port. The address of each select bit is listed in the memory map tables.

TABLE 42.

CFEA<3:0>	PLL_CK	ΔTpd–
0000 1000 1111	T = 10ns	Resolution = 312.5ps ΔTpd– = –2.5ns ΔTpd– = 0ns ΔTpd– = +2.1875ns
0000 1000 1111	T = 20ns	Resolution = 625ps ΔTpd– = –5.0ns ΔTpd– = 0ns ΔTpd– = +4.375ns

TABLE 43.

Sel-CA#-CFEA	Comp A Coarse Falling Edge Adjust
0	Coarse FEA Bypassed, Powered Down
1	Coarse FEA Active, Powered Up
Sel-CB#-CFEA	**Comp B Coarse Falling Edge Adjust**
0	Coarse FEA Bypassed, Powered Down
1	Coarse FEA Active, Powered Up

Power Reduction Mode

If the coarse falling edge adjust section is completely bypassed, the power to the delay cells is shut off and the total chip power consumption is reduced. This feature is useful in applications that do not require the coarse FEA function.

Output Stage

Each channel supports two comparator outputs (CA_# and CB_#) with the following characteristics:

1. Single ended outputs
2. 50Ω series terminated outputs
3. Programmable high and low levels.

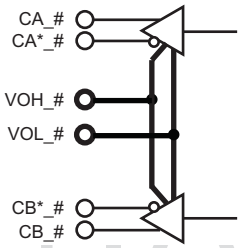


FIGURE 30.

Comparator Output Supply Levels

VOH and VOL are voltage power supply inputs that set the high and low level of CA_# and CB_#. VOH and VOL provide the current required to drive the off chip transmission line, and any DC current associated with any termination used Therefore, these inputs should be driven by a low impedance and low inductance source with ample current drive.

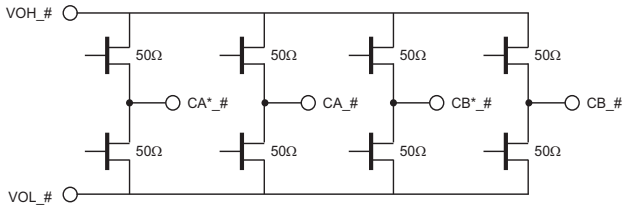


FIGURE 31.

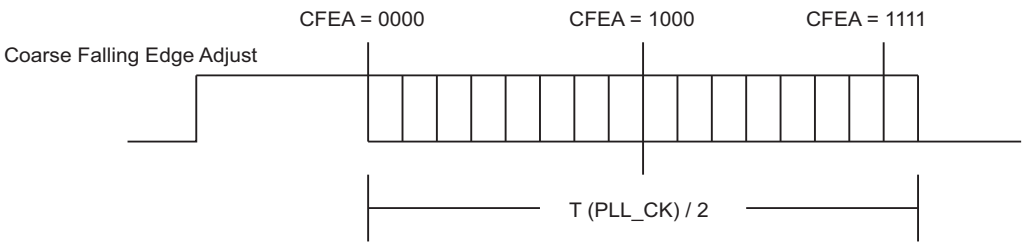


FIGURE 29. Coarse Falling Edge Adjust

Comparator Source Termination

In this configuration no external components are required, and a full amplitude signal is realized at the destination.

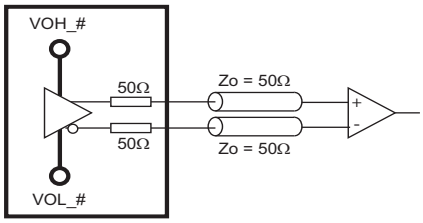


FIGURE 32.

Comparator Source and Destination Termination

In this configuration one external component is required, and a 50% amplitude signal is realized at the destination.

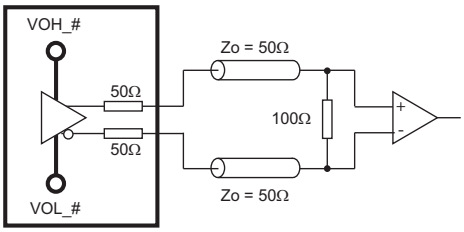


FIGURE 33.

Ring Oscillator

Each channel's data or enable path may be placed in a ring oscillator mode where the comparator is fed back into the driver. This mode is used mainly for test and calibration purposes.

.

TABLE 44.

Sel-RO-D#	Data Source
0	DATA_# (normal operation)
1	Ring#

Sel-RO-En#	Enable Source
0	EN_# (normal operation)
1	Ring#

The source for data and enable when configured as a ring oscillator is either CA# or CB#.

TABLE 45.

Sel -C#-RO	Feedback Signal
0	CA#
1	CB#

Ring Start Up

CPU-Pulse# is a write-only register that fires off a one-shot pulse that initiates the ring oscillating. The PMU port also controls which polarity of edge transition is the active edge that retriggers the loop.

TABLE 46.

Ring#-En	Edge#-Par	Ring Operation
0	X	Disabled
1	0	Enabled, Positive Edge
1	1	Enabled, Negative Edge

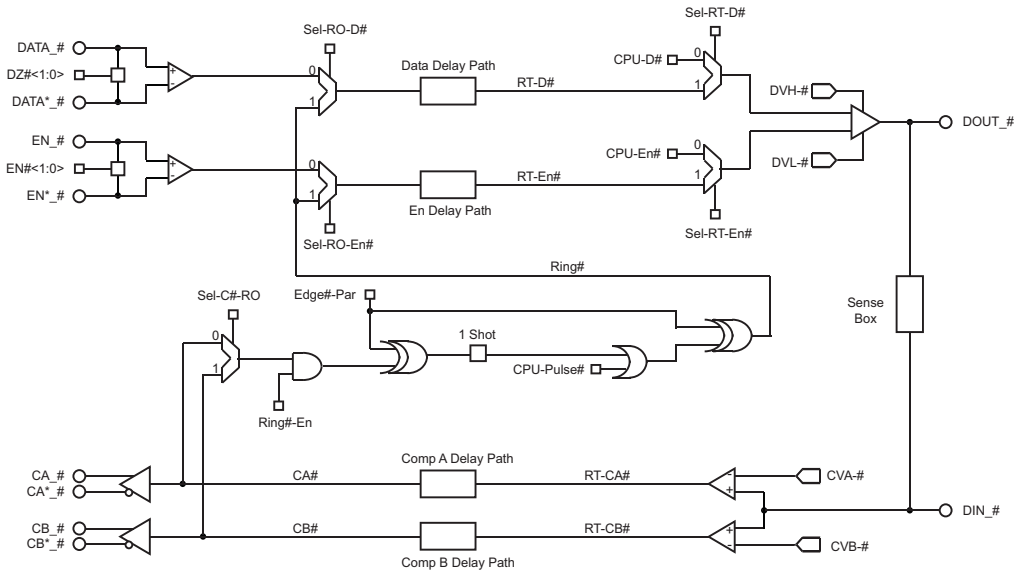


FIGURE 34. Ring Oscillator

Load

Overview

Each channel has an independent load with the following capabilities:

1. source and sink up to 24 mA
2. maintain a high impedance over a wide voltage
3. separate high and low commutating voltages
4. resistive load options.

Split Load

With independent high and low commutating voltages, the source and sink currents each have their own threshold voltage. If the voltage on the DIN_#, when the load is activated, is between the two commutating voltages, the load will remain in a high impedance state.

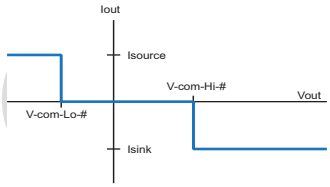


FIGURE 35.

The split load is useful as a transient voltage clamp on the transmission line between the pin electronics and the DUT. The split load may be configured like a traditional diode bridge by programming Vcom Hi-# = Vcom Lo-#.

Source and Sink Adjustment

The source and sink currents can be adjusted slightly upward or downward.

TABLE 47.

IL-Adj#<1:0>	Imax
00	Nominal
01	0.8 • Nominal
10	1.2 • Nominal
11	N/A

Maximum Current Levels

The source and sink current values may be set independently.

TABLE 48.

Isource<15:0>	Source Current	Vsource
0000 Hex	0mA	0V
FFFF Hex	24mA	+1V

Isink<15:0>	Sink Current	Vsink
0000 Hex	0mA	0V
FFFF Hex	24mA	+1V

Resolution = .3662µA

High Impedance

The source and sink currents may be controlled by either the CPU port or the EN input.

TABLE 49.

Sel-RT-Ld-En#	Ld-En#
0	CPU-Ld-En# (CPU control)
1	RT-Ld-En#* (Real Time control)

The on-chip switch makes the load on resistance ~50Ω.

TABLE 50.

Ld-En#	DIN_# to DOUT_#
0	Disconnected
1	Connected

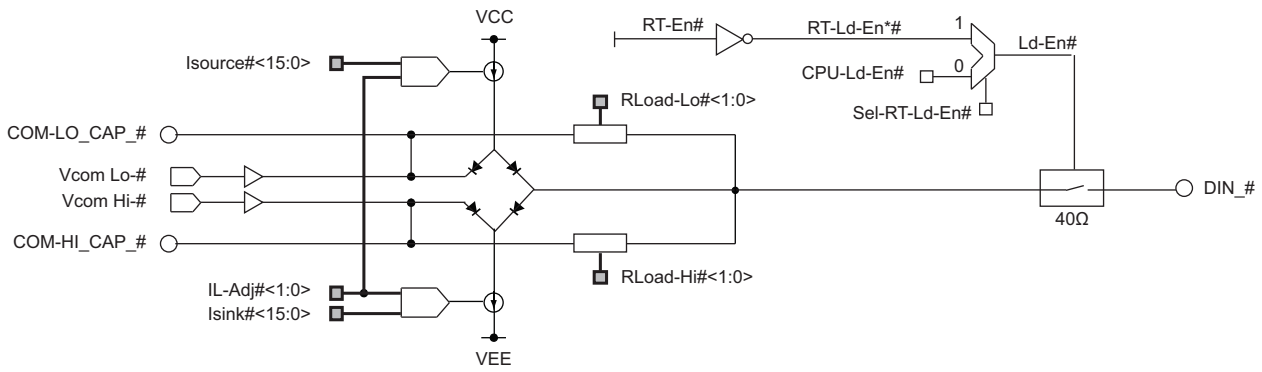


FIGURE 36. LOAD

Resistive Load

The load may also be configured as a selectable resistor to a programmable voltage. The resistive load is useful in applications with very low DUT output swings (where a traditional active load will not switch on and off completely or quickly) and also as a means of forcing the DUT to a known voltage when the DUT is in HiZ.

The source and sink currents should be programmed to 0 during normal operation of the resistive load.

High Impedance

The high and low resistive loads may be controlled by the CPU port or be under real-time control via the EN input signal.

TABLE 51.

Sel-RT-Ld-En#	Ld-En#
0	CPU-Ld-En# (CPU Control)
1	RT-Ld-En#* (Real Time Control)

When the resistive load is placed in HiZ it maintains a low leakage current when DIN_# is between the supply levels VCC and VEE.

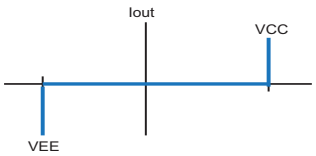


FIGURE 37.

Resistance Values

Each resistive load has two resistor values in parallel with the ability to connect either or both without restriction. The load resistance is in series with the HiZ switch impedance.

TABLE 52.

Rload Control Bit	Resistor Value
RLoad-Lo(Hi)#<1>	1KΩ
RLoad-Lo(Hi)#<0>	250Ω

By using different combinations of resistors and combining both the high and low buffers (Vcom Lo-# = Vcom Hi-#), a variety of equivalent impedances may be realized from 100Ω to 1 KΩ.

TABLE 53.

Rload-Lo<1:0>		Rload-HI<1:0>		Load Resistance
0	0	0	0	Open
0	0	0	1	290Ω
0	0	1	0	1KΩ
0	0	1	1	240Ω
0	1	0	0	290Ω
0	1	0	1	165Ω
0	1	1	0	240Ω
0	1	1	1	151Ω
1	0	0	0	1KΩ
1	0	0	1	240Ω
1	0	1	0	540Ω
1	0	1	1	207Ω
1	1	0	0	240Ω
1	1	0	1	151Ω
1	1	1	0	207Ω
1	1	1	1	140Ω

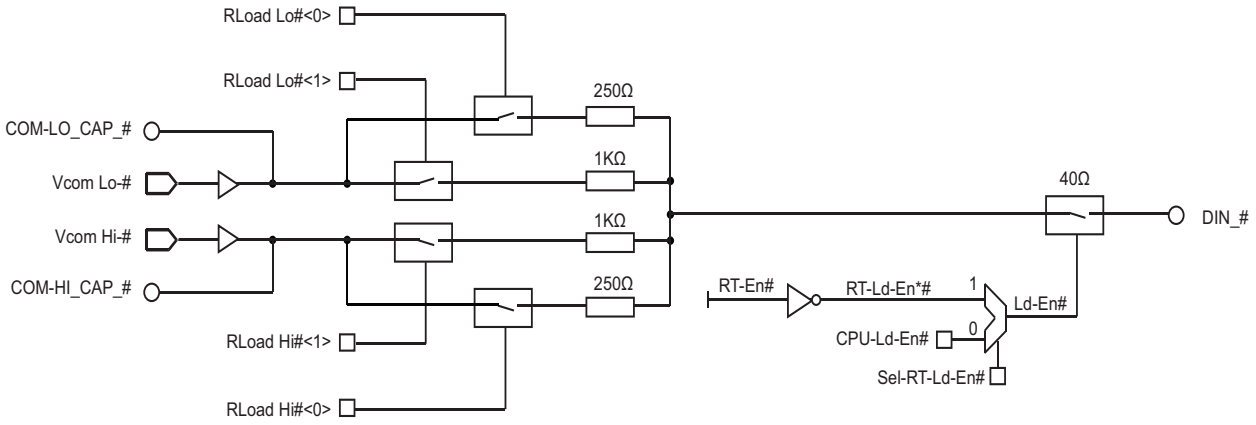


FIGURE 38.

DC Levels

Every functional block requires a variety of DC voltage levels in order to function properly. These levels are all generated on chip with a 16-bit DAC that is programmed through the CPU port.

There are 4 voltage range options. Various DC levels are grouped together, and the selected voltage range is common for all levels within each group.

TABLE 54.

Range Select<1:0>	Voltage Range	Output Voltage Swing (FS)	Resolution (LSB)
00	VR0	4V	61µV
01	VR1	8V	122µV
10	VR2	16V	244µV
11	VR3	32V	488µV

Range Select<1:0> = Drive#<1:0>
or Comp#<1:0>
or Vcom#<1:0>

The realizable voltage range is restricted by the power supply levels and headroom limitations. If a level is programmed beyond the recommended operating conditions, saturation will occur and the actual DC level will not match the desired programmed level.

Voltage Range Options

Within each DAC group, the voltage range selection is common and is programmed via the CPU port.

Level Programming

Voltage ranges VR0, VR1, VR2 and VR3 use the equation:

Vout = (Value - Vmid) • Gain + Offset + Vmid + DUT_GND

Current force mode (VIR) uses the equation:

Vout = (Value - Vmid) • Gain + Offset + Vmid

Value is described by the equation:

Value = {(DAC Code) / (2**N – 1)} • FS + Vmid – (FS / 2).

N = 16; 2**N – 1 = 65,535

The voltage range lower and upper limits are:

Vmin = Vmid – (FS / 2)
Vmax = Vmin + FS.

For I alarms and FI mode:

FS = 2V
Vmin = –1V
Vmid = 0V
Vmax = +1V.

For active loads (Isource and Isink):

FS = 1V
Vmin = 0V
Vmid = 0.5V
Vmax = 1.0V.

Offset and Gain

Each individual DC level has an independent offset and gain correction. These correction values allow the desired output level to be programmed at its true post calibrated value and to be loaded simultaneously across multiple pins without having to correct for per-pin errors. The range of possible offset voltage correction is a percentage of the full-scale voltage range of each particular voltage group.

TABLE 55.

Offset Code	Offset Value	Gain Code	Gain Value
0000H	–5.4% of FS	0000H	0.875
7FFFH	0	7FFFH	1.0
FFFFH	+5.4% of FS	FFFFH	1.125

Device Under Test Ground

The actual ground reference level at the DUT may be different than that used by the DAC reference. DUT_GND is a high impedance analog voltage input that provides a means of tracking the destination ground and making an additional offset to the programmed level so the programmed level is correct with respect to the DUT. Each channel has its own independent DUT_GND input.

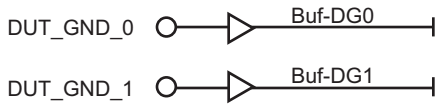


FIGURE 39.

The input at DUT_GND should be:

1. filtered for noise
2. stable
3. reflect the actual ground level at the DUT.

V_REF

V_REF is an analog input voltage that is used to program the on chip DC levels. V_REF should be held at +3.0V with respect to GND. Any noise or jitter on V_REF will contribute to the noise floor of the chip, and therefore V_REF should be as quiet and stable as possible.

There is one V_REF pin shared by all channels on the same chip.

V_REF Sensitivity

The above equations that predict the DAC output assume that V_REF = 3.000V. Any variation in V_REF at the input pin will affect Level by a 1:1 ratio before being multiplied by the gain.

Level = Programmed Level * (1 - (V_REF - 3.0))

Offset adjust has ample range to correct for deviations in V_REF, in addition to any offset requirements. As long as V_REF is held stable after calibration, deviation in V_REF from 3.0V will not affect DC accuracy.

Adjustable Vmid

To support applications that require a wide variety of voltage range options, the value for Vmid in the output level calculation is programmable. This adjustment allows the same total voltage swing in each of the different voltage ranges, only now that voltage span may be adjusted more positive or more negative.

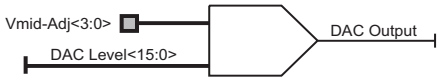


FIGURE 40.

Voltage Range	Vmid LSB	Vmid-Adj<3:0>	Vmid
VR0	125mV	0000 1111	+125mV +2.0V
VR1	250mV	0000 1111	+250mV +4.0V
VR2	500mV	0000 1111	+500mV +8.0V
VR3	1V	0000 1111	+1V +16.0V

Voltage Range Table

Several examples of different voltage ranges are shown in the table below. For simplicity in each example:

Gain Correction = 1.0

Offset Correction = 0.0V

DUT_GND = 0.0V.

Level Reference

All DC voltage levels are referenced to GND.

TABLE 56. Examples of Vmid Changing the Effective Voltage Output Range

Range	FS	Vmid-Adj>3:0>	Vmid	DAC Code	Output Voltage
VR0	4	0000	+0.125V	0000 Hex FFFF Hex	–1.875V +2.125V
VR0	4	1011	+1.5V	0000 Hex FFFF Hex	–0.5V +3.5V
VR0	4	1111	+2V	0000 Hex FFFF Hex	0V 4V
VR1	8	0000	+0.25V	0000 Hex FFFF Hex	–3.75V +4.25V
VR1	8	1011	+3V	0000 Hex FFFF Hex	–1V +7V
VR1	8	1111	+4V	0000 Hex FFFF Hex	0V +8V
VR2	16	0000	+0.5V	0000 Hex FFFF Hex	–7.5V +8.5V
VR2	16	1011	+6.0V	0000 Hex FFFF Hex	–2V +14V
VR2	16	1111	+8V	0000 Hex FFFF Hex	0V +16V
VR3	32	0000	+1V	0000 Hex FFFF Hex	–15V +17V
VR3	32	1011	+12V	0000 Hex FFFF Hex	–4V +28V
VR3	32	1111	+16V	0000 Hex FFFF Hex	0V +32V

Voltage Range Options vs. Function

Different functional blocks require different DC level voltage ranges. The allowed combinations are listed in the table below.

TABLE 57. Range Decode

Group	Functional Block	VR0	VR1	VR2	VR3	VIR	Range Select Bits<1:0>
Drive	Driver **DVH, DVL**		√	√	√		Drive#<1:0>
PMU	PMU Forcing Voltage **DVH**	√	√	√	√		Drive #<1:0>
Comp	Comparator Thresholds **CVA, CVB**	√	√	√	√		Comp#<1:0>
Load/Alarm	Source/Sink Currents **Isource, Isink, I-Al-Hi, I-Al-Lo**					√	N/A
Vcom	Commutating Voltages **V-com-Hi, V-com-Lo**	√	√	√	√		Vcom#<1:0>

Tracks DUT_GND (FV, MV)

Does NOT Track DUT_GND (FI, MI)

DC Calibration

The part is designed and tested to meet its DC accuracy specifications after a two-point, two-iteration calibration. The actual calibration points are different for each voltage range and may even be different for the same voltage range but for different functional blocks. In general, most calibration points will be at 20% and 80% of the full-scale value for that range. (The actual calibration points are listed separately for each functional block in the DC specification section.)

The test points are broken into two categories:

1. inner test
2. outer test.

The inner test is one specific test point (typically) at 50% of the full-scale value of the particular range. The outer test is usually taken at the end points of the voltage range, or 0% and 100% of the full-scale value.

In general, the inner test will be performed against tighter, more accurate limits, but every part shipped will be calibrated and tested against the limits in the specification section and is guaranteed to perform within those limits under the documented calibration technique.

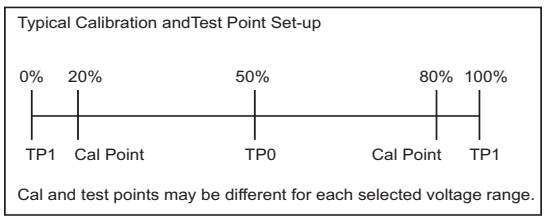


FIGURE 41.

System Level DC Accuracy

Other calibration schemes and techniques - using more or fewer calibration points or different test points, may also be employed. The resulting system-level accuracy may be superior or inferior to the part's specified limits and will be dependent on the details of the particular application.

Calibration Procedure

1. Calibrate the MONITOR
2. Calibrate the DAC using the DAC cal bits
3. Calibrate the offset DAC
4. Calibrate the Gain DAC
5. Calibrate the IL-Adjust
6. Calibrate the DC Level.

Level Calibration

INITIALIZE

- Select desired voltage range (VR0, VR1, VR2, VR3)
- Set Gain = 1.0; Offset = 0.0V

MEASURE

- Set Level 1 = Cal Point 1. Measure Output1' (low)
- Set Level 2 = Cal Point 2. Measure Output2' (high)

CALCULATE

- Gain' = (Output2' - Output1') / (Level 2 - Level1)
- Offset' = (Output2' - Vmid) – Gain' • (Level2 - Vmid)

FINISH

- Set Offset = - Offset' / Gain'
- Set Gain = 1.0 / Gain'

DAC Calibration

There is one dedicated 16-bit DAC used to generate the DC levels required. To facilitate superior DC accuracy, each DAC supports the ability to independently calibrate the top 5 MSBs.

The magnitude of the bit correction is an integer count of LSB voltage added to or subtracted from the individual bit weighting, and is therefore a function of the particular voltage range selected for each level. The DAC MSB adjustment is applied to the DC level prior to the gain correction.

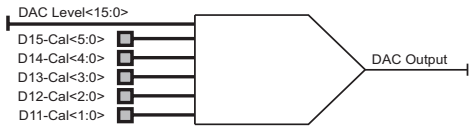


FIGURE 42.

TABLE 58. D15 Calibration

D15-Cal<5>	D15-Cal<4>	D15-Cal<3>	D15-Cal<2>	D15-Cal<1>	D15-Cal<0>	D15 Adjustment
0	1	1	1	1	1	+93 LSB
			•			•
0	0	0	0	0	1	+3 LSB
0	0	0	0	0	0	No Adjustment
1	0	0	0	0	0	No Adjustment
1	0	0	0	0	1	–3 LSB
			•			•
1	1	1	1	1	1	–93 LSB

TABLE 59. D14 Calibration

D14-Cal<4>	D14-Cal<3>	D14-Cal<2>	D14-Cal<1>	D14Cal<0>	D14 Adjustment
0	1	1	1	1	+45 LSB
		•			•
0	0	0	0	1	+3 LSB
0	0	0	0	0	No Adjustment
1	0	0	0	0	No Adjustment
1	0	0	0	1	–3 LSB
		•			•
1	1	1	1	1	–45 LSB

TABLE 60. D13 Calibration

D13-Cal<3>	D13-Cal<2>	D13-Cal<1>	D13Cal<0>	D13 Adjustment
0	1	1	1	+21 LSB
	•			•
0	0	0	1	+3 LSB
0	0	0	0	No Adjustment
1	0	0	0	No Adjustment
1	0	0	1	–3 LSB
	•			•
1	1	1	1	–21 LSB

TABLE 61. D12 Calibration

D12-Cal<2>	D12-Cal<1>	D12Cal<0>	D12 Adjustment
0	1	1	+9 LSB
0	1	0	+6 LSB
0	0	1	+3 LSB
0	0	0	No Adjustment
1	0	0	No Adjustment
1	0	1	–3 LSB
1	1	0	–6 LSB
1	1	1	–9 LSB

TABLE 62. D11 Calibration

D11-Cal<1>	D11Cal<0>	D11 Adjustment
0	1	+3 LSB
0	0	No Adjustment
1	0	No Adjustment
1	1	–3 LSB

TABLE 63. Cal Range vs. Voltage Range vs. DAC Bit

	D15	D14	D13	D12	D11
VR0	5.67mV	2.75mV	1.28mV	549µV	183µV
VR1	11.35mV	5.5mV	2.56mV	1.1mV	366µV
VR2	22.7mV	10.1mV	5.12mV	2.2mV	732µV
VR3	45.4mV	20.2mV	10.24mV	4.4mV	1.46mV

External Force / Sense

An external force and sense path exists to DIN_#. These paths are useful for:

1. connecting a central PMU to the DUT
2. DC calibration.

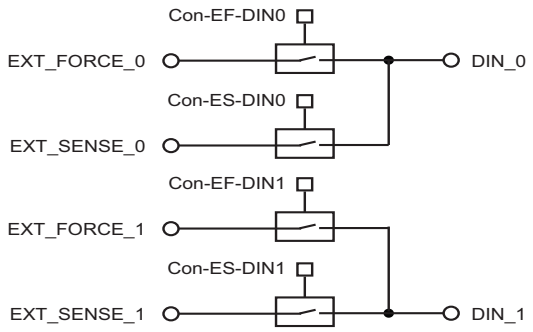


FIGURE 43.

TABLE 64.

Con-EF-DIN#	EXT_FORCE_# to DIN_#
0	Disconnected
1	Connected

Con-ES-DIN#	EXT_SENSE_# to DIN_#
0	Disconnected
1	Connected

Control Bits

There are two control bits per channel that provide digital outputs under CPU control. The outputs are open drain that sink current in a low state and go HiZ in a high state. Each output will typically require an external resistor in order to function properly if a voltage at the output is required.

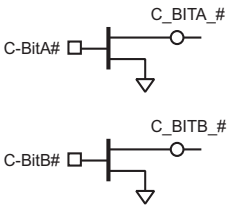


FIGURE 44.

TABLE 65.

C-BitA(B)#	C_BITA(B)_#
0	HiZ
1	Sinking Current

Diagnostics

Each channel has access to key internal nodes so that the voltage on these nodes may be monitored. This access is typically used for testing and diagnostic purposes.

Per Channel Diagnostic Options

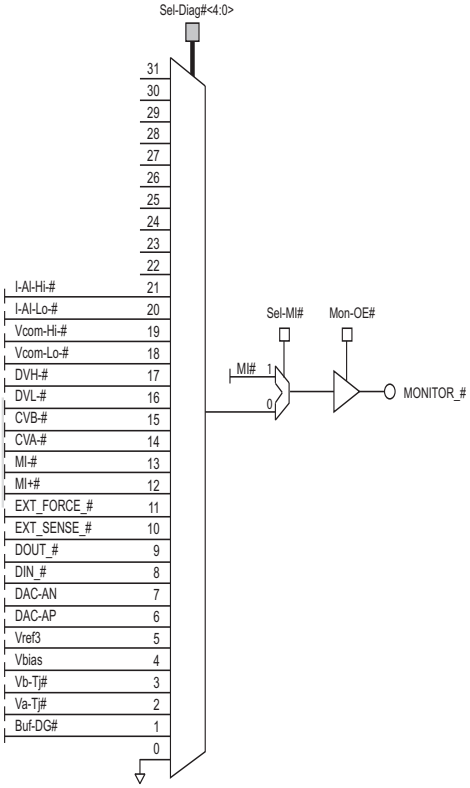


FIGURE 45.

Monitor

The selected diagnostic signal becomes available on the MONITOR output pin for that channel. MONITOR may be placed into a high-impedance state by the CPU port.

TABLE 66.

Mon-OE#	Sel-MI#	MONITOR_#
0	X	HiZ
1	0	Diagnostics#
1	1	MI#

Temperature Sensing

It is possible to measure and monitor the junction temperature on a per-channel basis. Test voltages Va-Tj and Vb-Tj are generated on chip and allow the calculation of the junction temperature. The equation is:

$$Tj = \{(Va\text{-}Tj - Vb\text{-}Tj) * 1{,}017\} - 127\ °C$$

Va-Tj and Vb-Tj must be read back separately through the PPMU and off the chip via the MONITOR pin for the calculation to be performed.

The on-chip temperature sensor provides a means for monitoring the relative temperature change of the IC. It is not intended for absolute temperature measurements.

Thermal Diodes

Direct real time junction temperature access is provided via a thermal diode. There is one diode per channel.

FIGURE 46.

The thermal diodes are useful when junction temperature needs to be tracked without going through the CPU port.

External References & Components

Many on-chip functional blocks reference a precision external:

1. Voltage
2. Frequency

By locking on-chip performance to an external reference, circuit performance will be more consistent over:

1. Temperature
2. Part-to-part distribution

V_REF

V_REF is an analog input voltage that is used to program the on-chip DAC levels. V_REF should be held at +3.0V. Any noise or jitter on V_REF will contribute to the noise floor of the chip; therefore V_REF should be filtered and quiet and stable as possible.

There is one V_REF shared by both channels.

R_EXT

R_EXT is a precision off-chip resistor used to generate precise and stable current sources on chip.

PLL Clock

PLL_CK is an external frequency that establishes the span and the resolution of all on-chip delay elements. There is one PLL_CK shared by both channels. *For any applications that do not use any delay elements, PLL_CK must be placed in a low state. Do NOT leave PLL_CK / PLL_CK* floating.*

PLL Filter Capacitor

A capacitor at pin CAP_PLL is used to compensate the op amp used in the PLL filter circuitry. The other end of the capacitor should be connected to ground.

Power Supply Restrictions

The following guidelines must be met to support proper operation:

1. VCC ≥ VDD
2. VEE ≤ GND
3. VDD ≥ GND

Schottky diodes are recommended on a once-per-board basis to protect against a power supply restriction violation.

To prevent latch-up, the required power-up sequence is:

1. VEE
2. VCC
3. VDD
4. VOH and VOL
5. VREF

Since it is not always possible to guarantee a particular power-up/power-down sequence, particularly if there is a power supply fault of some kind, schottky diodes are added as shown below.

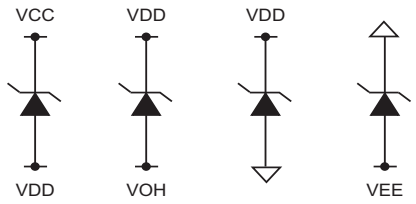


FIGURE 47.

These schottkies need to be of the power variety and should be added on a once-per-board basis. The point is to have the schottky voltage during a fault condition be less than a silicon junction diode. To that end, the schottky voltage should be less than 500mV. The sizing of the schottky needs to take into account the current that flows during the fault condition so that it's voltage doesn't exceed the 500mV.

The power-down sequence is just as essential as the power-up sequence stated above. The required power-down sequence is opposite of the power-up sequence, with the order stated below.

1. VREF
2. VOH and VOL
3. VDD
4. VCC
5. VEE

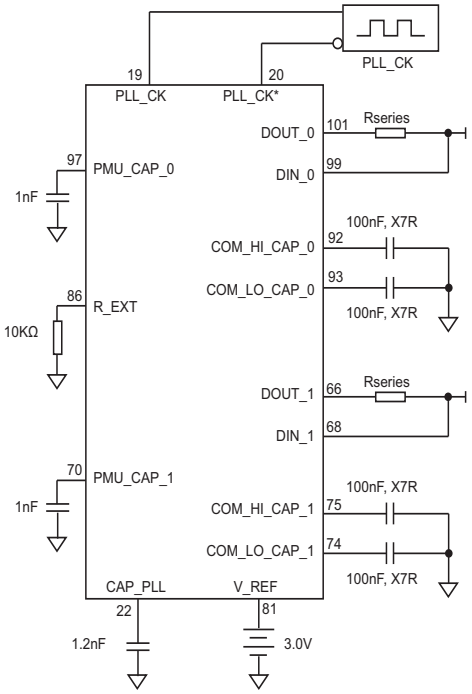


FIGURE 48.

Transmission Line Inductors

Depending on the particular application and specific details of the PC Board layout a series inductor may or may not be placed at the DOUT pin to compensate for the capacitance on that node. The actual inductor value is application-specific.

External Resistors

For 50Ω transmission line environments, an external resistor will need to be added to create a 50? source-terminated driver.

Decoupling Capacitors

The need for decoupling capacitors is dependent upon the particular application and is therefore system-dependent. There is nothing inherent in the chip design that mandates or requires these capacitors.

Commutating Buffer Capacitors

COM_LO_CAP_# and COM_HI_CAP_# are the outputs of the commutating buffers. o achieve good AC performance each requires an off-chip capacitor to provide or absorb any transient currents associated with the active load or the resistive load.

PMU Compensation Capacitors

PMU_CAP_# is used to help with PMU stability under large capacitive loads.

CPU Port

Overview

All on-board DACs and registers are controlled through the CPU serial data port, which is capable of writing to and reading back from the chip.

Address

Address words for every CPU transaction are all 16 bits in length and contain the destination of the data word for a write cycle, or the source to be read back for a read cycle. Address bits are shifted in LSB first, MSB last.

Data

Data words for every CPU transaction are all 16 bits in length and are loaded or read back LSB first, MSB last. The timing for data is different for a read cycle vs. a write cycle, as the drivers on the SDIO alternate between going into high impedance and driving the line.

Control Signals

There are 3 CPU interface signals: SDIO, CK, and STB. SDIO is a bi-directional data pin through which information is either loaded or written back. CK is the CPU port clock signal that transfers data back and forth. When data is going into the part, SDIO is latched on a rising edge of CK. When data is coming out of the part, SDIO is again updated on a rising edge of CK. STB is the control signal that identifies the beginning of a CPU transaction. STB remains high for the duration of the transaction, and must go low for at least 1 CK cycle before another CPU transaction may begin.

CK must be running at all times even if no CPU transactions are occurring. CK is used on-chip for other functions and MUST run continuously for correct chip operation.

Write Enable

Various register bits in the memory map tables require a write enable (WE) to allow those bits to be updated during a CPU write cycle. WE control allows some bits within an address to be changed while others are held constant. Each WE applies to all lower data bits until another WE is reached.

If WE = 1, the registers in the WE group will be written to. If WE = 0, the registers will not be updated.

If WE = 0, all data bits associated with that WE should be programmed to 0.

Read vs. Write Cycle

The first SDIO bit latched by CK in a transaction identifies the transaction type.

TABLE 67.

1st SDIO Bit	CPU Transaction Type
0	Read - Data flows out of the chip
1	Write - Data flows into the chip

Parallel Write

The second SDIO bit of a transaction indicates whether a parallel write occurs.

TABLE 68.

2nd SDIO Bit	CPU Transaction Type
0	Data goes to the selected channel
1	Data goes to both channels

A parallel write ignores the particular channel address and writes the information into the same location on all channels.

Reset

RESET is an external hardware reset signal that places all internal registers and control lines into a low state. Reset must be executed independently after a power up sequence. *RESET does NOT place the DAC level memory into a known state, so this information must always be loaded after a power up sequence.*

FIGURE 49.

RESET is active high.

In addition, the CPU port can execute a reset (as a write-only transaction). If the CPU-Reset address is written to, regardless of the value of any of the SDIO bits, CPU-Reset will fire a one-shot pulse that performs the same function as an external RESET. CPU-Reset is a write-only register.

Chip ID

Chip ID (see memory map tables) is a read-only function that identifies the product and the die revision.

TABLE 69.

Product-ID<11:0> (D15:D4)	Die-Rev<3:0> (D3:D0)
078 Hex (120 Decimal)	Die Revision

DAC Sample and Hold (S/H) State Machine

The internal DAC's used in the ISL55188-AS are S/H DACs. To update a single DAC level, it takes 387 clocks cycles. The clock used for this operation is the CPU interface clock. The first 256 clocks are used to select the desired level and let the DAC level settle. The next 128 clocks are needed to refresh the S/H. The 3 remaining clock cycles are used to control the state machine. To calculate the time to refresh one DAC level, multiply the CPU clock time by the number of clocks needed to update one level. If using a 25MHz clock the time needed is: 40ns • 387 cycles = 15.48µs. There are 24 total internal levels to the S/H DAC therefore , to update the entire DAC the time would be: 24 • 40ns • 387 cycles = 371.52µs.

The order the state machine uses to refresh the DAC matches the RAM address mapping: DVH0, DVH1, DVL0, DVL1, etc.. This order allows both channels to update whenever a parallel-channel write is performed for the same level. Whenever writing to a specific level, the state machine will complete the current level already being processed and then jump to the level just written. After the selected level is written, the state machine then proceeds in the normal order from this level forward (i.e. it doesn't jump back). Therefore you should assume that, at worst case, it takes 774 clocks to update a single level after being written, 387 to complete the current level, plus 387 to update the desired level. One caveat to this is with a parallel-channel write. There will still be, at worst case, 774 clocks to update the first (lower numbered) channel of the parallel write. The other channel in the parallel-channel write will be updated in sequence after the first one. That means that if channel 0 and channel 1 are written as part of a parallel-channel write, channel 0 could take 774 clocks to update (worst case) and then channel 1 will update 387 clocks later. Care should be taken when continuously writing to a particular level such that other levels are not starved of being refreshed by the CPU clock. If this happens, levels can droop out of specification.

Address Description

Information is stored on-chip in two ways:

1. RAM
2. Registers

Each storage mechanism is then broken into two categories:

1. Per Pin resources
2. Central resources

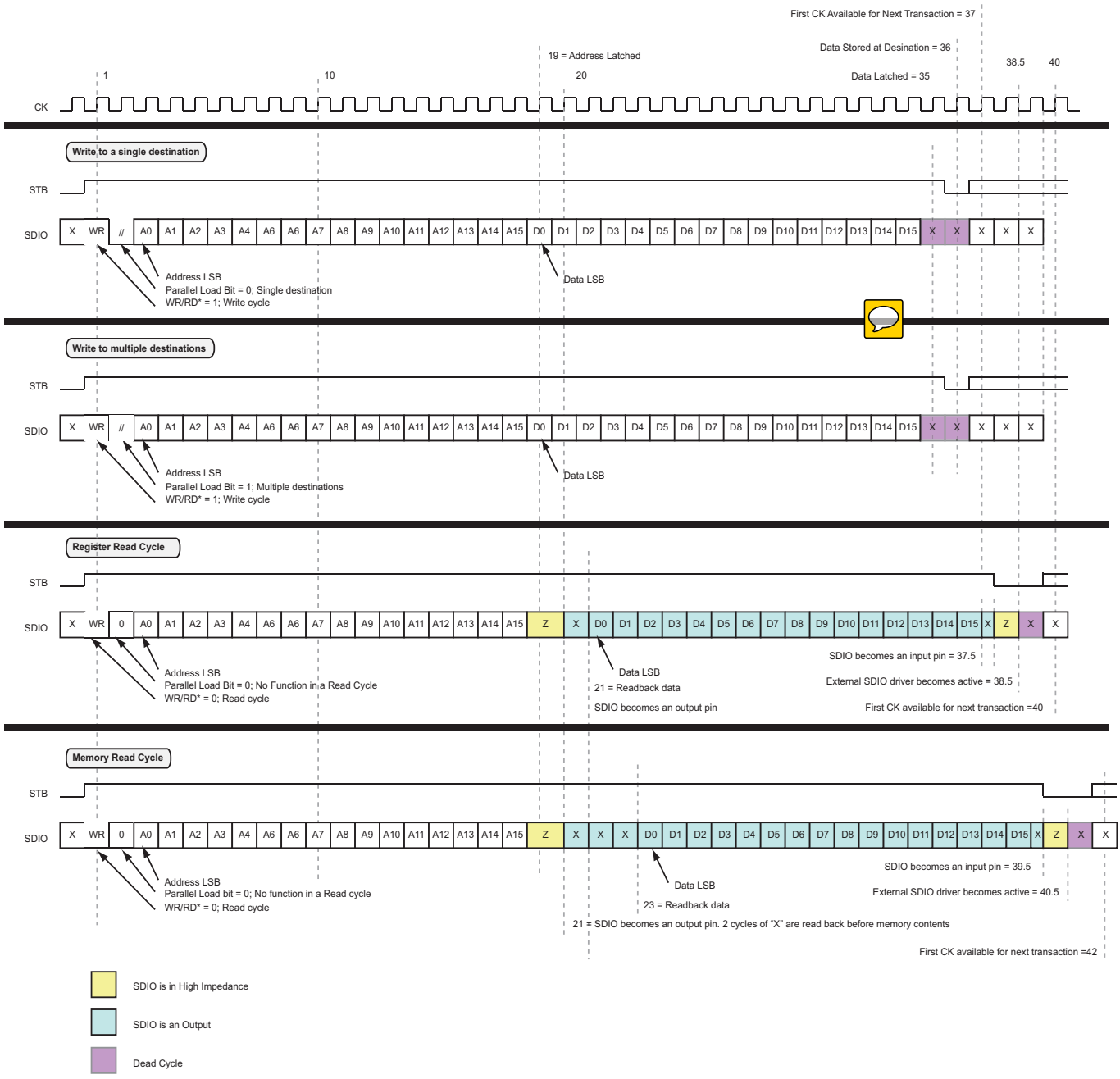
The address space is partitioned into several different segments to clearly mark the resource type and function.

Unused register bits should be written as a logical "0" and read back as don't care "X" conditions.

TABLE 70.

Per Pin Resource RAM Storage																
Register Bit	Central Bit	Channel Address							DAC Function		Resource Address					Description
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0	0	0	0	0	A4	A3	A2	A1	A0	Channel 0 DC Levels
0	0	0	0	0	0	0	0	0	0	1	A4	A3	A2	A1	A0	Channel 0 DC Level Offset Values
0	0	0	0	0	0	0	0	0	1	0	A4	A3	A2	A1	A0	Channel 0 DC Level Gain Values
0	0	0	0	0	0	0	0	0	1	1	A4	A3	A2	A1	A0	Not Used
0	0	0	0	0	0	0	0	1	0	0	A4	A3	A2	A1	A0	Channel 1 DC Levels
0	0	0	0	0	0	0	0	1	0	1	A4	A3	A2	A1	A0	Channel 1 DC Level Offset Values
0	0	0	0	0	0	0	0	1	1	0	A4	A3	A2	A1	A0	Channel 1 DC Level Gain Values
0	0	0	0	0	0	0	0	1	1	1	A4	A3	A2	A1	A0	Not Used
Per Pin Resource Register Storage																
Register Bit	Central Bit	Channel Address							Resource Address							Description
1	0	0	0	0	0	0	0	0	A6	A5	A4	A3	A2	A1	A0	Channel 0 Registers
1	0	0	0	0	0	0	0	1	A6	A5	A4	A3	A2	A1	A0	Channel 1 Registers
Central Resource Register Storage																
Register Bit	Central Bit	Unused Bits							Resource Address							Description
1	1	0	0	0	0	0	0	0	A6	A5	A4	A3	A2	A1	A0	Central Resource Registers

Protocol Timing Diagram



Address Space - Per Pin DC Levels

Per Pin Resource RAM Storage																
Register Bit	Central Bit	Channel Address							DAC Function		Resource Address					Description
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0	0	#	0	0	0	0	0	0	0	DVH-#
0	0	0	0	0	0	0	0	#	0	0	0	0	0	0	1	DVL-#
0	0	0	0	0	0	0	0	#	0	0	0	0	0	1	0	CVA-#
0	0	0	0	0	0	0	0	#	0	0	0	0	0	1	1	CVB-#
0	0	0	0	0	0	0	0	#	0	0	0	0	1	0	0	Vcom Hi-#
0	0	0	0	0	0	0	0	#	0	0	0	0	1	0	1	Vcom Lo-#
0	0	0	0	0	0	0	0	#	0	0	0	0	1	1	0	ISource-#
0	0	0	0	0	0	0	0	#	0	0	0	0	1	1	1	ISink-#
0	0	0	0	0	0	0	0	#	0	0	0	1	0	0	0	I-AI-Hi-#
0	0	0	0	0	0	0	0	#	0	0	0	1	0	0	1	I-AI-Lo-#
0	0	0	0	0	0	0	0	#	0	0	10 - 31					Not Used
0	0	0	0	0	0	0	0	#	0	1	0	0	0	0	0	DVH-# Offset
0	0	0	0	0	0	0	0	#	0	1	0	0	0	0	1	DVL-# Offset
0	0	0	0	0	0	0	0	#	0	1	0	0	0	1	0	CVA-# Offset
0	0	0	0	0	0	0	0	#	0	1	0	0	0	1	1	CVB-# Offset
0	0	0	0	0	0	0	0	#	0	1	0	0	1	0	0	Vcom Hi-# Offset
0	0	0	0	0	0	0	0	#	0	1	0	0	1	0	1	Vcom Lo-# Offset
0	0	0	0	0	0	0	0	#	0	1	0	0	1	1	0	ISource-# Offset
0	0	0	0	0	0	0	0	#	0	1	0	0	1	1	1	ISink-# Offset
0	0	0	0	0	0	0	0	#	0	1	0	1	0	0	0	I-AI-Hi-# Offset
0	0	0	0	0	0	0	0	#	0	1	0	1	0	0	1	I-AI-Lo-# Offset
0	0	0	0	0	0	0	0	#	0	1	10 - 31					Not Used
0	0	0	0	0	0	0	0	#	1	0	0	0	0	0	0	DVH-# Gain
0	0	0	0	0	0	0	0	#	1	0	0	0	0	0	1	DVL-# Gain
0	0	0	0	0	0	0	0	#	1	0	0	0	0	1	0	CVA-# Gain
0	0	0	0	0	0	0	0	#	1	0	0	0	0	1	1	CVB-# Gain
0	0	0	0	0	0	0	0	#	1	0	0	0	1	0	0	Vcom Hi-# Gain
0	0	0	0	0	0	0	0	#	1	0	0	0	1	0	1	Vcom Lo-# Gain
0	0	0	0	0	0	0	0	#	1	0	0	0	1	1	0	ISource-# Gain
0	0	0	0	0	0	0	0	#	1	0	0	0	1	1	1	ISink-# Gain
0	0	0	0	0	0	0	0	#	1	0	0	1	0	0	0	I-AI-Hi-# Gain
0	0	0	0	0	0	0	0	#	1	0	0	1	0	0	1	I-AI-Lo-# Gain
0	0	0	0	0	0	0	0	#	1	0	10 - 31					Not Used
0	0	0	0	0	0	0	0	#	1	1	0 - 31					Not Used

Per Pin Registers

Channel 0 - 1 Control Registers (0 ≤ # ≤1)																				
Register Bit	Central Bit	Channel Address	Resource Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Description
1	0	#	0	En#	D#						WE	Sel-RO-En#	Sel-RO-D#	WE	Sel-RT-En#	CPU-En#	WE	Sel-RT-D#	CPU-D#	Driver Path Configuration
1	0	#	1	WE	Dr-Bias#<2>	Dr-Bias#<1>	Dr-Bias#<0>	WE	SR+#<4>	SR+#<3>	SR+#<2>	SR+#<1>	SR+#<0>	WE	SR-#<4>	SR-#<3>	SR-#<2>	SR-#<1>	SR-#<0>	Driver Output Configuration
1	0	#	2		WE	Sel-D#-CFEA	WE	D#-CFEA<3>	D#-CFEA<2>	D#-CFEA<1>	D#-CFEA<0>	WE	Sel-D#-CD	WE	D#-CD<4>	D#-CD<3>	D#-CD<2>	D#-CD<1>	D#-CD<0>	Data Path Deskew
1	0	#	3	WE	Sel-CFEA+#	Sel-En#-CFEA	WE	En#-CFEA<3>	En#-CFEA<2>	En#-CFEA<1>	En#-CFEA<0>	WE	Sel-En#-CD	WE	En#-CD<4>	En#-CD<3>	En#-CD<2>	En#-CD<1>	En#-CD<0>	Enable Path Deskew
1	0	#	4			OI-Hi#	OI-Lo#	Global-OI#	WE	CPU-Pulse#	WE	CPU-OI-Reset#	WE	Ring#-En	Edge#-Par	WE	Sel-C#-RO	WE	CPU-OI-En#	Current Clamps/Ring Oscillator
1	0	#	5	WE	PMU-Cap-En#	WE	Sel-FB#<2>	Sel-FB#<1>	Sel-FB#<0>	WE	Sel-MI+#<1>	Sel-MI+#<0>	WE	Sel-MI-#<1>	Sel-MI-#<0>	WE	IR#<2>	IR#<1>	IR#<0>	Current Measure (I Sense Box)
1	0	#	6		WE	C-BitB#	C-BitA#	WE	Con-EF-Din#	WE	Con-ES-DIN#	WE	Reserved	WE	EZ#<1>	EZ#<0>	WE	DZ#<1>	DZ#<0>	On-Chip Terminations/Switches
1	0	#	7		WE	I-Limit-Dis#	WE	Sel-Gnd-Ref#	Gnd-Ref-OE#	WE	Sel-Diag#<4>	Sel-Diag#<3>	Sel-Diag#<2>	Sel-Diag#<1>	Sel-Diag#<0>	WE	Mon-OE#	WE	Sel-MI#	Monitor/Diagnostics

Read Only

Write Only

Per Pin Registers - continued

Channel 0 - 1 Control Registers (0 ≤ # ≤1)																				
Register Bit	Central Bit	Channel Address	Resource Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Description
1	0	#	8-63																	Not Used
1	0	#	64 40H	RT-CB#	RT-CA#	Diff-Comp					WE	Sel-Diff-B#	Sel-Diff-A#	WE	Sel-RT-C#	WE	Sel-OI#	CPU-CB#	CPU-CA#	Comparator Path Configuration
1	0	#	65 41H		WE	Sel-CA#-CFEA	WE	CA#-CFEA<3>	CA#-CFEA<2>	CA#-CFEA<1>	CA#-CFEA<0>	WE	Sel-CA#-CD	WE	CA#-CD<4>	CA#-CD-<3>	CA#-CD-<2>	CA#-CD-<1>	CA#-CD-<0>	Comp A Path Deskew
1	0	#	66 42H		WE	Sel-CB#-CFEA	WE	CB#-CFEA<3>	CB#-CFEA<2>	CB#-CFEA<1>	CB#-CFEA<0>	WE	Sel-CB#-CD	WE	CB#-CD<4>	CB#-CD<3>	CB#-CD<2>	CB#-CD<1>	CB#-CD<0>	Comp B Path Deskew
1	0	#	67 43H								WE	RLoad-Lo#<1>	RLoad-Lo#<0>	WE	RLoad-Hi#<1>	RLoad-Hi#<0>	WE	CPU-Ld-En#	Sel-RT-Ld-En#	Load Configuration
1	0	#	68 44H					WE	IL-Adj#<1>	IL-Adj#<0>	WE	Vcom#<1>	Vcom#<0>	WE	Comp#<1>	Comp#<0>	WE	Drive#<1>	Drive#<0>	Voltage Range Selection
1	0	#	69-127																	Not Used

Read Only

Central Resource Register

Central Resource Control Registers																			
Register Bit	Central Bit	Channel Address	Resource Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Description
1	1	0	0				WE	D14-Cal<4>	D14-Cal<3>	D14-Cal<2>	D14-Cal<1>	D14-Cal<0>	WE	D15-Cal<5>	D15-Cal<4>	D15-Cal<3>	D15-Cal<2>	D15-Cal<1>	D15-Cal<0>	Upper DAC Bit Calibration
1	1	0	1					WE	D11-Cal<1>	D11-Cal<0>	WE	D12-Cal<2>	D12-Cal<1>	D12-Cal<0>	WE	D13-Cal<3>	D13-Cal<2>	D13-Cal<1>	D13-Cal<0>	Mid DAC Bit Calibration
1	1	0	2	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CPU Reset
1	1	0	3				WE	PLL-Dis	WE	F-Clamp<1>	F-Clamp<0>	WE	PLL-Z<1>	PLL-Z<0>	WE	Vmid-Adj<3>	Vmid-Adj<2>	Vmid-Adj<1>	Vmid-Adj<0>	Vmid/PLL
1	1	0	4													WE	Diff-Z	WE	Not Used	Differential Comparator
1	1	0	5-126																	Not Used
1	1	0	127	Product-ID<11>	Product-ID<10>	Product-ID<9>	Product-ID<8>	Product-ID<7>	Product-ID<6>	Product-ID<5>	Product-ID<4>	Product-ID<3>	Product-ID<2>	Product-ID<1>	Product-ID<0>	Die-Rev<3>	Die-Rev<2>	Die-Rev<1>	Die-Rev<0>	Die ID

Read Only

Write Only

Manufacturing Information

Moisture Sensitivity

ISL55188-AS is a Level 3 (JEDEC Standard 033A) moisture-sensitive part. All Pre-Production and Production shipments will undergo the following process post final test:

- Baked @ +125°C ± 5°C for a duration ≥ 16 hours
- Vacuum sealed in a moisture barrier bag (MBB) within 30 minutes after being removed from the oven.

PCB Assembly

The floor life is the time from the opening of the MBB to when the unit is soldered onto a PCB.

Chip Floor Life ≤ 168 Hours

Units that exceed this floor life must be baked before being soldered to a PCB.

Solder Profile

The recommended solder profile is dependent upon whether the PCB assembly process is lead-free or not.

TABLE 71.

Profile Feature	Pb-Free Assembly
Average Ramp-Up Rate (Tsmax to Tp)	3°C/sec (max)
Preheat • Min Temp (Ts min) • Max Temp (Ts max) • Time (min to max) (ts)	 150°C 200°C 60 - 120 sec
Ts max to Tp • Ramp-Up Rate	 3°C/sec (max)
Time Above • Temperature (T_L) • Time (t_L)	 217°C 60 - 150 sec
Peak Package Body Temperature	260°C
Time within 5°C of Actual Peak Temp (tp)	20 - 30 sec
Average Ramp-Down Rate (tp to Tsmax)	6°C/sec (max)
Time 25°C to Peak Temperature	8 minutes (max)

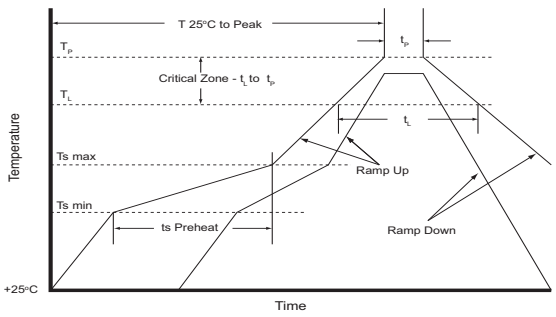


FIGURE 50.

Package Thermal Analysis

Junction Temperature

Maintaining a low and controlled junction temperature is a critical aspect of any system design. Lower junction temperatures translate directly into superior system reliability. A more stable junction temperature translates directly into superior AC and DC accuracy.

The junction temperature follows the equation:

$$Tj = Pd \bullet \theta JA + Ta$$

Tj = Junction Temperature

Pd = Power Dissipation

θJA = Thermal Resistance (Junction to Ambient)

Ta = Ambient Temerature

Heat can flow out of the package through two mechanisms:

- conduction
- convection

Conduction

Conduction occurs when power dissipated inside the chip flows out through the leads of the package and into the printed circuit board. While this heat flow path exists in every application, most of the heat flow will NOT occur with thermal conduction into the PCB.

Conduction also occurs in applications using liquid cooling, in which case most of the heat will flow directly out of the top of the package through the exposed heat slug and into the liquid cooled heat sink. The heat sink represents a low thermal resistance path to a large thermal mass with a controlled temperature.

The total thermal resistance is the series combination of the resistance from the junction to case (exposed paddle) (θJC) plus the resistance from the case to ambient (θCA)

Convection

The most common cooling scheme is to use airflow and (potentially) a heat sink on each part. In this configuration, most of the heat will exit the package via convection, as it flows through the die, into the paddle, and off the chip into the surrounding air flow.

Thermal Resistance

Each system will have its own unique cooling strategy and overall (θJA. However, the resistance between the junction and the case is a critical and common component to the thermal analysis in all designs.

$$\theta JA = \theta JC + \theta CA$$

θCA is determined by the system environment of the part and is therefore application specific. θJC is determined by the construction of the part.

θJC Calculation

θJC = θ(silicon)

+ θdie attach)

+ θ(paddle).

θJC = .072°C/W + .61°C / W + .006°C/W

θJC = .688°C/W.

The calculation is based upon ideal assumptions and it should be treated as a best-case value.

The thermal resistance of any material is defined by the equation:

θ = (Intrinsic material resistivity) • Thickness/Area

or

θ = Thickness / (Intrinsic material conductivity • Area).

Intrinsic Thermal Conductivity

Die Attach Thermal Conductivity = 1.4W/M°K

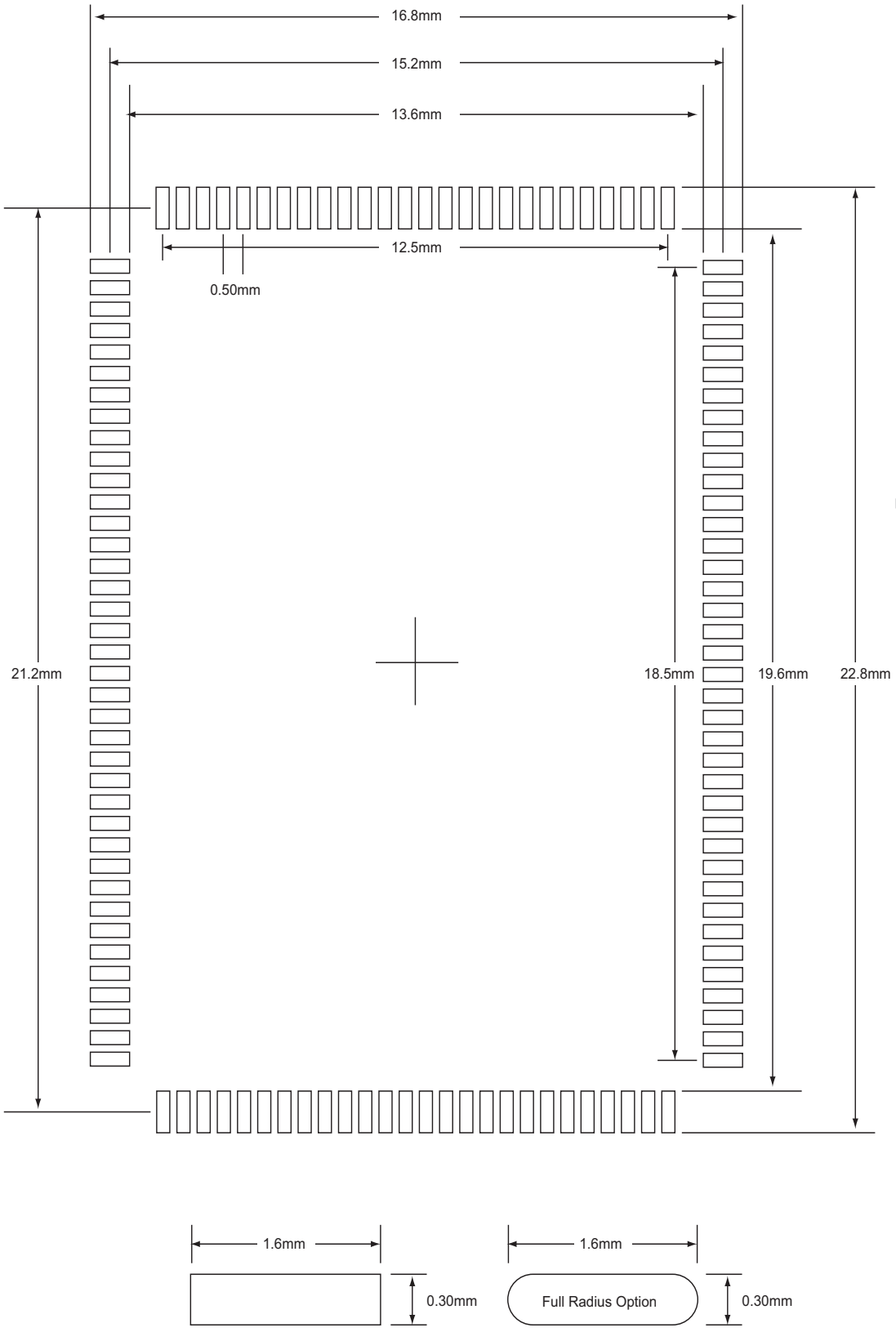
Silicon Thermal Conductivity = 141.2W/M°K

Paddle Thermal Conductivity = 263W/M°K

Plastic Thermal Conductivity = 0.88W/M°K

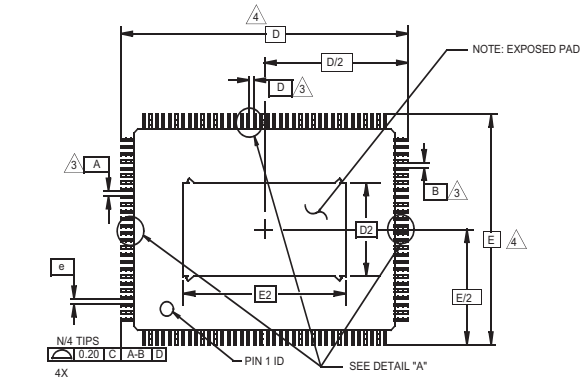
(Although some heat will flow throw the plastic package, the molding compound conductivity is not specifically used in the calculation of θJC through the paddle. The assumption is that all heat flow will go through the paddle and none through the surrounding plastic.)

Recommended PCB Footprint

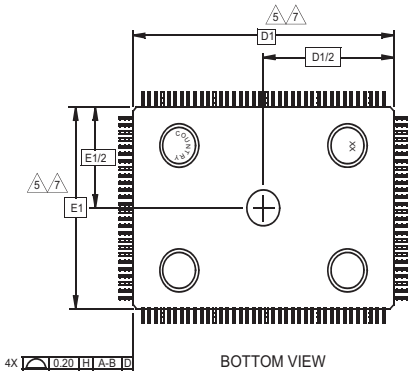


Package Information

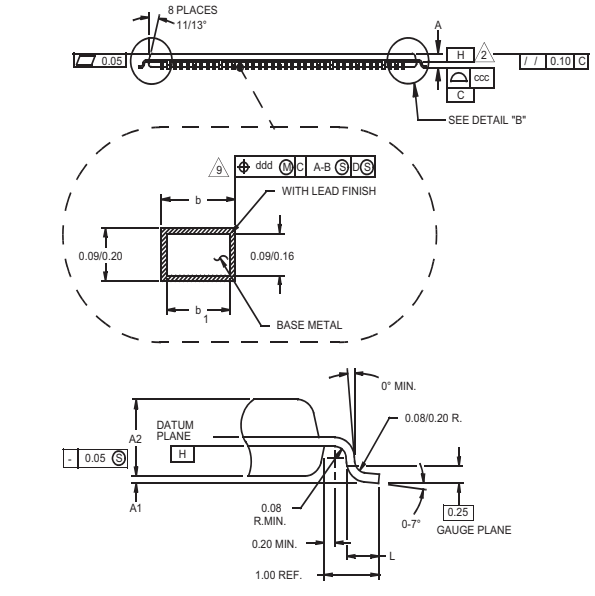
Thin Plastic Quad Flatpack Package with Top Exposed Pad (TEP-LQFP)



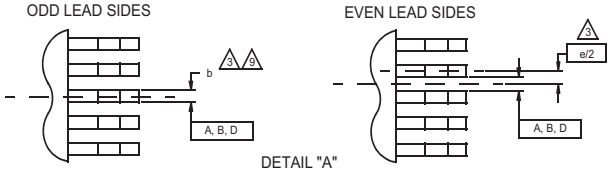
TOP VIEW



BOTTOM VIEW



DETAIL "B"



DETAIL "A"

Q128.14x20B

128 Lead Thin Quad Flatpack with Top Exposed Pad

SYMBOL	MILLIMETERS BHB MIN	NOM	MAX	NOTES
A	-	-	1.60	
A1	0.05	-	0.15	13
A2	1.35	1.40	1.45	
D		22 BSC		4
D1		20 BSC		7, 8
D2		12.20 BSC		14
E		16 BSC		4
E1		14 BSC		7, 8
E2		8.35 BSC		14
L	0.45	0.60	0.75	
N		128		
e		0.50 BSC		
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc			0.08	
ddd			0.08	

Rev. 0 3/09

NOTES:

1. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
2. Datum plane H located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and D to be determined at center lines between leads where leads exit plastic body at datum plane H.
4. To be determined at seating plane C.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.254mm per side on D1 and E1 dimensions.
6. “N” is the total number of terminals.
7. These dimensions to be determined at datum plane H.
8. Package top dimensions are smaller than package bottom dimensions and top of package will not overhang bottom of package.
9. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located at the lower radius or the foot.
10. Controlling dimension: millimeter.
11. Maximum allowable die thickness to be assembled in this package family is 0.38 millimeters.
12. This outline conforms to JEDEC publication 95 Registration MS-026, variations BHA & BHB.
13. A1 is defined as the distance from the seating plane to the lowest point of the package body.
14. Dimensions D2 and E2 represent the size of the exposed pad. The actual dimensions may be reduced up to 0.76mm due to mold flash.

Revision History

Revision Date	Description of Changes
September 30	• Page 15: Note 40 - change “test the internal references via Test & Cal Mux to “test the comparator outputs using a binary search. • Page 20: Notes 53 & 54 - change= R_EXT = 10V to R-EXT = 10kΩ • Page 32: Table 19 - change “Minimum slew rate for driver (slowest)” to “Maximum slew rate for driver (fastest)” • Page 33: Table 23 - IR0 - change .50kΩ to 50kΩ • Page 40: Split Load, second paragraph - change “split load is useful as a voltage clamp” to “split load is useful as a transient voltage clamp”
April 16, 2015	• Change part # from ISL55188 to ISL5188-AS • Page 16: Current Alarms - changed method to test current alarms. • Page 20: Table 7: VR0 & VR1 - change FV Tests Points from -0.5V/0µA to 0.0V/0µA; VR3, IR1 - change FV Tests points from 0.0V/-Imax to +0.5V/-Imax • Page 25: Coarse Delay - Spec #25120: change min/max from 1.6/2.8 to 1.5/3.0 - Spec #25130: change min/max from 7.5/12.5 to 6.0/16.0 • Page 25: Coarse Falling Edge Adjust - Spec #25230: change min/max from 5.0/7.2 to 4.0/10.0 - Spec #25240: change min/max from -3.3/-1.8 to -4.0/-1.0 - Spec #25250: change min/max from 1.6/3.0 to 0.5/4.0 - Spec #25270: change min/max from -800/+800 to -1000/+1000 • Page 62: Change part number from ISL55188CNEZ to ISL55188CNEZ-AS
April 1, 2015	• Reformat from Intersil to Elevate Semiconductor format • Page 1: Block diagram - flip comparator deskew

Revision Date 2014 / 09 / 08		Data sheet valid for Die revisions 10 and above.
Old Page #	**New Page #**	**Changes**
18	18	Update figure at bottom of page.

Revision Date 2014 / 05 / 21		Data sheet valid for Die revisions 10 and above.
Old Page #	**New Page #**	**Changes**
36	36	Power Supply Restrictions: Add power-down sequence; update diagram, add new paragraph to end of section.

Revision Date 2014 / 04 / 01		Data sheet valid for Die revisions 10 and above.
Old Page #	**New Page #**	**Changes**
16	16	Slew Rate Adjust Table: Update entire table.
16	16	Driver Bias Table; Update entire table.
34	35	Temperature Sensing: Update equation; add new paragraph at end of section.
35	36	Power Supply Restrictions: Update entire section.
48	49	Analog Pins, Test Environment – change: Tested at VCC and VEE to Tested at VCC and VEE + 0.25V
54	55	Current Alarms: Spec #s 14510 – 14550: Change all Min to -5; change all Max to +5
55	56	Measure Voltage Test Environment: Change Tested at MONITOR = VCC, VEE to Tested at MONITOR = VCC, VEE + 0.25V

Revision Date 2014 / 02 / 14		Data sheet valid for Die revisions 10 and above.
Old Page #	**New Page #**	**Changes**

16 36	16 36	Slew Rate Adjust Table: Update SR column values Add DAC Sample and Hold Section .

Revision Date 2014 / 01 / 14		**Data sheet valid for Die revisions 10 and above.**
Old Page #	**New Page #**	**Changes**
All	All	Change from “Preliminary” to “Production”.
9	9	Updated Package Diagram
57	57	Test Points Table: VR1, FV Test Points: Change -1V to -0.5V.

Revision Date 2013 / 10 / 07		**Data sheet valid for Die revisions 10 and above.**
Old Page #	**New Page #**	**Changes**
17	17	Bottom Diagram: Change I-Cl-Hi# to I-Al-Hi#
49	49	Update spec numbers; Add “Level” before DAC
50	50	Add Conditions to “Offset DAC Calibration”; Add “ED” to Test Environment
53	53	Add “Ical” to Spec # 10900
53	53	Update “Ical” description in Test Environment
55	55	Add “MI Common Mode” Table
57	57	Add Test Environment section
61	61	Load Table: Change “comparator” to “Load”

Ordering Information

PART NUMBER (NOTE 1)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)
ISL55188CNEZ-AS	ISL55188CNEZ	+25 to +100	128 Lead, 14x20mm TQFP w/top exposed heat slug

NOTE:

1. These Elevate Semiconductor Pb-free plastic packaged products employ special Pb-free material sets), molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Elevate Semiconductor Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.