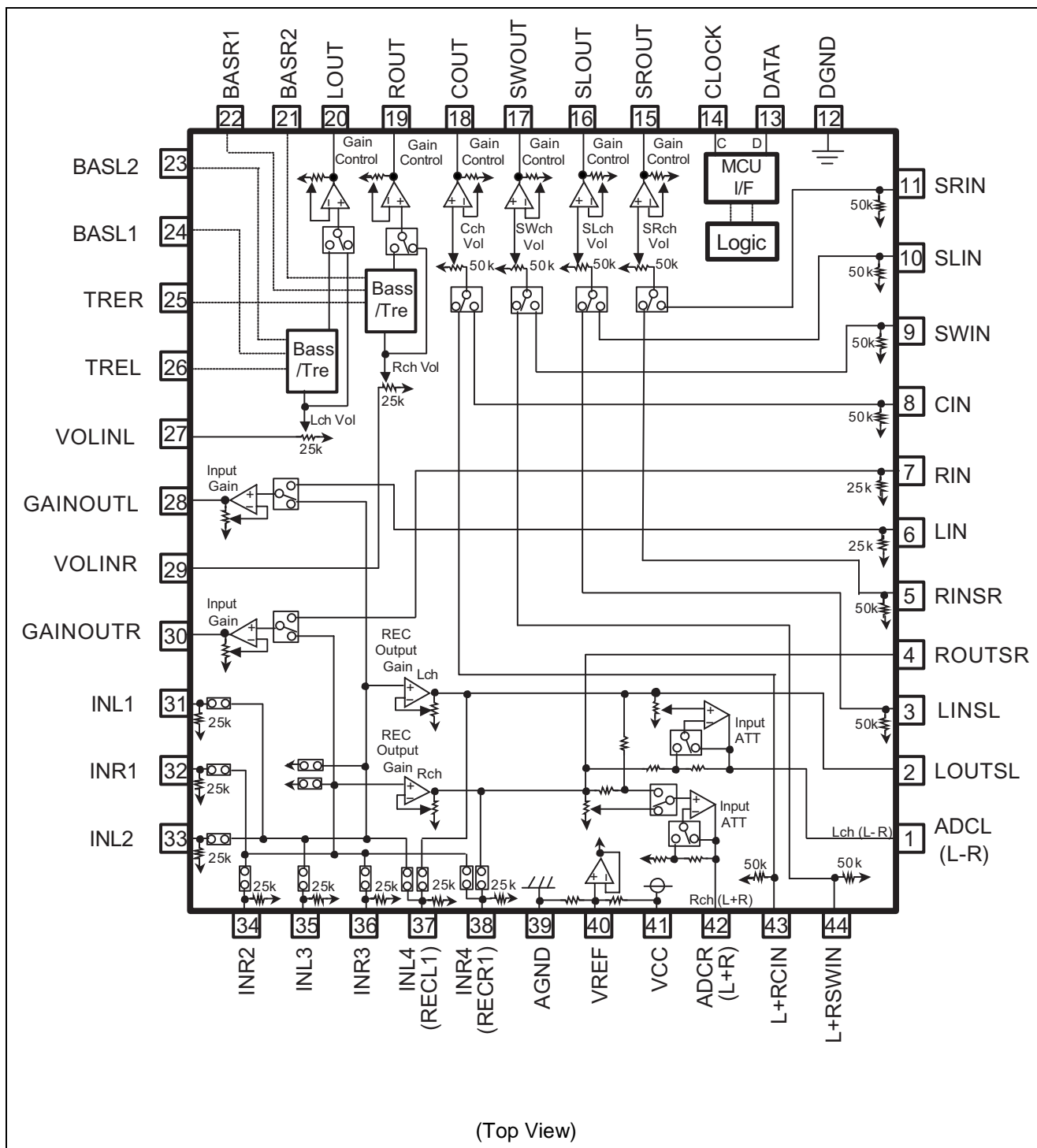


Block Diagram and Pin Configuration

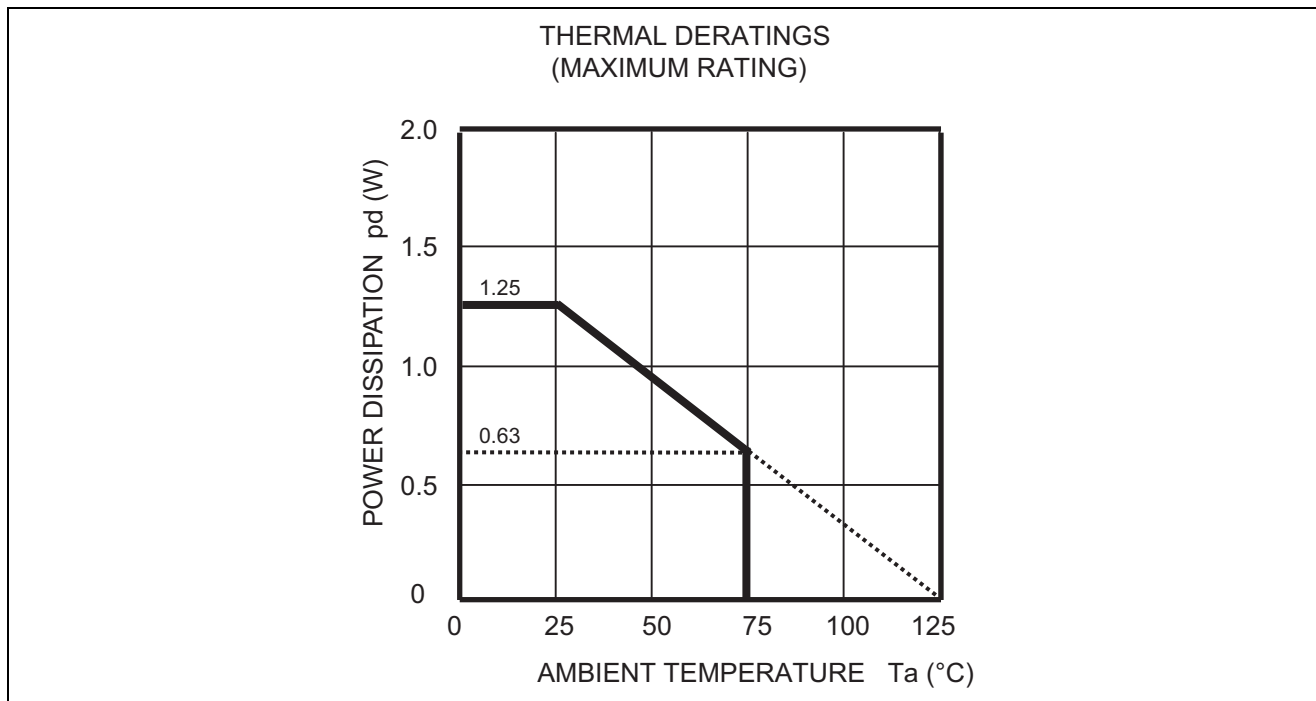


Pin Description

Pin No.	Name	Function
1	ADCL (L-R)	Output pin for ADC (and L-R output)
2	LOUTSL	L channel pre-output (REC output) for SL channel
3	LINSL	SL channel input from L channel pre-output (REC output)
4	ROUTSR	R channel pre-output (REC output) for SR channel
5	RINSR	SR channel input from R channel pre-output (REC output)
6, 7, 8, 9, 10, 11	LIN, RIN, CIN, SWIN, SLIN, SRIN	Input pin of L/R/C/SW/SL/SR channel (Multi)
12	DGND	Digital ground
13	DATA	Input pin of control data
14	CLOCK	Input pin of control clock
15, 16, 17, 18, 19, 20	SROUT, SLOUT, SWOUT, COUT, ROUT, LOUT	Output pin of SR/SL/SW/C/R/L channel
21, 22 23, 24	BASR1, BASR2, BASL1, BASL2	Frequency characteristic setting pin of R/L channel tone control (BASS)
25, 26	TRER, TREL	Frequency characteristic setting pin of R/L channel tone control (Treble)
27, 29	VOLINL, VOLINR	Input pin of L/R channel volume
28, 30	GAINOUTL, GAINOUTR	Output pin of L/R channel Input gain
31,33,35, 32,34,36	INL1, 2, 3, INR1, 2, 3	Input pin of L/R channel (Input selector)
37, 38	INL4/RECL1, INR4/RECR1	Input pin of L/R channel (Input selector) can use REC output pin
39	AGND	Analog ground
40	VREF	1/2 V _{CC} input
41	VCC	Power supply to internal analog circuit
42	ADCR(L+R)	Output pin for ADC(and L+R output)
43	L+RCIN	L+R input for C channel
44	L+RSWIN	L+R input for SW channel

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Condition
Power supply	Supply voltage	10.5	V	V_{CC}
Power dissipation	P_d	1.25	W	$T_a \leq 25^\circ\text{C}$
Thermal derating	K	12.5	mW/ $^\circ\text{C}$	$T_a > 25^\circ\text{C}$
Operating temperature	T_{opr}	-20 to +75	$^\circ\text{C}$	
Storage temperature	T_{stg}	-40 to +125	$^\circ\text{C}$	

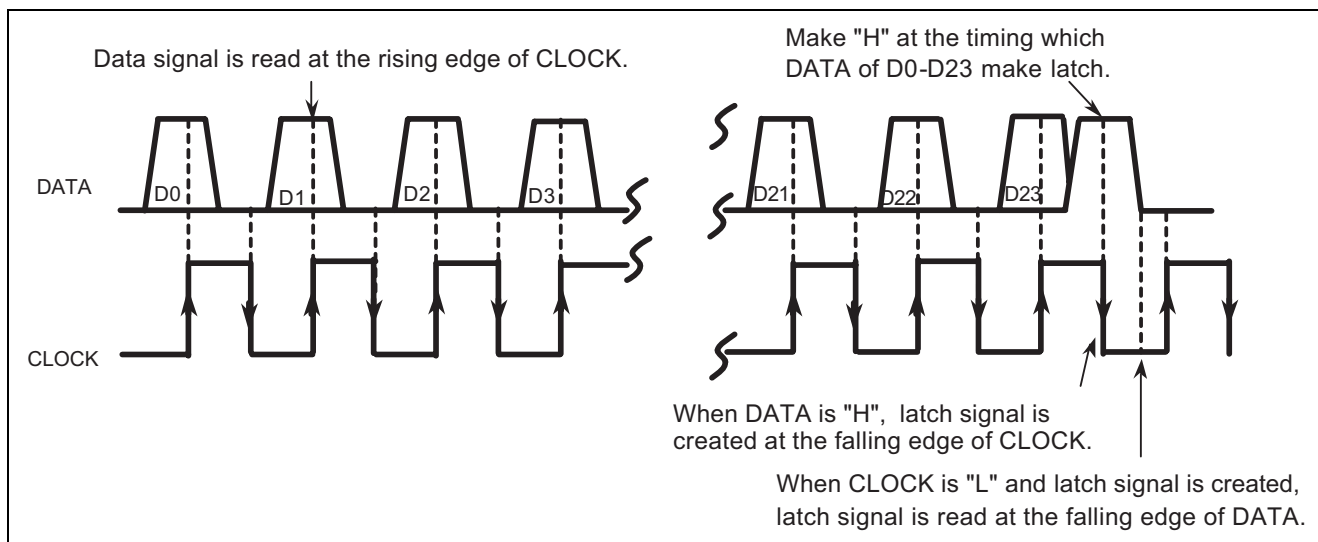


Recommended Operating Conditions

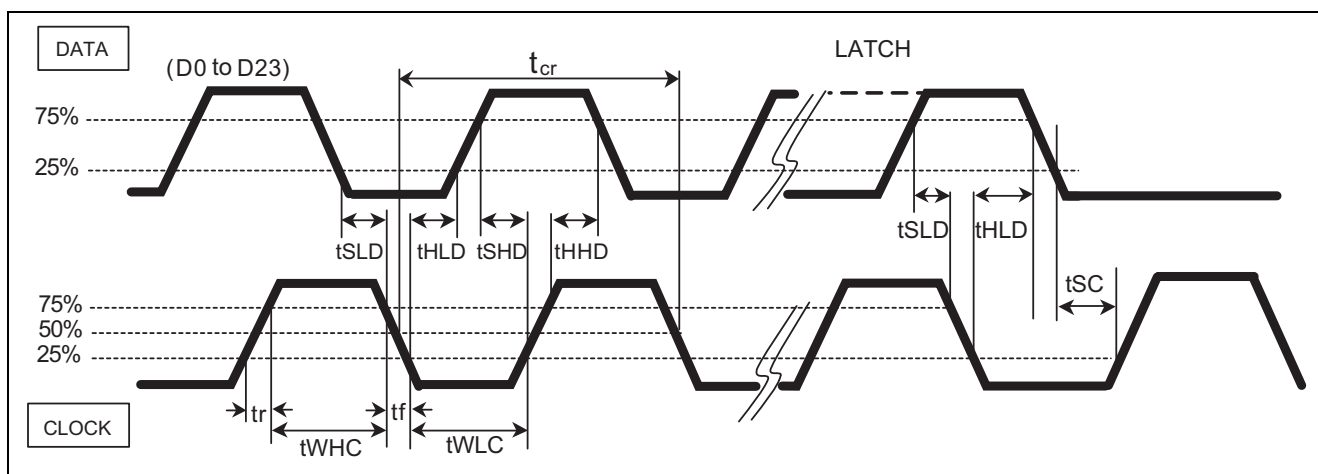
($T_a = 25^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply voltage	V_{CC}	8.0	9.0	10.0	V	
Logic "H" level input voltage	V_{IH}	2.7	—	5.5	V	$V_{CC} = 9\text{V}$
Logic "L" level input voltage	V_{IL}	0	—	0.7	V	$V_{CC} = 9\text{V}$

Relationship Between Data and Clock



Clock and Data Timings



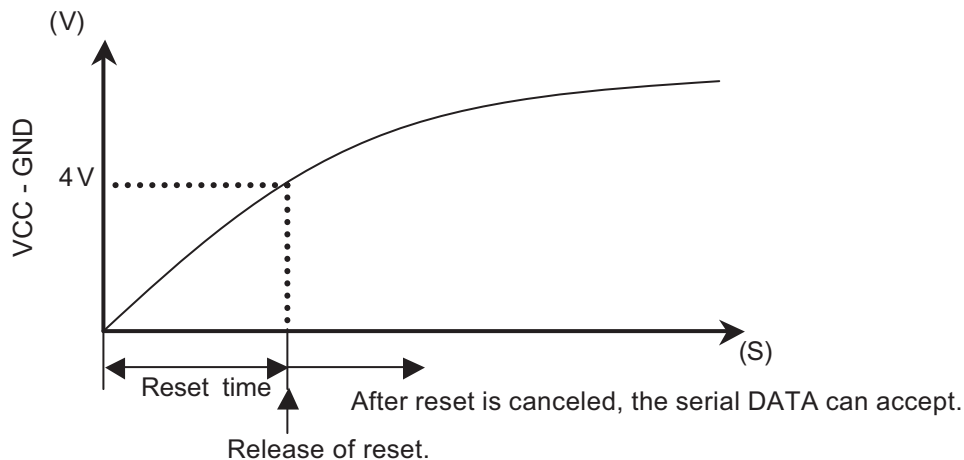
Timing Definition of Digital Block

Parameter	Symbol	Limits			Unit
		Min	Typ	Max	
CLOCK cycle time	t _{cr}	8	—	—	μs
CLOCK pulse width ("H" level)	t _{WHC}	3.2	—	—	
CLOCK pulse width ("L" level)	t _{WLC}	3.2	—	—	
Rising time of clock and data	t _r	—	—	0.8	
Falling time of clock and data	t _f	—	—	0.8	
DATA setup time (Rising time of clock)	t _{SHD}	1.6	—	—	
DATA setup time (Falling time of clock)	t _{SLD}	1.6	—	—	
DATA hold time ("H" level)	t _{HHD}	1.6	—	—	
DATA hold time ("L" level)	t _{HLD}	1.6	—	—	
CLOCK setup time	t _{SC}	1.6	—	—	

Power on Reset

This IC built-in the power on reset function.

The voltage of VCC-GND less than 4V, the serial DATA can not accept.



Data Control Specification

Initialize all data of the 4 formats when digital power supply (V_{CC}) turns on.

Prohibit using except specified data code as follows.

Slot1																							
D0a	D1a	D2a	D3a	D4a	D5a	D6a	D7a	D8a	D9a	D10a	D11a	D12a	D13a	D14a	D15a	D16a	D17a	D18a	D19a	D20a	D21a	D22	D23
(1)Input Selector			(2) REC Out	(3) REC- Output Gain Control	(4) ADC Input ATT		(5) L/R Input	(6) Bass/ Tone Control Bypass					(7) Treble				(8) SL/SR /C/SW Input	(9) Input Gain			0	0	0


Slot2																							
D0b	D1b	D2b	D3b	D4b	D5b	D6b	D7b	D8b	D9b	D10b	D11b	D12b	D13b	D14b	D15b	D16b	D17b	D18b	D19b	D20b	D21b	D22	D23
(10) Lch Gain Control			(11)Lch Volume						(10) RchGain Control			(11)Rch Volume						0	0	0	1		

Slot3																							
D0c	D1c	D2c	D3c	D4c	D5c	D6c	D7c	D8c	D9c	D10c	D11c	D12c	D13c	D14c	D15c	D16c	D17c	D18c	D19c	D20c	D21c	D22	D23
(10) CchGain Control			(11)Cch Volume						(10) SWch Gain Control			(11)SWch Volume						0	0	1	0		

Slot4																							
D0d	D1d	D2d	D3d	D4d	D5d	D6d	D7d	D8d	D9d	D10d	D11d	D12d	D13d	D14d	D15d	D16d	D17d	D18d	D19d	D20d	D21d	D22	D23
(10) SLchGain Control			(11)SLch Volume						(10) SRch Gain Control			(11)SRch Volume						0	0	1	1		

Note: No guarantee except for these codes.

Setting Code

 It's initial setting when power is turned on.

(1) Input Selector

Setting	D0a	D1a	D2a
ALL OFF	0	0	0
IN1	0	1	0
IN2	1	0	0
IN3	1	1	0
IN4*1	0	0	1

Note: No guarantee except for these codes.

(2) REC Output

REC output	REC1
Setting	D3a
OFF	0
ON	1*1

*1: When IN4 selected, REC1 can not use.

IN4	REC1	D0a	D1a	D2a	D3a
ON	OFF	0	0	1	1

(3) REC-Output Gain Control

Gain setting	D4a	D5a
0dB	0	0
+2dB	0	1
+4dB	1	0
+6dB	1	1

(4) ADC Input ATT


*2

ATT setting	D6a	D7a
0dB	0	0
-6dB	0	1
-12dB	1	0
-18dB	1	1

*2: When L \pm R selected, ADC input ATT can not use.

(5) L/R Input

Setting	D8a
Selector in	0
Multi in	1

 It's initial setting when power is turned on.

(6) Bass/Bypass (Tone control is bypass)

Gain setting	D9a	D10a	D11a	D12a
+14dB	1	1	1	1
+12dB	1	1	1	0
+10dB	1	1	0	1
+8dB	1	1	0	0
+6dB	1	0	1	1
+4dB	1	0	1	0
+2dB	1	0	0	1
0dB	1	0	0	0
-2dB	0	0	0	1
-4dB	0	0	1	0
-6dB	0	0	1	1
-8dB	0	1	0	0
-10dB	0	1	0	1
-12dB	0	1	1	0
-14dB	0	1	1	1
Bypass ^{*3}	0	0	0	0

^{*3}: Tone control is bypass.

(7) Treble

Gain setting	D13a	D14a	D15a	D16a
+14dB	1	1	1	1
+12dB	1	1	1	0
+10dB	1	1	0	1
+8dB	1	1	0	0
+6dB	1	0	1	1
+4dB	1	0	1	0
+2dB	1	0	0	1
0dB	1/0	0	0	0
-2dB	0	0	0	1
-4dB	0	0	1	0
-6dB	0	0	1	1
-8dB	0	1	0	0
-10dB	0	1	0	1
-12dB	0	1	1	0
-14dB	0	1	1	1

(8) SL/ SR/ C/ SW Input ^{*2}

Setting	D17a
L ± R in	0 ^{*2}
Multi in	1

^{*2}: When L ± R selected, ADC input ATT can not use.


(9) Input Gain

Gain setting	D18a	D19a	D20a
0dB	0	0	0
+2dB	0	0	1
+4dB	0	1	0
+6dB	0	1	1
+8dB	1	0	0
+10dB	1	0	1
+12dB	1	1	0
+14dB	1	1	1

(10) Gain Control

Gain setting	Lch	D0b	D1b	D2b
	Rch	D10b	D11b	D12b
	Cch	D0c	D1c	D2c
	SWch	D10c	D11c	D12c
	SLch	D0d	D1d	D2d
	SRch	D10d	D11d	D12d
0dB		0	0	0
+2dB		0	0	1
+4dB		0	1	0
+6dB		0	1	1
+8dB		1	0	0
+10dB		1	0	1
+12dB		1	1	0
+14dB		1	1	1

(11) 6channels Volume

 It's initial setting when power is turned on.

ATT	Lch	D3b	D4b	D5b	D6b	D7b	D8b	D9b
	Rch	D13b	D14b	D15b	D16b	D17b	D18b	D19b
	Cch	D3c	D4c	D5c	D6c	D7c	D8c	D9c
	SWch	D13c	D14c	D15c	D16c	D17c	D18c	D19c
	SLch	D3d	D4d	D5d	D6d	D7d	D8d	D9d
	SRch	D13d	D14d	D15d	D16d	D17d	D18d	D19d
0dB		0	0	0	0	0	0	0
-1dB		0	0	0	0	0	0	1
-2dB		0	0	0	0	0	1	0
-3dB		0	0	0	0	0	1	1
-4dB		0	0	0	0	1	0	0
-5dB		0	0	0	0	1	0	1
-6dB		0	0	0	0	1	1	0
-7dB		0	0	0	0	1	1	1
-8dB		0	0	0	1	0	0	0
-9dB		0	0	0	1	0	0	1
-10dB		0	0	0	1	0	1	0
-11dB		0	0	0	1	0	1	1
-12dB		0	0	0	1	1	0	0
-13dB		0	0	0	1	1	0	1
-14dB		0	0	0	1	1	1	0
-15dB		0	0	0	1	1	1	1
-16dB		0	0	1	0	0	0	0
-17dB		0	0	1	0	0	0	1
-18dB		0	0	1	0	0	1	0
-19dB		0	0	1	0	0	1	1
-20dB		0	0	1	0	1	0	0
-21dB		0	0	1	0	1	0	1
-22dB		0	0	1	0	1	1	0
-23dB		0	0	1	0	1	1	1
-24dB		0	0	1	1	0	0	0
-25dB		0	0	1	1	0	0	1
-26dB		0	0	1	1	0	1	0
-27dB		0	0	1	1	0	1	1
-28dB		0	0	1	1	1	0	0
-29dB		0	0	1	1	1	0	1
-30dB		0	0	1	1	1	1	0
-31dB		0	0	1	1	1	1	1
-32dB		0	1	0	0	0	0	0
-33dB		0	1	0	0	0	0	1
-34dB		0	1	0	0	0	1	0
-35dB		0	1	0	0	0	1	1
-36dB		0	1	0	0	1	0	0
-37dB		0	1	0	0	1	0	1
-38dB		0	1	0	0	1	1	0
-39dB		0	1	0	0	1	1	1
-40dB		0	1	0	1	0	0	0
-41dB		0	1	0	1	0	0	1
-42dB		0	1	0	1	0	1	0
-43dB		0	1	0	1	0	1	1

ATT	Lch	D3b	D4b	D5b	D6b	D7b	D8b	D9b
	Rch	D13b	D14b	D15b	D16b	D17b	D18b	D19b
	Cch	D3c	D4c	D5c	D6c	D7c	D8c	D9c
	SWch	D13c	D14c	D15c	D16c	D17c	D18c	D19c
	SLch	D3d	D4d	D5d	D6d	D7d	D8d	D9d
	SRch	D13d	D14d	D15d	D16d	D17d	D18d	D19d
-44dB	0	1	0	1	1	0	0	
-45dB	0	1	0	1	1	0	1	
-46dB	0	1	0	1	1	1	0	
-47dB	0	1	0	1	1	1	1	
-48dB	0	1	1	0	0	0	0	
-49dB	0	1	1	0	0	0	1	
-50dB	0	1	1	0	0	1	0	
-51dB	0	1	1	0	0	1	1	
-52dB	0	1	1	0	1	0	0	
-53dB	0	1	1	0	1	0	1	
-54dB	0	1	1	0	1	1	0	
-55dB	0	1	1	0	1	1	1	
-56dB	0	1	1	1	0	0	0	
-57dB	0	1	1	1	0	0	1	
-58dB	0	1	1	1	0	1	0	
-59dB	0	1	1	1	0	1	1	
-60dB	0	1	1	1	1	0	0	
-61dB	0	1	1	1	1	0	1	
-62dB	0	1	1	1	1	1	0	
-63dB	0	1	1	1	1	1	1	
-64dB	1	0	0	0	0	0	0	
-65dB	1	0	0	0	0	0	1	
-66dB	1	0	0	0	0	1	0	
-67dB	1	0	0	0	0	1	1	
-68dB	1	0	0	0	1	0	0	
-69dB	1	0	0	0	1	0	1	
-70dB	1	0	0	0	1	1	0	
-71dB	1	0	0	0	1	1	1	
-72dB	1	0	0	1	0	0	0	
-73dB	1	0	0	1	0	0	1	
-74dB	1	0	0	1	0	1	0	
-75dB	1	0	0	1	0	1	1	
-76dB	1	0	0	1	1	0	0	
-77dB	1	0	0	1	1	0	1	
-78dB	1	0	0	1	1	1	0	
-79dB	1	0	0	1	1	1	1	
-80dB	1	0	1	0	0	0	0	
-81dB	1	0	1	0	0	0	1	
-82dB	1	0	1	0	0	1	0	
-83dB	1	0	1	0	0	1	1	
-84dB	1	0	1	0	1	0	0	
-85dB	1	0	1	0	1	0	1	
-86dB	1	0	1	0	1	1	0	
-87dB	1	0	1	0	1	1	1	
-88dB	1	0	1	1	0	0	0	
-89dB	1	0	1	1	0	0	1	
-90dB	1	0	1	1	1	0	0	

ATT	Lch	D3b	D4b	D5b	D6b	D7b	D8b	D9b
	Rch	D13b	D14b	D15b	D16b	D17b	D18b	D19b
	Cch	D3c	D4c	D5c	D6c	D7c	D8c	D9c
	SWch	D13c	D14c	D15c	D16c	D17c	D18c	D19c
	SLch	D3d	D4d	D5d	D6d	D7d	D8d	D9d
	SRch	D13d	D14d	D15d	D16d	D17d	D18d	D19d
-91dB		1	0	1	1	0	1	1
-92dB		1	0	1	1	1	0	0
-93dB		1	0	1	1	1	0	1
-94dB		1	0	1	1	1	1	0
-95dB		1	0	1	1	1	1	1
-96dB		1	1	0	0	0	0	0
-97dB		1	1	0	0	0	0	1
-98dB		1	1	0	0	0	1	0
-99dB		1	1	0	0	0	1	1
-∞dB		1	1	1/0	1/0	1	1/0	1/0

Note: No guarantee except for these codes.

Electrical Characteristics

Unless otherwise noted, $T_a = 25^\circ\text{C}$, $V_{CC} = 9\text{V}$, $f = 1\text{kHz}$, Volume = 0dB, Input selector = IN1, Input gain = 0db, Gain control = 0dB, ADC input ATT = 0dB, Tone = Bypass, L/R input = Selector in, SL/SR/C/SW input = L±R in

(1) Power supply characteristics

Parameter	Symbol	Limits			Unit	Test condition
		Min	Typ	Max		
Analog power supply circuit current	I_{CC}	—	35	55	mA	With $V_{CC} = 9\text{V}$ V_{CC} current, when no signal is provided

(2) Input/Output characteristics (OVER ALL)

Parameter	Symbol	Limits			Unit	Test condition	
		Min	Typ	Max			
Input resistance	Rin	17	25	33	k Ω	6 to 11, 31 to 36 pin	
Maximum output voltage	VOM	1.8	2.2	—	Vrms	6 to 11pin input, 15 to 20pin output, THD = 1%, RL = 10k Ω , Output gain control = +6dB	
Pass gain	Gv	-2.0	0	2.0	dB	6 to 11pin input, 15 to 20pin output, Vi = 0.3Vrms, FLAT	
Total harmonic distortion	THD	—	0.005	0.02	%	6 to 11pin input, 15 to 20pin output, BW: 400Hz to 30kHz, f = 1kHz, Vo = 0.5Vrms, RL = 10k Ω	
Balance of mutual channels	CBAL	-0.5	0	0.5	dB	31,32pin input, 19,20pin output, Vi = 0.3Vrms	
Output noise voltage	Vono1	—	2	6	μ Vrms	JIS-A, Rg = 0 Ω , 19,20pin output, Volume = - ∞ dB setting	Output gain control = 0dB
		—	9	18			Output gain control = +14dB
	Vono2	—	2	6		JIS-A, Rg = 0 Ω , 19,20pin output, Volume = 0dB setting	Output gain control = 0dB
		—	9	18			Output gain control = +14dB
	Vono3	—	2	6		JIS-A, Rg = 0 Ω , 15 to 18pin output, Volume = 0dB setting	Output gain control = 0dB
		—	9	18			Output gain control = +14dB
Selector separation	SS1	—	-90	-70	dB	< Input selector > Vo = 1Vrms, Rg = 0 Ω , RL = 10k Ω , JIS-A	
	SS2	—	-90	-70		< Multi input selector > Vo = 1Vrms, Rg = 0 Ω , RL = 10k Ω , JIS-A	
Channel separation	CS	—	-90	-70		Vo = 1Vrms, Rg = 0 Ω , RL = 10k Ω , JIS-A	

(3) 6 channel Volume characteristics

Parameter	Symbol	Limits			Unit	Test condition
		Min	Typ	Max		
Maximum attenuation	ATTmax	—	-105	-95	dB	Vi = 2Vrms, JIS-A, VOL = - ∞ dB
Volume gain gang error of mutual channels	Dvol	-0.5	0	+0.5	dB	Volume = 0dB

(4) Tone control characteristics

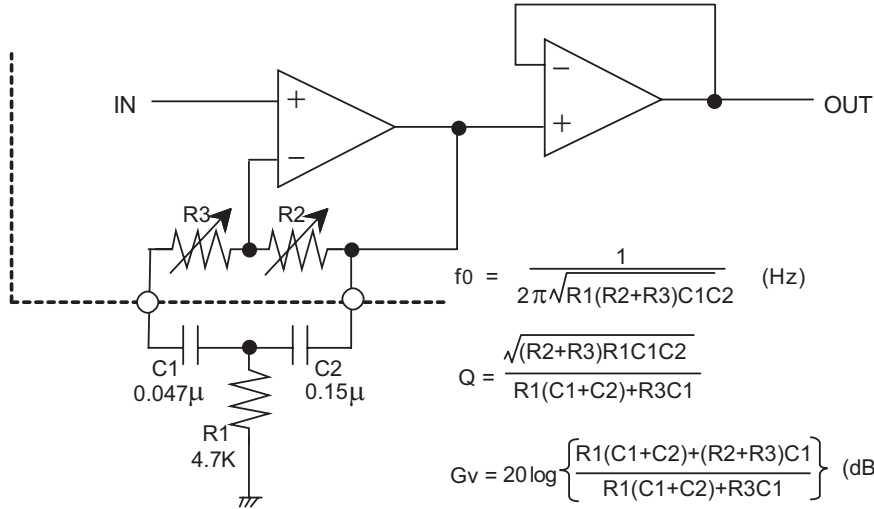
Unless otherwise noted, Tone ON/OFF = ON

Parameter	Symbol	Limits			Unit	Test condition
		Min	Typ	Max		
Tone control voltage gain (Boost/Bass)	G (BASS) B	+11	+14	+17	dB	f = 100Hz Bass +14dB setting
Tone control voltage gain (Cut/Bass)	G (BASS) C	-17	-14	-11	dB	f = 100Hz Bass -14dB setting
Tone control voltage gain (Boost/Treble)	G (TRE) B	+11	+14	+17	dB	f = 10kHz Treble +14dB setting
Tone control voltage gain (Cut/Treble)	G (TRE) C	-17	-14	-11	dB	f = 10kHz Treble -10dB setting
Balance of mutual channels	BALT	-2	0	+2	dB	Bass setting +14, -14dB Treble setting +14, -14dB

Tone Control

(1) Bass

< Boost >

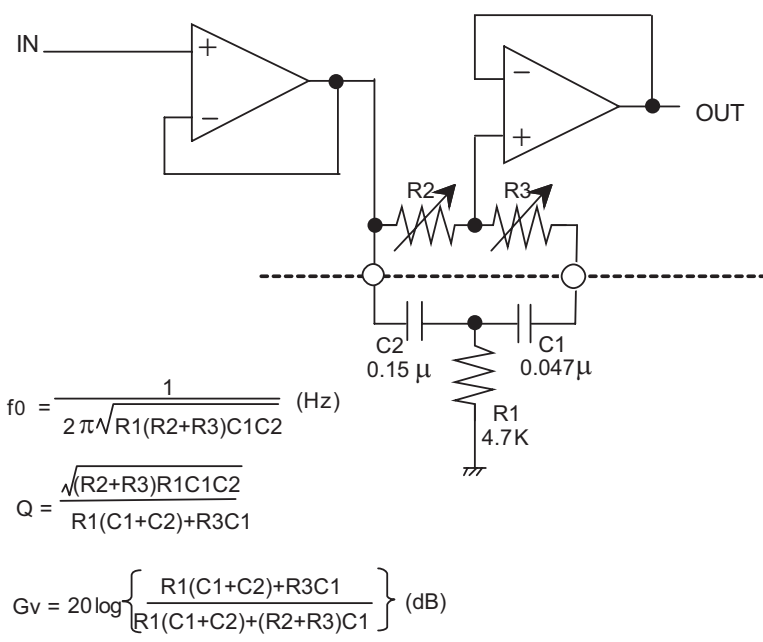


[Designed Parameter]

R1=4.7kΩ, C1=0.047μF, C2=0.15μF

Gain Setting	Designed Parameter	
	R3(kΩ)	R2(kΩ)
+14dB	0.19	79.81
+12dB	5.21	74.66
+10dB	11.83	68.17
+8dB	19.99	60.01
+6dB	30.27	49.73
+4dB	43.21	36.79
+2dB	59.49	20.51

< Cut >

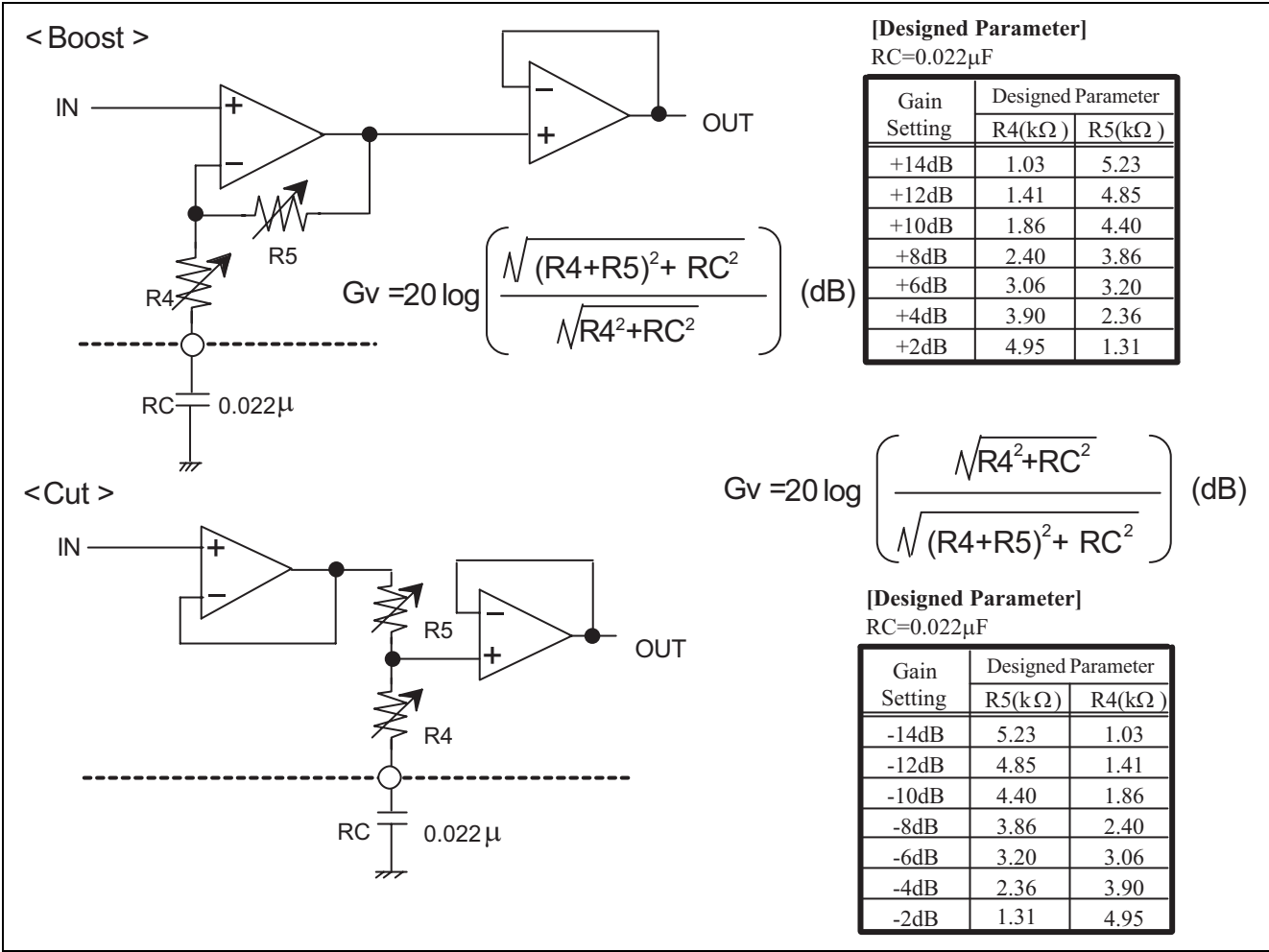


[Designed Parameter]

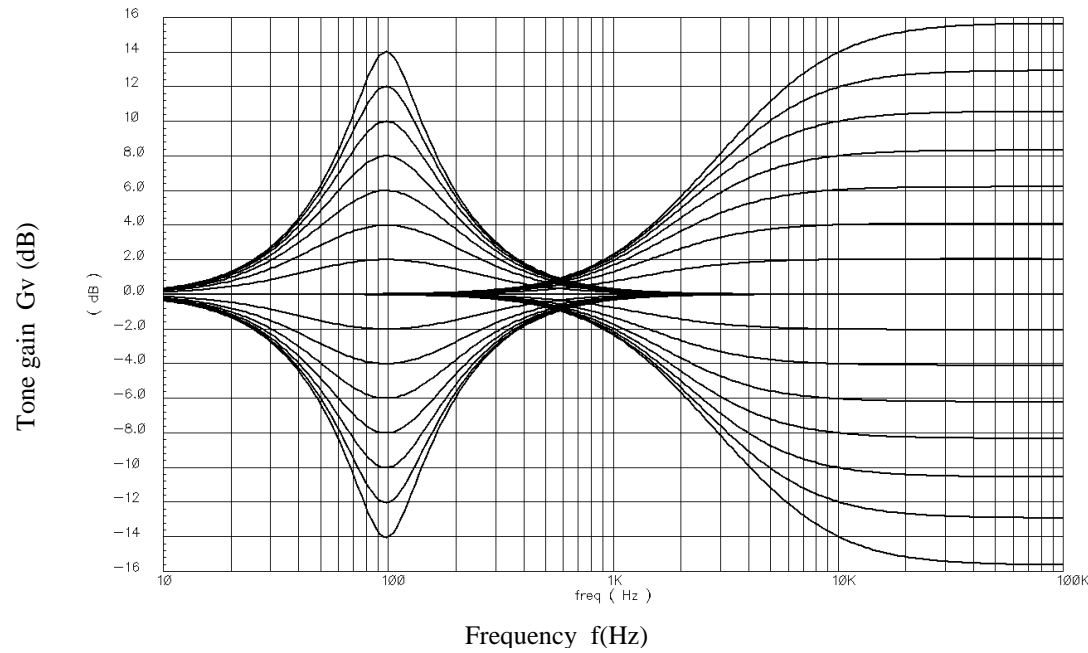
R1=4.7kΩ, C1=0.047μF, C2=0.15μF

Gain Setting	Designed Parameter	
	R2(kΩ)	R3(kΩ)
-14dB	79.81	0.19
-12dB	74.66	5.21
-10dB	68.17	11.83
-8dB	60.01	19.99
-6dB	49.73	30.27
-4dB	36.79	43.21
-2dB	20.51	59.49

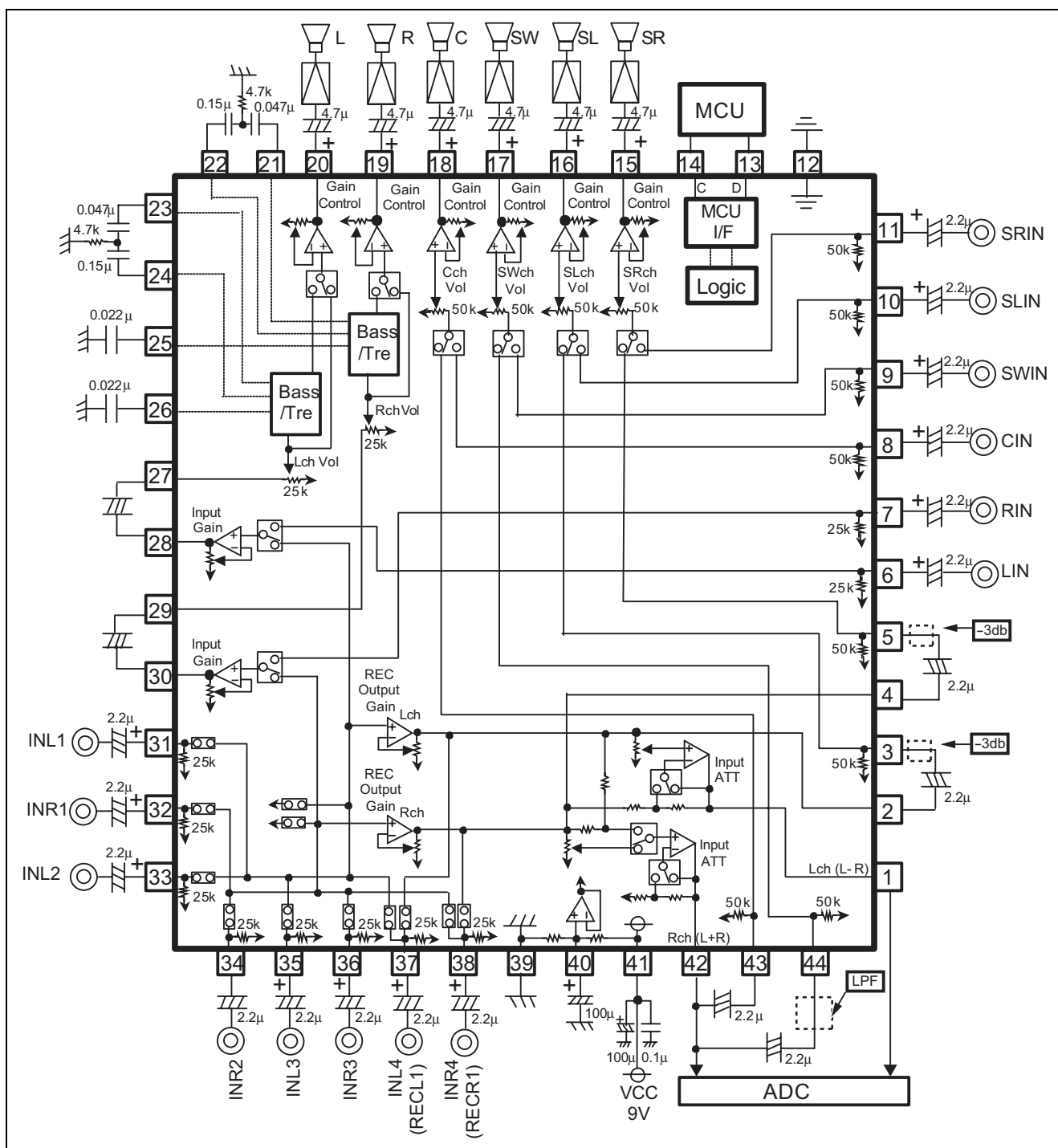
(2) Treble



Curve of characteristics



Application Example



Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
 2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
 3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
 4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
 5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
 6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
 7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
 8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.
-



RENESAS SALES OFFICES

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.

Unit 205, AZIA Center, No.133 Yincheng Rd (n), Pudong District, Shanghai 200120, China
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510