# TDA7442
TDA7442D

TONE CONTROL AND SURROUND
DIGITALLY CONTROLLED AUDIO PROCESSOR

- 4 STEREO INPUTS
- INPUT ATTENUATION CONTROL IN 0.5dB STEP
- TREBLE AND BASS CONTROL
- TWO SURROUND MODE AVAILABLE WITH 4 SELECTABLE RESPONSES:
  - MUSIC
  - SIMULATED STEREO
- TWO SPEAKER ATTENUATORS:
  - 2 INDEPENDENT SPEAKER CONTROLS IN 1dB STEPS FOR BALANCE FACILITY
  - INDEPENDENT MUTE FUNCTION
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL BUS
- 2 MONITOR OUTPUT (ONLY FOR TDA7442)

DESCRIPTION

The TDA7442/42D is volume tone (bass and treble) balance (Left/Right) processors for quality audio applications in TV and Hi-Fi systems.
It reproduces surround sound by using a pro-

SO28   **SDIP32**

ORDERING NUMBER: TDA7442D (SO28)
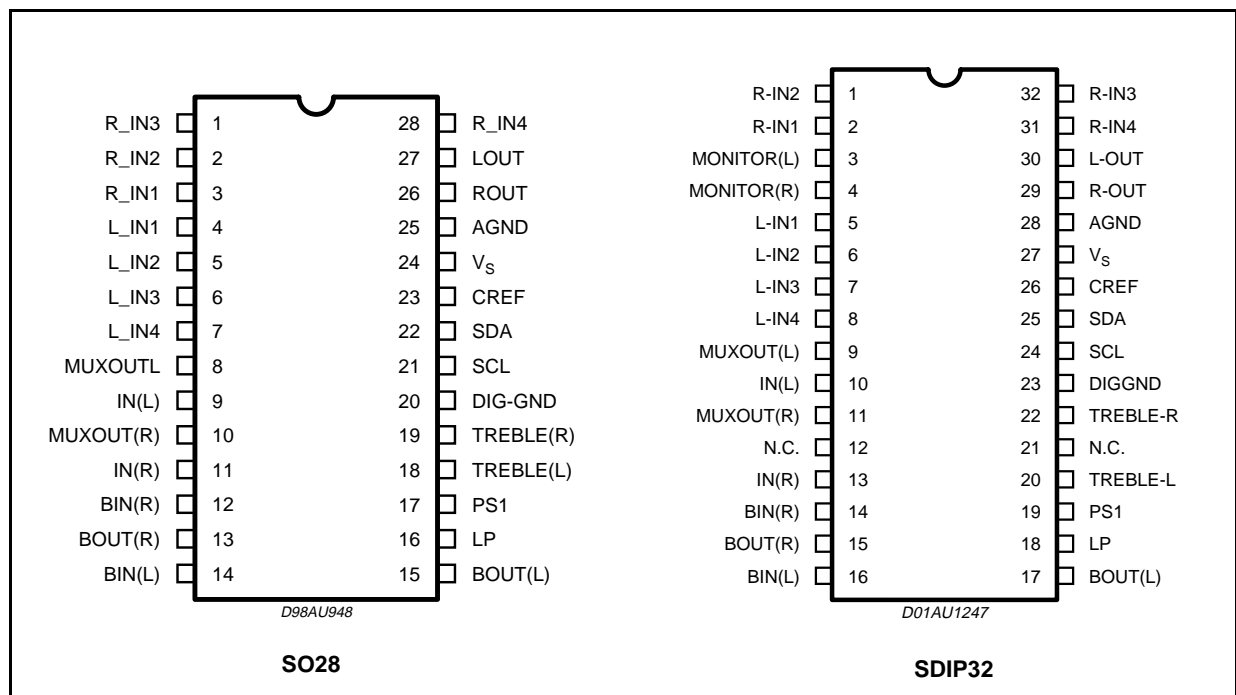TDA7442 (SDIP32)
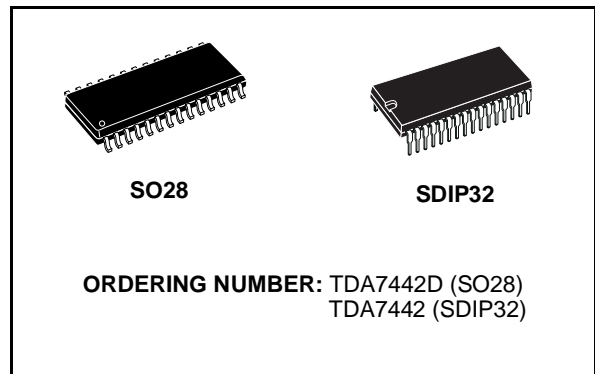
grammable phase shifter. Control of all the functions is accomplished by serial bus.
The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.
Thanks to the BIPOLAR/CMOS Technology used, Low Distortion, Low Noise and DC stepping are obtained.

PIN CONNECTIONS

R_IN3	1		28	R_IN4
R_IN2	2		27	LOUT
R_IN1	3		26	ROUT
L_IN1	4		25	AGND
L_IN2	5		24	V_S
L_IN3	6		23	CREF
L_IN4	7		22	SDA
MUXOUTL	8		21	SCL
IN(L)	9		20	DIG-GND
MUXOUT(R)	10		19	TREBLE(R)
IN(R)	11		18	TREBLE(L)
BIN(R)	12		17	PS1
BOUT(R)	13		16	LP
BIN(L)	14		15	BOUT(L)

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SO28

R-IN2	1		32	R-IN3
R-IN1	2		31	R-IN4
MONITOR(L)	3		30	L-OUT
MONITOR(R)	4		29	R-OUT
L-IN1	5		28	AGND
L-IN2	6		27	V_S
L-IN3	7		26	CREF
L-IN4	8		25	SDA
MUXOUT(L)	9		24	SCL
IN(L)	10		23	DIGGND
MUXOUT(R)	11		22	TREBLE-R
N.C.	12		21	N.C.
IN(R)	13		20	TREBLE-L
BIN(R)	14		19	PS1
BOUT(R)	15		18	LP
BIN(L)	16		17	BOUT(L)

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SDIP32

BLOCK DIAGRAM (TDA7442)

BLOCK DIAGRAM (TDA7442D)

QUICK REFERENCE DATA

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	7	9	10.2	V
V_{CL}	Max. input signal handling	2			Vrms
THD	Total Harmonic Distortion V = 1Vrms f = 1KHz		0.01	0.1	%
S/N	Signal to Noise Ratio V out = 1Vrms (mode = OFF)		106		dB
S_C	Channel Separation f = 1KHz		90		dB
	Treble Control (2db step)	-14		+14	dB
	Bass Control (2dB step)	-14		+14	dB
	Balance Control 1dB step (LCH, RCH)	-79		0	dB
	Mute Attenuation		100		dB

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max.	85	°C/W

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	11	V
T_{amb}	Operating Ambient Temperature	-10 to 85	°C
T_{stg}	Storage Temperature Range	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (refer to the test circuit T_{amb} = 25°C, V_S = 9V, R_L = 10KΩ, V_{in} = 1Vrms; R_G = 600Ω, all controls flat (G = 0dB), Effect Ctrl = -6dB, MODE = OFF; f = 1KHz unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		7	9	10.2	V
I_S	Supply Current		10	18	26	mA
SVR	Ripple Rejection	L_{CH} / $R_{CH out}$, Mode = OFF	60	80		dB
INPUT STAGE						
R_{IN}	Input Resistance		35	50	65	KΩ
V_{CL}	Clipping Level	THD = 0.3%	2	2.5		Vrms
C_{RANGE}	Control Range			31.5		dB
A_{VMIN}	Min. Attenuation		-1	0	1	dB
A_{VMAX}	Max. Attenuation		31	31.5	32	dB
A_{STEP}	Step Resolution			0.5	1	dB
BASS CONTROL						
Gb	Control Range	Max. Boost/cut	±11.5	±14.0	±16.0	dB
B_{STEP}	Step Resolution		1	2	3	dB
R_B	Internal Feedback Resistance		32	44	56	KΩ
TREBLE CONTROL						
Gt	Control Range	Max. Boost/cut	±13.0	±14.0	±15.0	dB
T_{STEP}	Step Resolution		1	2	3	dB
EFFECT CONTROL						
C_{RANGE}	Control Range		- 21		- 6	dB
S_{STEP}	Step Resolution		0.5	1	1.5	dB
SURROUND SOUND MATRIX PHASE						
R_{PS10}	Phase Shifter 1: D1 = 0, D0 = 0		8.3	11.8	15.2	KΩ
R_{PS11}	Phase Shifter 1: D1 = 0, D0 = 1		10	14.1	18.3	KΩ
R_{PS12}	Phase Shifter 1: D1 = 1, D0 = 0		12.6	17.9	23.3	KΩ
R_{PS13}	Phase Shifter 1: D1 = 1, D0 = 1		26.4	37.3	48.85	KΩ

SURROUND SOUND MATRIX

TEST CONDITION (Phase Resistor Selection D0=0, D1=1, D2=0. D3=1, D4=0, D5=1, D6=0, D7=1

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{OFF}	In-phase Gain (OFF)	Mode OFF, Input signal of 1kHz, 1.4 V_{p-p}, $R_{in} \rightarrow R_{out}$ $L_{in} \rightarrow L_{out}$	-1	0	1	dB
D_{GOFF}	LR In-phase Gain Difference (OFF)	Mode OFF, Input signal of 1kHz, 1.4 V_{p-p} $R_{in} \rightarrow R_{out}$, $L_{in} \rightarrow L_{out}$	-1	0	1	dB
G_{MUS}	In-phase Gain (Music)	Music mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V_{p-p} ($R_{in} \rightarrow R_{out}$), ($L_{in} \rightarrow L_{out}$)		7		dB
D_{GMUS}	LR In-phase Gain Difference (Music)	Music mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V_{p-p} ($R_{in} \rightarrow R_{out}$) - ($L_{in} \rightarrow L_{out}$)		0		dB

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SPEAKER ATTENUATORS						
C_{range}	Control Range			79		dB
S_{STEP}	Step Resolution		-0.5	1	1.5	dB
E_A	Attenuation set error	Av = 0 to -20dB	-1.5	0	1.5	dB
		Av = -20 to -79dB	-3	0	2	dB
V_{DC}	DC Steps	adjacent att. steps	-3	0	3	mV
A_{MUTE}	Output Mute Condition		+70	100		dB
R_{VEA}	Input Impedance		21	30	39	KΩ
AUDIO OUTPUTS						
$N_{O(OFF)}$	Output Noise (OFF)	Output Mute, Flat B_W = 20Hz to 20KHz		4 5		µVrms µVrms
$N_{O(MUS)}$	Output Noise (Music)	Mode = Music , B_W = 20Hz to 20KHz,		30		mVrms
$N_{O(PSEUDO)}$	Output Noise (Pseudo Stereo)	Mode = Pseudo Stereo B_W = 20Hz to 20KHz,		30		mVrms
d	Distorsion	Av = 0 ; V_{in} = 1Vrms		0.01	0.1	%
S_C	Channel Separation		70	90		dB
V_{OCL}	Clipping Level	d = 0.3%	2	2.5		Vrms
R_{OUT}	Output Resistance		10	30	50	Ω
V_{OUT}	DC Voltage Level			3.8		V
MONITOR OUTPUTS						
d	Distorsion	Av = 0 ; V_{in} = 1Vrms		0.01	0.1	%
S_C	Channel Separation		70	90		dB
V_{OCL}	Clipping Level	d = 0.3%	2	2.5		Vrms
R_{OUT}	Output Resistance		20	50	70	Ω
V_{OUT}	DC Voltage Level			4.5		V
BUS INPUTS						
V_{IL}	Input Low Voltage				1	V
V_{IH}	Input High Voltage		3			V
I_{IN}	Input Current		-5		+5	µA
V_O	Output Voltage SDA Acknowledge	I_O = 1.6mA			0.4	V

I²C BUS INTERFACE

Data transmission from microprocessor to the TDA7442D and viceversa takes place through the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

Data Validity

As shown in fig. 3, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Start and Stop Conditions

As shown in fig.4 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

Byte Format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an ac-knowledge bit. The MSB is transferred first.

Acknowledge

The master (μP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 5). The peripheral (audioprocessor) that ac-knowledges has to pull-down (LOW) the SDA line during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledge after the recep-tion of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can gen-erate the STOP information in order to abort the transfer.

Transmission without Acknowledge

Avoiding to detect the acknowledge of the audio-processor, the μP can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking.

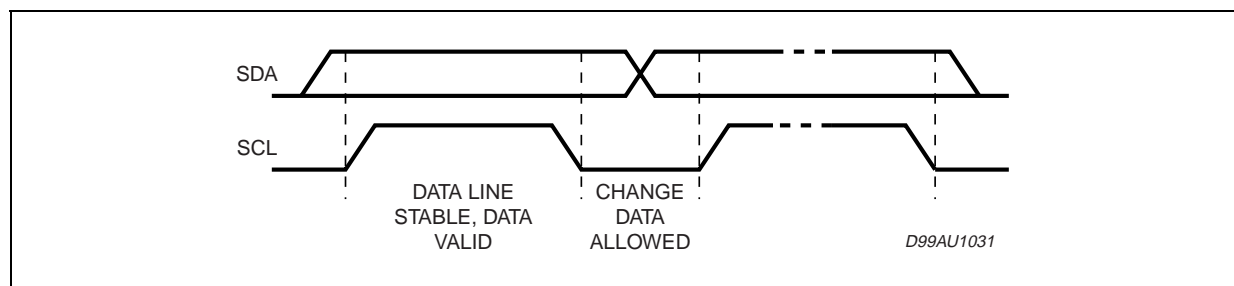**Figure 3:** Data Validity on the I²CBUS
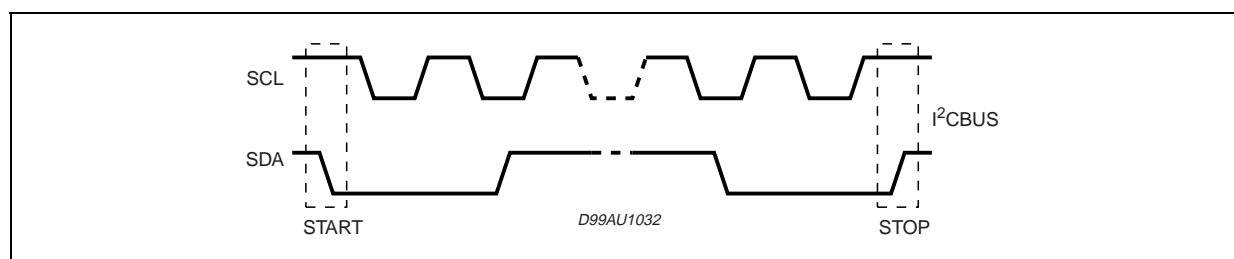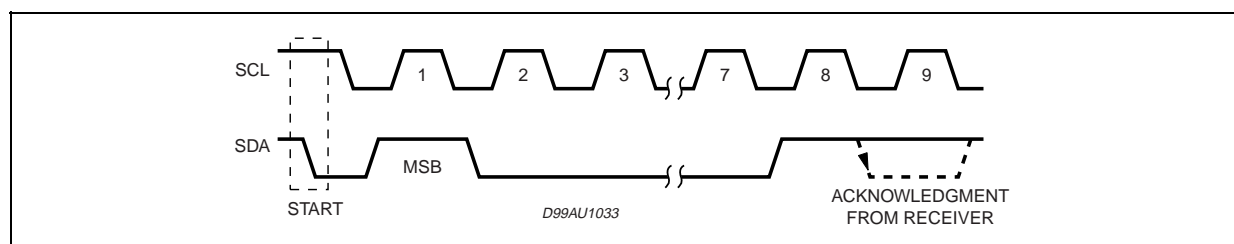

Figure 4: Timing Diagram of I²CBUS

F**igure 5:** Acknowledge on the I²CBUS
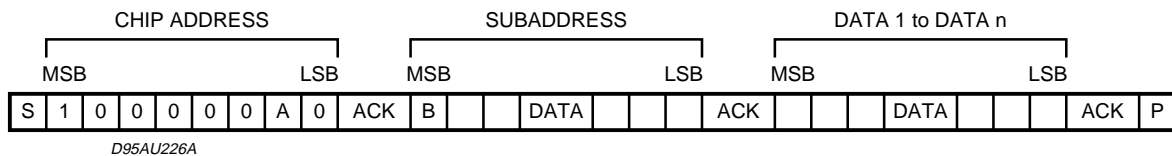
SOFTWARE SPECIFICATION

Interface Protocol

The interface protocol comprises:
- A start condition (S)
- A chip address byte, containing the TDA7442D address
- A subaddress bytes
- A sequence of data (N byte + achnowledge)
- A stop condition (P)

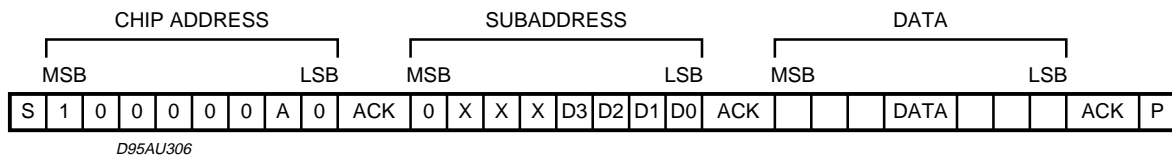|	CHIP ADDRESS									SUBADDRESS						DATA 1 to DATA n						
	MSB						LSB			MSB			LSB			MSB			LSB			
S	1	0	0	0	0	0	A	0	ACK	B		DATA			ACK			DATA			ACK	P

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ACK = Achnowledge
S = Start
P = Stop
A = Address
B = Auto Increment

EXAMPLES

No Incremental Bus
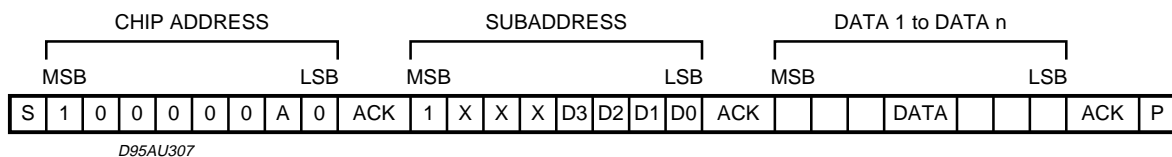
The TDA7442D receives a start condition, the correct chip address, a subaddress with the MSB = 0 (no incremental bus), N-datas (all these datas concern the subaddress selected), a stop condition.

	CHIP ADDRESS									SUBADDRESS									DATA						
	MSB						LSB			MSB							LSB		MSB				LSB		
S	1	0	0	0	0	0	A	0	ACK	0	X	X	X	D3	D2	D1	D0	ACK			DATA			ACK	P

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Incremental Bus

The TDA7442D receive s a start condition, the correct chip address, a subaddress with the MSB = 1 (incremental bus): now it is in a loop condition with an autoincrease of the subaddress whereas SUBADDRESS from "1XXX1010" to "1XXX1111" of DATA are ignored.

The DATA 1 concern thesubaddress sent, and the DATA 2 concern the subaddress sent plus one in the loop etc, and at the end it receivers the stop condition.

	CHIP ADDRESS									SUBADDRESS									DATA 1 to DATA n						
	MSB						LSB			MSB							LSB		MSB				LSB		
S	1	0	0	0	0	0	A	0	ACK	1	X	X	X	D3	D2	D1	D0	ACK			DATA			ACK	P

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DATA BYTES

Address = 80(HEX)

FUNCTION SELECTION:

The first byte (subaddress)

MSB							LSB	SUBADDRESS
D7	D6	D5	D4	D3	D2	D1	D0	
B	X	X	X	0	0	0	0	INPUT ATTENUATION
B	X	X	X	0	0	0	1	SURROUND & OUT & EFFECT CONTROL
B	X	X	X	0	0	1	0	PHASE RESISTOR
B	X	X	X	0	0	1	1	BASS
B	X	X	X	0	1	0	0	TREBLE
B	X	X	X	0	1	0	1	SPEAKER ATTENUATION "L"
B	X	X	X	0	1	1	0	SPEAKER ATTENUATION "R"
B	X	X	X	0	1	1	1	NOT ALLOWED
B	X	X	X	1	0	0	0	NOT ALLOWED
B	X	X	X	1	0	0	1	INPUT MULTIPLEXER

B = 1 incremental bus; active

B = 0 no incremental bus;

X = indifferent 0,1

INPUT ATTENUATION SELECTION

MSB							LSB	INPUT ATTENUATION
D7	D6	D5	D4	D3	D2	D1	D0	**0.5 dB STEPS**
	1				0	0	0	0
	1				0	0	1	-0.5
	1				0	1	0	-1
	1				0	1	1	-1.5
	1				1	0	0	-2
	1				1	0	1	-2.5
	1				1	1	0	-3
	1				1	1	1	-3.5
								4 dB STEPS
	1	0	0	0				0
	1	0	0	1				-4
	1	0	1	0				-8
	1	0	1	1				-12
	1	1	0	0				-16
	1	1	0	1				-20
	1	1	1	0				-24
	1	1	1	1				-28

INPUT ATTENUATION = 0 ~ -31.5dB

SURROUND SELECTION

MSB							LSB	
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**SURROUND MODE**
						0	0	SIMULATED STEREO
						0	1	MUSIC
						1	0	OFF
								OUT
					0			VAR
					1			FIX
								EFFECT CONTROL
	0	0	0	0				-6
	0	0	0	1				-7
	0	0	1	0				-8
	0	0	1	1				-9
	0	1	0	0				-10
	0	1	0	1				-11
	0	1	1	0				-12
	0	1	1	1				-13
	1	0	0	0				-14
	1	0	0	1				-15
	1	0	1	0				-16
	1	0	1	1				-17
	1	1	0	0				-18
	1	1	0	1				-19
	1	1	1	0				-20
	1	1	1	1				-21

PHASE RESISTOR SELECTION

MSB							LSB	**SURROUND PHASE RESISTOR**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**PHASE SHIFT 1 (KΩ)**
						0	0	12
						0	1	14
						1	0	18
						1	1	37

BASS SELECTION

MSB							LSB	BASS
D7	D6	D5	D4	D3	D2	D1	D0	2 dB STEPS
X	X	X	1	0	0	0	0	-14
X	X	X	1	0	0	0	1	-12
X	X	X	1	0	0	1	0	-10
X	X	X	1	0	0	1	1	-8
X	X	X	1	0	1	0	0	-6
X	X	X	1	0	1	0	1	-4
X	X	X	1	0	1	1	0	-2
X	X	X	1	0	1	1	1	0
X	X	X	1	1	1	1	1	0
X	X	X	1	1	1	1	0	2
X	X	X	1	1	1	0	1	4
X	X	X	1	1	1	0	0	6
X	X	X	1	1	0	1	1	8
X	X	X	1	1	0	1	0	10
X	X	X	1	1	0	0	1	12
X	X	X	1	1	0	0	0	14

SPEAKER SELECTION

MSB							LSB	SPEAKER/ATT
D7	D6	D5	D4	D3	D2	D1	D0	1 dB STEPS
X					0	0	0	0
X					0	0	1	-1
X					0	1	0	-2
X					0	1	1	-3
X					1	0	0	-4
X					1	0	1	-5
X					1	1	0	-6
X					1	1	1	-7
								8 dB STEPS
X	0	0	0	0				0
X	0	0	0	1				-8
X	0	0	1	0				-16
X	0	0	1	1				-24
X	0	1	0	0				-32
X	0	1	0	1				-40
X	0	1	1	0				-48
X	0	1	1	1				-56
X	1	0	0	0				-64
X	1	0	0	1				-72
								MUTE
X	1	0	1	X				
X	1	1	X	X				

X = INDIFFERENT 0,1
SPEAKER ATTENUATION = 0dB ~ -79dB

TREBLE SELECTION

MSB							LSB	TREBLE
D7	D6	D5	D4	D3	D2	D1	D0	2 dB STEPS
0	0	0	0	1	1	1	0	-14
0	0	0	1	1	1	1	0	-12
0	0	1	0	1	1	1	0	-10
0	0	1	1	1	1	1	0	-8
0	1	0	0	1	1	1	0	-6
0	1	0	1	1	1	1	0	-4
0	1	1	0	1	1	1	0	-2
0	1	1	1	1	1	1	0	0
1	1	1	1	1	1	1	0	0
1	1	1	0	1	1	1	0	2
1	1	0	1	1	1	1	0	4
1	1	0	0	1	1	1	0	6
1	0	1	1	1	1	1	0	8
1	0	1	0	1	1	1	0	10
1	0	0	1	1	1	1	0	12
1	0	0	0	1	1	1	0	14

INPUT SELECTION

MSB							LSB	
D7	D6	D5	D4	D3	D2	D1	D0	INPUT MULTIPLEXER
X					0	0	0	IN2
X					0	1	0	IN3
X					1	0	0	IN4
X					1	1	0	IN1

POWER ON RESET

BASS	2dB
TREBLE	0dB
SURROUND & OUT CONTROL+ EFFECT CONTROL	OFF + FIX + MAX ATTENUATION
SPEAKER ATTENUATION L &R	MUTE
INPUT ATTENUATION	MAX ATTENUATION
INPUT	IN1

PIN: TREBLE-L, TREBLE-R

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PIN: VOUT REF

D95AU233A
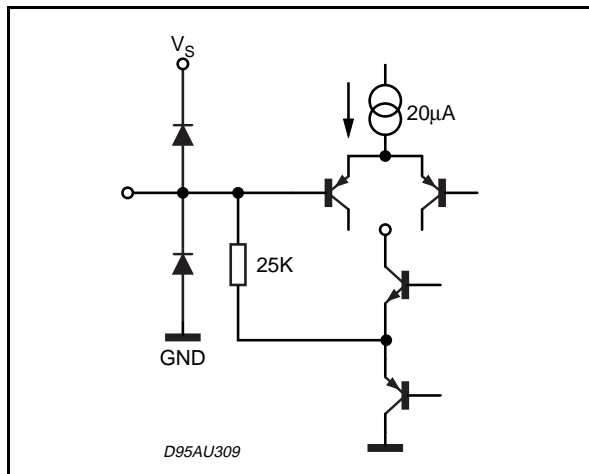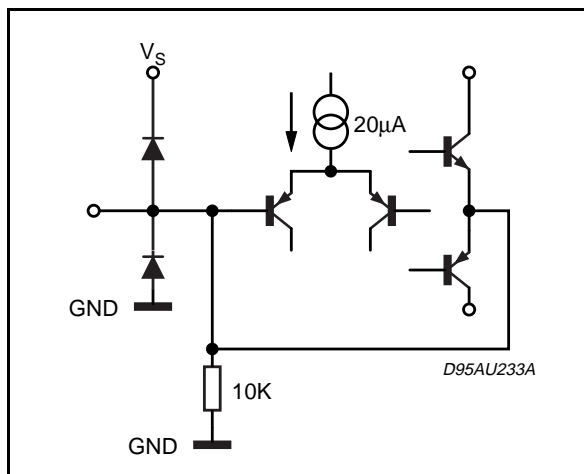
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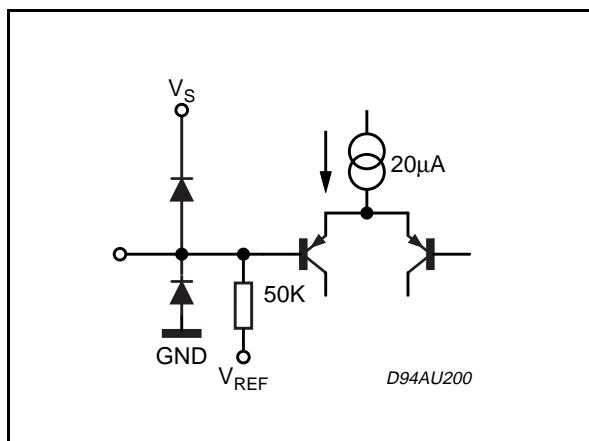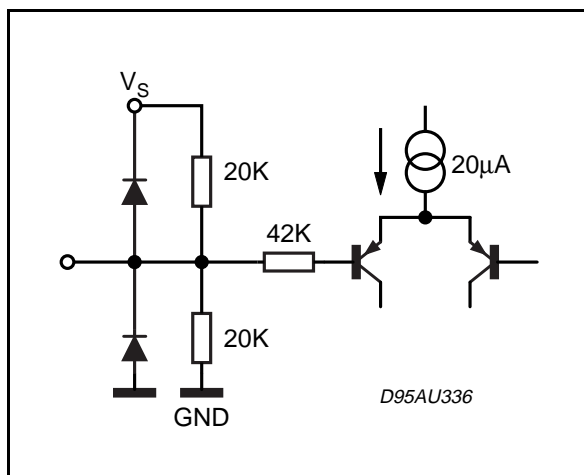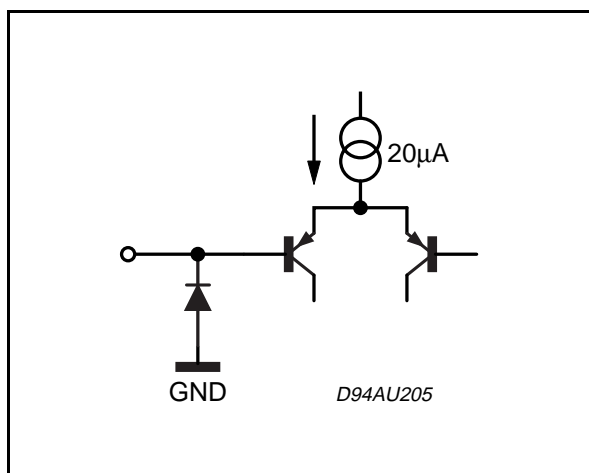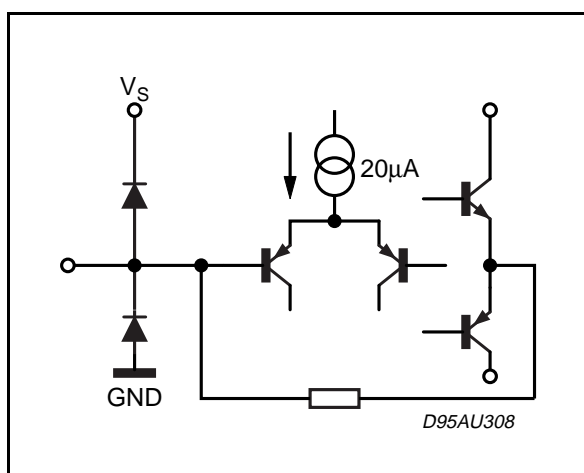
D94AU200

PIN: CREF

D95AU336

PIN: SCL, SDA

D94AU205

PIN: LP

D95AU308

PIN: L-OUT, R-OUT

D95AU230

PIN: BASS-LI, BASS-RI

D98AU949

PIN: BASS-LO, BASS-RO

D98AU950
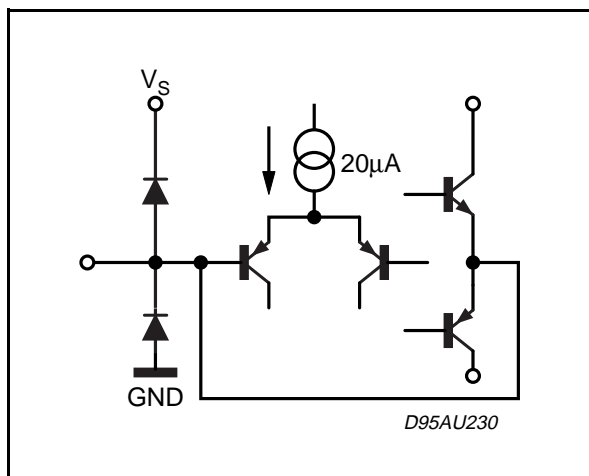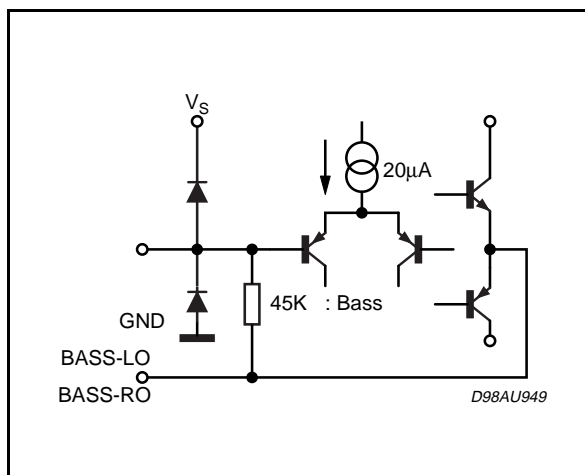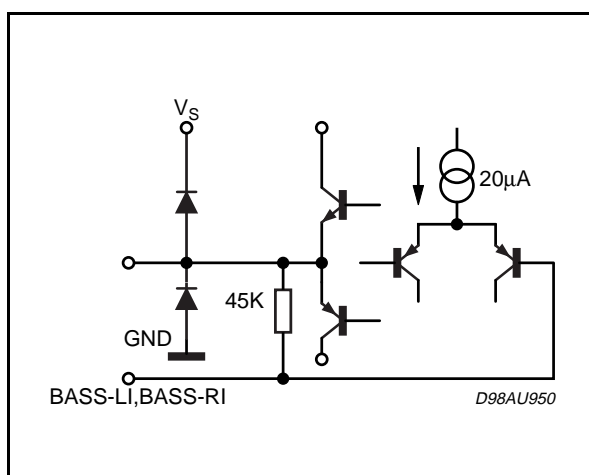
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8 ° (max.)					

OUTLINE AND MECHANICAL DATA
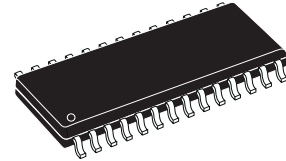
SO28
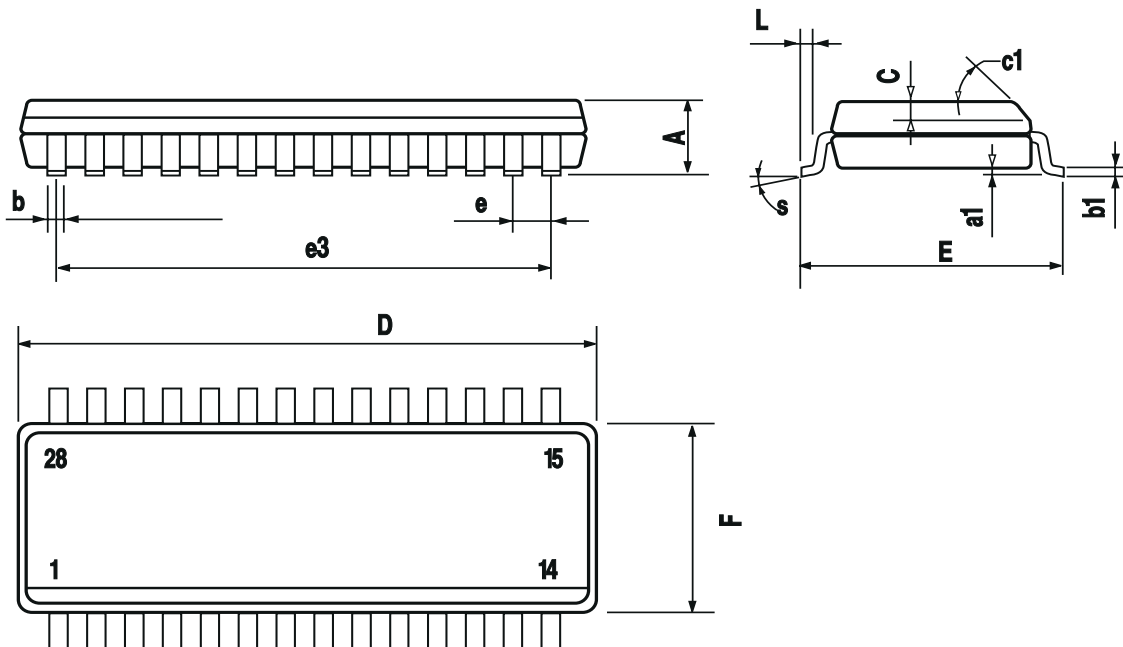
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.556	3.759	5.080	0.14	0.147	0.2
A1	0.508			0.020		
A2	3.048	3.556	4.572	0.12	0.14	0.18
B	0.356	0.457	0.584	0.014	0.018	0.023
B1	0.762	1.016	1.397	0.03	0.04	0.055
C	0.203	0.254	0.356	0.008	0.01	0.014
D	27.43	27.94	28.45	1.08	1.1	1.12
E	9.906	10.41	11.05	0.39	0.409	0.433
E1	7.620	8.890	9.398	0.3	0.35	0.37
e		1.778			0.070	
eA		10.16			0.400	
eB			12.70			0.500
L	2.540	3.048	3.810	0.1	0.12	0.15

**OUTLINE AND
MECHANICAL DATA**
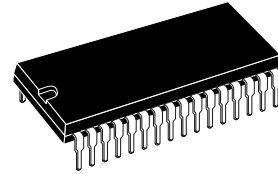
**SDIP32
(Shrink Plastic Dip 32L)**

SDIP32M

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