Compact Subnanosecond Pulse Generator Using Avalanche Transistors for Cell Electroperturbation Studies

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ABSTRACT

Research on the electroperturbation effects of ultrashort high field pulses in cancer cells requires subnanosecond rise time, high voltage pulses delivered to low impedance biological loads. Here we present a compact solid-state pulse generator developed for this application. The pulse is generated by switching a chain of avalanche transistors configured as a tapered transmission line from high voltage to ground. The system features a built in 1400:1 capacitively compensated resistive voltage divider. The divider, with a 3 dB point at 910 MHz, overcomes challenges in the direct measurement of the high frequency components of the output pulse. The generator is capable of producing a 0.8 ns rise time, 1.3 ns wide, 1.1 kV pulse into a 50 Ω load at a maximum repetition rate of 200 kHz. Techniques to implement physical layouting strategies to achieve subnanosecond rise times are outlined. Problems faced in integrating the subnanosecond pulse generator with a biological load are discussed. This pulse generator will be used in experiments aimed at electromanipulation of intracellular biomolecular structures.

Index Terms — **Avalanche breakdown, pulse power systems, voltage dividers, bioelectric phenomena, electroperturbation, biomembranes.**

1 INTRODUCTION

EXPERIMENTAL studies have shown that nanoelectropulses (nanosecond MV/m electric fields) trigger intracellular calcium release, translocate phosphatidylserine (PS) across the cell membrane, cause chromatin rearrangement and induce programmed cell death (apoptosis) in malignant cells without permanently damaging the outer cell membrane. [1-3] These effects have, among other things, generated interest in the electromanipulation of intracellular structures for inducing apoptosis and understanding gene transfection mechanisms.

Effective manipulation of intracellular structures using electropulses requires pulses that are short enough to bypass the cytoplasmic membrane and deposit their energy across intracellular membrane-bound structures. According to molecular dynamics simulations, electropulses that can create transmembrane fields of the order of 5-20 MV/m (i.e. transmembrane potential of >1 V) cause nanometer-diameter pores to form in the phospholipid bilayers within 1 – 2 ns of application. This indicates that subnanosecond risetime 5-20 MV/m pulses could minimize nanoporation of the cell membrane, enable the voltage across the inner membranes to exceed that across the outer membrane, and allow intracellular electromanipulation to dominate over membrane effects [2].

Since current state of the art pulse generation technology for biological cell loads is limited to 3-4 ns 10 MV/m pulses [4], there is a need for developing high field sub-nanosecond electric pulse generation techniques to facilitate studies aimed at manipulating intracellular biomolecular structures.

The design specifications for the pulse generator are calculated based on the desired electric fields and the geometry of the electrode micro-chamber containing the cells under study. For example, for a micro-machined chamber with electrodes spaced 100 μm apart from each other, a 5-20 MV/m field requirement translates into voltage requirements of 500 V to 2 kV. The design target for this pulse generator was a sub-nanosecond rise time, pulse duration of about 1 ns and a peak voltage that can be varied from 500 V to 2 kV without affecting other pulse parameters. The design values for the pulse generator were

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obtained based on an average output peak value of 1.25 kV. The system was designed to drive an effective load impedance of 50 Ω, giving us a peak current of 25 A. A repetition rate of the order of several kilohertz is required to observe the effects of many pulses on the cells with good statistics.

We have designed and constructed a pulse generator for biological experiments according to the above requirements. Our circuit adapts a generation architecture used to drive a high impedance capacitive Pockel's cell load to one that can deliver low energy pulsed fields to a low impedance biological loads. The system is also capable of directly measuring the subnanosecond kilovolt output pulse.

2 DESIGN

2.1 AVALANCHE TRANSISTORS

Existing pulse generators used in ultra-short pulse electro-perturbation research are based on diode opening switch and saturable core transformer based designs [4]. These designs are limited to >2 ns rise times because of inherent limitations in the diode switching characteristics. Avalanche transistors, with nonlinear high gain characteristics, have been known to switch in the 100s of picosecond regime, and were therefore chosen to be suitable for our design goals [5,6]. Like in [5], we chose SOT-23 Zetex FMMT417 avalanche transistors because of their high VCBO rating (320 V) and compact low inductance packaging. Further, these transistors have a peak collector current rating of 60 A for pulses shorter than 20 ns and are therefore more than well suited to our peak current requirement of 25 A.

2.2 TRIGGER CIRCUIT

The basic circuit is a series chain of avalanche transistors and capacitors configured as a tapered transmission line from high voltage to ground [5]. The circuit diagram is shown in Figure 1. The line is switched from high voltage to ground by triggering the bottom of the transistor cascade via an amorphous saturable core TX_1 from Toshiba.

Before the circuit is triggered, the first transistor appears to have an open base and a common emitter. Therefore it is more prone to V_{CEO} than a shorted base-emitter type V_{CBO} breakdown. The V_{CEO} breakdown occurs at a lower voltage of 100 V and is characterized by current runaway. The avalanche breakdown is more desirable because it lets us hold off a much higher voltage (~V_{CBO} = 320 V) across the first transistor. Moreover a V_{CBO} avalanche breakdown of the first transistor generates the charge carriers needed to cause the succeeding stages to avalanche.

To force the first low-side transistor into VCBO avalanche breakdown, the trigger signal must force the base to be shorted to the emitter. This can be achieved by driving TX_1 to saturation – i.e. by having a trigger signal that is short and rises as fast as 0.5-1 ns.

2.3 TAPERED TRANSMISSION LINE CONFIGURATION

A tapered transmission line is used to ensure that the rise time sharpens progressively from stage to stage. The rise time can sharpen progressively only if every stage avalanches faster than the previous stage i.e. if each stage has a greater over voltage across it than the previous stage. Since it is a series chain, current through each stage remains approximately the same. Therefore, successive stages are designed to have higher impedance than the preceding ones, with the first stage having the lowest impedance.

The low impedance of the 1st stage causes its collector to be placed close to ground upon triggering. Since stage 1 goes into avalanche breakdown upon triggering, it feeds in the avalanche current necessary to turn on stage 2 and overvolt it. Since stage 2 has higher impedance than stage 1, there is a larger over voltage across stage 2 than across stage 1. This causes stage 2 to go into faster non-destructive avalanche breakdown than stage 1. Stage 2 then feeds in

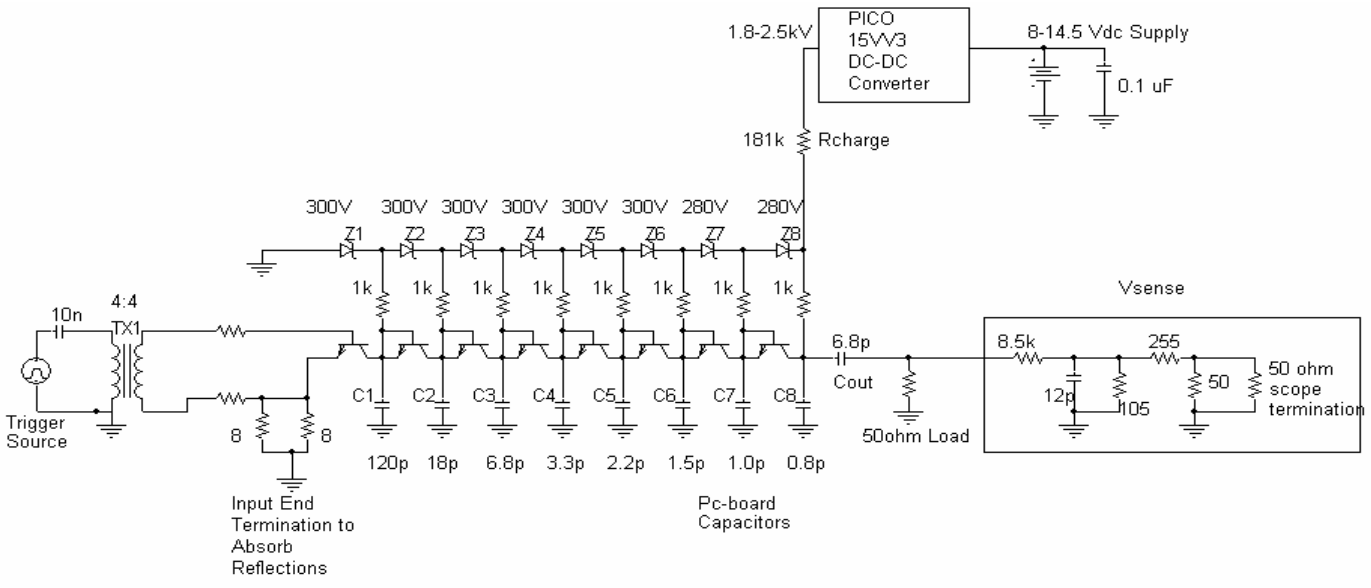

Figure 1. Complete avalanche pulse generator circuit.

avalanche current to stage 3, causing it to turn on faster and go into an even faster avalanche breakdown. Successive stages avalanche faster and faster in a similar fashion to cause C_8 to discharge into ground within several 100 picoseconds. This gives us an output pulse rise time of the order of 100s of picoseconds. By choosing C_{out} such that $R_{load}*C_{out}$ is small, we can control the fall time and obtain a sub-nanosecond output pulse.

Since the impedance of each succeeding stage is less than that of preceding stages, the effective transmission line impedance, $Z = \sqrt{}(L/C)$, is tapered so the lower end stages have higher capacitances. This helps keep the avalanche current on until the higher end stages have turned on.

The capacitance for the first stage is chosen so as to allow it to switch 200 V within a rise time of 1 ns. Since the desired current in the chain is 25 A, the capacitance C_1 is given by:

$$C1 = \Delta Q / \Delta V = I \times dt / dV = 25A \times 1ns / 200V = 125pF \qquad (2)$$

The closest commercially available value is 120 pF. Modeling the Zetex transistor as having an inherent inductance of L = 2 nH [5], and using the formula $Z = \sqrt{}(L/C)$, C_1 = 120 pF gives a first stage impedance of 4 Ω. The impedance of the line must therefore taper uniformly from 4 Ω at the triggered end to the 50 Ω load impedance at the high end.

A preliminary characterization of the FMMT 417 transistors revealed that about half of the DC voltage across any transistor would be applied to the load when the transistor is in avalanche mode. But to keep transistors out of their breakdown region, the DC voltage across every transistor is limited to V_{CBO} = 320 V. Therefore the number of stages for a 1.25 kV output pulse is given by:

$$N = V / (0.5 * VCBO) = 1250 / 160 = 7.8 \cong 8 \qquad (1)$$

It is desirable to keep the tapering smooth so as to avoid significant reflections due to abrupt impedance jumps. So to taper from 4 Ω to 50 Ω in 8 stages, we can estimate a linear impedance taper of (50-4)/7 = 6.6 Ω per stage. This lets us calculate the capacitances $C_2 – C_8$, as shown in Table 1. All capacitors used are NPO type ATC 100C capacitors rated at 2500 V. They are chosen since they are ultra low ESR components that have very low variability (~5%) over the rated voltage range.

Table 1. Capacitances in the tapered transmission line

Stage Number	Impedance (Ω)	Capacitance (pF)
2	10.5	18
3	17.1	6.8
4	24.6	3.3
5	30.1	2.2
6	36.5	1.5
7	44.7	1.0
8	50	0.8

Since the resulting configuration is a discretely tapered transmission line with finite impedance jumps, reflections are unavoidable. Reflections degrade the output waveform by causing a jittery rising edge and a long tail. Reflections also degrade the transistors over time. Therefore, we have placed two paralleled input termination resistors each having a value of 8 Ω - to match the impedance of the triggered end and absorb any reflections. This technique of designing the tapered transmission line, first reported in [5], forces the line to behave like a two-end terminated coax cable. It ensures a smooth rise, and improves reliability of the pulse generator by ensuring that reflections going back and forth will not re-trigger the transistors.

2.4 DC CHARGING CIRCUIT

The dc bias for the transistor chain needs to be divided uniformly among the 8 stages. If some transistors have higher dc collector to emitter bias than others, they turn on due to dc overvoltage and the circuit produces pulses spuriously before an external trigger signal is supplied. The symmetry of voltage division is achieved by using a chain of high voltage zener diodes (Z_1-Z_8). Previously, avalanche pulse generator designers have used 320 V zener diodes to ensure that transistors are not biased beyond their V_{CBO} rating.

In practice, however, this choice of zener diodes is not completely effective in maintaining equal dc voltage bias across all 8 transistors. In order for all 8 diodes to hold off their nominal voltages, the zener chain needs to conduct a nominal current, I_z of 1-1.2 mA from high voltage end to ground. However, if the nominal zener voltage is high enough for the transistors to 'turn on' under dc collector to emitter bias, the higher end transistors will draw significant leakage current from the zener chain. Leakage of current from the zener diode chain at the high end causes insufficient current supply to the lower end diodes. This prevents the lower end diodes from maintaining their nominal zener voltages. Thus most of the 2.5 kV dc supply is dropped across the higher end transistors, and very little across the lower end transistors. This has two effects: a) the lower end transistors cannot avalanche when triggered, because they do not have a high enough dc collector to emitter bias to drive them into V_{CBO} breakdown; b) the higher end transistors are overvolted well beyond their V_{CBO} rating and avalanche unpredictably without any external triggering. The above problems clamp the peak output pulse voltage to ~ 1.25 kV –which is about half of the design value because only the higher half of the transistor chain is contributing to the output pulse.

We have found that using 280-300 V zener diodes instead of the obvious choice of 320 V overcomes this problem. A characterization of leakage current versus voltage showed that the transistors start drawing significant leakage currents (currents greater than 1/10 of the nominal I_z i.e. ~100 μA) from the zener chain if they have a dc VCE greater than 280-300 V (Figure 2).

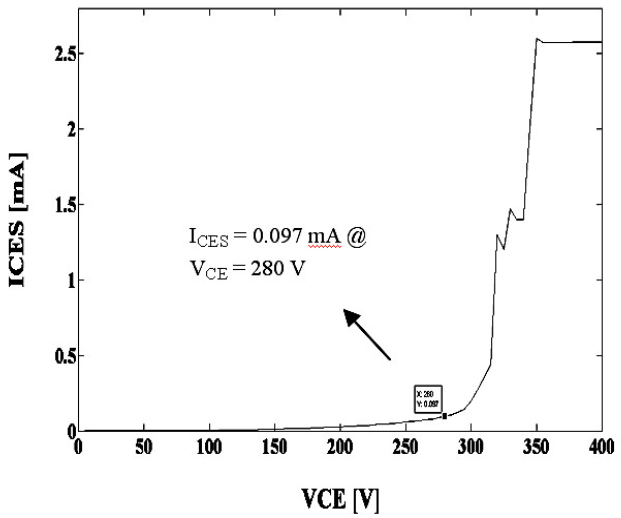

Figure 2. Empirically obtained leakage curve for the Zetex FMMT 417 avalanche transistor - I_{CES} is collector to emitter current under a reverse collector to emitter voltage = V_{CE} when base is shorted to emitter.

Further, since the higher end capacitors charge up before the lower end capacitors, and the higher end zeners turn on before the lower end ones, it is important to make sure that the higher-end transistors have lower dc reverse collector to emitter bias than transistors on the low voltage end of the chain. This ensures that the high-end transistors only turn on due to a non-destructive avalanche breakdown triggered by the lower end transistors, and not by spurious dc overvolting. Therefore, the zener diodes across the 2 high-end transistors have been chosen to be 280 V rated IN5109 components, as opposed to the other 6 - which are IN5110 components rated at 300 V.

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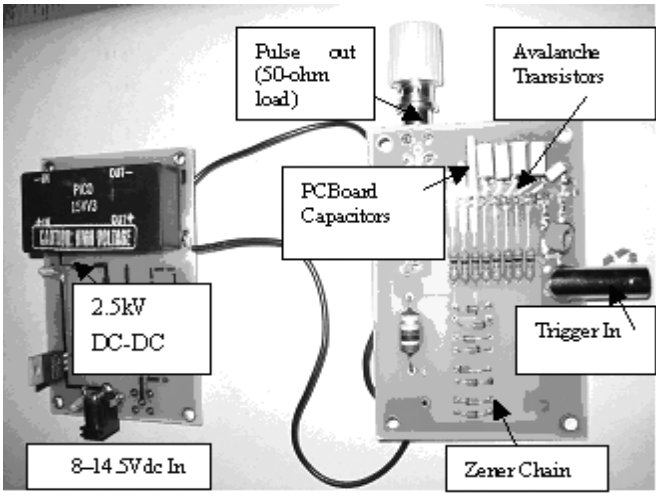

Figure 3. Avalanche pulse generator circuit board assembly – the PC Board capacitors are traces that integrate easily with the avalanche transistor chain and supporting circuitry.

2.5 PHYSICAL LAYOUT

Control of parasitics in the physical layout is critical to generating pulses in the sub-nanosecond regime. In addition to using carefully selected low parasitic surface mount components in the pulse generating section of the circuit, all interconnections have been made short to ensure low parasitic inductances. Further, we used pads on a double-sided 0.062" FR-4 epoxy glass laminate pc-board for capacitors C_6-C_8 instead of soldering on 3 ATC capacitors. Since the pc-board dielectric has a low series inductance, this improves the pulse rise time significantly. Previous attempts to use pc-board capacitances for low values of capacitors [5] have used complex construction techniques such as dielectric wedges to accommodate the avalanche transistors and their bias networks with the pc-board capacitors. However, our design simply lays out the capacitors as pc-board traces (Figure 3) that easily connect to the transistors.

The tradeoff of this technique is that capacitance values of 0.8 – 1.5 pF require long traces because the dielectric

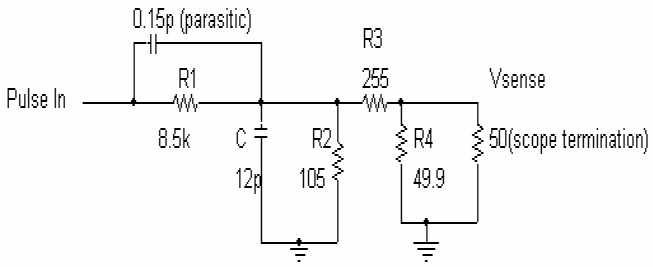

Figure 4a. Voltage Divider schematic

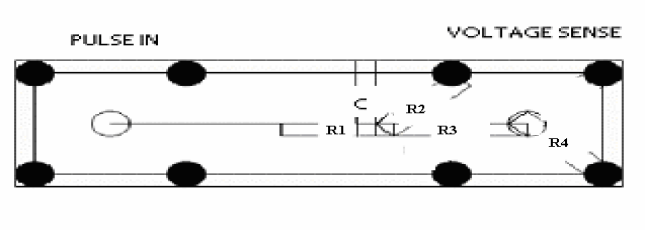

Figure 4b. Schematic of the voltage divider layout on a two layer pc-board. Components are labeled as in Figure 4a. The connectors (with ground needles placed at the darkened circles) are SMA type with their leads protruding out on the component side. The divider has a ground plane running uniformly underneath it.

constant of the pc-board is a low 4.6. The electrical length of these traces may cause these pc-board capacitors to behave non-ideally - as unterminated transmission lines – to cause some ringing on the tail end of the pulse. An improved version with high dielectric/thinner pc-board may be better suited for laying out pc-board capacitors without occupying large board areas – but this would require extra parasitic tolerance in other parts of the circuit.

3 MEASUREMENT

Direct measurement of kilovolt transitions in hundreds of picoseconds has been a challenging design problem. Voltage division techniques based on inductive coupling or

capacitive compensation are impractical because of limitations imposed by component self resonant frequencies. The lack of reliable broadband voltage dividers has caused other avalanche transistor pulse generator designers to infer output pulse characteristics using indirect methods [5, 6].

Our system features a custom-made high bandwidth, capacitively compensated resistive voltage divider (Figure 4). The divider is built into the pulse generator and enables direct, measurement of our subnanosecond high voltage pulse. The nominal voltage division ratio is 1400:1 and the divider has a +3 dB point at 910MHz.

The divider has a resistive backbone, and is built on a standard 2-layer printed circuit board. Resistors are SMT 1206 package metalized film chip resistors. Because of the proximity of contacts on a ceramic substrate, these resistors have a shunt parasitic capacitance of 0.1-0.2 pF. To overcome the bandwidth limitation imposed by this parasitic, capacitive compensation is necessary [7]. The compensation capacitor C is of type ATC100A from American Technical Ceramics Corp. These are high quality microwave capacitors, having low loss and high self-resonant frequency. The divider has been designed as a two stage resistive divider to minimize the number of compensating capacitors needed to maintain a flat attenuation over our desired bandwidth. This minimizes the dependence of the frequency response on the self-resonant frequencies of these components.

The layout of the divider is designed to minimize parasitic interferences (Figure 4b). All components are placed on their sides to ensure small footprints and minimal parasitic capacitance to ground. In particular, resistors on the low side of the divider are mounted directly onto the SMA connector to eliminate stray interconnect inductances.

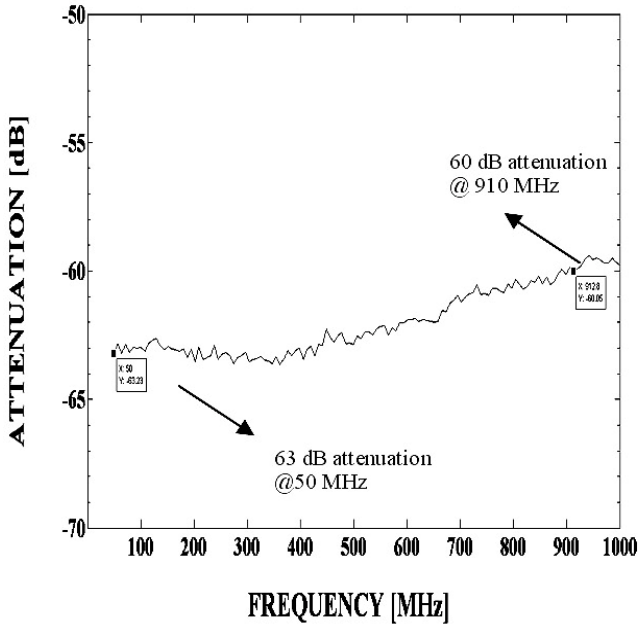

Figure 5. Frequency response of compensated resistive voltage divider designed to measure subnanosecond rise time pulses. Attenuation is amplitude of S21/ (1+S11) in dB, as measured on an Agilent 8720ET Network Analyzer. Measurement span is 50 MHz to 1 GHz.

This technique also minimizes any distortion in frequency response that may arise from capacitive coupling to the high voltage end. The frequency response (Figure 5) of the divider is measured on an Agilent 8720ET network analyzer. The divider's bandwidth is limited by the self-resonance of the compensation capacitor, and other high frequency resonances.

The following 2 sections discuss operation of the pulse generator into a 50 Ω resistive load and a micro-machined slide [8] containing biological cells in liquid suspension.

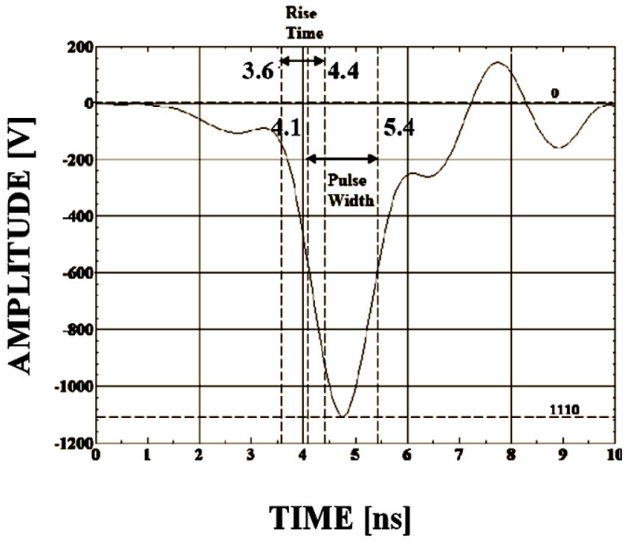

Figure 6. Output pulse into 50 Ω resistive load as measured by the custom divider in Figures 4, 5. Pulse width = (5.4 – 4.1) ns = 1.3 ns, and rise time = (4.4 – 3.6) ns = 0.8 ns

4 OPERATION: 50 Ω RESISTIVE LOAD

Repetition rate is limited to 200 kHz by pulse current heating of the transistors. The maximum power dissipation in the zener diodes, and the $R_{charge}*C_1$ time constant are limiting factors too.

The all solid-state nature of the pulse generator ensures reproducible pulses and increases reliability. The typical output into a 50 Ω resistive load is as shown in Figure 6. The pulse amplitude is 1110 V; rise time (10% to 90%) is 0.8 ns, and the full width half maximum (FWHM) is 1.3 ns. The energy delivered by the generator to this matched load is a low 32 μJ.

The pulse amplitude increases from 900 V to 1100 V as the voltage supply is varied from 8 V to 14.5 V. The pulse width and rise time are fairly independent of the amplitude.

5 BIOLOGICAL LOAD AND INTEGRATION

The biological load is an instrumented microscope slide, containing gold deposited electrodes separated by 100 μm. The cell solution is put into the micro chamber between electrodes, and covered by a glass cover slip [8]. The load impedance of this setup when the cell solution is loaded is of the order of 100s of ohms. Different cell solutions could have different impedance values, and the effects of pulsed electric fields could also cause variability in load impedance during

experimentation. Therefore, the pulse generator has been designed to drive an effective load impedance of 50 Ω– designed as the parallel combination of a small SMT resistor and the loaded micro chamber. This is advantageous because we can easily interface the pulse generator output to the load using a 50 Ω coaxial cable. The paralleling of a small resistor with the higher impedance cell slide also allows for a good match over variable cell impedances – as changes in biological loads would not significantly affect the effective load seen by the pulse generator [9].

The block diagram of the setup used to deliver pulses into the above biological load is shown in Figure 7. The setup enables us to image, real-time, pulse-induced effects under a Zeiss Axiovert microscope. The PC-board placed on the insert stage of the microscope serves a dual purpose. Firstly, it is an interface between the pulse generator and electrodes on the microscope slide containing the cell sample under study. Secondly and more importantly, it contains the custom-made voltage divider (Figures 4, 5) to monitor pulse characteristics at the load. This monitoring is important for two reasons – a) to ensure that all connections are in place and the pulse is delivered to the load and b) monitor pulse shape at the load - it could be different from the pulse measured at the point of pulse generation since the biological load is not a perfectly resistive 50 Ω load.

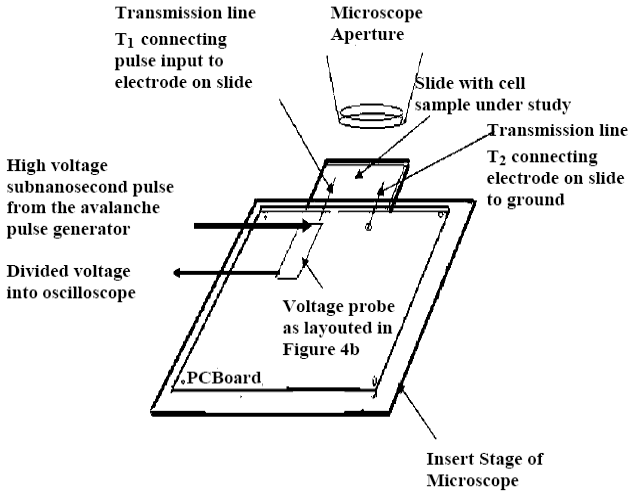

Figure 7. Schematic of the setup that integrates the avalanche pulse generator with the biological load and the microscope.

Figure 8 shows the output pulse of the avalanche pulser – interfaced to the biological load - as measured by the voltage monitor on the insert stage. This output pulse has ~ half the pulse amplitude (600 V) and ~1.5 times the pulse width (2.1 ns) of the output pulse delivered into a purely resistive 50 Ω load (Figure 6).

There are two possible reasons for this distortion of pulse parameters., and both of them arise from the physical configuration of the interfacing setup shown in Figure 8 – particularly the transmission lines T_1 and T_2 connecting the electrodes on the slide to the 50 Ω cable delivering the output pulse to the load.

Firstly, transmission lines T_1 and T_2 introduce load parasitics that could distort pulse shape by causing

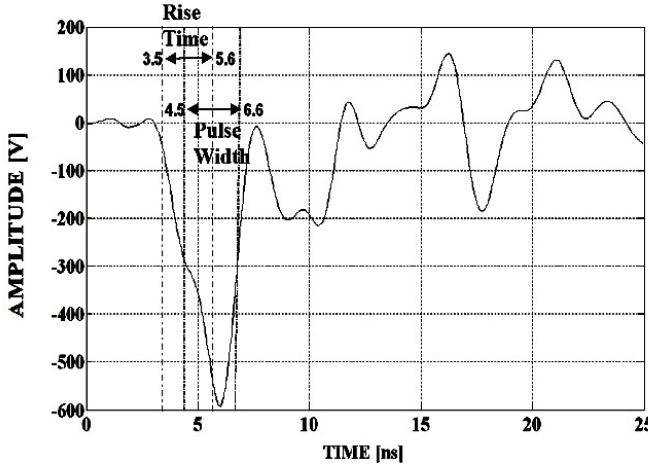

Figure 8. The output of the avalanche pulse generator into a loaded slide as measured by the custom-made voltage monitor (described in Section 3) on the microscope insert stage. Pulse is rising from 3.5 ns to 5.6 ns, and pulse width is seen as 6.6 – 4.5 ns = 2.1 ns.

impedance mismatch between the tapered transmission line in the pulse generator and the load.

Secondly, transmission lines T_1 and T_2 affect the accuracy of the voltage divider on the insert stage pc-board by capacitively coupling to the high impedance end of the voltage divider. This capacitive coupling limits the bandwidth of the voltage divider to ~250 MHz (Figure 9) – which is in stark contrast with the frequency responses of the same voltage divider measuring the pulse delivered to a 50 Ω resistive load (Figure 4 and Figure 7). This bandwidth limitation could mean that the measurement in Figure 8 is a distorted version of the actual pulse delivered.

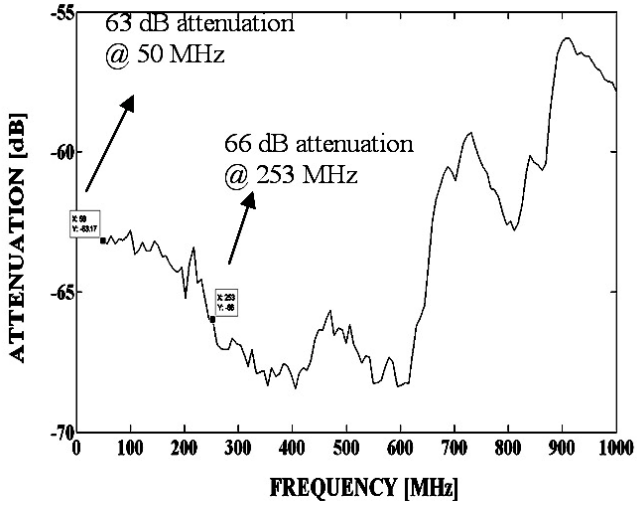

Figure 9. Frequency response of the compensated resistive voltage divider (Figure 4), interfaced with the micro-chamber containing cells in suspension. Attenuation is amplitude of S21/ (1+S11) in dB, as measured on an Agilent 8720ET Network Analyzer. Measurement span is 50 MHz to 1 GHz.

Therefore, redesigning the microscope/slide interface with a careful consideration of the parasitics, high frequency resonances and coupling issues will a) ensure a good match between the pulse generator and the load, and b) allow for reliable and measurable delivery of our 1.1 kV 1.3 ns pulses to biological loads.

7 CONCLUSION

We have designed an avalanche transistor switched pulse generator to produce 1.1 kV pulses with a rise time of 0.8 ns and pulse width of 1.3 ns. The generator features an inbuilt voltage divider for direct measurement of high frequency components of the pulse. Further development of the subnanosecond pulse generator for biological experimentation requires redesign of the configuration of the micro-chamber, and the electric interface between the generator and the load.

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