LUNDS UNIVERSITET
Lunds Tekniska Högskola

Institutionen för datavetenskap
Krzysztof Kuchcinski

Tentamen i kursen
EDAN15: Konstruktion av inbyggda system (Design of Embedded Systems)

2017-08-25, kl. 8-13

Sal:
Sparta C

Hjälpmedel:
Inga

Resultat anslås:
Senast 2017-09-08

Poänggränser:
Max 40 p., för godkännande krävs ca 20 p.

Jourhavande lärare:
Krzysztof Kuchcinski, tel. 22 23414

The answers to the questions can be written in Swedish or English.

Good luck!
Lycka till!

1 (3 p.)

Explain the term "design space exploration" used in embedded systems design. What does it mean that designers make "trade-offs" between different design parameters? Enumerate at least three parameters that are usually considered and illustrate possible trade-offs with examples.

2 (3 p.)

Explain the main ideas behind the following design flow models used for embedded systems:

- stepwise refinement model,
- hardware/software co-design,
- top-down, and
- bottom-up model.

3 (3 p.)

The data-flow model of computation gains increasing interest in embedded systems. Explain shortly the data-flow model and its basic components, *actors*, *tokens* and *firing rules*. List four application areas that fit this model very well.

4 (3 p.)

Figure 1 depicts a simple system, modeled using marked Petri net, consisting of two tasks. The tasks cannot be in state P_4 and P_5 simultaneously. Analyze behavior of this system using reachability tree. That is

- draw a reachability tree for the Petri net from Figure 1, and
- using the reachability tree explain why the system cannot be in state when both P_4 and P_5 are marked.

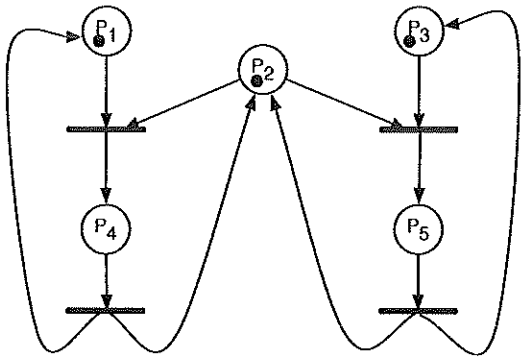

Figure 1: Petri net model of a system.

5 (5 p.)

FIR (Finite Impulse Response) filters are one of the most basic building blocks used in digital signal processing. The output y of an N-tap FIR filter is given by the equation below

$$y_t = a_0 x_t + a_1 y_{t-1} + \cdots + a_N y_{t-N-1}$$

where x_t is the input to the filter at clock tick t, y_{t-1} is the output value at previous clock tick, and so forth. $a_0, a_1, \ldots, a_{N-1}$ are the filter's coefficients.

Write synthesizeable VHDL code for the entity and architecture that implements the 4-tap FIR filter presented in the assignment above. Assume that the filter's coefficients are integers and are equal $a_0 = 2$, $a_1 = 5$, $a_2 = 4$ and $a_3 = 3$.

6 (6 p.)

Write the synthesizeable behavioral VHDL code that implements the synchronous finite state machine (FSM) depicted in figure 2. This FSM detects pattern 110 and it has initial state S_0. Assume that an input ('0' or '1') comes each clock cycle. Implement this FSM with *asynchronous* reset and assume that at signal `reset = '0'` the FSM should return to state S_0.

Arcs of the FSM are labeled with two binary values separated by "/" indicating input and output signal respectively, e.g. 0/1 indicates input signal equal 0 and output signal equal 1.

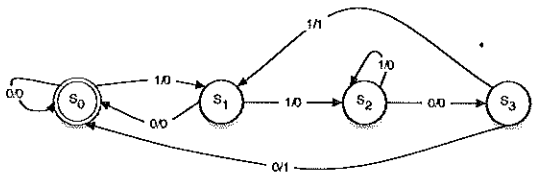

Figure 2: FSM model for detection of sequence 110.

7 (4 p.)

System partitioning can be done using partitioning or clustering algorithms. These algorithms use either *objective* or *closeness* functions to make appropriate decisions on system partitioning. Answer the following questions, assuming that our goal is to minimize the communication cost between partitions or clusters.

a) How are *objective* or *closeness* functions defined?

b) How partitioning or clustering objectives, such as minimum communication between partitions, are reflected in objective or closeness functions? Give examples for both cases.

Give examples of objective and closeness function in your discussion.

8 (5 p.)

Using list scheduling, make the schedule for the data dependency graph depicted in Figure 3. Assume that you can use one adder and two pipelined multipliers. Adders have 1 clock cycle delay and multipliers 2 clock cycles delay (two pipeline stages, 1 cycle for each pipeline stage). Answer the following questions:

a) How do you compute the priorities? Write down the priority for each operation.
b) What is the number of clock cycles for execution of this model?

Give the sequence of steps taken by the list scheduling algorithm that lead to your solution. For each step specify the list of nodes that were considered for scheduling.

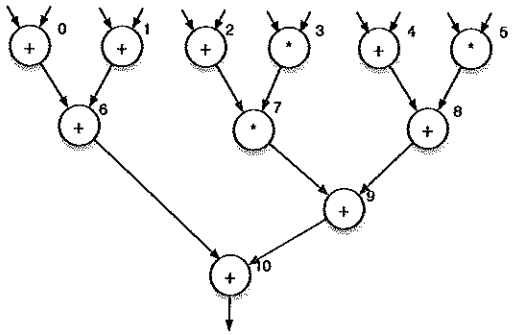

Figure 3: An example of data dependency graph

9 (5 p.)

Describe briefly Earliest Deadline First (EDF) scheduling. The presentations should include the following parts:

a) describe the task model and execution assumptions,
b) the method to assign priorities to tasks, and
c) discussion whether EDF can provide the optimal schedule and the condition for scheduliability of tasks.

Draw the EDF schedule for the task set from Table 1 for the first 12 times units.

Task	Period	WCET
1	3	1
2	6	2
3	12	3

Table 1: Task set for EDF scheduling.

10 (3 p.)

What is the formula for power consumption in CMOS technology? Discuss how the power consumption of a design can be minimized considering the parameters of this formula. Specifically, explain how parallelization of computations can be used, not only to speed-up a design, but also to reduce its power consumption.

11 (3 p.)

Discuss briefly the SCAN path testability improvement technique. In the discussion include the following points:

a) the general idea of the SCAN path and the role of two LFSR registers, and
b) give the motivation why SCAN path improves test generation and testing time.

What are the main advantages and disadvantages of this method?