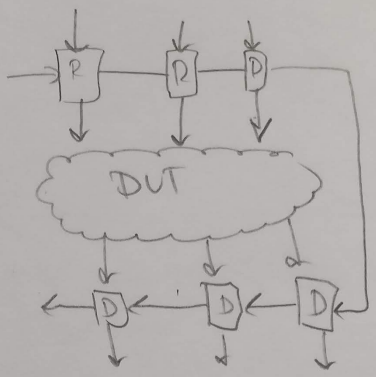
SCAN is a structural technique to test fabricated ASIC's.
This method use Flipflops connected together as a Serial Chain. In normal mode this serial connection is not used, just when the system should be tested. Then a testpattern is send sequentially to scan_in by enabeling scan_enable and afterwards the system executes and the results are read through the scan_out pin.



The motivation behind the scan-chain is that it uses less pins than a testpoint implementation where one flipflop is connected to one pin. Another good point is that the testpattern can be changed for a specific test. The testingtime is improved because it is possible to automatize the whole testing.

(2)

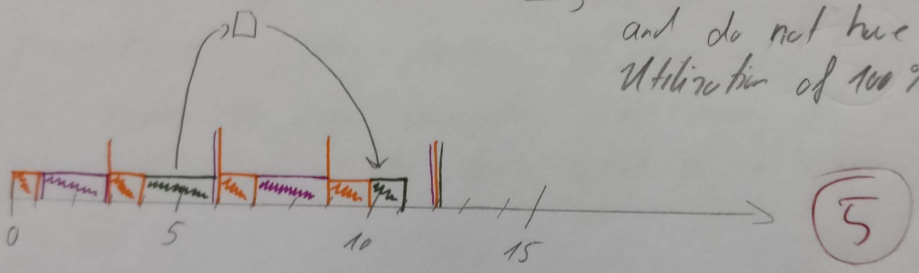
N15 0006 VEP
HSAMM

(a)

Rate Monotonic Scheduling (RMS) is a dynamic scheduling with fixed priorities. It is executed on a single core processor and just one task is allowed to use the same resources at the same time. The priorities are given by the length of the period time. A short period time ends up on a high priority, so a long period time means low priority. RMS is a optimum in the sense that no other dynamic scheduling with fixed priorities is better. RMS garantes the schedulability when the utilization is smaller then $n(2^{1/n} - 1)$.

$$\text{utilization} = \sum \frac{C_i}{T_i} \leq n(2^{1/n} - 1)$$

$\Rightarrow$ The task set is schedulable and do not have a Utilization of 100 %

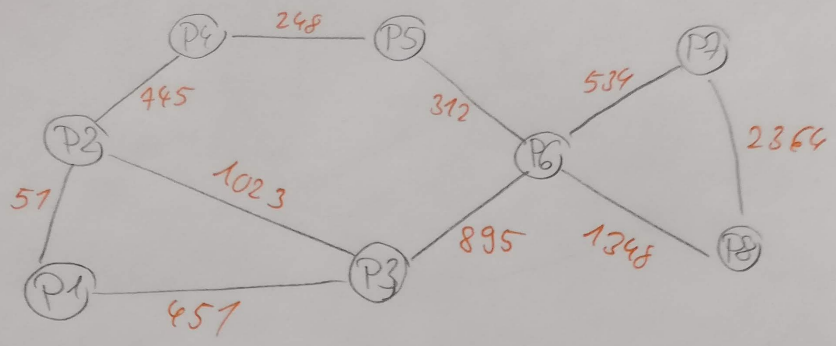


(5)

Task	Period	WCET	Priority	
1	3	1	3	—
2	6	2	2	—
3	12	3	1	—

N15006VEP
HSAUVIC

(6)



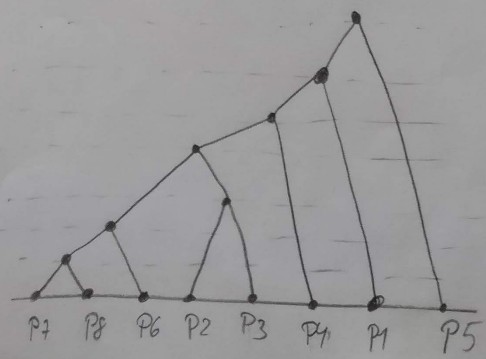
closenessFunction = clF = $\begin{cases} w_{n1,n2} \\ \max(w_{n1,n2}) \end{cases}$

1. {P3} and {P5} = / no direct connection
2. {P3} and {P6} = 895
3. {P6, P7} and {P8} = 2364

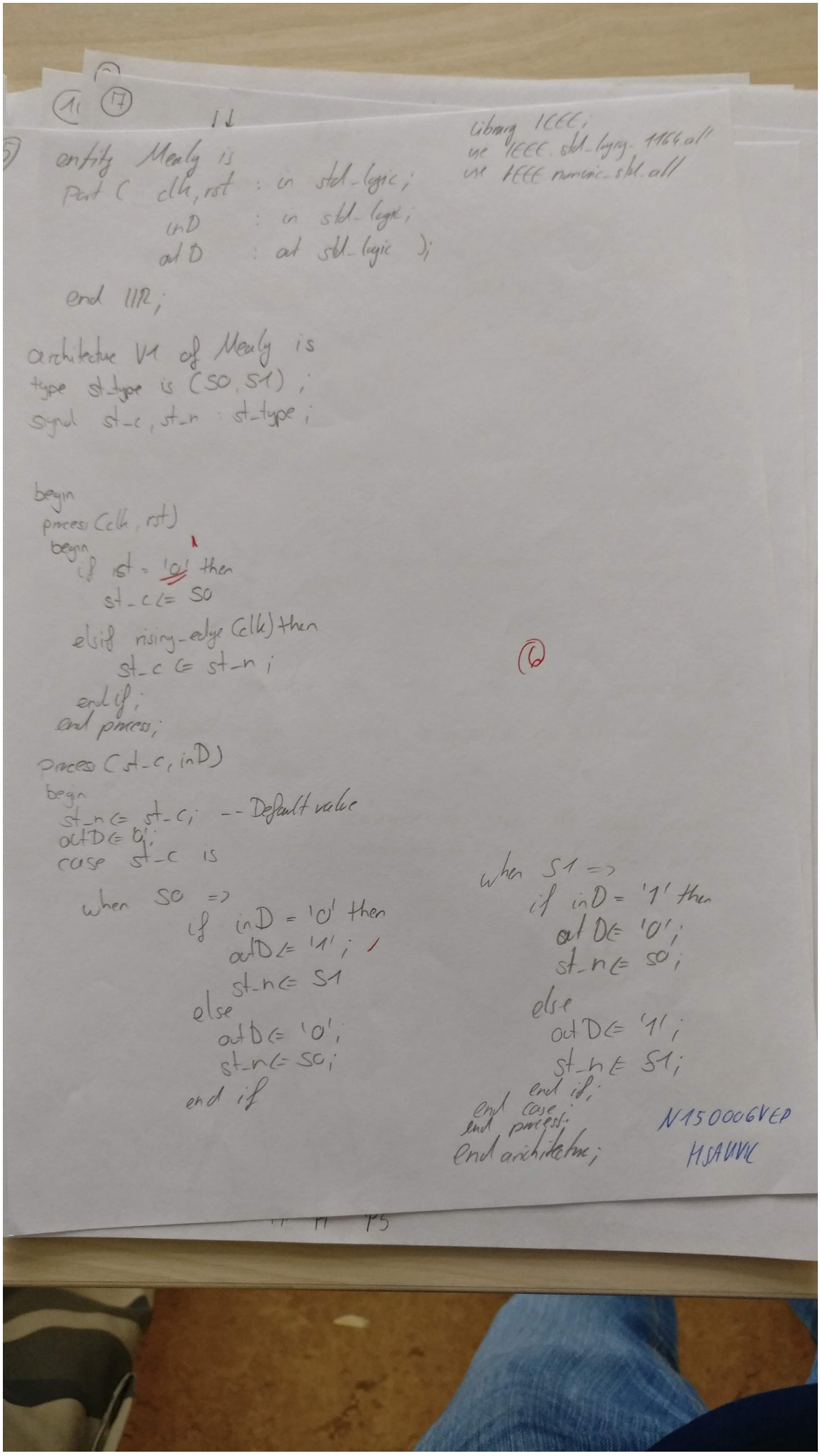
A cluster should combine two task with a hight communication cost, that would mean it would be good to combine the last case to one cluster.

Hierarchical clusking is a technique to show the clusk result. You start with the highest communication cost and finish with the lowest.

(4)



N15000GVEP
HSAVNC

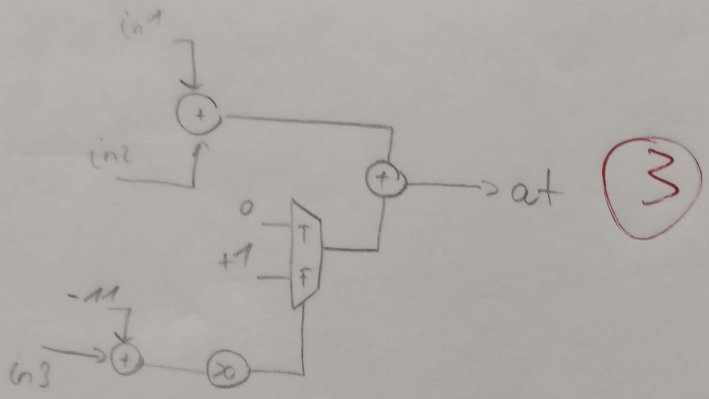


```
library IEEE;
use IEEE.std_logic_1164.all
use IEEE.numeric_std.all

entity Mealy is
Port ( clk, rst : in std_logic;
       inD      : in std_logic;
       outD     : out std_logic );
end IIR;

architecture V1 of Mealy is
type st_type is (S0, S1);
signal st_c, st_n : st_type;

begin
process (clk, rst)
begin
   if rst = '0' then
      st_c <= S0
   elsif rising_edge (clk) then
      st_c <= st_n;
   end if;
end process;

process (st_c, inD)
begin
   st_n <= st_c;  -- Default value
   outD <= '0';
   case st_c is

      when S0 =>
            if inD = '0' then
               outD <= '1';
               st_n <= S1
            else
               outD <= '0';
               st_n <= S0;
            end if

      when S1 =>
            if inD = '1' then
               outD <= '0';
               st_n <= S0;
            else
               outD <= '1';
               st_n <= S1;
            end if;
   end case;
end process;
end architecture;
```

N15006VEP
MSAUVC

④ $y_n = x_n + \frac{1}{2} y_{n-1} + \frac{1}{4} y_{n-2}$

② Actor ⊕ ⊳ ▷



3